Electrochemical and Solid-State Letters, **15** (3) H75-H77 (2012) H75
1099-0062/2012/15(3)/H75/3/$28.00 © The Electrochemical Society

Early Failure Induced by Phase Transformation in Microjoints for Chip-Level Integration

Ren-Shin Cheng,[a] Hung-Jen Chang,[b] Tao-Chih Chang,[a,z] and Jung-Hua Chou[b]

[a]*Industrial Technology Research Institute, Chutung, Hsinchu 31040, Taiwan*
[b]*Department of Engineering Science, National Cheng Kung University, Tainan 70101, Taiwan*

The undercut issue of the Cu/Ni/Sn2.5Ag microbump has been solved by reducing the Cu seed layer thickness and dry etching, but the bump height uniformity was degraded. Therefore, microjoints with different standoff heights were acquired by both thermocompressive bonding and reflow soldering. The numerical analyses indicated that the microjoints with a lower standoff sustained a higher fatigue stress under temperature cycling and the growth of Ni_3Sn_4 layer was more rapid because of a shorter diffusion route, which hastened the formation of micropores in the interconnection zone and was the root-cause of early failure.
© 2012 The Electrochemical Society. [DOI: 10.1149/2.023203esl] All rights reserved.

Manuscript submitted November 14, 2011; revised manuscript received December 9, 2011. Published January 9, 2012.

Three-dimensional integrated circuit (3DIC) technology has been proved to be with a smaller form-factor and a good electric performance,[1] and is believed being the next generation architecture to integrate homogeneous or heterogeneous devices in a module or sub-system.

For the demand of a cost-effective manufacture, wafer-level stacking by Cu to Cu, oxide to oxide and hybrid interconnection are highly focused,[2–4] but it is still a little bit far from the market because of the yield loss resulted from known good die issue.[5] Therefore, we believe the chip-level stacking technologies including chip to chip (C2C) and chip to wafer (C2W) by microbumps are much closer to fabrication.

As per the results reported previously,[6–8] the microbump composed of 5 μm Cu/3 μm Ni/5 μm Sn2.5Ag with a diameter of 18 μm and a pitch of 30 μm has been used to stack dies, but most of them adopted fluxless thermocompressive bonding (TCB) to prepare the test vehicles because the flux-contained reflow soldering is considered being not suitable to use due to that the cleaning of flux residues inside the microgap is very difficult.[9,10] Nevertheless, the conventional reflow technique is still the most cost-effective bonding process for chip stacking, therefore some researchers used reflow after temporally bonding to join microbumps[9,10] but extra-cost was also produced due to the pre-bonding process.

Industrial Technology Research Institute (ITRI) has successfully achieved the 20 μm pitch microjoints for chip stacking by a conventional reflow technique without any pretreatments,[11] but the long-term reliability is not good enough for mass production. The root-cause of early failure is attributed to the overgrowth of intermetallic compound in the microjoints with a lower standoff height as heated but the mechanism is not clear up to now.

In order to learn the effect of standoff height on the reliability performance and establish the failure mechanism of the reflow bonded microjoints, a local model for numerical analyses was built to study the stress / strain contours of the microjoints with different standoff heights, and a focused ion beam (FIB) equipment was used to clarify the microstructures in this investigation.

Experimental

The assembly of the CoC test vehicles was accomplished by a conventional flip chip packaging technique, firstly a WS-6400 flux from Senju Metal was applied to the Si interposer, and then the chips with 20 μm pitch were picked and placed on it by a SÜSS FC-150 bonder. After reflow soldering at a peak temperature of 245°C, the flux residues inside the microgaps between the chips and the interposer was respectively cleaned by Kyzen 2302 solvent and EnviroSense Enviro Gold #817 saponifier at 60°C for 20 min, the microgaps were then sealed by Namics U8443-14 capillary type underfill. Afterwards, the assemblies were preconditioned to sieve out the well-bonded ones for the prediction of lifespan. Additionally, the microjoints formed by TCB were used as a control group in this study.

In order to understand the various thermal fatigue behaviors coming from the diversities of microjoint standoff heights, a three-dimensional finite element global model and a local model of critical microjoints were established by ANSYS software to contour the stress / strain contributions of the reflow bonded microjoints under temperature cycling. The material properties of the elements including Si, solder microbump, underfill, Cu pillar, Ni layer, Al trace and passivation layer have been given in the previous studies,[12,13] and were assumed being linear-elastic and isotropic except Sn2.5Ag microbump and Cu pillar. The creep model of microbump was shown in the following equation,[12]

$$d\varepsilon/dt = 5 \times 10^{-6} \cdot \sigma^{11} \cdot \exp\left(-\frac{79.8}{kT}\right)$$

where ε is creep strain, t is time in second, σ is stress in MPa, T is temperature in K and k is Boltzmann's constant.

The microstructures of microjoints were not only cross-sectioned by grinding and observed by a field-emission scanning electron microscope (FESEM, JEOL, Japan) but also prepared and studied by a focused ion beam (FIB, Helios 600, FEI) to prevent the miscarriages from grinding.

Results and Discussion

Figure 1a showed the cross-section of the reflow bonded microjoints, the oxides on the surface of microbumps reacted with the activators and were hydrolyzed in the flux as heated in the activation zone (150 ∼ 180°C) and the solderability of the solder alloy was therefore improved, which enhanced the efficiency of self-alignment and made the microbumps interconnect precisely.

According to the EDS analyses, the intermetallic compound (IMC) formed at the interface was identified being Ni_3Sn_4, and was highly corresponded to the finding that Ni_3Sn_4 is the predominant phase formed at the interface between solder alloy and Ni under bump metallization (UBM) when Pb-bear and Pb-free solders reacts with Ni.[14,15] The thicknesses of the Ni_3Sn_4 at the interfaces between Ni layer and Sn2.5Ag solder alloy next to the chip and the interposer were measured and averaged being 1.7 ± 0.6 μm and 1.3 ± 0.3 μm, respectively. Accordingly, the Ni_3Sn_4 layer close to the chip was around 23% thicker than that close to the interposer because there was an original Ni_3Sn_4 layer existed before the assembly.

In the literatures of Zhan et al.[7] and Huang et al.,[16] it has been found that the thickness of the Ni_3Sn_4 layer at chip-side is much thinner than that at interposer-side because a thermal gradient exists when TCB is implementing, and which results in the formation of Sn depletion zone and makes microjoints fail after hundreds cycles of temperature

[z] E-mail: TaoChih@itri.org.tw

Downloaded on 2016-09-16 to IP 130.203.136.75 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

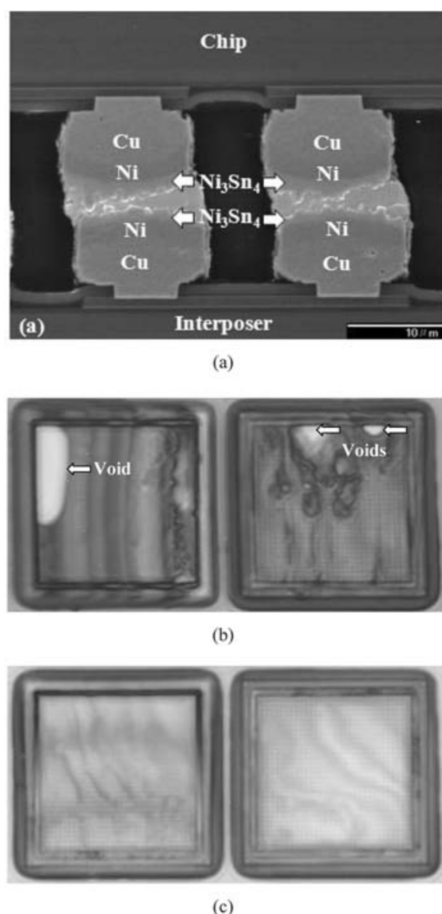

Figure 1. Morphologies of (a) the reflow bonded microjoints, (b) C-SAM image of the microgap cleaned by the solvent and then sealed by underfill, and (c) C-SAM image of the microgap cleaned by the saponifier and then sealed by underfill.

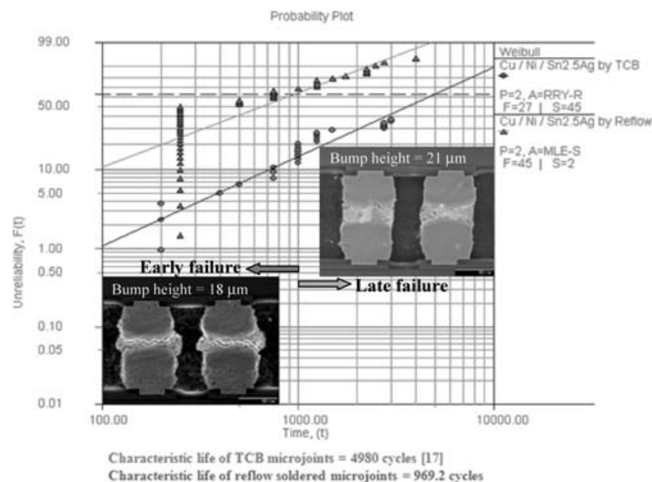

Figure 2. Lifespan comparison of the TCB and the reflow soldered microjoints under temperature cycling.

cycling. Furthermore, the same phenomenon is also found by Lee et al.[17] in the 4 μm Cu/4 μm Sn reflow bonded microjoints. Comparing with those results, the interconnection of microbumps by reflow soldering was thought to be advantageous to reduce the discrepancy in the thicknesses of Ni_3Sn_4 layer because the original one at chip-side slowed down the dissolution of Ni atoms into the liquid solder alloy, and the Ni layers at both chip-side and interposer-side reacted with liquid solder alloy equally in the isothermal reflow soldering without thermal gradient.

The C-SAM images of the microgaps cleaned by the solvent and the saponifier then sealed by underfill were respectively exhibited in Figures 1b and 1c, no gas void was detected in the latter one, indicating that the saponifier was more effective to remove the flux residues inside the microgaps than the solvent, and a flip-chip-compatible bonding technology for microbump assembly has been successfully established in this work.

In Figure 2, the Weibull analyses of the mcirojoints produced by different bonding methods were compared, and the cross-sections of early and late failures were included. The characteristic life of the TCB case has been determined to be 4,298 cycles in the report of Huang et al.,[16] and that of the reflowed one under the same test condition was calculated to be 969.2 cycles, indicating that TCB was more effective to produce reliable microjoints for chip stacking because the defects resulted from the formation and growth of Ni_3Sn_4 as soldered was eliminated by the pressure, as Saber et al.[18] reported. Based on the statistics of 12 failed samples after 250 cycles of TCT, the microjoints with a standoff height less than 18 μm were early failed easily. Oppositely, the lifespan was significantly prolonged when the standoff height was above 20 μm.

A simulation model was established by the boundary conditions of various standoff heights of 18 μm and 21 μm showed in Figure 2, and the stress contours were given in Figure 3. Accordingly, the thermal fatigue stress concentrated at the interfaces between the Ni layer

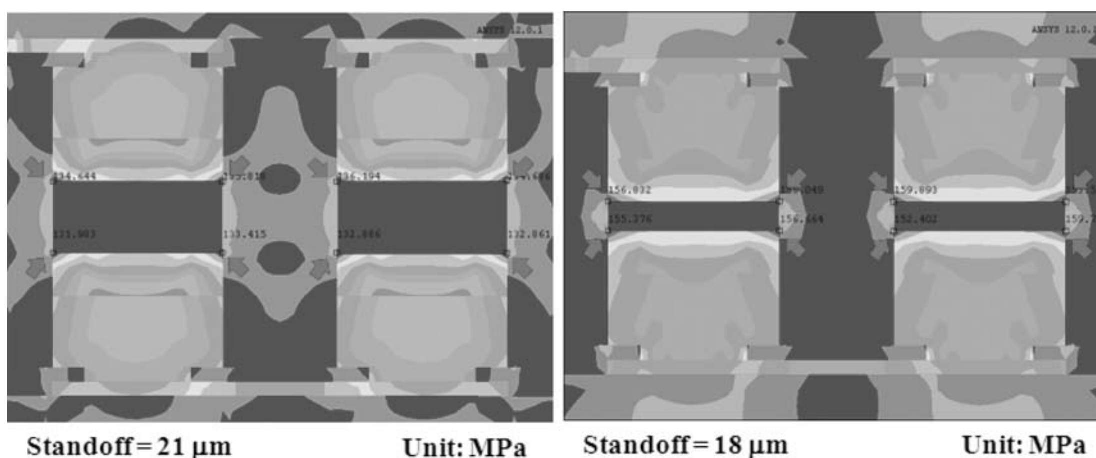

Figure 3. Stress contours of the microjoints with different standoff heights.

Downloaded on 2016-09-16 to IP 130.203.136.75 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

and the Sn2.5Ag microbump at both chip-side and interposer-side. Furthermore, the variations of the stress values at different locations were less than 3%, which was quite different to the stress behavior of the board-level solder joints with stress concentration at chip-side[19] because the fatigue stress was coming from the expansion of underfill and the dramatic warpage of printed circuit board, respectively.

As per Figure 3, the microjoints with a standoff height of 18 μm sustained 10% higher thermal fatigue stress than the ones with a standoff height of 21 μm. It has been pointed out that a thicker intermetallic layer at the interface between solder alloy and solder pad is beneficial to decrease the normal stress and to enhance the resistance to deformation for board-level solder joints.[20] However, the proportion of Ni_3Sn_4 in the microjoint with a shorter standoff height was much higher than that of the other case. Furthermore, Ni_3Sn_4 is more brittle than solder alloy and is not easily deformed to release the stress, therefore the microjoints with a lower solder volume suffered a higher thermal fatigue stress as temperature cycled.

In order to eliminate the disturbance from the defects induced by the formation and growth of Ni_3Sn_4 as soldered without pressure, the microjoints formed by TCB and then experienced TCT up to 3000 cycles were cross-sectioned by FIB, and the morphologies were shown in Figure 4. Accordingly, some tiny micropores (MPs) were found in the interconnection zone of the microjoints with a standoff height of 17.2 μm because of the growth of Ni_3Sn_4[16] and the accumulation of Ag_3Sn[21] as heated, which brought a volume contraction of 10.7% by the reaction of $3Ni + 4Sn \rightarrow Ni_3Sn_4$,[22] and that was 36.18% accompanied the reaction of $Ag + 3Sn \rightarrow Ag_3Sn$, based on the calculated atomic volume of Ag_3Sn of 18.3 $Å^3$.[23]

As Figure 4 showed, the dimension of micropores increased significantly when the standoff height of microjoints was reduced to 15 μm because a shorter diffusion distance catalyzed the reactions mentioned above, and the volume of solder alloy was insufficient to grow together.[18] Unlike the TCB microjoints, the defects might form as early as in the pressure-free reflow soldering. An example has been given in the report of Lee et al.[17] that the shear strength of TCB microjoints is much higher than that of reflow-soldered ones. Furthermore, the growth of Ni_3Sn_4 in the reflow-soldered microjoints under temperature cycling was balance and the interfacial fracture found in the TCB microjoints was no longer found in it.[11] Correspondingly, the disconnection of the microjoints assembled by reflow was ascribed to the large-sized micropores in the interconnection zone. As a higher thermal fatigue stress was exerted on the microjoints with a lower standoff height, the early failure occurred, and the lifespan was therefore degraded.

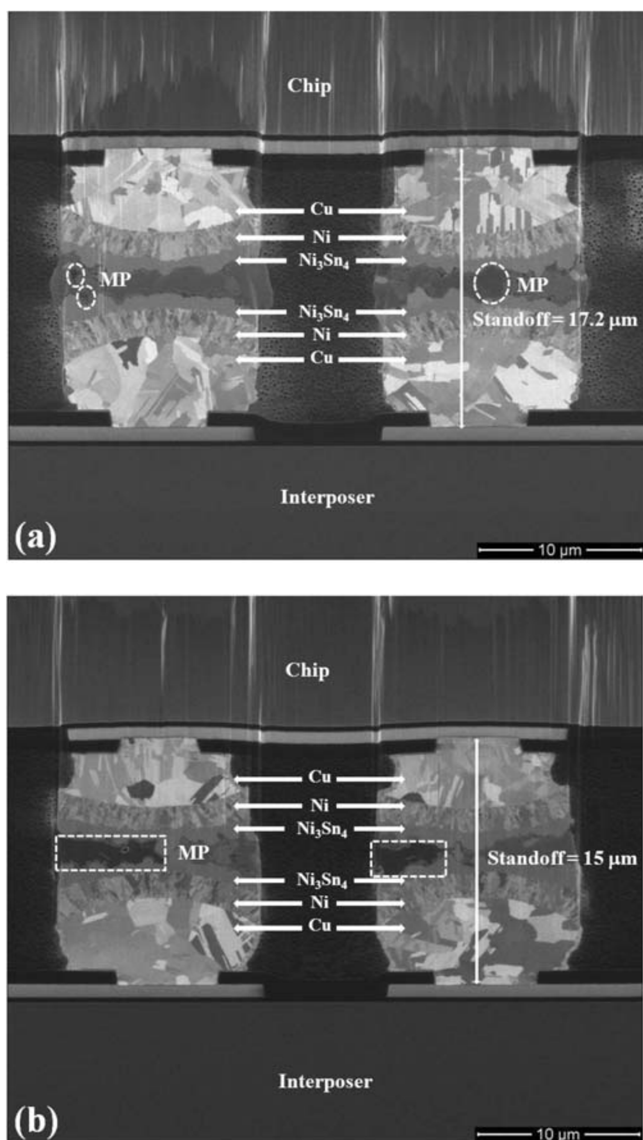

Figure 4. FIB images of the TCB microjoints with (a) standoff height of 17.2 μm and (b) standoff height of 15 μm experienced TCT up to 3000 cycles.

Conclusions

Based on the results of numerical analyses and experiments, a higher thermal fatigue stress and defects induced by phase transformation were found in the microjoints with a lower standoff height indeed, which resulted in the early failure and the degradation of lifespan if the chip stacking was carried out by a conventional reflow soldering process.

References

1. P. R. Morrow, C. M. Park, S. Ramanathan, M. J. Kobrinsky, and M. Harmes, *IEEE Electron Device Lett.*, **27**(5), 335 (2006).
2. C. S. Tan and R. Reif, *Electrochem. Solid State Lett.*, **8**(6), G147 (2005).
3. C. Ventosa, C. Morales, L. Libralesso, F. Fournel, A. M. Papon, D. Lafond, H. Moriceau, J. D. Penot, and F. Rieutord, *Electrochem. Solid State Lett.*, **12**(10), H373 (2009).
4. D. F. Lim, X. F. Ang, J. Wei, C. M. Ng, and C. S. Tan, *Electrochem. Solid State Lett.*, **13**(12), H412 (2010).
5. K. Sakuma et al., *IBM J. Res. & Dev.*, **52**(6), 611 (2008).
6. C. J. Zhan et al., in *Proceedings of International Microsystems Packaging Assembly and Circuits Technology Conference*, IEEE, p. 154 (2009).
7. C. J. Zhan et al., in *Proceedings of Electronic Components and Technology Conference*, IEEE, p. 1043 (2010).
8. Y. M. Lin et al., in *Proceedings of Electronic Components and Technology Conference*, IEEE, p. 351 (2011).
9. A. Yu et al., in *Proceedings of Electronic Components and Technology Conference*, IEEE, p. 6 (2009).
10. N. Khan et al., in *Proceedings of Electronic Components and Technology Conference*, IEEE, p. 884 (2010).
11. T. C. Chang et al., in *Proceedings of International Conference on Electronics Packaging*, JIEP and IEEE, p. 221 (2011).
12. S. Wiese and S. Rzepka, *Microelectron. Reliab.*, **44**, 1893 (2004).
13. R. Iannuzzelli, in *Proceedings of Electronic Components and Technology Conference*, IEEE, p. 410 (1991).
14. W. K. Choi, S. Y. Jang, J. H. Kim, K. W. Paik, and H. M. Lee, *J. Mater. Res.*, **17**, 597 (2002).
15. M. O. Alam and Y. C. Chan, *J. Appl. Phys.*, **98**, 123527/1-4 (2005).
16. S. Y. Huang et al., in *Proceedings of Electronic Components and Technology Conference*, IEEE, p. 886 (2011).
17. C. K. Lee et al., in *Proceedings of Electronic Components and Technology Conference*, IEEE, p. 1468 (2011).
18. S. Bader, W. Gust, and H. Hieber, *Acta Metall. Mater.*, **43**, 329 (1995).
19. M. N. Tamin and Y. B. Liew, in *Proceedings of National Seminar on Computational and Experimental Mechanics*, Computational & Experimental Mechanics Research Group, p. 351 (2005).
20. H. J. Chang, J. H. Chou, T. C. Chang, C. J. Zhan, M. H. Hon, and C. S. Hsi, *J. Electron. Packaging*, **133**, 0210004/1–8 (2011).
21. R. W. Yang, Y. W. Chang, C. Chen, T. C. Chang, C. J. Zhan, and J. Y. Juang, in *Proceedings of International Microsystems Packaging Assembly and Circuits Technology Conference*, IEEE, p. 1 (2010).
22. H. D. Blair, T. Y. Pan, and J. M. Nicholson, in *Proceedings of Electronic Component Technology Conference*, IEEE, p. 259 (1998).
23. H. Dong, L. Fan, K. S. Moon, C. P. Wong, and M. I. Baskes, *Modelling Simul. Mater. Sci. Eng.*, **13**, 1279 (2005).

Downloaded on 2016-09-16 to IP 130.203.136.75 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).