Materials Science Forum
ISSN: 1662-9752, Vols. 821-823, pp 847-850
doi:10.4028/www.scientific.net/MSF.821-823.847

Submitted: 2014-09-12
Revised: 2014-11-24
Accepted: 2015-01-05
Online: 2015-06-30

27 kV, 20 A 4H-SiC n-IGBTs

Edward Van Brunt[1, a*], Lin Cheng[1], Michael J. O'Loughlin[1], Jim Richmond[1], Vipindas Pala[1], John Palmour[1], Charles W. Tipton[2], and Charles Scozzie[2].

[1]Cree, Inc. 4600 Silicon Drive, Durham, NC 27703, USA

[2]U.S. Army Research Laboratory, 2800 Powder Mill Rd. Adelphi, MD, USA

[a] Edward_Vanbrunt@cree.com

Keywords: 4H-SiC, n-IGBTs, Ultra High Voltage

Abstract. We report our recently developed 27 kV, 20 A 4H-SiC n-IGBTs. Blocking voltages exceeding 24 kV were achieved by utilizing thick (210 μm and 230 μm), lightly doped N- drift layers with an appropriate edge termination. Prior to the device fabrication, an ambipolar carrier lifetime of greater than 10 μs was measured on both drift regions by the microwave photoconductivity decay technique. The SiC n-IGBTs exhibit an on-state voltage of 11.8 V at a forward current of 20 A and a gate bias of 20 V at 25 °C. The devices have a chip size of 0.81 cm^2 and an active conducting area of 0.28 cm^2. Double-pulse switching measurements carried out at up to 16 kV and 20 A demonstrate the robust operation of the device under hard-switched conditions; coupled thermal analysis indicates that the devices can operate at a forward current of up to 10 A in a hard-switched environment at a frequency of more than 3 kHz and a bus voltage of 14 kV.

Introduction

Recent advances in material quality have led to the availability of ultra-thick 4″ 4H-SiC epi-layers capable of supporting devices with blocking voltages in excess of 20 kV [1]. Devices in this blocking voltage regime are of interest to reduce the number of series-connected devices in future power transmission applications [2]. Although using unipolar power switches such as power MOSFETs confer a benefit to the maximum possible switching frequency, to achieve simultaneous high current and high voltage handling capability, bipolar devices such as IGBTs or thyristors are preferred.

4H-SiC Ultra-high blocking voltage device development has been hindered in the past by low as-grown ambipolar carrier lifetimes, which are typically on the order of 1 μs for as-grown material [3]. A reduction of lifetime limiting deep levels can be achieved by changing epitaxial growth conditions [4], at the cost of poor surface morphology, which is not conducive to the fabrication of large-area devices capable of handling high on-state currents. The development of lifetime enhancement procedures [3,5] has resulted in ambipolar lifetimes of 10 μs or more for thick 4H-SiC n-type epitaxial layers. This enables the continued scaling of 4H-SiC device blocking voltage. Without high lifetime, minority carrier diffusion lengths are too short to guarantee complete conductivity modulation of the drift region.

This work describes the development of 4H-SiC n-IGBTs designed for a nominal avalanche rating of 24 kV fabricated on 210 μm and 230 μm thick epitaxial blocking layers with doping concentrations in the range of $1\sim2.5\times10^{14}$ cm^{-3}. A high blocking voltage of 27.5 kV was achieved by utilizing a 230 μm drift region. A lifetime enhancement treatment consisting of 15 hours of thermal oxidation increased as-grown ambipolar carrier lifetime from 1.6 μs to over 10 μs. On-state voltages of 11.8 V at 20 A forward current and 25 °C were achieved, which corresponds to a DC rating of 20 A current capability at a thermal power limit of 300 W (370 W/cm^2).

Device Design and Fabrication

A simplified cross-section and macro-photograph of the fabricated SiC n-IGBTs are shown in Fig. 1. Two different designs were selected for evaluation: a deep punch-through design (210 μm

thick, 1×10^{14} cm^{-3} doped, $V_{PT} \approx 4$ kV) and a soft punch-through design (230 µm thick, 2.5×10^{14} cm^{-3} doped, $V_{PT} \approx 12$ kV). It is perceived that soft punch-through drift regions will result in lower dv/dt transients during switching [6], and thus lower capacitive current spikes from the antiparallel diode and increased Electromagnetic Compatibility (EMC). Both drift region designs result in calculated parallel plane breakdown voltages greater than 24 kV [7]. The n-type field-stop buffer was approximately 1-2 µm thick, and doped sufficiently to avoid reach-through breakdown at the avalanche voltage. A 1.5 mm wide edge termination consisting of floating guard rings was used to alleviate high electric fields at the active region edge. Prior to device fabrication, a lifetime enhancement procedure consisting of 15 hours of thermal oxidation at 1300 °C was performed to increase the as-grown drift ambipolar lifetime from less than 2 µs to more than 10 µs. Details of the device fabrication can be found in reference [1].

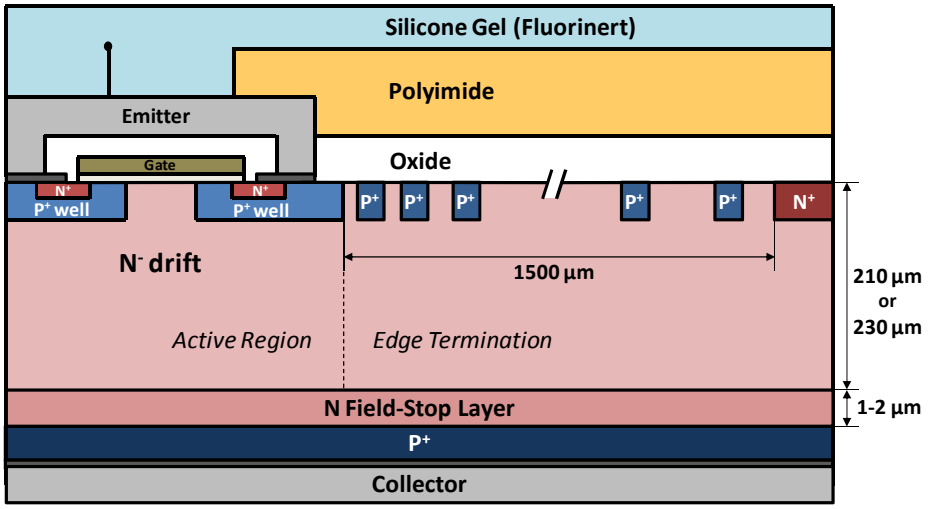

Fig. 1 (a). Cross section of fabricated 4H-SiC n-IGBTs including passivation scheme to achieve high blocking voltage.

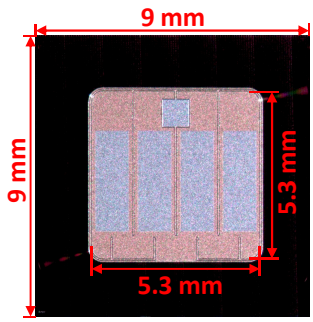

Fig. 1 (b). Plan view macro-photograph of fabricated n-IGBT die.

Device Static Characteristics

The static IV characteristics measured in pulse mode for both device blocking layers are shown in Fig. 2. A positive temperature coefficient is observed for both device blocking layers. At room temperature, the on-state forward voltage drop at 20 A for the n-IGBT with a 210 µm drift region was 11.7 V, and 11.8 V for the IGBT with a 230 µm thick drift region.

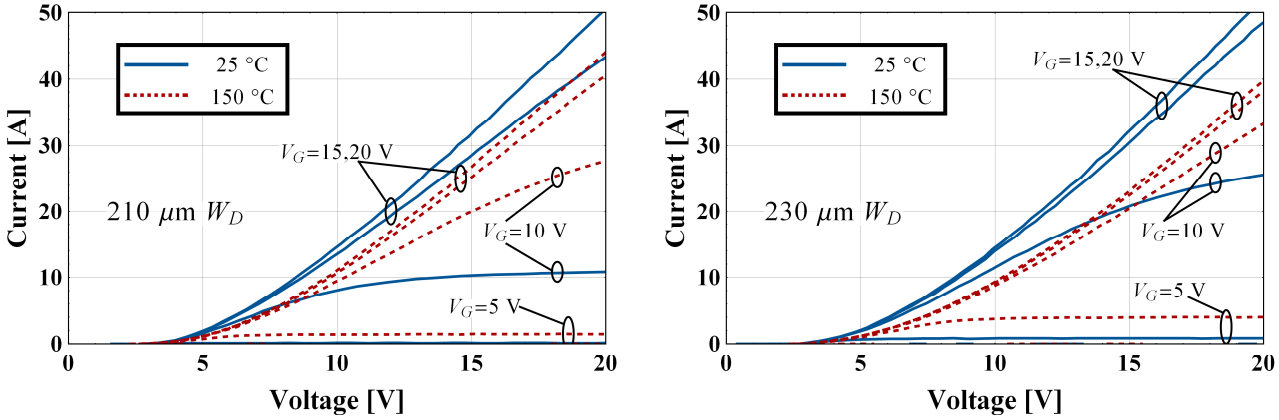

Fig. 2. IV characteristics of IGBT with 210 µm drift region (left) and 230 µm drift region (right)

The devices have approximately the same on-state forward voltage drop with 20 V gate bias across the range of operating currents, indicating that the minority carrier lifetime is sufficient to guarantee conductivity modulation of the drift region. The static forward blocking current-voltage characteristic for the best measured device is shown in Fig. 3, showing under 10 µA of leakage at

27.5 kV. Device threshold voltages at 1 μA of current and V_C=10 V were greater than 2 V, guaranteeing normally-off operation.

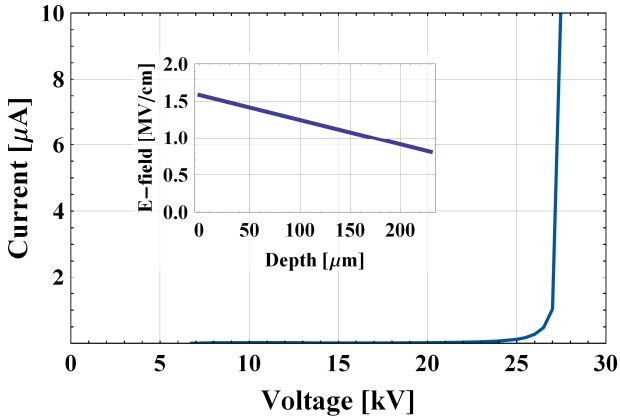

Fig. 3. Static blocking characteristics for n-IGBT with 230 μm thick drift region at with V_{GS}=0 V. Inset: Calculated electric field with applied voltage of 27.5 kV.

Device Dynamic Performance

The inductive load double-pulse turn-off switching waveforms at a bus voltage of 14 kV and load current of 20 A at 25 °C, 75 °C, and 125 °C are shown in Fig. 4. Two series 10 kV JBS diodes with balance resistors were used as a freewheeling device; the air-core load inductor used had a value of 13.8 mH. The current "notch" observed immediately after the initial voltage rise is a result of the diode capacitance; computations of current flow through the diode capacitance exactly match the observed current drop. A low impedance gate drive was used to switch the device as quickly as possible. As can be seen, increasing temperature leads to increased stored charge for both devices, and thus increased switching times and larger turn-off losses. Switching times for both devices are comparable across the range of temperature, however, the deep punch-through device (W_D=210 μm) has a faster transition to the bus voltage upon punch-through, which is desirable from a turn-off energy standpoint. The soft punch-through design (W_D=230 μm) requires more voltage to reach the punch-through condition, and thus has a higher instantaneous power loss for a longer period of time during the switching transient.

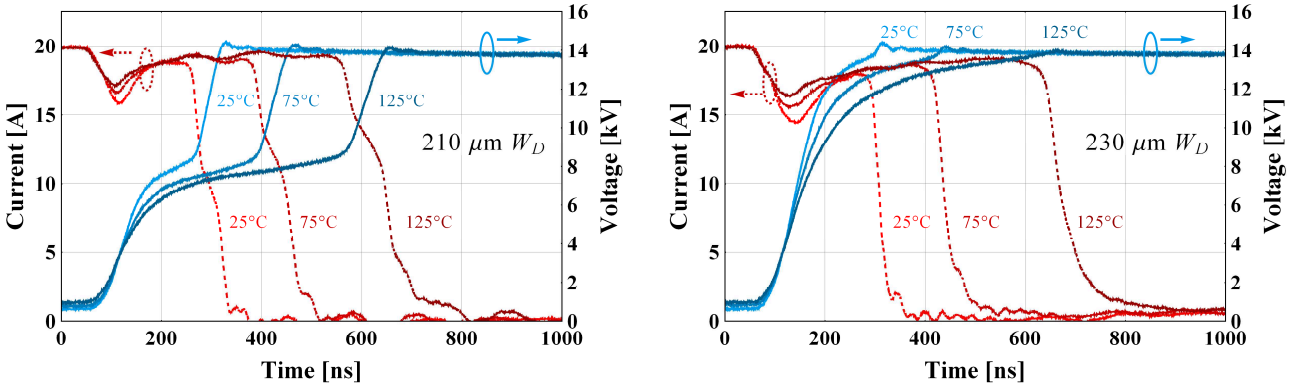

Fig. 4. 14 kV, 20 A double pulse switching waveforms for n-IGBT with 210 μm deep punch-through drift region (left) and 230 μm soft punch-through drift region (right).

It should be noted that although the deep punch-through design has a fast transition to the blocking voltage upon punch-through, the values of dv/dt observed for this device are not dissimilar to the values observed for the soft-punch through design. The peak value of dv/dt for the deep-punch through device is 120 kV/μs, and occurs during the fast transition to the bus voltage after punch-through; this peak is comparable to the dv/dt of 100 kV/us that occurs immediately after switching. Conversely, as a consequence of its slightly higher transconductance (Fig. 2), the soft punch-through design has a peak dv/dt of 170 kV/us that occurs early in the turn-off transient. Thus, the deep punch-through design is preferred not only from a turn-off energy standpoint, but for EMC as well.

Performance Evaluation and Discussion

Based on the measured current-voltage characteristics and switching loss characteristics across current and temperature, the static current rating as well as dynamic thermal performance of the fabricated IGBTs in a converter application can be evaluated. The static current rating can be

determined by considering a thermal power limit of 300 W (370 W/cm^2 for the 0.81 cm^2 die). This rating corresponds to a thermal resistance of 0.2 K/W, a junction temperature of 150 °C, and a module base-plate temperature of 90 °C. Based on this and the IV characteristic shown in Fig. 2, the devices can be rated at 20 A DC at T_J=150 °C and V_F=14.0 V.

Thermal analysis was conducted to the switching and conduction loss components of both the deep punch-through and soft-punch through devices. Linear models were fit to the measured conduction and switching losses of both device types and evaluated for a boost chopper application at 50% duty cycle; the resultant coupled thermal system was solved for a junction temperature of 150 °C. To ensure thermal stability, the inequality $\partial P(f, I_F, T)/\partial T \cdot R_{TH} \leq 1$ must be satisfied [8]; the operating points shown in Fig. 5 are far below this limit. The analysis indicates that the deep punch-through design with a thinner drift region is capable of operation at 10 A and a switching frequency of more than 3.0 kHz at T_J=150 °C, and the soft-punch through design is capable of 10 A at 2.3 kHz. The deep punch-through device was switched at a bus voltage of up to 16 kV. The turn-off and -on switching loci for the 16 kV bus voltage and 20 A forward current are shown in Fig. 6.

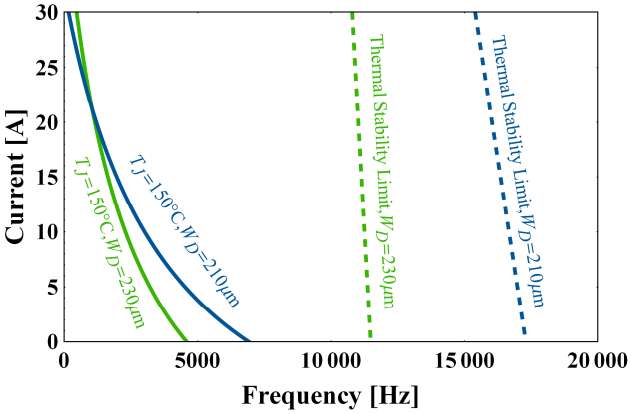

Fig. 5. Frequency limit/current for hard-switched boost chopper as determined by coupled thermal analysis with T_J=150 °C, V_{BUS}=14 kV

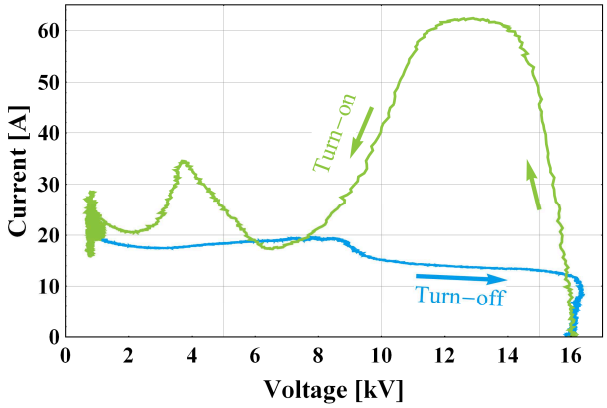

Fig. 6. Measured turn-on and turn-off switching loci for deep punch-through device at V_{BUS}=16 kV, 20 A operation at 125 °C

Conclusion

4H-SiC n-IGBTs with an avalanche breakdown voltage of 27.5 kV and total area of 0.81 cm^2 have been successfully fabricated. Devices with 210 μm, lighter doped drift regions had superior overall performance to devices with 230 μm, heavier doped drift regions with no penalty to the maximum observed switching dv/dt, and are thus a preferred design for ultra-high voltage applications.

Acknowledgement: Research was sponsored by the Army Research Laboratory and was accomplished under Cooperative Agreement Number W911NF-10-2-0038. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Army Research Laboratory or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein.

References

[1] E. Van Brunt et al, Proc. ISPSD 2014, pp. 358-361, 2014
[2] Q. Zhang et al, IEEE Trans Power Electronics, vol. 25, no. 12, pp 2889-2896, 2010
[3] L. Cheng et al, Proc. MRS Spring Meeting 2013, pp. 329-333
[4] T. Kimoto et al, Jpn. J. Appl. Phys., vol. 42, no. 12, pp. 7294-7295, 2003.
[5] T. Hiyoshi et al, Appl. Phys. Expr 2, 041101, 2009
[6] B. J. Baliga, "Advanced High Voltage Device Concepts," Springer, 2012
[7] A. O. Konstantinov et al, App. Phys. Lett., vol. 71, pp 90-92, 1997
[8] H. Wang et al, Proc. IAS 2005, pp. 388-392, 2005.

Silicon Carbide and Related Materials 2014
10.4028/www.scientific.net/MSF.821-823

27 kV, 20 A 4H-SiC n-IGBTs
10.4028/www.scientific.net/MSF.821-823.847

DOI References
[2] Q. Zhang et al, IEEE Trans Power Electronics, vol. 25, no. 12, pp.2889-2896, (2010).
10.1109/TPEL.2010.2079956
[4] T. Kimoto et al, Jpn. J. Appl. Phys., vol. 42, no. 12, pp.7294-7295, (2003).
10.1143/JJAP.42.7294
[5] T. Hiyoshi et al, Appl. Phys. Expr 2, 041101, (2009).
10.1143/APEX.2.041101
[6] B. J. Baliga, Advanced High Voltage Device Concepts, Springer, (2012).
10.1007/978-1-4614-0269-5
[7] A. O. Konstantinov et al, App. Phys. Lett., vol. 71, pp.90-92, (1997).
10.1063/1.119478