SI-GE PHOTODETECTION TECHNOLOGIES FOR INTEGRATED OPTOELECTRONICS

A DISSERTATION

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OF STANFORD UNIVERSITY

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

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September 2007

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and quality, as dissertation for the degree of Doctor of Philosophy.

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(Prof. Mark Brongersma)

Approved for the University Committee on Graduate Studies

In the name of Allah, the most compassionate, the most merciful…

All truths are easy to understand once they are discovered;

the point is to discover them.

Galileo Galilei

ABSTRACT

The communications bottleneck is identified as one of the grand challenges in the progress of silicon computation. While individual logic elements have become significantly faster, computational speed is limited by the communication between different parts of a processor. Traditional copper wires are efficient at short distances, but they suffer excessive power dissipation and delay in global lines, and cannot cope with the ever growing bandwidth demand. Moreover, with the chip architectures evolving towards a modular design, the requirements for increased bandwidth density further strain the electrical interconnects. Optical interconnects (OIs) can provide a solution to the communication bottleneck by alleviating significant power dissipation and delay problems faced by copper wires. Monolithically integrated photodetectors with very low capacitance are sought after for the receiver end of high performance OIs.

In the first part of this dissertation, Ge based metal-semiconductor-metal (MSM) optical detectors integrated on Silicon are discussed. The Ge layer is grown by a novel multi-step Ge-on-Si direct epitaxial growth technique. An important byproduct of this growth technique is tensile strain within the Ge film, resulting in enhanced absorption around 1550 nm. Experimental results of electrical and optical characterization of Ge detectors are presented. A very high responsivity of 0.84 A/W at 1550 nm is reported. The results of physical investigation of the origin of strain in the Ge layers are presented, and a significant red shift in the absorption edge of Ge is reported in the grown films.

A novel CMOS compatible optoelectronic switch is introduced in the second part of this dissertation. The proposed device is a Si MOSFET with Ge gate. The basic operation of the proposed device was investigated by simulations. An experimental proof-of-principle operation was demonstrated. The gate photocurrent is amplified by the MOSFET gain at the drain terminal. 1000 × amplification was reported. The speed of the device and the potential of complementary function in are discussed by simulations.

ACKNOWLEDGEMENTS

I not only use all of the brains I have, but all I can borrow.

Woodrow Wilson

It is close to the end of my six-year-long adventure here at Stanford… My father always said "starting something is almost like finishing it". That view can only be truly understood at the end.

Stanford gave me all the great opportunities that a Ph.D. student should have. The perfect blend of research and education, combined with a beautiful climate and wonderful neighborhood put Stanford way ahead of other top universities within the US.

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Fatih Sarioglu, Utkan Demirci, Omer Oralkan, Ragip Pala, Ryohei Urata, Noah Helman, Jon Roth, Kailash Gopalakrishnan, Il Wung Jung, Yaocheng Liu, Raymond Woo.

No words would ever do justice to express my deepest thanks and gratitude to my most wonderful family – my parents and my sister, Reyyan. I will be eternally grateful to them for being there for me at all times. Their continuous love, sacrifice, support and encouragement have allowed me to pursue my ambitions…

… In what is following, you will read about a part of my technical experience here at Stanford. Of course it is difficult to fit everything in one thesis; and most probably there are a lot of details I have left out. Nevertheless, I hope the following pages will provide you with a coherent story of our optoelectronic technologies.

DEDICATION

To my sister Reyyan and my loving parents

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CHAPTER 1: INTRODUCTION

Somewhere, something incredible is waiting to be known.
Carl Sagan

This dissertation describes our contributions to the integrated photonics, optical detection technologies and optoelectronic transformation devices [1-25]. This introductory chapter begins with a brief historical background and discussion of the motivation of this work. The limitations of electrical wires and benefits of optical links are summarized. Finally, the organization of the dissertation is presented.

1.1 MOTIVATION

Since their invention more than half a century ago, transistors have driven and dominated the semiconductor industry. In 1965, five years after the first practical demonstration of metal oxide semiconductor field effect transistor (MOSFET), Gordon Moore observed that the number of transistors in an integrated circuit (IC) was doubling every two years [26] as a result of a dramatic scaling of the feature sizes. While individual logic elements have become significantly smaller and faster, computational speed is limited by the communication between different parts of digital systems. This bottleneck is identified as one of the grand challenges in the progress of integrated electronics [27].

The chain of telecommunication systems from ultra-long distances in metro networks down to chip scale communications versus the business volume of the corresponding technology is illustrated in Fig. 1.1 [28]. Since the introduction of low-loss silica fibers, optics has been dominating the long haul communications and it has consistently made its way down to shorter distances. Today, optics has moved deep into systems and already reached into the server cabinet as depicted in Fig. 1.2 [29]. There are many physical reasons for replacing electrical cables with optics [30-34]. Signals in both optical and electrical links are carried by electromagnetic waves. Information in typical electrical wires such as coaxial cables propagates almost at the velocity of light similar to that in optical links as illustrated in Fig. 1.3 [34]. However, as the modulation frequencies

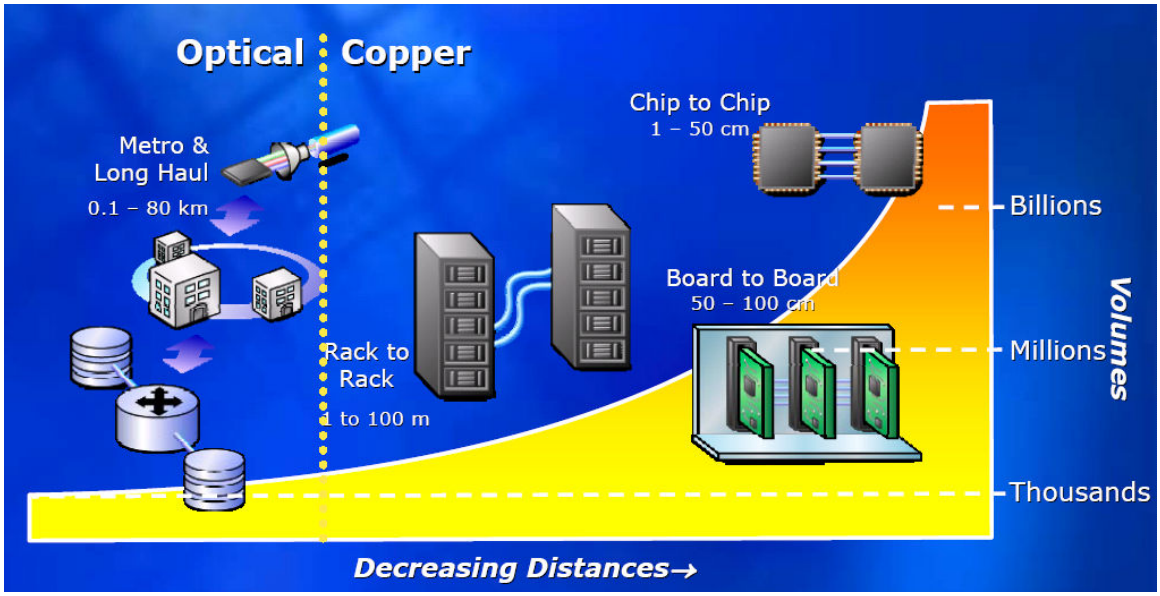
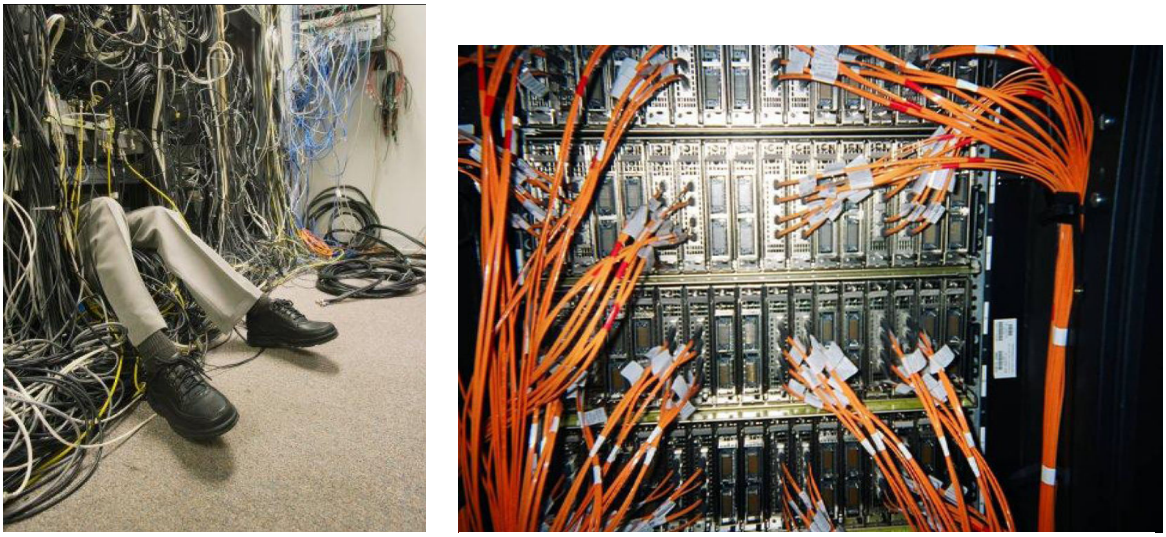


Fig. 1.1 The chain of communication systems versus the length of the interconnection and the business volume of the corresponding technology.



(a) (b)

Fig. 1.2 A typical server cabinet with (a) electrical cables (b) optical links interconnecting between different sections.

increase, the traditional electrical wires are becoming increasingly resistive and the signals move at a slower rate due to dissipative wave propagation. Even the low-loss electrical wires suffer from skin effect, the phenomenon by which conduction takes place only in an increasingly thin layer near the surface of a conductor at higher frequencies. Signal distortion is becoming a significant problem in deeply scaled wires due to increasing copper resistivity and signal attenuation. Furthermore, electrical wires suffer from cross-talk due to electromagnetic interference. The cost of electrical lines has become an important issue. In other words, it is increasingly more expensive to run electrical wires at growing bitrates.

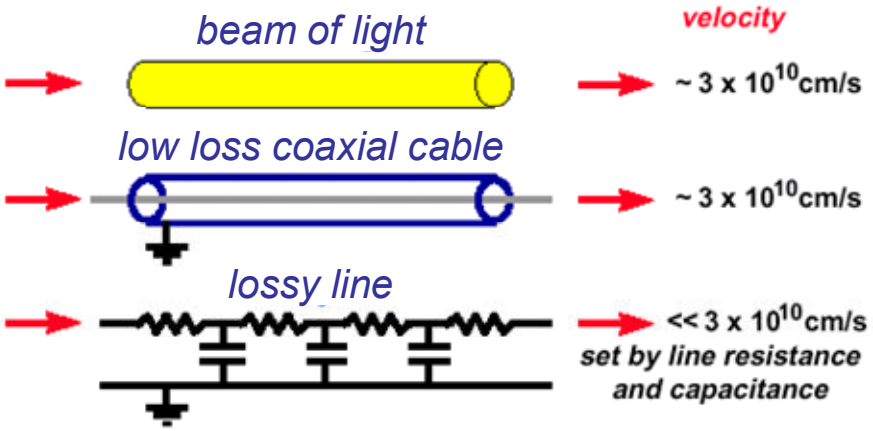


Fig. 1.3 Illustration of types of optical and electrical propagation and their velocities. (After [34])

An excellent review of the potential benefits offered by optical interconnections is presented in [34] based on the fundamental physical differences of the higher frequency, shorter wavelength and larger photon energy of optics compared to electrical interconnections. Optics has negligible propagation loss from large bandwidth signals because the carrier frequency of light is very high compared to any practical modulation frequency. On the other hand, electrical interconnections suffer from significant signal distortion and frequency dependent cross-talk at high modulation frequencies. Optics further enjoy unique benefits such as increased timing precision owing to short optical pulses and the ability to transmit multi-channels down a single optical link thanks to wavelength division multiplexing. Both of these advantages are quite common and easy

to produce in optics. Another substantial advantage of optics is the relative ease of guiding the optical wave. The transmitted signal can be confined into the material boundaries of the guiding medium owing to the small wavelength of the optical signals. The large photon energy of light provides voltage isolation between the transmitter and receiver. In addition, optics inherently offers an eloquent solution to the impedance matching crisis faced by electronics owing to the quantum nature of the physical processes [34-37]. While electronic devices have high impedance and low capacitance, the communication between such devices rely on low impedance and high capacitance transmission lines. Line drivers are employed to match the impedance which results in increased power dissipation and chip area at high operation frequencies. Thanks to the quantum nature of the optical impedance transformers, the classical field or voltage is irrelevant. For instance, in a photodiode, the number of electrons and hence the classical voltage that can be extracted is related to the number of photons, therefore the optical power.

1.2 ORGANIZATION OF THE DISSERTATION

Chapter 2 is a brief introduction to advantages and challenges of optical interconnections. The challenges facing electrical wires particularly in chip-to-chip and on-chip communications are summarized. The architecture and operation of traditional optical interconnections are introduced with emphasis on the receiving end of the link.

Chapter 3 describes the dark current reduction mechanisms in metal-semiconductor-metal photodetectors by using asymmetric workfunction and area metal electrodes. Each technique is also demonstrated experimentally on Si and Ge wafers.

Chapter 4 reports on the integration of high efficiency Ge-based photodetectors with Si. The challenge of obtaining high quality Ge layers on Si is briefly described with a summary of past research. The first part of this chapter introduces a new technique to grow Ge heteroepitaxially on Si and presents the characterization results of the layers. The second part explores photodetectors built using such layers and reports the experimental performance of the detectors.

Chapter 5 describes the integration of photodetectors with waveguides based on a robust polymer technology. The polymer waveguide technology which was developed elsewhere is briefly introduced. The experimental results of coupling light into photodetectors and influence of the polymer processing on detector performance are presented.

Chapter 6 presents the optoelectronic switch, a newly introduced optical-to-electronic transformer. This chapter begins with a historical background on phototransistors and FET based optical detectors. The first part of Chapter 6 discusses the structure and the operation of the switch. The principle of the device is explored by simulations and demonstrated by experiments. The second part of this chapter focuses on various applications and benefits of the switch as an optical to electronic conversion device.

Chapter 7 concludes with a brief summary of the key achievements of the dissertation, and briefly discusses future work.

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CHAPTER 2: OPTICAL INTERCONNECTIONS: POTENTIALS AND CHALLENGES

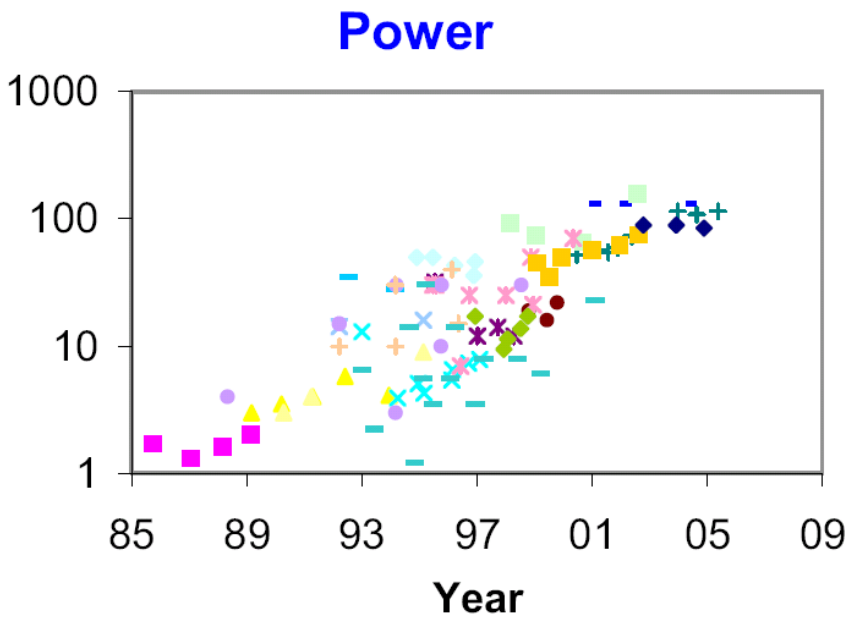
This chapter gives a brief introduction to the critical directions and challenges optical interconnections. The problems facing electrical wires particularly in chip-to-chip and on-chip communications are summarized. The architecture and operation of traditional optical interconnections are introduced with emphasis on the receiving end of the link.

2.1 INTRODUCTION

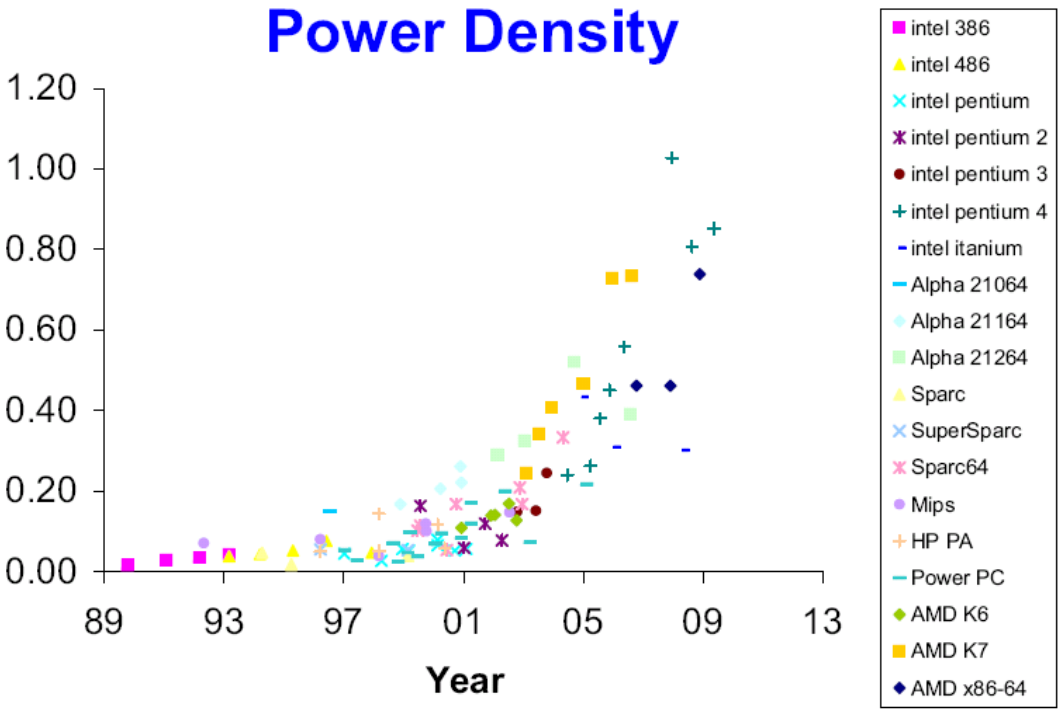
In the past decades, the number of functions per chip has grown exponentially as individual logic units became significantly faster and smaller in size. Today, all leading-edge microprocessors have transistor gate lengths and minimum line widths that are smaller than 100 nm. For the past 20 years, the total power dissipation on a chip has increased by two orders of magnitude from a couple of Watts to several 100s of Watts as shown in Fig. 2.1(a) [1]. The power density is rising at an even faster rate because the chip area is no longer increasing, Fig. 2.1(b). Electrical wires, which are efficient at short distances, begin to face fundamental limitations including excessive power dissipation, insufficient communication bandwidth, and signal latency [1-7]. Optical interconnects can provide a solution to the communications bottleneck by alleviating problems faced by electrical wires [8-14].

2.2 INTER-CHIP INTERCONNECTS

Short distance links can be identified in three categories: (1) board-to-board, (2) chip-to-chip, and (3) on-chip. Optical interconnections are under active development for backplane applications [15,16]. The power dissipation of off-chip electrical and optical links vs. interconnect length are plotted in Fig. 2.2 for different technology nodes [17]. The critical length is defined as the length beyond which optics become more power efficient compared to their electrical counterparts. Fig. 2.2 shows that, as technology scales, optical links will become more power efficient at shorter distances. They are promising to increase the throughput and reduce cross-talk [12].



(a)



(b)

Fig. 2.1 (a) Total chip power vs. the year of introduction. (b) Chip power density vs. the year of introduction.

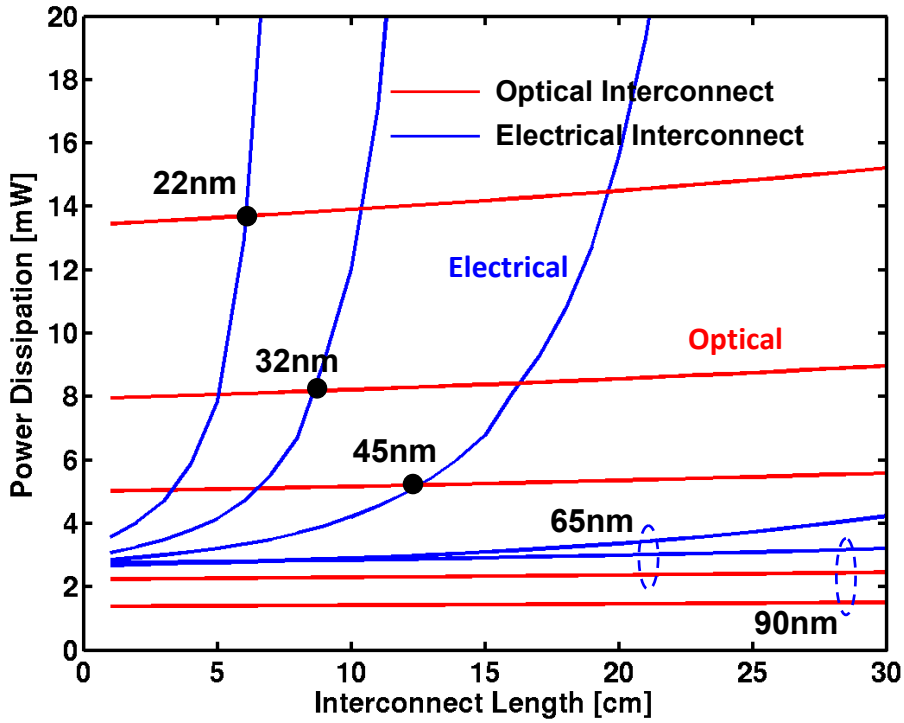


Fig. 2.2 Power dissipation of chip-to-chip interconnections vs. distance.

2.3 INTRA-CHIP INTERCONNECTS

Recently, considerable attention is being paid to determine the feasibility of on-chip optical interconnects [9,13,14,18]. Modern on-chip electrical interconnections utilize copper wires surrounded by a low permittivity dielectric to propagate a signal. Global links on the chip that use long wires tend to exhibit high signal delays, and cross-talk noise. Fig. 2.3 plots the interconnect delay vs. length for on-chip links [9]. The electrical wire delay increases quadratically with distance because both line resistance and capacitance increase with the length of the wire. Long wires are broken down into shorter segments and signal repeaters are used to drive individual segments. This reduces the overall interconnect delay as it makes the delay linear with the interconnect length rather than quadratic. However, as the number of repeaters increase, so does the area and power penalty associated with the repeater circuitry.

Optics is promising to reduce overall interconnect power dissipation. Furthermore, it can increase timing precision by reducing the delay, skew and jitter. Moreover, optical interconnects do not suffer from electromagnetic interference.

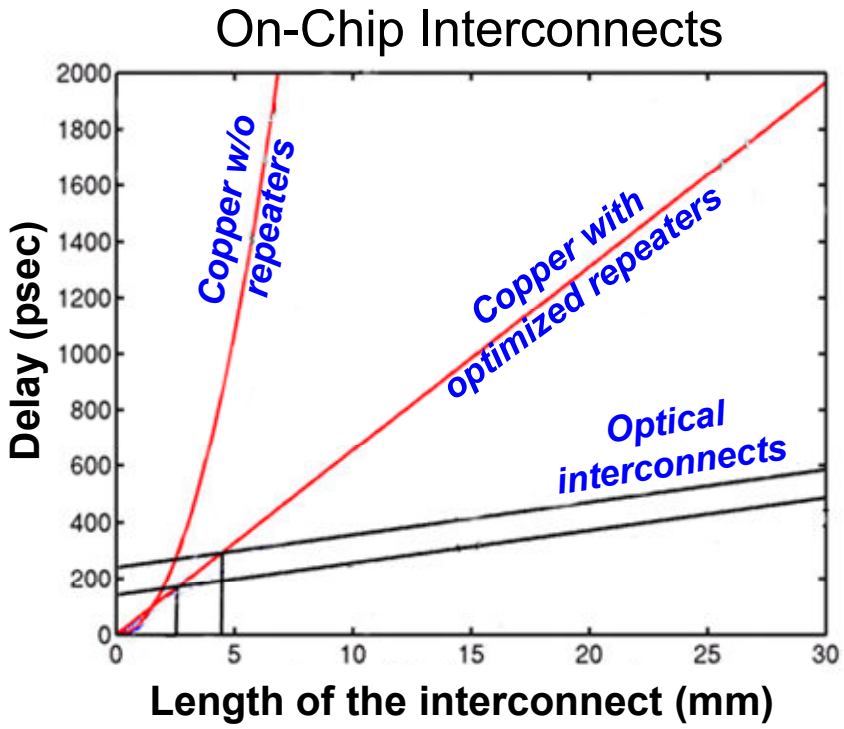


Fig. 2.3 Delay of on-chip electrical and optical links vs. interconnect length.

2.4 ANATOMY OF OPTICAL INTERCONNECTS

There are certain challenges for optics to meet in order to compete with electrical interconnections. Typical optical interconnects require high-speed and low power electronics as well as optical components. Fig. 2.4 illustrates the block diagram of a typical optical link in which light is generated by a continuous wave laser. The modulator is driven by electronic circuits such that it converts the electrical logic signal into an optical signal. The transmitted optical signal propagates in the waveguide to the receiving-end of the optical link. The photodetector converts the optical signal into electrical current which is then converted to electrical voltage by the transimpedance amplifier. The subsequent electronic circuitry amplifies the voltage to the logic level.

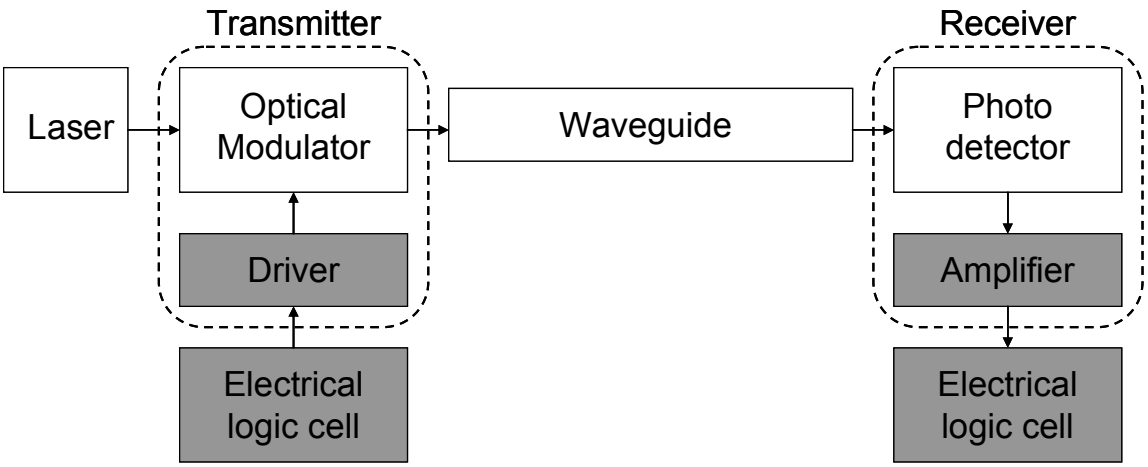


Fig. 2.4 Block diagram of a typical optical interconnect.

2.5 MONOLITHIC INTEGRATION

It is crucial to place the optics in close vicinity to the electronic biasing and amplification circuitry to minimize parasitic effects. In order to realize high performance and low-cost optical links, it is highly desirable to integrate optical components such as the modulator, waveguide and the photodetector with the advanced silicon transistor technology. Recent research has tackled this challenge with significant promise for highly integrated modulators [19-26], silicon-on-insulator (SOI) waveguide technology [27,28], and silicon-germanium based photodetectors [29-39]. In this dissertation, most of the attention will be paid to the receiving-end of optical links, particularly on optical detection technologies and novel optical to electronic transformers.

The absorption coefficients vs. photon wavelength for various semiconductors including Silicon are plotted in Fig. 2.5 [31]. Si is a poor material for optical detection due to its indirect bandgap (E_g) as illustrated in the E-k diagram, Fig. 2.6(a). In addition, the fact that $E_g \sim 1.12$ eV renders it transparent in the near infrared (1300 - 1550 nm), the low-loss window of telecommunication silica fibers. Therefore, a suitable detection material that is efficient in the near infrared and simultaneously compatible with Si is vital for realizing low-cost optical interconnects. This is the point where Germanium comes into the picture as a very promising candidate. Though an indirect bandgap

material (E_g ~ 0.66 eV), Ge is a strong absorber at the near infrared thanks to its direct band transition at 0.8 eV, as shown in Fig. 2.6(b). Furthermore, carrier mobility in Ge is higher than in Si, promising faster operation. The smaller bandgap results in somewhat higher thermally generated noise in Ge-based devices. The most attractive feature of Ge is its compatibility with Si and low temperature processing capability.

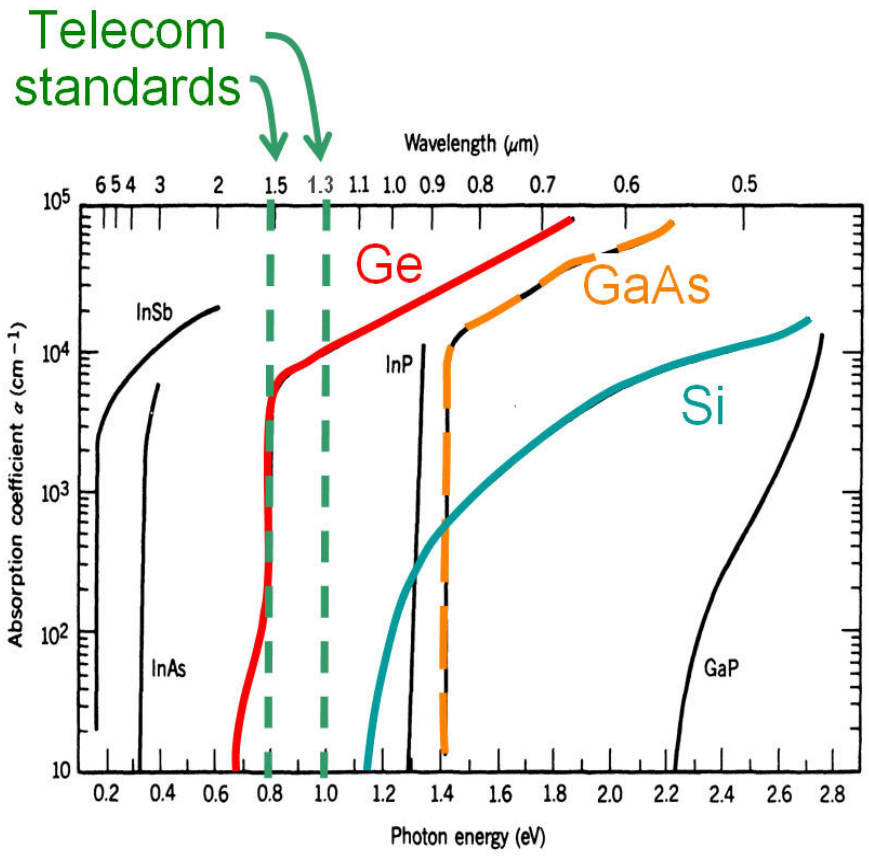
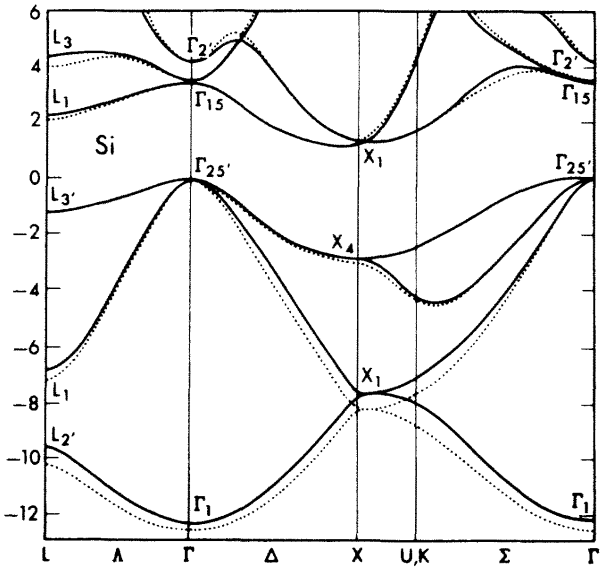
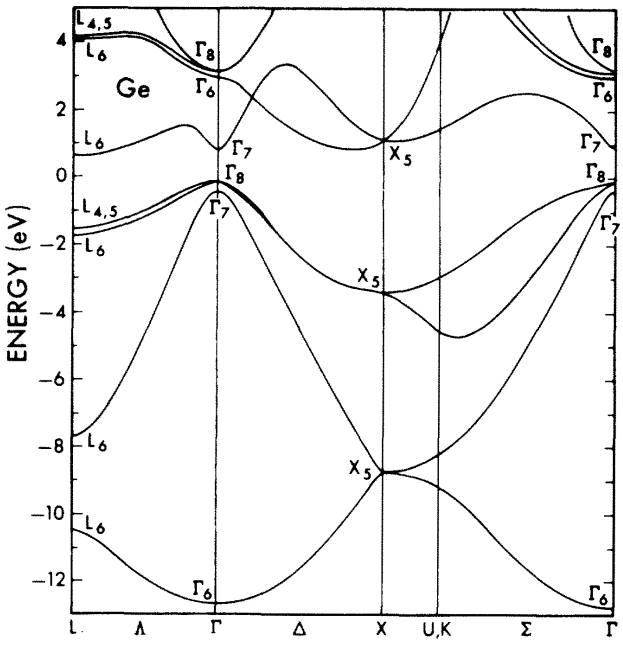


Fig. 2.5 Absorption coefficient for various semiconductors vs. photon energy.

Historically, several devices have been investigated as photodetectors. The most significant among these are p-i-n photodiodes (PIN), avalanche photodiodes (APD) and metal-semiconductor-metal (MSM) detectors. On-chip and chip-to-chip optical interconnection applications will require a large number of high speed photodetectors to be densely integrated with Si electronics at a low-enough cost. APDs provide high sensitivity owing to impact ionization gain. However, APDs are relatively slow and require high bias voltages (20 V/μm) to achieve desired ionization rates.



(a)



(b)

Fig. 2.6 Band structures of (a) Si and (b) Ge (After [41])

The design of APDs is further complicated by the thermal constraints on today's high-end microprocessors. Both PIN and MSM diodes are intrinsically fast devices. However, the relatively large capacitance of PIN detectors limits high speed operation because of RC delay. Furthermore, the fabrication process of MSM detectors is considerably simpler making them attractive from an integration perspective, as well. One drawback of MSM diodes is the relatively higher dark current characteristics, which raises the noise floor and contributes to static power dissipation. Chapter 3 will address this issue in MSMs and will propose techniques to reduce the leakage.

2.6 SUMMARY

In conclusion, both chip-to-chip and on-chip electrical interconnections are facing power, delay and area limitations. Structural and material innovations can only delay the severe problems associated with electrical wires. Optics offers fundamental physical advantages to overcome the limitations faced by copper wires. Thanks to its unexploited benefits such as short pulses, wavelength division multiplexing and the quantum nature of the communication, optics can potentially increase the timing precision, bandwidth density and eliminate the impedance mismatch problem. In a typical optical link, high speed electronics are required to interface with additional optical components. Therefore, monolithic integration of optics with Si electronics is essential to realize low cost and high performance interconnections. Germanium is a promising candidate to bridge low cost electronics with the advantages of optics.

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CHAPTER 3: EFFECTIVE DARK CURRENT SUPPRESSION WITH ASYMMETRIC METAL-SEMICONDUCTOR-METAL OPTICAL DETECTORS IN GROUP IV SEMICONDUCTORS

If I have a thousand ideas and only one turns out to be good, I am satisfied.
Alfred Nobel

This chapter describes the theoretical and experimental study of asymmetric electrode design schemes to suppress the leakage in MSM (metal-semiconductor-metal) photodetectors. Specifically, we report measurements of optical detectors with asymmetric workfunction and asymmetric area electrodes. We demonstrate significant dark current reduction without sacrificing the photo-response and the speed of the detectors. Fabrication, electrical and optical characterization measurements, and the relevant data analysis together with the principles of the theory of the reported Si and Ge MSM photodetectors were primarily conducted by Ali K. Okyay under the supervision of Krishna C. Saraswat. The author would like to acknowledge Dr. Chi On Chui for his help in fabrication process of the photodetectors and fruitful discussions. Some of the significant results presented in this chapter have also been published in *Photon. Technol. Lett.* Vol. 15, 1585, (2003) and *Appl. Phys. Lett.* Vol. 88, 063506, (2005).

3.1 INTRODUCTION

High efficiency and low power photodetectors (PDs) operating at 1.3–1.55 μm (low attenuation regimes of silica fibers) are always sought after in both long-haul and local area communication systems. Historically, direct bandgap III–V semiconductors have been employed to provide efficient detection, however, their hybrid integration with the Si integrated circuit (IC) is complicated [1]. In a monolithically integrated system, the detectors could be closely interconnected to the biasing/driving and amplifying electronic circuitry [2], exhibiting the best possible performance.

The near-infrared photodetection and compatibility with Si technology of Ge-based (Group IV) materials, allow simultaneous fabrication of PDs and Si

complementary metal–oxide–semiconductor (CMOS) receiver circuits in a monolithically integrated fashion [3-5]. Amongst PD structures, the MSM is one of the most promising candidates for receiver optoelectronic integrated circuits (OEICs) due to the ease of integration with preamplifier circuits, low detector capacitance, internal gain, and large device bandwidth [6-9]. Nonetheless, the large dark current (I_{dark}) associated with a lower bandgap and thus low Schottky barrier MSMs like Ge and Si would lead to extra power consumption. The heat generated from this extra power has to be dissipated through the already very hot Si IC substrate. Therefore, a device with low operating voltage (and hence power) while having good noise immunity is always preferred in OEIC applications. Incorporation of a wide bandgap layer within the metal-semiconductor contacts was attempted to enhance the barrier height in III–V MSMs [10], however, similar heterostructures could not be achieved with Group IV material alone. The idea of asymmetric MSM structures to lower I_{dark} was first investigated in low-energy backscattered electron detection in e-beam microcolumns [11], but not for optical applications in Group IV semiconductors. A similar technique was applied for III–V MSM PDs as well [12]. In this work, we examine both theoretically and experimentally the idea of applying asymmetric metal electrodes to significantly suppress MSM-PD I_{dark} by modifying the Schottky barrier heights preferentially [13,14]. We will first discuss the fundamentals of current transport in MSM structures.

3.2 ANALYTIC CURRENT TRANSPORT MODEL IN MSM STRUCTURES

The current-voltage characteristics of an MSM structure are explained based on the thermionic emission theory. An MSM structure is essentially two metal-semiconductor contacts connected back to back. The basic form of a metal-semiconductor-metal structure is a two terminal device having a uniformly doped semiconductor slice with metal contacts on the opposite sides of the slice as depicted in Fig. 3.1(a). Under thermal equilibrium, the energy band diagram of an MSM structure is shown in Fig. 3.1(b). In this figure, ϕ_{n1} and ϕ_{n2} are the electron barrier heights for the two contacts and, V_{b1} and V_{b2} are the built-in potentials respectively, and L is the thickness of the slice. If the areas of the contacts are equal and $\phi_{n1} = \phi_{n2}$, we have a symmetrical MSM structure.

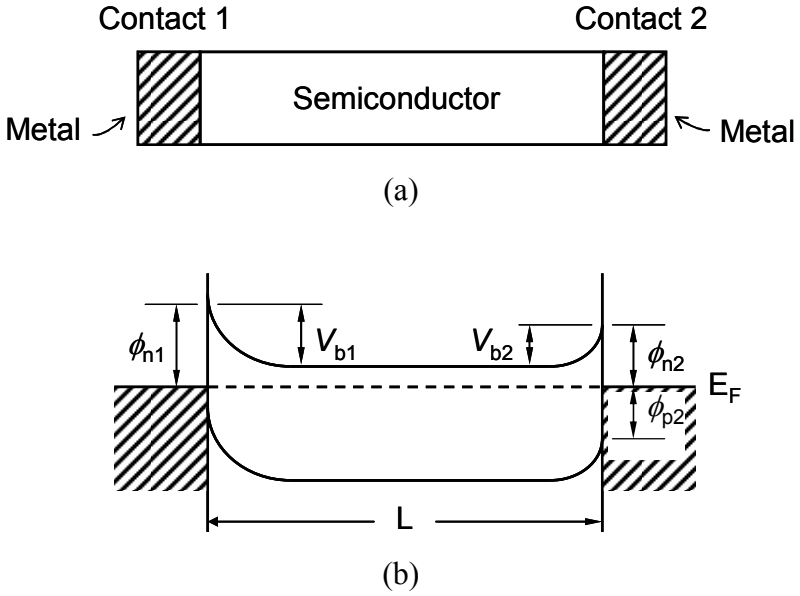


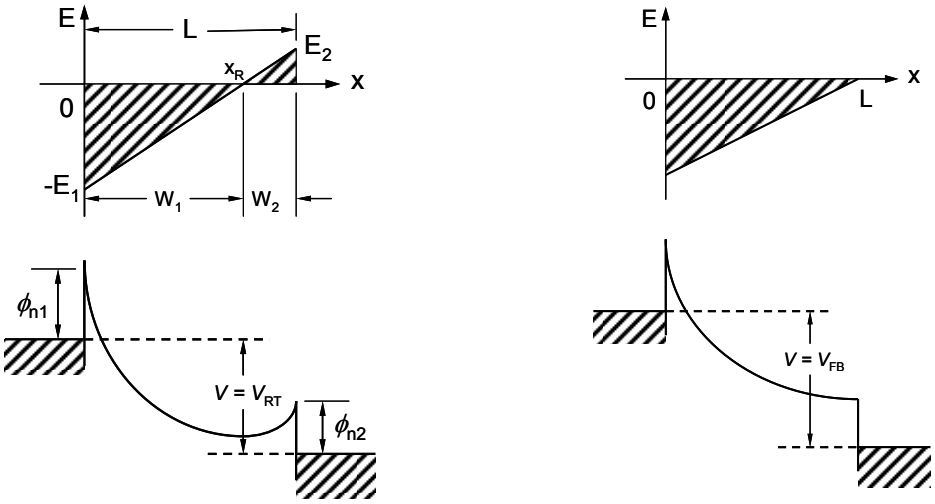
Fig. 3.1(a) Schematic diagram of a metal-semiconductor-metal structure.
(b) The corresponding energy band diagram at thermal equilibrium where ϕ_{n1} and ϕ_{n2} are the electron barrier heights, and V_{b1} and V_{b2} are the built-in potentials for contacts 1 and 2, respectively.

Under an applied voltage, one of the contacts (contact 1) is reverse biased and the other (contact 2) is forward biased [15,16]. As the applied voltage increases, the reverse biased depletion region will eventually reach through to the forward biased depletion region, as illustrated in Fig. 3.2(a). The corresponding voltage is called the reach-through voltage, V_{RT}.

As the voltage increases further, the electric field at $x = L$ becomes zero and the energy band at $x = L$ becomes flat. This point is the flat-band condition with the corresponding flat-band voltage, V_{FB}, shown in Fig. 3.2(b). For voltages in excess of V_{FB}, the energy band is bent further downward. The maximum voltage that can be applied to the MSM is limited by the avalanche breakdown near the maximum field at contact 1.

3.3 ELECTRON AND HOLE CURRENTS

When a negative voltage is applied to the metal-semiconductor contact 1 with respect to contact 2, the barrier ϕ_{n1} is reverse biased and ϕ_{n2} is forward biased. Fig. 3.3(a), (b) and (c) show the charge distribution, electric field distribution, and energy band diagram,



(a) (b)

Fig. 3.2(a) Field distribution and energy diagram of an MSM structure at reach-through.
(b) Condition of flat-band at which the energy band at $x = L$ becomes flat.

respectively, for a small applied voltage. The electron current comes about because of the thermionic emission of electrons from contact 1 and the hole current is due to thermionic emission of holes at contact 2. Those emitted holes which diffuse from x_2 to x_1 constitute the hole current. The injected hole current from contact 2 is generally much smaller than the electron current before the reach-through condition. Therefore, the electron currents across both barriers must be equal required by the current continuity [17]. For low biases such that the sum of the depletion widths W_1 and W_2 are smaller than the thickness L, the charge distribution of an MSM structure is shown in Fig. 3.3(a) for an n-type semiconductor with ionized impurity concentration N_d. The corresponding electric field and the potential distribution are obtained from the integrations of the Poisson equation and are shown in Fig. 3.3(b) and (c), respectively.

The applied voltage V is shared between the two contacts, so that

$$V = V_1 + V_2 \tag{3.1}$$

From the current continuity requirements, and assuming same area for both contacts we have

$$J_{n1} = J_{n2} \tag{3.2}$$

The reverse current density J_{n1} for the contact 1 is given by [18]

$$J_{n1} = A_n^* T^2 e^{-\beta\phi_{n1}} e^{\beta(\Delta\phi_{n1}+\alpha_1 E_1)}(1 - e^{-\beta V_1}) \tag{3.3}$$

where A_n^* is the effective Richardson constant for electrons, T the temperature, $\beta = q/kT$, E_1 the maximum electric field (at $x = 0$), α_1 the intrinsic barrier lowering coefficient [19-21], and $\Delta\phi_{n1}$ the Schottky barrier lowering given by

$$\Delta\phi_{n1} = \sqrt{\frac{qE_1}{4\pi\varepsilon_s}} \tag{3.4}$$

with

$$E_1 = \sqrt{\frac{2qN_d}{\varepsilon_s}(V_1 + V_{b1})} \tag{3.5}$$

The forward current density J_{n2} is similarly given by

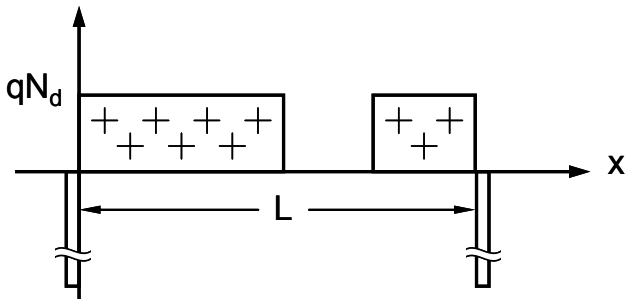
$$J_{n2} = A_n^* T^2 e^{-\beta\phi_{n2}} e^{\beta(\Delta\phi_{n2}+\alpha_2 E_2)}(e^{\beta V_2} - 1) \tag{3.6}$$

where $\Delta\phi_{n2}$ can be obtained by equation (3.4) with $(V_{b2} - V_2)$ term replacing $(V_1 + V_{b1})$. Substitution of equations (3.3) and (3.6) into (3.2) yields the relationship between V_1 and V_2. This can be solved numerically or graphically in conjunction with equation (3.1).

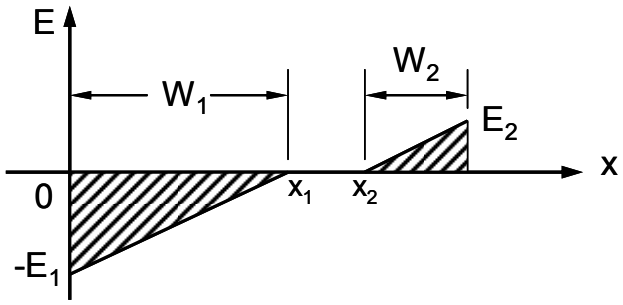
The depletion layer width is given by

$$W_1 = \sqrt{\frac{2\varepsilon_s}{qN_d}(V_1 + V_{b1})} \tag{3.7a}$$

$$W_2 = \sqrt{\frac{2\varepsilon_s}{qN_d}(V_{b2} - V_2)} \tag{3.7b}$$



(a)



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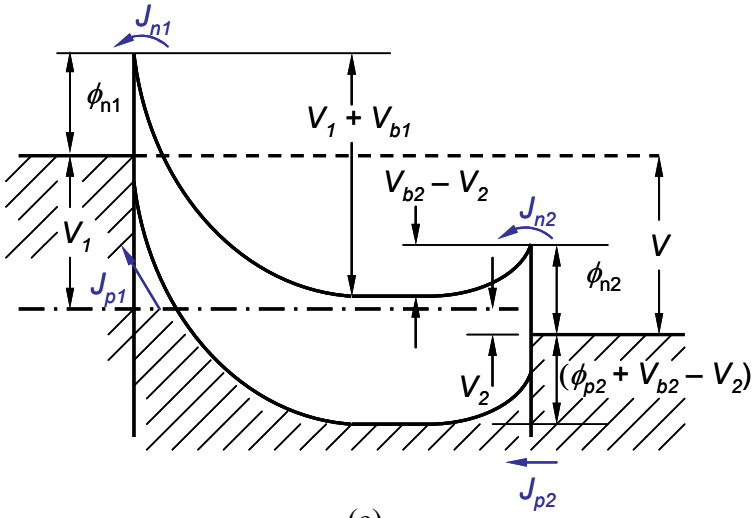

(c)

Fig. 3.3(a) The charge distribution,
(b) electric field,
(c) and potential profile of an MSM structure under bias with positive voltage applied on contact 2. The contact 1 is reverse biased and contact 2 is forward biased.

Similar analysis can be done for the hole currents in the structure. In the end, the saturation current densities for electrons and holes are given by [17]

$$J_{ns} = A_n^* T^2 e^{-q\phi_{n1}/kT} \tag{3.8a}$$

$$J_{ps} = A_p^* T^2 e^{-q\phi_{p2}/kT} \tag{3.8b}$$

Therefore, these currents can be varied over many orders of magnitude by varying the barrier heights of the two contacts.

At reach-through the structure is entirely depleted and V_{RT} can be obtained from the condition ($W_1 + W_2 = L$). With further increase in V, the hole current from the forward biased contact begins to increase rapidly as the hole barrier ($\phi_{p2} + V_{b2} - V_2$) is lowered. Similarly, the flat-band voltage V_{FB} can be obtained from the condition ($W_2 = 0$).

3.4 ASYMMETRIC WORKFUNTION METAL ELECTRODES

3.4.1 Theory and simulations

The two major sources of MSM dark current are carrier injection over the Schottky barriers (J_{n1} and J_{p2}) and current associated with the thermally generated electron-hole pairs (J_3 and J_4), as shown in Fig. 3.4. MSMs with mid-gap workfunction (Φ_m) electrodes have conventionally been used to minimize dark current, after which J_{n1} has the major contribution.

Upon using a different metal with a larger workfunction at the contact 1 ($\Phi_{m1} > \Phi_{m2}$), one could selectively raise the electron injection barrier (ϕ_{n1}) to further suppress I_{dark}. Although this reduction phenomenon was analyzed before [12], its impact on the photocurrent (I_{photo}) from the device stand point was not clear. To evaluate the overall performance, two-dimensional (2D) simulations were done using ATLAS^{TM} for a Si-based MSM. Illustrated in Fig. 3.5 are the detector photo and dark currents at different voltage bias. When Φ_{m1} was increased by 0.35 eV, at fixed Φ_{m2}, the dark current dropped by 5 orders of magnitude (at 5 V) without sacrificing the photocurrent, showing promise

with this asymmetric scheme. Values of workfunction for various metals are shown in Fig. 3.6. The experimental species were chosen from metals available at the time.

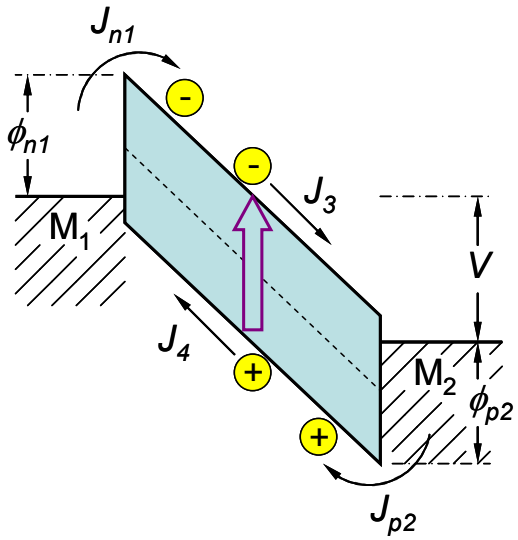

Fig. 3.4 Simplified energy band diagram illustration of sources of dark current in an MSM PD under external voltage bias.

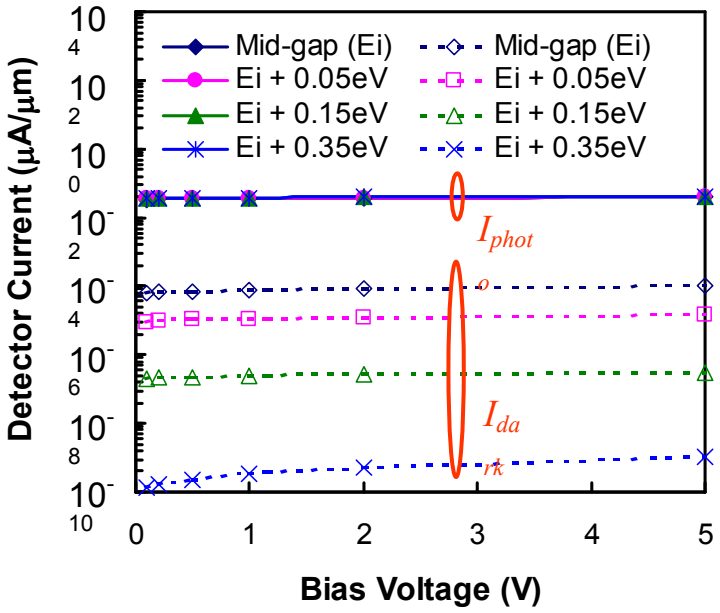

Fig. 3.5 Simulated PD currents versus bias voltage at both zero and 50 nW/μm^2 illuminations. An MSM structure per unit width with 2 μm inter-electrode spacing and 2 μm thick Si substrate was used. Φ_{m2} was arbitrarily fixed at 4.2 eV with various Φ_{m1}. Light was at normal incident from the top with a wavelength of 623 nm.

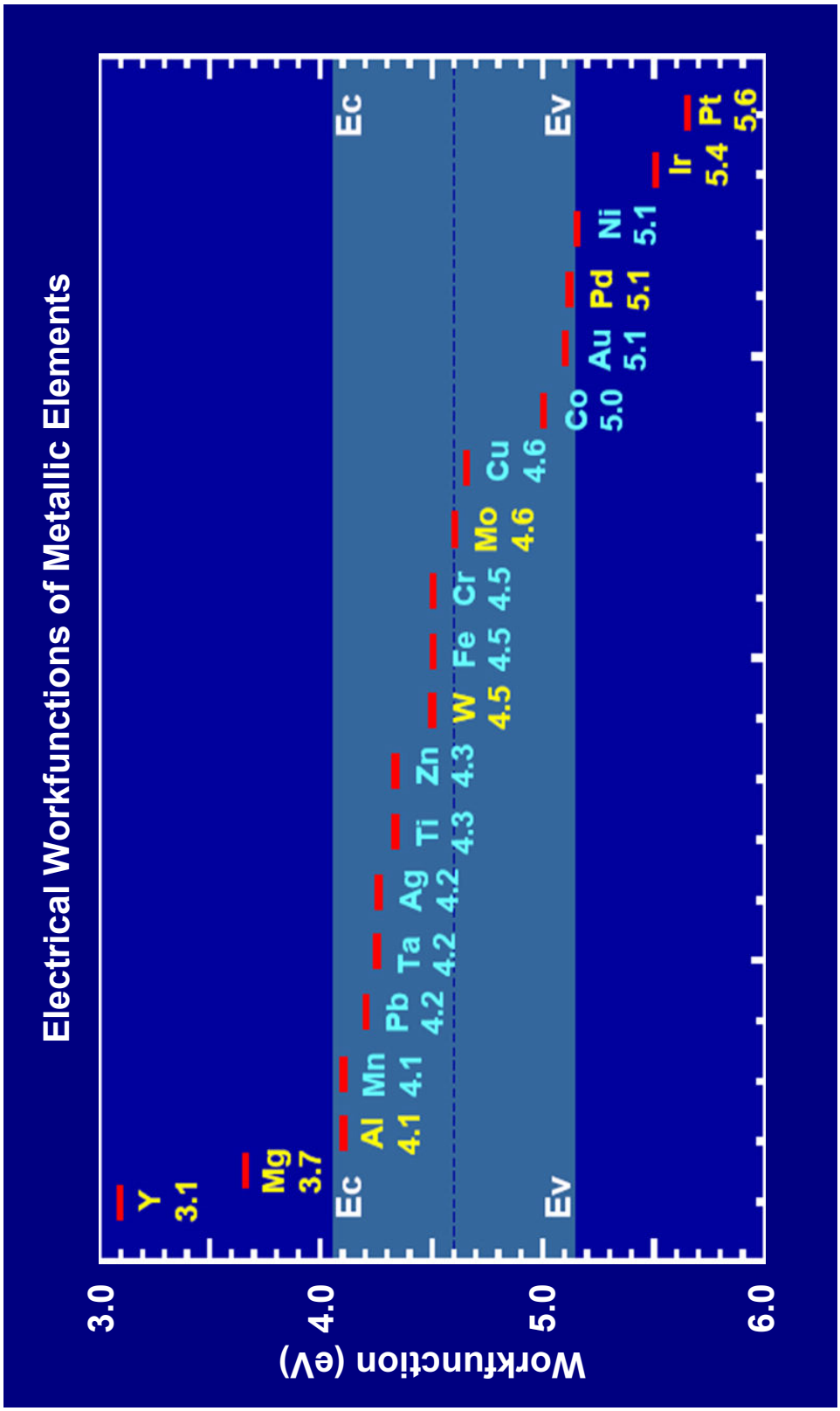

Fig. 3.6 Electrical workfunction of metallic elements.

3.4.2 Fabrication

MSM detectors with interdigitated electrode width and spacing ranging from 1 to 10 μm in the active absorption regions of 10^2 – 10^4 μm^2 were designed on the same mask. The starting substrates were (100) oriented p-type (~10^{15} cm^{-3}) Si wafers and n-type (~10^{16} cm^{-3}) Ge wafers. Low substrate doping concentrations were chosen to allow low voltage device operation. Si and Ge native oxides were first removed by dilute HF and DI water rinse [22] respectively, followed by metal electrode e-beam evaporation and photoresist liftoff. About 150 Å of Ti, Cr, or Ni were used for workfunction control and adhesion, topped with ~ 350 Å of Au to allow high-speed measurements. Only one lithography step was required for the case of symmetric electrodes while two for the asymmetric case. No thermal treatments were performed afterwards to avoid interdiffusion and alloying between semiconductor and metal. An SEM (scanning electron microscope) image of the completed device is shown in Fig. 3.7.

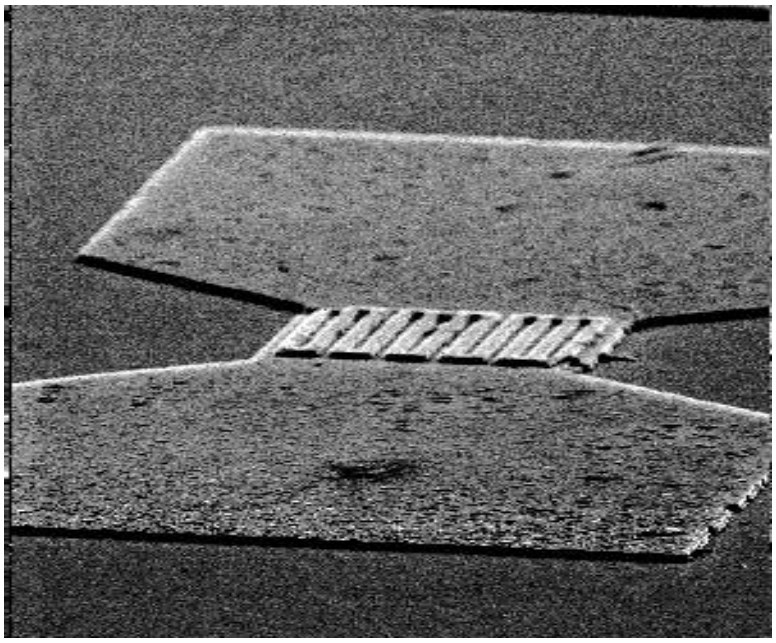

Fig. 3.7 SEM image of a completed MSM photodetector. Interdigitated fingers are shown. Metal pads fan out from the active area for probing.

3.4.3 Experimental results and discussion

Before taking any PD current–voltage (*I-V*) measurements, Schottky diode behavior was first verified for individual MSM electrodes with the substrate. *I-V* across the two MSM electrodes was then checked to show back-to-back Schottky diode behavior. In the case of an asymmetric MSM, since the two metal electrode workfunctions are different, the positive polarity of the voltage bias should be applied to the electrode with relatively lower workfunction such that the same level of semiconductor depletion could be accomplished at a lower bias, taking the advantage of asymmetry.

Fig. 3.8 and Fig. 3.9 show the *I-V*, under both dark and illumination at 632 nm (for Si) and 1480 nm (for Ge), from both symmetric and asymmetric MSM-PDs on Si and Ge substrates. Since Ge has a lower bandgap than Si, *I-V* measurements were made only up to 1.5 V corresponding to their lower voltage operations. Only Ti or Ni was used as the metal electrodes for the symmetric case, whereas in the asymmetric case, Ti and Ni were used on one electrode apiece. As illustrated in Fig. 3.8 for Si MSMs, the I_{photo} obtained at

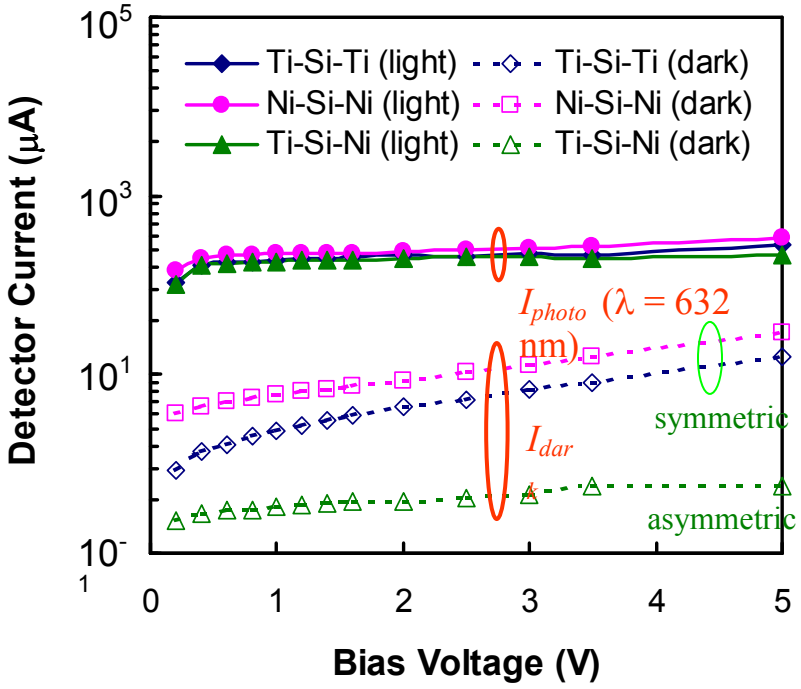

Fig. 3.8 Experimental photoresponse and dark currents measured from both symmetric (Ti or Ni electrodes only) and asymmetric (Ti and Ni electrodes together) MSM-PDs on Si substrate. The MSM-PDs investigated had 5 μm × 5 μm fingers (width × spacing) and area of 10^4 μm^2.

the same input optical power are of the same order in all cases, however, the lowest I_{dark} was obtained in the asymmetric case (Ti–Si–Ni). Similarly, the I_{dark} for the Ti–Ge–Ni PD is the least with the same I_{photo} compared to the symmetric Ge MSMs as shown in Fig. 3.9. It is noteworthy that the MSM-PD structure employed here has not been optimized for I_{dark} suppression. For instance, the MSM active area surfaces were not intentionally passivated to minimize surface leakage, and the large probing pads were in intimate contact with the substrate together with the interdigitated fingers. The demonstrated I_{dark} reduction is solely attributed the application of the asymmetric electrodes, rationalizing the theory discussed above. In addition to the *I-V* characteristics, the ratio of detector

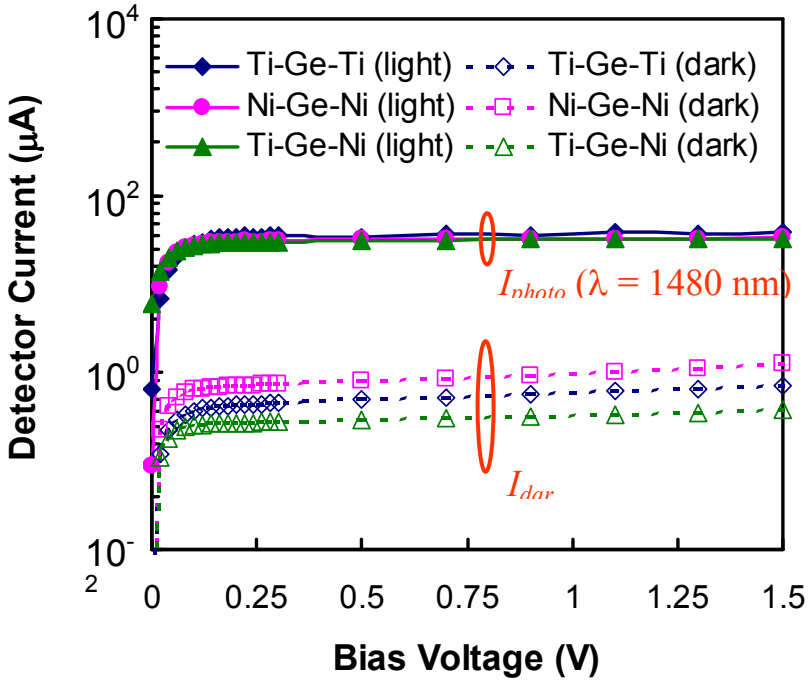

Fig. 3.9 Experimental photoresponse and dark currents measured from both symmetric (Ti or Ni electrodes only) and asymmetric (Ti and Ni electrodes together) MSM-PDs on Ge substrate. The MSM-PDs investigated had 5 μm × 5 μm fingers (width × spacing) and area of 10^4 μm^2.

photocurrent-to-dark current, i.e., $PDR = I_{photo} / I_{dark}$, is often quoted for performance evaluations as an optically controlled electronic switch. However, I_{photo} has a direct dependence on the input optical power (P_{opt}) that is subjectively reflected in the *PDR* as well. Apparently, the *PDR* normalized to the input optical power (*NPDR*) would be a more objective metrics for assessment:

$$NPDR = \frac{I_{photo}/I_{dark}}{P_{optical}} = \frac{I_{photo}/P_{optical}}{I_{dark}} = \frac{\Re}{I_{dark}} = \frac{1}{NEP}\sqrt{\frac{2q}{I_{dark}}} \tag{3.9}$$

where $\Re$ is the responsivity in amp/watt, q is the electronic charge in coulomb, and *NEP* is the dark current (or shot noise) component of noise-equivalent power in terms of Watt/Hz^{½}. Using the *NPDR* in (3.9), one could compare the responsivity and *NEP* of different detectors for the given amount of I_{dark}. Moreover, if the wavelength of illumination is also fixed, one could have a direct comparison of the external quantum efficiency (η) for different detectors at a fixed I_{dark}.

Fig. 3.10 shows the *NPDR* extracted for various Ge MSMs with both symmetric and asymmetric metal electrodes of the same geometry and active absorption area. Clearly, the asymmetric MSMs give a substantial enhancement in *NPDR* than their symmetric counterparts. The major reason for the *NPDR* enhancement is accredited to effective I_{dark}

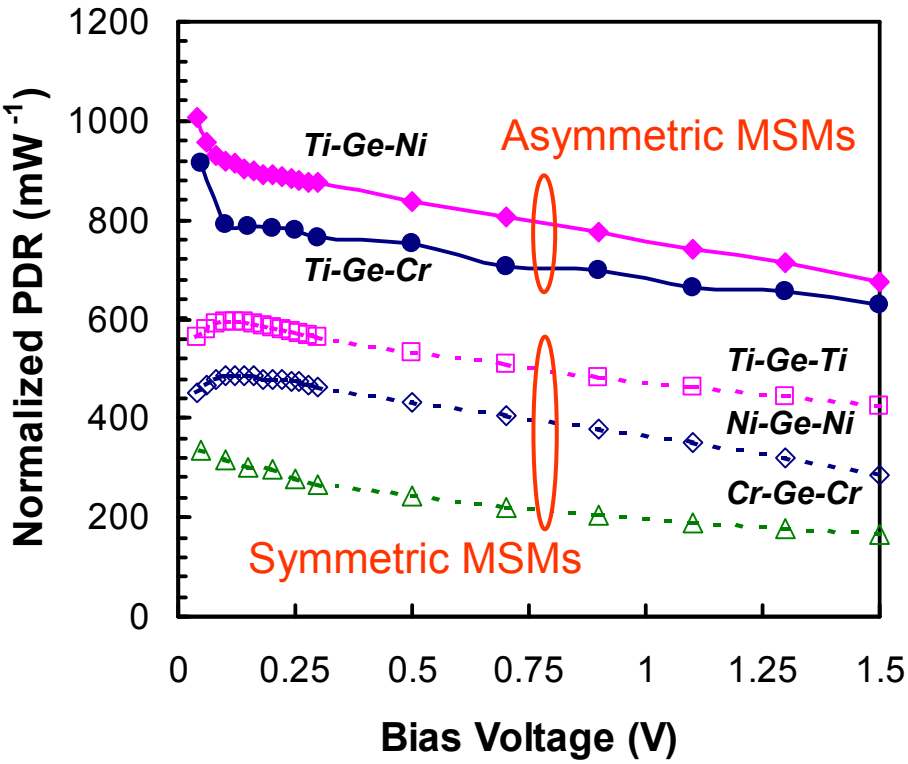

Fig. 3.10 Normalized photocurrent-to-dark current ratio (*NPDR*) extracted from various Ge symmetric and asymmetric MSMs with 5 μm × 5 μm fingers and area of 10^4 μm^2 under 1480 nm illumination.

suppression with the asymmetric workfunction electrode scheme without costing a significant reduction in I_{photo} as exemplified in Fig. 3.8 and 3.9. At 1 V bias, the highest *NPDR* of ~ 757 mW^{-1} was obtained for Ti–Ge–Ni PD (1.6 × higher than Ti–Ge–Ti and 2.1 × more than Ni–Ge–Ni). Similarly, Ti-Ge-Cr PD revealed a 1.4 × and 3.5 × improvement versus Ti–Ge–Ti and Cr–Ge–Cr respectively. For both MSM types at 1480 nm, $\Re \approx 0.3$ A/W and $\eta \approx 25\%$, while $\Re \approx 0.21$ A/W and $\eta \approx 20\%$, at 1320 nm illumination. The *NEP*s from Ti–Ge–Ti and Ni–Ge–Ni PDs are 1.86 and 2.81 $pW/Hz^{½}$, respectively, and both are larger than the 1.70 $pW/Hz^{½}$ from Ti–Ge–Ni PD. The *NPDR* (and η) could be raised further with optimizations like the incorporation of different metals to provide higher asymmetry (in order to obtain a larger built-in electric field to facilitate low voltage bias operations) and anti-reflection coatings. From both symmetric and asymmetric MSMs with 2 μm finger spacing at 1 V bias, the measured 3 dB bandwidths were similar (~795 MHz) demonstrating no bandwidth degradation due to asymmetry.

The effect of MSM sizing was studied using the *NPDR* metric. Fig. 3.11 exhibits one of the MSM design tradeoffs. Since the active substrate area beneath the electrode is

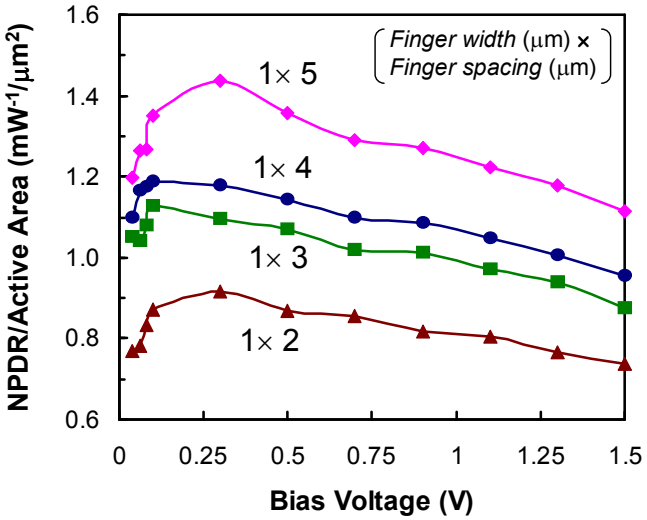

Fig. 3.11 The effect of varying MSM finger spacing on the extracted *NPDR* normalized to the active unblocked absorption area. Ti–Ge–Ni PDs were used as an example with fixed finger width of 1 μm at λ = 1320 nm illumination.

always blocked from optical absorption, the MSM finger width is usually minimized for maximum efficiency. With the minimum finger width (1 μm in this case) and fixed active area (limited by laser spot size), the *NPDR* normalized to the active unblocked area still increased with larger finger spacing. This could be attributed to the I_{dark} drops with increasing finger spacing at the same bias voltage (i.e., decreasing E-field). However, one would also expect degradation in detector bandwidth with increasing finger spacing, as these detectors are mostly transit time limited. For instance, the 3-dB bandwidth of the 2 μm finger spacing MSM drops from ~ 795 to ~ 320 MHz on a 5 μm MSM. Nonetheless, under the circumstances where the finger spacing could not be tuned, the asymmetric scheme proposed above should be exercised to lower I_{dark} and raise the *NPDR*. Fig. 3.12 summarizes the application specific trade-offs in the design of these detectors.

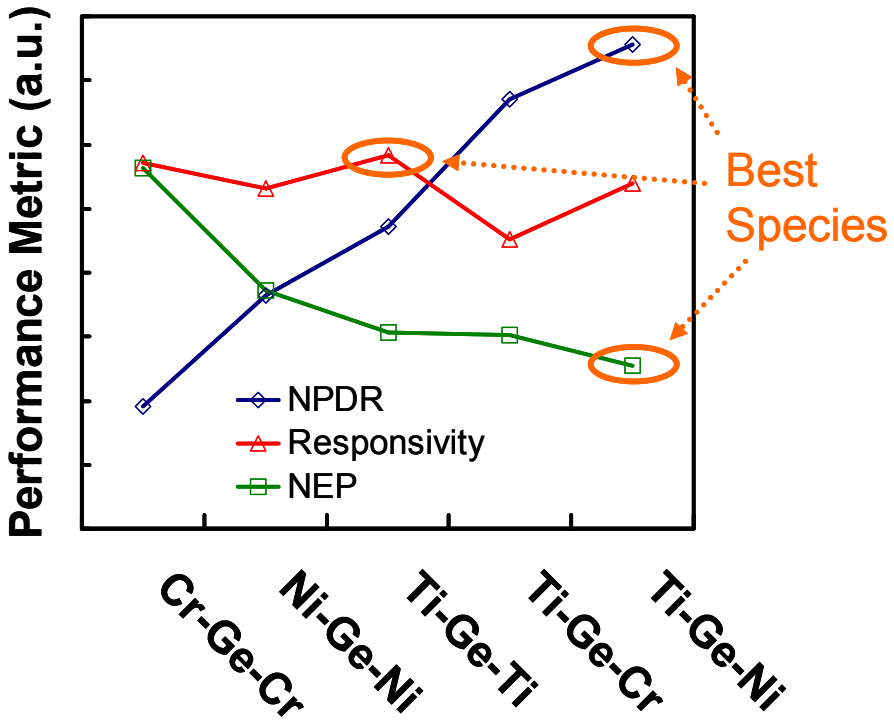

Fig. 3.12 Comparison of *NPDR*, *NEP* and $\Re$ of symmetric and asymmetric MSMs.

3.5 ASYMMETRIC CONTACT AREA METAL ELECTRODES

3.5.1 Theory and simulations

Traditionally, the principle of asymmetric area electrodes is being used in commercial plasma systems [23] in which one of the electrodes is the sample chuck and the other electrode is generally chosen as the large conducting casing of the tool. The unequal are electrodes in an RF sputtering system, for instance, cause a non-uniform electric field distribution as illustrated in Fig. 3.13. On a basic MSM structure with two back-to-back Schottky diodes, we have investigated the possibility to suppress leakage current by utilizing asymmetric area contacts. Under an applied potential, an identical current flows through the electrodes to satisfy the current continuity requirement. The current density (J) at the small-area contact exceeds that of the larger contact. The higher J is accompanied with larger electric field widening the depletion layer around the smaller-area contact encroaching towards the larger one. This in turn decreases the reach through voltage.

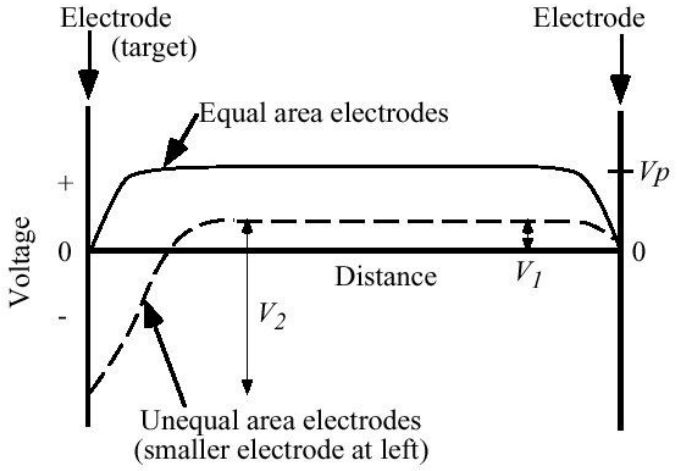

Fig. 3.13 The potential profile in an unequal electrode area RF sputtering system.

2-dimensional simulations of Si-based interdigitated MSM structures were carried out using MEDICI^{TM} to verify I_{dark} reduction with the area asymmetry scheme. Total contact area (A_{total}) and electrode spacing were kept constant while varying the asymmetry. Fig. 3.14 plots detector current without illumination versus contact area asymmetry – defined

as the ratio of electrode areas – showing reduction in current with increasing asymmetry. Simulations were done on an MSM structure per unit width with 1 μm inter-electrode spacing and 5 μm Si thickness [24].

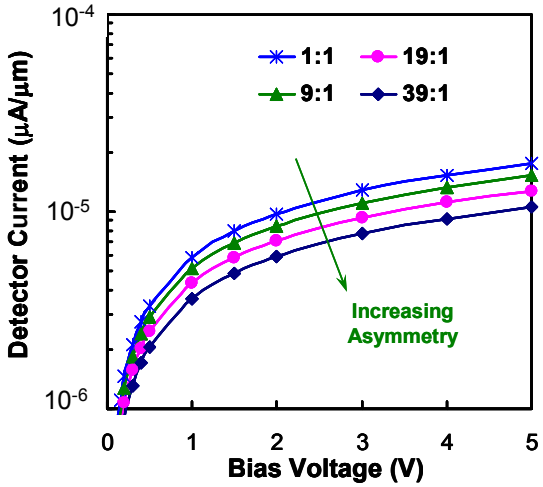

Fig. 3.14 Simulated dark current reduction in MSMs with increasing contact area asymmetry. The total contact area of each detector is fixed in the simulations. Simulations were done on MSMs with 1 μm inter-electrode spacing on 5 μm thick Si substrate.

3.5.2 Fabrication

MSM-PDs with a range of contact area asymmetries were fabricated on lightly doped (~10^{15} cm^{-3}) *p*-type Si wafers with (100) surface orientation. Native oxide was removed by dilute HF followed by metal e-beam evaporation and photoresist liftoff for patterning the electrodes. 150 Å of Ti and 350 Å of Au stack were used as metal electrodes. Ti was chosen to improve adhesion and because its workfunction is close to the midgap of Si providing high injection barriers for both electrons and holes at the Schottky contacts. Fig. 3.15 shows a SEM of one such MSM detector with the definition of the critical dimensions. Detectors with circular geometry were chosen to avoid secondary effects such as fringing fields and obtain uniform electric field distribution along the contacts.

In the circular design, there are three factors that influence the total dark current. These are $A_{total} = \pi \times \left(R_1^2 + R_3^2 - R_2^2\right)$, inter-electrode spacing ($R_2 - R_1$), and the contact area asymmetry which is defined as the ratio of the area of the ring (A_{ring}) to the area of

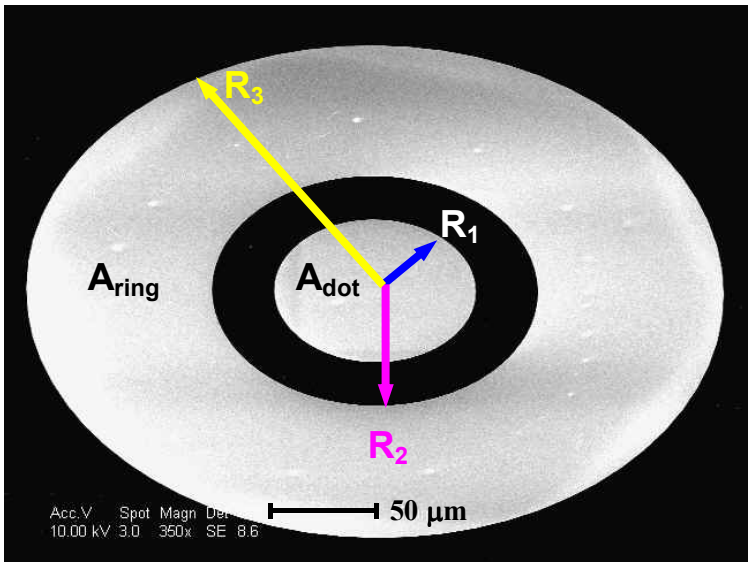

Fig. 3.15 SEM image of a completed circular MSM photodetector with asymmetric contact area. Critical dimensions are defined with the arrows.

the dot (A_{dot}). Two different series of MSMs (L_1 and L_2) were designed in order to extract the influence of asymmetry on I_{dark}. The L_1 series consists of the samples S_1 to S_7 in which R_1 is fixed while R_2 is increasing. In the samples S_8 through S_{12}, which make up the L_2 series, $R_2 - R_1$ is fixed while R_1 is varied.

3.5.3 Experimental results and discussion

Current-voltage measurements were taken with the bigger electrode grounded and the smaller one positively biased. Such a configuration reverse-biases the latter electrode as the substrate is lightly doped *p*-type Si. Dark *I-V* measurement results for such a bias polarity are illustrated in Fig. 3.16. Photodetector species S_8-S_{12} have fixed electrode spacing, but varying contact area asymmetries as indicated in the inset in Fig. 3.16. I_{dark} is highest for S_{12} and is reduced toward the most asymmetric case, S_8. The trend plotted in Fig. 3.17 shows the leakage of $S_8 - S_{12}$ at a fixed voltage bias of 3 V after I_{dark} is scaled by the total contact area. Considerable I_{dark} drop (2 ×) is obtained at 3 V bias for MSMs with identical total electrode area and spacing, but varying contact area asymmetry [25]. Similarly, I_{dark} scaled by A_{total} vs asymmetry measured for the L_1 series detectors is shown in Fig. 3.17 for the sake of completeness. A steeper trend is observed in L_1 series, since

both increasing inter-electrode spacing with increasing asymmetry act to reduce the dark current.

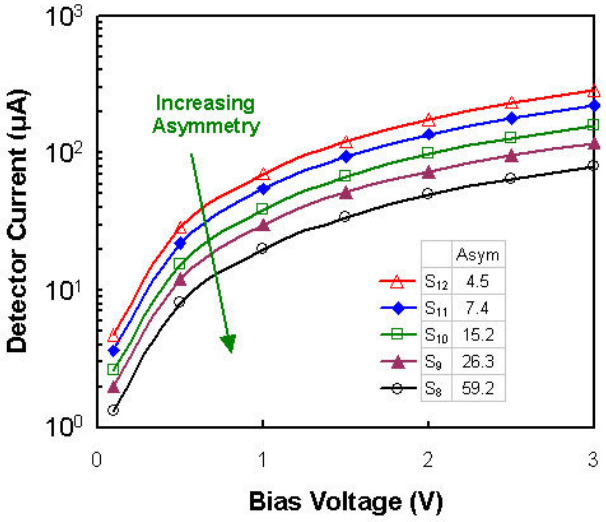

Fig. 3.16 Experimental *I-V* under dark conditions. Dark current decreases from S_{12} to S_8 in the same direction as increasing area asymmetry.

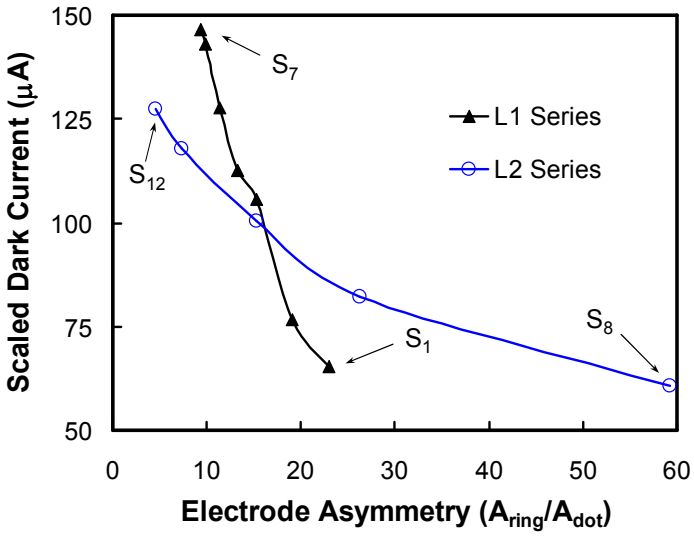

Fig. 3.17 I_{dark} (scaled by A_{total}) versus area asymmetry. From S_{12} to S_8, I_{dark} decreases in the same direction as increasing asymmetry. L_1 series show a steeper reduction in I_{dark} due to increasing asymmetry and electrode spacing.

Photoresponse of the detectors is also investigated for performance evaluations as an optically-controlled electronic switch. The ratio of detector photocurrent to dark current normalized to the input optical power (*NPDR*) is used as an objective metric

for performance assessment as described above. Photodetectors were illuminated by red light ($\lambda \sim 632$ nm) and the photocurrent was monitored while the beam was translated relative to the electrodes. For fair comparison, measurements were recorded at the beam location corresponding to the highest photoresponse for each detector. Responsivity values of ~ 0.2 A/W were obtained with no significant degradation to the light-on state. *NPDR* versus applied bias is plotted in Fig. 3.18 representing clear enhancement of *NPDR* with electrode area asymmetry. The major contribution to the increase in *NPDR* is attributed to effective I_{dark} suppression by the proposed asymmetric electrode scheme without compromising the photocurrent.

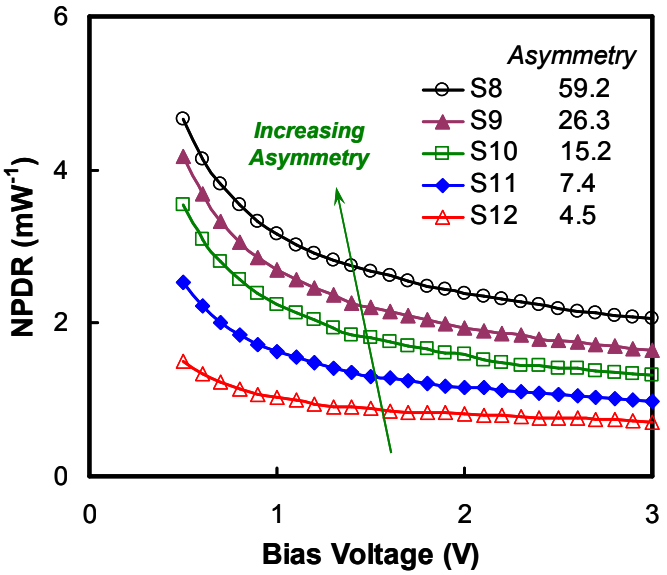

Fig. 3.18 *NPDR* extracted under 632 nm illumination. *NPDR* is higher for larger asymmetry photodetectors due to reduced I_{dark} with increasing electrode asymmetry and no significant degradation in photoresponse.

3.6 CONCLUSIONS

We have demonstrated, with simulations and experiments, the application of asymmetric workfunction electrodes in Group IV MSM-PDs to effectively suppress dark current for optical applications. A new metric *NPDR* was introduced by normalizing detector on-to-off current ratio to input optical power, indexing an improvement of at least 1.4 × with the asymmetric scheme. Finally, the impact of MSM sizing was also investigated.

We have demonstrated for the first time the application of asymmetric area electrodes in MSM-PDs to effectively suppress dark current. Improvement in *NPDR* by a factor of up to 3 × was demonstrated with the asymmetric MSM-PDs. We believe that these results are particularly important and promising for its potential applications in low power and voltage photodetectors for densely integrated optoelectronic ICs.

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CHAPTER 4: HIGH PERFORMANCE GERMANIUM OPTICAL DETECTORS INTEGRATED ON SILICON

Judge a man by his questions rather than by his answers.
Voltaire

This chapter describes the experimental study of high sensitivity germanium based metal-semiconductor-metal photodetectors integrated with silicon. We report the fabrication and characterization of optical detectors on heteroepitaxially grown Ge directly on Si. We demonstrate photodetectors with very high responsivity at telecommunication standard wavelengths. We describe the influence of strain on detector responsivity and present physical characterization results. The heteroepitaxial growth technique was developed and the study of dislocation density was conducted by Ammar Nayfeh under the supervision of Krishna C. Saraswat [1,2,18]. X-ray diffraction measurements were taken by Nevran Ozguven. Layer growth and detector fabrication, electrical and optical characterization measurements, and the relevant data analysis together with the theoretical analysis of the presented Ge MSM photodetectors were primarily conducted by Ali K. Okyay under the supervision of Krishna C. Saraswat. Parts of this chapter have already been published in [4].

4.1 INTRODUCTION

The widespread demand for high-speed data communications is driving the optical communications industry into devising more cost-effective ways of meeting these demands. Presently, full monolithic integration of photonic elements with the Si-based electronics of the optical communications infrastructure has become one of the major focuses of research within this industry. Therefore, Si-based optoelectronics, photodetectors in particular, have received considerable attention. The lack of sensitivity Si possesses at wavelengths beyond 1100 nm makes it unsuitable for photodetection in the 1300–1550 nm wavelength range.

Germanium is a viable candidate for integration with Si, given its sensitivity around the 1300–1550 nm wavelength range as well as its compatibility with integrated circuit technologies for low-cost transceivers. A particularly important application is the integration of Ge photodetectors with Si or Si_3N_4 waveguides and Si based electronic devices for the distribution and detection of optical signals at wavelengths of 1300 nm and 1550 nm on Si. In order to integrate Ge onto Si, it is pivotal to develop new methods for heteroepitaxial Ge technology because Ge growth on Si is hampered by the large lattice mismatch (4.2%). The large lattice mismatch causes two major problems when Ge is epitaxially grown on Si: (1) the introduction of high density of misfit dislocations and threading dislocations in the epilayer, and (2) high surface roughness due to island growth. High surface roughness causes difficulties in process integration. In addition, a Ge photodetector with a high threading dislocation density would suffer from large leakage currents, as well as reduced responsivity resulting from carrier recombination at the dislocation defect sites within the Ge layer.

Initially, we have attempted to build Ge-based photodetectors on deposited polycrystalline films. The results we obtain and a summary of drawbacks associated with that technology can be found in Appendix I. In the following sections, we report on the fabrication and demonstration of high quality Ge based MSM-PDs using a recently developed procedure, Multiple Hydrogen Annealing for Heteroepitaxy (MHAH) [1-3], for growing high quality heteroepitaxial germanium layers on silicon. We demonstrate responsivities as high as 0.84 A/W at 1550 nm and 2 V reverse bias [4-6].

4.1.1 Review of epitaxial growth mechanism

The growth mechanics are governed by the physics of nucleation and growth processes. Theoretically, equilibrium epitaxial growth modes are determined by the free energy of the substrate surface (σ_s), the interface free energy (σ_i), and the surface free energy of the heteroepitaxial layer (σ_f). In reality, no growth can occur at equilibrium; film growth always experiences kinetics and thermodynamics. However, it is useful to consider this ideal limit for the fundamental material analysis [7]. Under equilibrium conditions, the crystalline growth can be classified into three basic modes, depicted

schematically in Fig. 4.1 [8]. These are the Frank-Van der Merwe (layer-by-layer growth), Volmer-Weber (islanding growth), and Stranski-Krastanov (layer-by-layer growth followed by islanding growth) [9]. The inequality $\sigma_s > \sigma_f + \sigma_i$ sets the condition for the epitaxial film to wet the substrate representing the layer-by-by growth [10]. The opposite extreme ($\sigma_s < \sigma_f + \sigma_i$) obtains islanding growth. In the intermediate case, the adlayer initially wets the substrate, but because of lattice mismatch, as the layer thickness increases, strain energy contributes to σ_i, to the point at which the film no longer wets the substrate. Subsequently, islands and misfit dislocations are formed to relieve strain. The thickness beyond which the onset of misfit dislocation is favorable is the critical thickness.

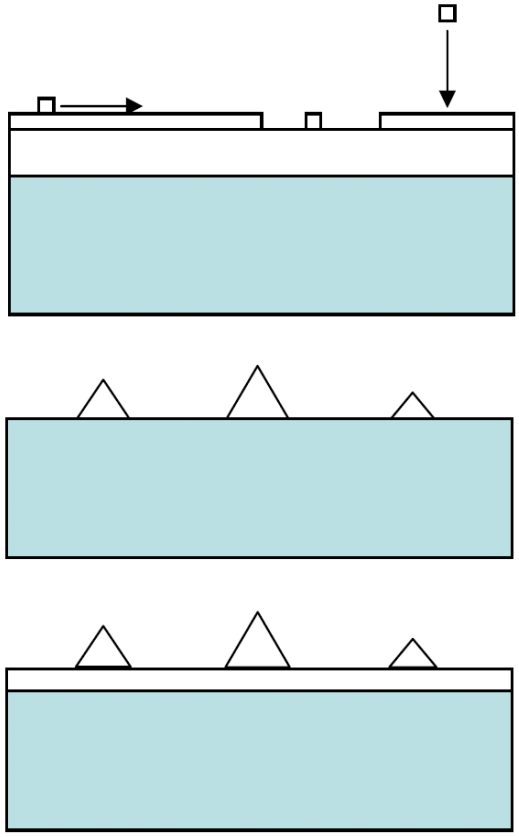

Fig. 4.1 Schematic illustration of the three equilibrium growth modes: (a) Frank-van de Merwe (layer-by-layer), (b) Volmer-Weber (Cluster), and (c) Stranski-Krastanov (layer-cluster)

In a vapor deposition system, growth occurs by supersaturation, in which the vapor pressure is higher than that at equilibrium. Growth thermodynamics and kinetics can be partially controlled by substrate temperature and chamber pressure. A variety of growth-front morphologies can be obtained depending on which kinetic process is rate-limiting [11]. Three kinetic growth modes are:

1. *Layer-by-layer growth*: This growth is observed when the growth rate is low or the substrate temperature is sufficiently high to accommodate adatoms diffusion. In this growth mode, adatoms have sufficient mobility to find one another. Nucleated two dimensional (2-D) islands can grow and ultimately fill in the initial starting surface. This growth mode usually shows an increase of surface roughness with increasing layer thickness because the previously deposited layer is never completely filled before the next layer nucleates.

2. *Island growth*: This type of growth occurs for relatively high deposition rate and slow lateral adatoms diffusion. In this growth mode, atoms migrate only on the order of a few lattice sites before they incorporate into the growing film. Growth under these conditions leads to a rough surface for which the roughness amplitude increases with increasing film thickness.

3. *Stranski-Krastanov (SK)*: A smooth surface during deposition will be achieved when deposited atoms have sufficient time to migrate and incorporate into a step before other atoms are deposited on the surface. The balance of forces will change during the growth if the materials have large lattice mismatch and associated strain. The first few layers will comprise a continuous, smooth film that usually has properties that differ from the bulk. Islanding happens to relieve the misfit strain. The clusters grow in size and density until the islands begin to merge in what is known as a coalescence phenomenon which decreases the island density allowing further nucleation to occur. This continues until a connected network with unfilled channels and voids develops. Finally, the voids are filled and a continuous film results.

It has been shown that the condition for SK growth is that the lattice mismatch is between 3% and 7% [12]. In the case of epitaxial growth of Ge on Si with large lattice mismatch, the Ge-Ge bond is weaker than the Si-Si bond, leading to a smaller surface energy. Consequently, the system of Ge/Si is usually discussed as a classical model for the Stranski-Krastanov growth mode. The critical thickness is generally considered to be 5 nm [7]. After the formation of one or more monolayers, subsequent layer growth becomes unfavorable and island growth begins to relieve the misfit strain. It has been reported that for pure Ge deposited on Si (001), by the third monolayer, strain energy can no longer be released by 2-D growth, and the growth mode changes from 2-D to 3-D, accompanied with the increased surface roughness. At a later stage, these 3-D structures relax to the Ge lattice constant and produce a high density of misfit dislocations between the substrate/epilayer interface and islands in the epilayers.

4.1.2 Origin of threading dislocations

In lattice mismatched systems such as the Ge/Si system, misfit-dislocations develop during the growth to relax the lattice mismatch between the Ge epilayer and the Si substrate. These misfit-dislocations relax the lattice mismatch between Ge and Si by introducing extra half planes of atoms. These misfit-dislocations are confined to the interface between the Ge epilayer and the Si substrate and are energetically stable when the Ge thickness is larger than the critical thickness for misfit-dislocation formation [13-16].

Threading dislocations are the by-products of the formation of misfit-dislocations and do not relax strain due to lattice mismatch. Threading-dislocations are left in the epilayers because dislocations cannot end in a crystal and have to either form a loop or terminate at a free surface. Since the epilayer surface is the nearest free surface to the epi-substrate interface, these threading-dislocations typically thread from the epi-substrate interface to the epilayer surface. Since devices are usually built close to the epilayer surface, these threading-dislocations can easily affect the performance of devices built on epilayers. Therefore, the reduction of threading-dislocation densities in epilayers grown on lattice mismatched substrate is important.

4.1.3 Quantifying dislocation density

Cross sectional TEM (transmission electron microscopy) is an excellent way to study the defects in the grown film, however, it is difficult to quantify them due to the small viewing area. There are two main methods that are most accepted and widely used to determine threading dislocation density: (1) plan-view TEM, and (2) defect etching. In the defect etching method, dislocations are etched at a higher rate than the layer itself, hence the etch pits appear visible using an optical microscope [17]. These etch pits correspond to the dislocations and can be counted to determine threading dislocation density. In the plan-view TEM method, dislocations appear as crystal imperfections in the lattice, and can be counted as well. Threading dislocation density is reported as a density per cm^2. Typical values of threading dislocation density for the germanium on silicon system range from 10^{10} to 2×10^6 cm^{-2} [18]. The large range is due to the numerous methods published on growing germanium on silicon.

4.1.4 Literature review of techniques for reducing threading dislocations

Historically, many novel ideas and techniques have been introduced to grow high quality Ge layers heteroepitaxially on Si and allow the fabrication of efficient optical detectors as well as MOSFET transistors. These have resulted in threading dislocation densities in the range of $10^7 - 10^9$ cm^{-2}. The following summarizes important research publications in this area over the past three decades in an attempt to present the "state of the art" in this field.

1. *Graded buffer layers*: In 1983, Bean and co-workers demonstrated that Ge_xSi_{1-x} layers can be grown on Si substrates over a full range of alloy compositions at temperatures from 400-750ºC by molecular beam epitaxy (MBE) [19]. At a given temperature, films can be grown in a smooth, two-dimensional manner up to a critical germanium fraction, x_c. The growth becomes rough beyond x_c, which, for instance, increases from 0.1 at 750ºC to 1.0 at ~ 550ºC. RBS (Rutherford ion back scattering) and TEM measurements indicate good crystallinity over a wide range of growth conditions and that the lattice mismatch between Ge_xSi_{1-x} and Si layers can be accommodated by elastic lattice distortion rather than misfit dislocation

formation. Fitzgerald and co-workers later showed that by growing SiGe relaxed graded buffer layers on Si at high temperature, high quality relaxed epilayers with 0-100% Ge can be grown on Si [20-22]. Their idea is to prevent massive dislocation nucleation, interaction and multiplication events that increase threading dislocations. This is done by staying within the low mismatch region with the introduction of each grading layer, which introduces a small number of new dislocations while providing the strain to glide dislocations out of the edge of the substrate.

2. *Superlattice buffer layers*: Luryi and co-workers used superlattice buffer layers to avoid the large lattice mismatch, and demonstrated p-i-n Ge detectors on Si with a quantum efficiency of 40% at 1300 nm [23]. Strained layer superlattices are essentially several low-misfit layers on top of each other. The idea is that strain can act as a barrier to the vertical movement of threading dislocations [24].

3. *Low temperature Si buffer layer*: Several groups have reported that the insertion of a low-temperature MBE grown Si buffer can dramatically reduce the threading dislocation density in the SiGe layer. The mechanism for this improvement is not clear [25-29]. It has been suggested that point defects in a low-temperature Si buffer layer can trap the dislocations [30].

4. *Very high temperature MBE*: Malta and co-workers showed heteroepitaxial growth of Ge on Si by MBE at 900ºC. A highly faceted interface results, indicating localized Ge melting and subsequent local alloying with Si [17]. This phenomenon is associated with extensive threading dislocation confinement near the Ge/Si interface. Etch pit density measurements obtained on Ge films that had undergone interfacial melting were as low as 10^5 cm^{-2}.

5. *Cyclic thermal annealing*: A number of groups have reported that in-situ thermal treatment can reduce threading dislocation density in GaAs grown on Si [31-33]. Kimerling and co-workers later showed that heteroepitaxial growth followed by cyclic thermal annealing can also reduce dislocation density in Ge/Si systems [34]. They grow a thin Ge buffer layer followed by thick layer at elevated

temperature and subject the film to cyclic thermal treatment. With such technologies, p-i-n detectors have been built on 4 μm Ge layers grown on Si using a low temperature buffer layer, yielding responsivity ($\Re$) of 0.89 A/W at 1300 nm. Moreover, with this technology, 52% quantum efficiency at 1300 nm was demonstrated on 1 μm Ge films grown on Si [35].

6. *Selective growth*: Epitaxial growth on patterned substrates has been shown to reduce the overall threading dislocation density. In small misfit systems, growth on small patterns reduces the misfit dislocation density and dislocation interactions and therefore the threading dislocation densities [36,37]. Growth in small areas also reduces the distance the threading dislocations need to travel before they reach the sides of the epilayer [38,39]. If the threading dislocations thread to the epilayer surface at a certain direction, it is possible to reduce the dislocation density by blocking threading dislocations using amorphous materials such as SiO_2 and Si_3N_4. Epitaxial necking [40,41], conformal growth [42], epitaxial lateral overgrowth [43,44] and pendeo-epitaxy [45] are methods based on this idea.

7. *Strain-relaxed buffer layers*: Using dual strain-relaxed buffer layers, very high 3dB bandwidth up to 38.9 GHz was demonstrated on vertical p-i-n detectors with 300 nm intrinsic regions [46]. Thin SiGe buffer layers with different Ge compositions were also used to relieve some of the strain during growth [47].

8. *Nanoscale Ge seeds*: Li and co-workers demonstrated that high quality Ge can be grown on Si covered with a thin layer of chemical SiO_2 [48]. When the oxidized Si substrate is exposed to a Ge molecular beam, 7-nm-wide seed pads form in the oxide layer and "touchdown" on the underlying Si. Upon continued exposure, Ge selectively grows on the seed pads rather than on SiO_2 and the seeds coalesce to form an epitaxial lateral overgrowth (ELO) layer. The Ge ELO is free of dislocation network, but stacking faults exist near the Ge-SiO_2 interface. A fraction of these stacking faults propagate to the surface, resulting in etch pit

density less than 2×10^6 cm^{-2}. The high quality of Ge ELO is attributed to a high density of nanoscale Ge seed pads interspaced by 2-12 nm wide SiO_2 patches.

9. *Compliant substrates*: If threading dislocations can thread into the substrate rather than into the epilayer, dislocation-free layers can be obtained. This has been reported by the application of the compliant substrate technology [49,50]. Several groups have reported epilayers with very low threading dislocation densities by introducing a thin compliant substrate by wafer bonding or by thinning of SOI wafer [51-53].

Recently, a method utilizing multiple steps of growth and annealing in a hydrogen ambient was introduced by Nayfeh et al. [1-3] to grow high quality Ge on Si with low threading dislocation density. In this technique, a thin Ge film is grown heteroepitaxially on Si and in-situ annealed at a higher temperature in an H_2 ambient which reduces the surface roughness by 90% and facilitates stress relief in the first few hundred angstroms. Subsequent Ge growth is homoepitaxy on a virtual Ge lattice with no additional defects forming. From our experiments, we find this method more controllable in addition to shorter anneal times required. Hence, this technique was used for fabrication of integrated Ge photodetectors on Si.

4.2 EXPERIMENTAL PROCEDURE

All of the experiments including heteroepitaxial Ge growth on Si and subsequent fabrication of photodetectors were carried out in the Stanford Nanofabrication Facility. The film growth and the study of dislocations were carried out in collaboration with Ammar Nayfeh. It should be noted that only a highlight of the dislocation extraction and modeling will be presented here which is detailed in Ammar Nayfeh's PhD thesis [18].

4.2.1 Heteroepitaxy of Ge on Si

A cold wall ASM Epsilon-two reduced pressure chemical vapor deposition (RP/CVD) reactor is used for Ge heteroepitaxy on Si. A schematic of the reactor wafer path is shown in Fig. 4.2. Dual load locks feed an exchange chamber through which a Bernoulli-effect wand moves wafers between the two load locks and the process

chamber, avoiding excess oxygen contamination in the reactor chamber. The load locks and the exchange chamber are purged with facility nitrogen. The heating is via two linear lamp arrays, one above and one below the susceptor. The susceptor is graphite, with rotating piece surrounded by an immobile ring, as illustrated in the schematic of the quartz wafer chamber in Fig. 4.3. Typical depositions are carried out with a rotation rate of 35 revolutions per minute. The base pressure of the RP/CVD chamber is 0.49 mTorr. The reaction gases used were SiH_4 for Si and GeH_4 for Ge deposition. H_2 were flown into the reactor for controlling the reaction pressure, typically around 10 Torr.

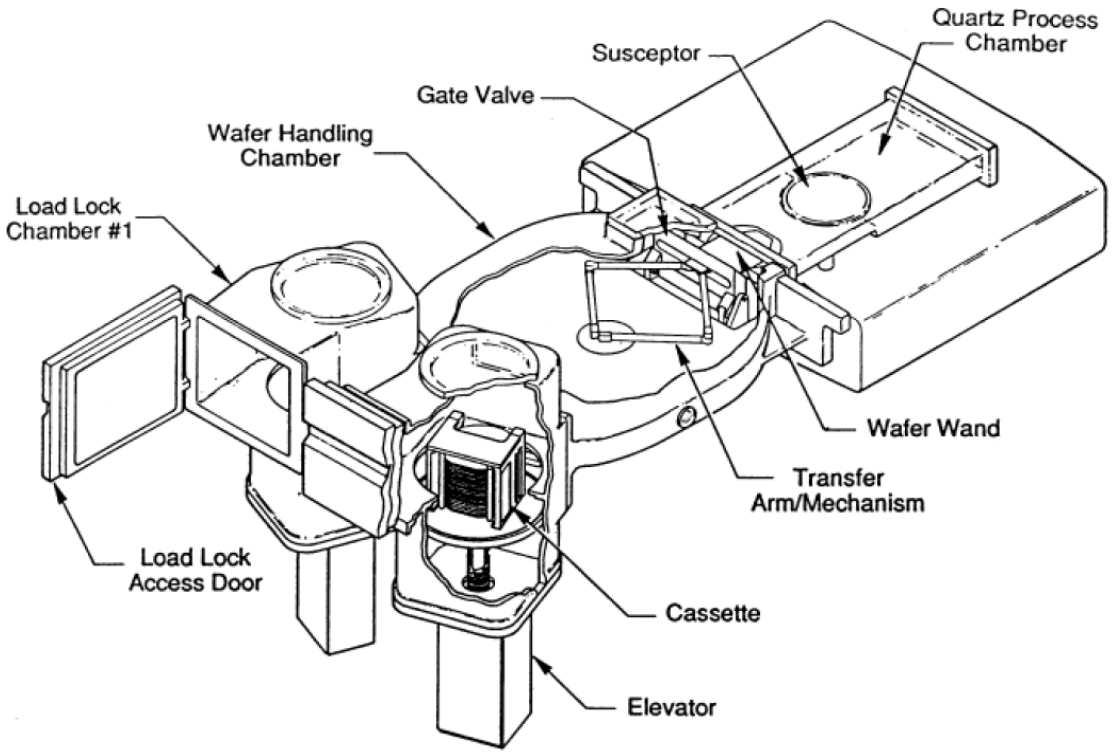

Fig. 4.2 ASM basic wafer-handling section drawing, courtesy of ASM Epitaxy

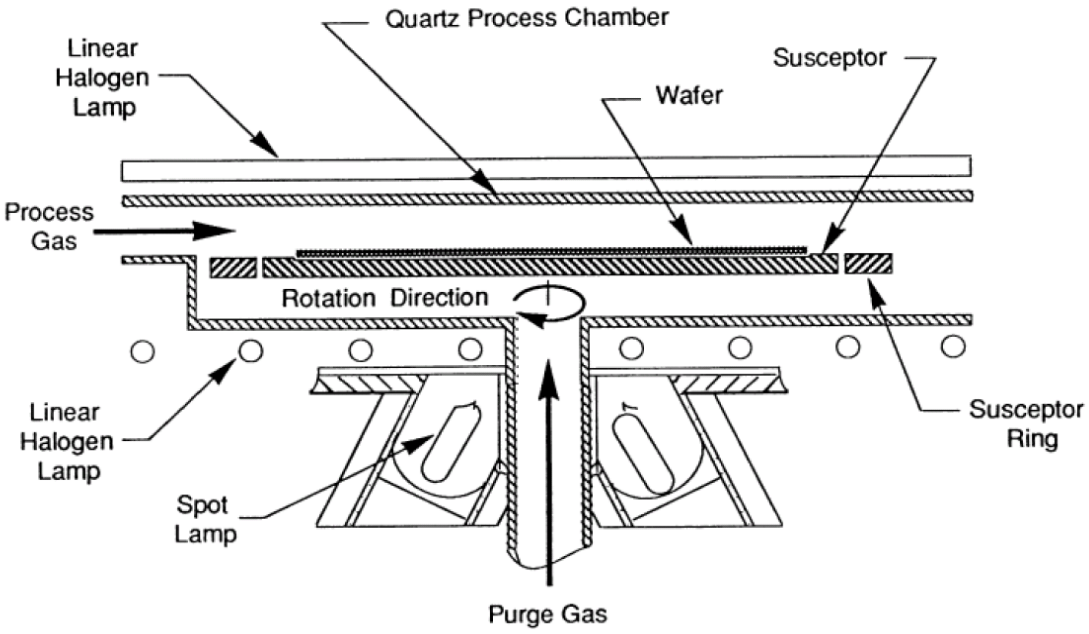

Fig. 4.3 Reactor quartz susceptor and lamp arrays drawing, courtesy of ASM

In a CVD process, there are seven main steps [54], as highlighted with numbers in Fig. 4.4. The reactants are transported to the deposition region (1) followed by diffusion of reactants from the gas stream through the boundary layer to the wafer surface (2). The reactants are adsorbed on the wafer surface (3). Chemical decomposition and reaction take place on the surface accompanied with surface migration to attachment sites (4). Byproducts are desorbed from the surface (5), and flow to the main gas stream by diffusion (6). Finally, a thermal process is used to force away the byproducts from the deposition region (7).

Epitaxial growth is a special form of CVD process when the grown film takes the crystal lattice of the underlying substrate. Ideally, the grown substrate will be single crystal if the underlying substrate is single crystal. Previous research showed that the Ge-grown-on-Si process is surface reaction limited at temperatures below 450ºC and is mass transport limited above 450ºC. This has been observed both in rapid thermal chemical

deposition systems and in ultrahigh vacuum chemical vapor deposition (UHV/CVD) systems [55,56]. It has also been reported that at 330ºC [57] (or 350ºC [58]), Ge growth occurs in an SK-related 2-D layer-by-layer mode. The major part of the relaxation process occurs during the deposition of the first two monolayers and the relaxation occurs primarily by the generation of misfit dislocations at the Ge/Si interface. Above 375ºC, growth occurs by the 3-D kinetically rough mode, in which islands form and the Ge surface roughness dramatically increases [58]. This is usually accompanied by a high dislocation density, increased leakage current, and degraded device performance. When the temperature increases above 600ºC, the step flow growth mode with reduced threading dislocation density and continuous 2-D growth is observed [17,59,60].

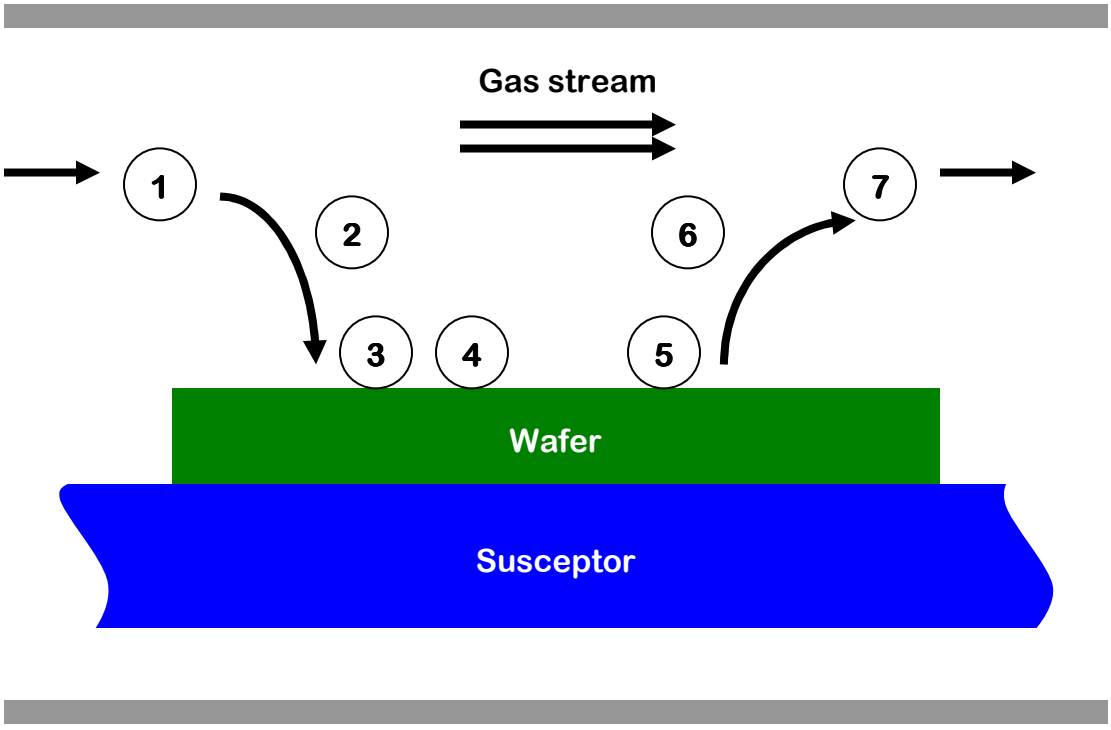

Fig. 4.4 The seven parts of a CVD process

The starting substrates are 4" Si (001) wafers with resistivity in the range of 1-5 Ω-cm. An ultra-clean surface before the epitaxy is essential in order to ensure good crystal quality. This is achieved using a standard clean consisting of two main steps to remove organic and metallic contaminants. The organic and gross contaminants such as scribe dust are removed using a 4:1 volume ratio mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) at 90ºC for 10 minutes. A thin chemical oxide is formed on the surface of Si substrate due to the oxidizing nature of H_2O_2 and this can be removed by a dilute hydrofluoric acid (HF). Following the removal of organics, the wafers are cleaned in a 5:1:1 volume ratio mixture of de-ionized (DI) water, hydrochloric acid (HCl) and H_2O_2 at 70ºC for 10 minutes in order to remove alkali ions and other metallic contaminants. H_2O_2 oxidizes the surface while HCl reacts with most metals to form soluble chlorides. Similar to the previous step, a chemical oxide forms on the surface during this clean. This chemical oxide and any native oxide on the surface of the wafer will prevent good epitaxial growth, hence they need to be removed. A 30 sec etch in 50:1 diluted HF solution is used to remove the oxides from the surface. To ensure no native oxide grows on the surface, wafers are loaded into the reactor immediately after the cleaning. The wafers are kept in the load lock for 30 min where they are purged with nitrogen to drive out any additional moisture on the surface. This step also helps avoid oxygen incorporation into the process chamber during wafer transfer. During this step, the process chamber is etched to remove deposition residuals from the previous run.

The first step in all growth recipes is to etch the process chamber before transferring the wafer from the load lock. This pre-growth-etch is standardized for all recipes and is performed at an elevated temperature with HCl flown as the etchant. Following this step, the wafer is loaded into the process chamber and it is subjected to a hydrogen bake at 950ºC. This bake is essential for good quality epitaxy and it ensures the removal of the native oxide on the surface. A thin Ge layer (150-200 nm) is grown at 400ºC with a total pressure of 10 Torr. The resulting films have high surface roughness (~ 25 nm) and defect density. The films are then in-situ annealed in H_2 ambient at 80 Torr between 825-850ºC for 60 min. The hydrogen annealing is the heart of this technique and facilitates the reduction of both the surface roughness and the dislocation density [18,61]. The rest of the growth now becomes a homoepitaxy of Ge on a virtual substrate, hence no more

dislocations are introduced. The cycle of growth and hydrogen annealing steps is repeated until the desired film thickness is achieved. A typical growth recipe with the pre-deposition hydrogen bake and the film growth including the process gases is provided in Appendix II. It should be noted that no dopant gases are introduced during the epitaxy hence the Ge films are intrinsic, facilitating low voltage operation.

4.2.2 Photodetector fabrication

The surface of the Ge film needs to be passivated to avoid surface leakage currents. This is especially important for lateral metal-semiconductor-metal (MSM) photodetectors, in which the highest electric fields are at the surface. The native oxide of Ge is not stable (it is volatile and water soluble) and hence it cannot endure CMOS processing [62-64]. Alternative surface passivation technologies for Ge are ongoing research subjects for MOSFET applications as well. Various metal oxides [65-67] and nitrided germanium oxide capped with SiO_2 [68] are promising candidates as gate dielectrics. No mature technology existed at the time of our experiments; therefore, SiO_2 is used for surface passivation. Following the epitaxial growth, the wafers are coated with CVD SiO_2 at 400°C. This layer also acts as an anti-reflection coating to minimize reflections from the surface. The electrodes are defined by photolithography and patterned by standard photoresist lift-off. Prior to metal deposition, the CVD SiO_2 is removed from the electrodes with a buffered HF etchant. Metal electrodes are formed by electron-beam (e-beam) evaporation from high purity targets. 15 nm of Ti, Ni and Cr are used for workfunction control and adhesion, capped with 35 nm Au for probing. An outline of the process is shown in Fig. 4.5 with an SEM image of the final structure. MSM detectors with finger width and spacing ranging from 1-10 μm were designed with active absorption areas of 10^2-10^4 μm^2. No thermal treatments are performed afterward to avoid interdiffusion and alloying between semiconductor and metal.

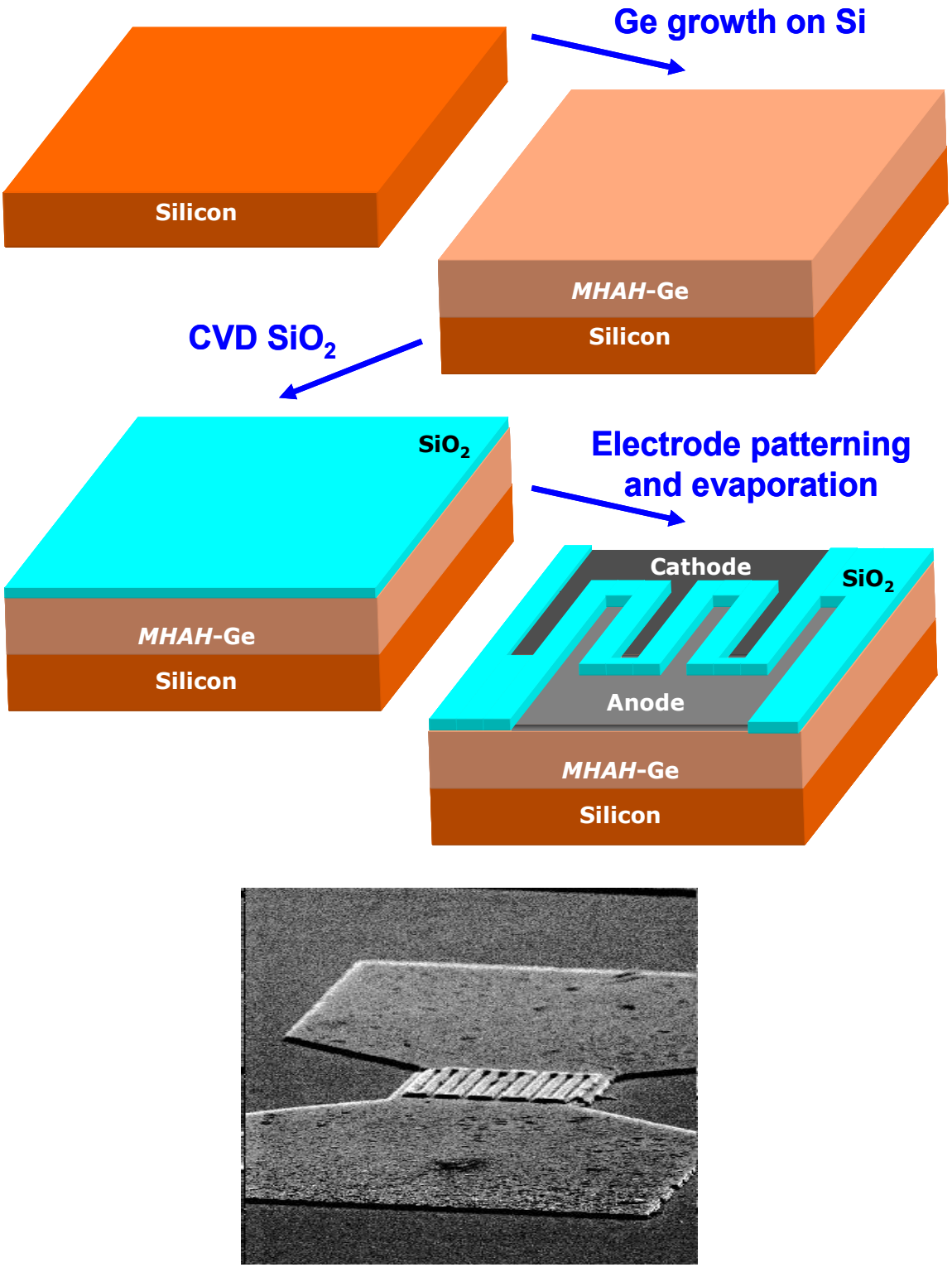

Fig. 4.5 Photodetector fabrication process flow. The SEM image of a completed MSM is shown at the bottom.

4.3 RESULTS AND DISCUSSION

The results presented here are in the order of physical characterization of the grown films including surface roughness and dislocation density, followed by electrical characterization and photoresponse of the optical detectors.

4.3.1 Surface roughness and dislocation density

Atomic force microscopy (AFM) is used to extract the surface roughness of the films. As-grown films without the hydrogen annealing exhibit ~ 25 nm rms surface roughness. After annealing, surface roughness is reduced to 2.9 nm in thick films. These results are in good agreement with the suggested surface roughness reduction model explained by Nayfeh et al. which attributes the roughness reduction to hydrogen-mediated Ge diffusion and the reconstruction of the surface [1,2]. It was shown that hydrogen annealing can reduce surface roughness by 90% when performed at an optimized temperature. Annealed wafers tend to assume a shinier surface by visual inspection compared to the dull appearance of the as-grown samples. The hydrogen annealing is especially critical for the first layer of Ge as this will provide a smooth template for subsequent growth.

The reduction in dislocation density with hydrogen annealing is illustrated in Fig. 4.6 and Fig. 4.7 [18]. A cross-sectional TEM image of a 1-μm-thick as-grown Ge layer on Si at 400°C is presented in Fig. 4.6. The dislocations have formed at the Ge/Si interface and have threaded to the surface. Fig. 4.7 on the other hand, is a cross-sectional TEM image of a two step MHAH growth that yielded a ~ 400 nm Ge layer on Si. Near the surface, the dislocation density is reduced while near the Ge/Si interface the dislocation density is very large.

Plan-view TEM is employed to quantify the dislocation density in the films. The samples are prepared by grinding from the back side of the Si substrate down to ~ 100 μm thickness. A 70-μm-deep dimple is carved into the sample, again from the back side, which is followed by ion milling to further thin the sample. Fig. 4.8 depicts a typical sample prepared for measurement.

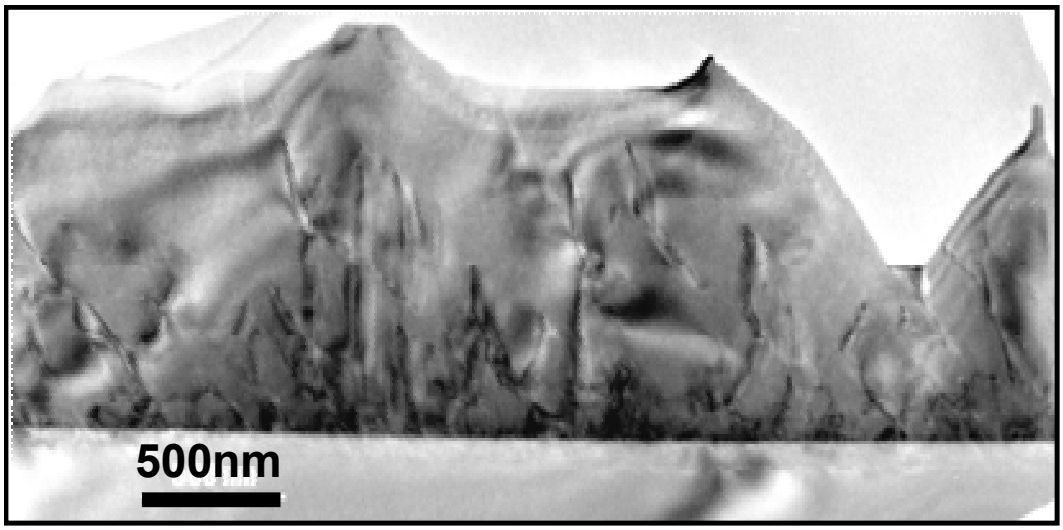

Fig. 4.6 Cross sectional TEM image of 1-μm-thick as-grown Ge layer on Si at 400°C. Misfit dislocations at the Ge/Si interface thread to the surface.

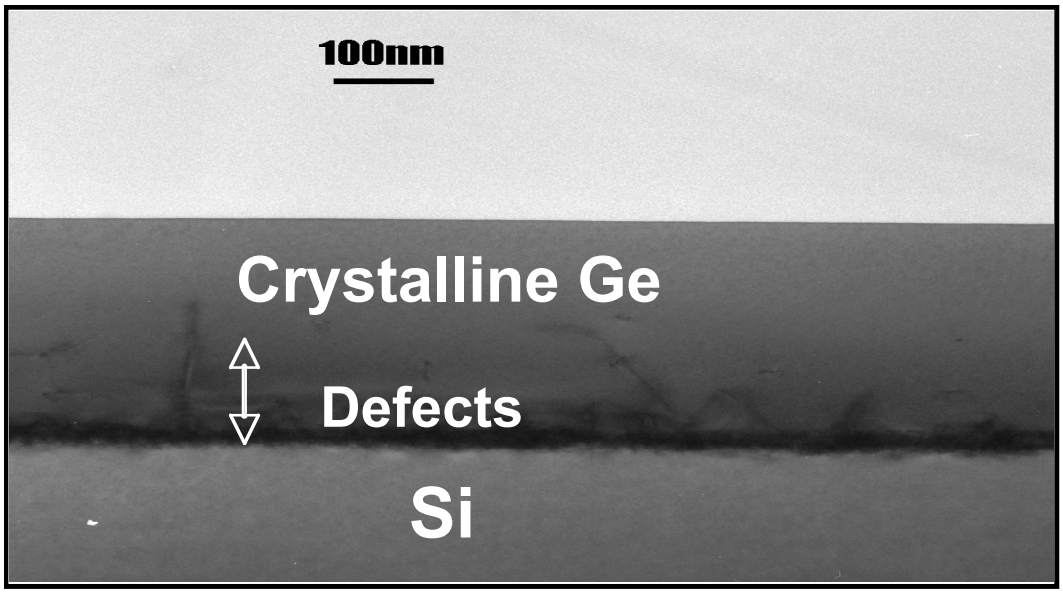

Fig. 4.7 Cross sectional TEM image of 400-nm-thick Ge layer grown on Si at 400°C followed by 1 hr anneal in H_2 ambient at 825°C. Both defect density and surface roughness are reduced. Most of the defects are concentrated at the Ge/Si interface, while the surface is low in defect density.

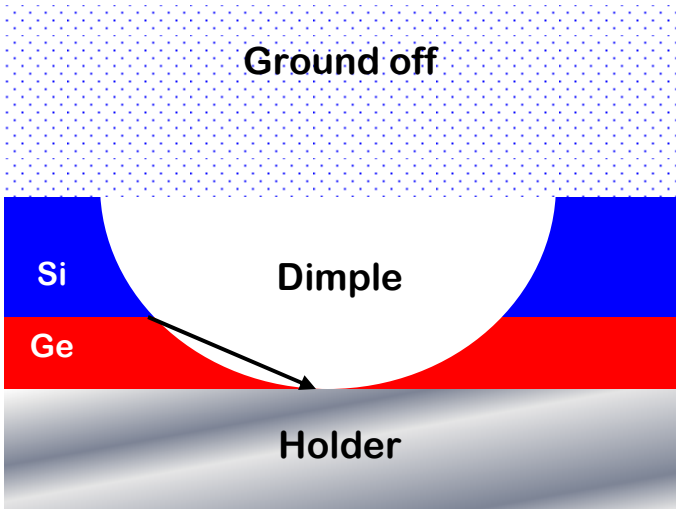

Fig. 4.8 Schematic of the plan-view sample after preparation for measurement.

The plan-view TEM image of the 400 nm thick Ge film is shown in Fig. 4.9. The arrow points in the direction of thinner sample towards the surface, indicating drastic reduction in the dislocation density. Threading dislocation density for the top 100 nm of the film is extracted to be 2×10^{8} cm^{-2}. The lowest dislocation density is obtained from a thick film. In the first step, a Ge layer is grown at 400°C at a reduced pressure of 10 Torr. This is followed by hydrogen annealing for 1 h at 825°C and at a pressure of 80 Torr, which yielded ~ 155 nm of Ge with RMS surface roughness of 2.9 nm. The first set of growth and anneal steps are repeated a second time. After the second growth and anneal, a two-step growth process is carried out with only one additional hydrogen anneal with the goal of achieving a thick layer of Ge. The growth temperature is increased to 460°C for 15 min for the first growth step. To further increase the growth rate, the temperature is raised to 500°C for 15 min duration. Finally, 1 hour hydrogen annealing at 700°C completed the process, yielding a 4.5 μm epitaxial Ge layer. The plan-view TEM image of this sample is shown in Fig. 4.10. The extracted threading dislocation density is < 7×10^{7} cm^{-2}. The reduction in the dislocation density is attributed to the motion of dislocations during the annealing steps. The velocity of dislocations vs. temperature is calculated for relaxed Ge layers grown on Si [69]. The peak velocity occurs at 825°C, which is the temperature used for hydrogen annealing of the grown layers.

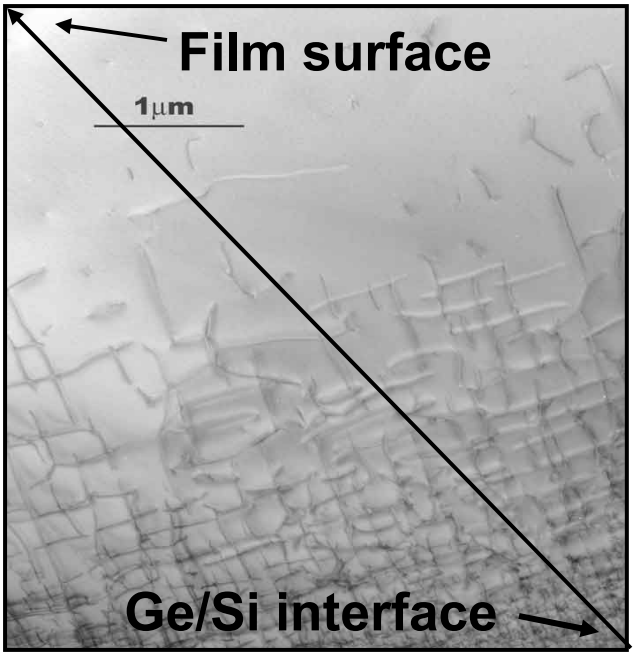

Fig. 4.9 Plan-view TEM image of 400-nm-thick Ge layer grown on Si by MHAH technique. The sample becomes thinner in the direction of the arrow, indicated in the previous figure as well. The upper layer of the film shows drastic reduction in defect density.

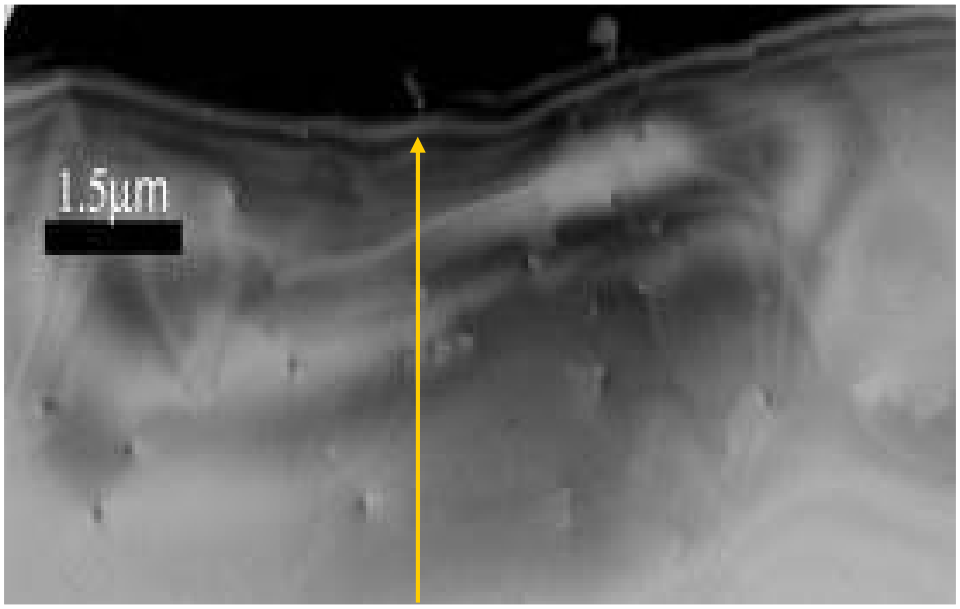

Fig. 4.10 Plan-view TEM image of a 4.5-μm-thick MHAH-grown Ge layer on Si. 200-nm-depth from the surface is shown. Dislocation density is reduced to less than 7×10^{7} cm^{-2}.

In addition, our collaborators with Canon repeated this process using an industry standard reactor with a double growth and double annealing with the second annealing done at 700°C. A 50× reduction in threading dislocation density was obtained from the as-grown case with final density of 1.5×10^{7} cm^{-2}. Fig. 4.11 shows the plan-view TEM images from these samples.

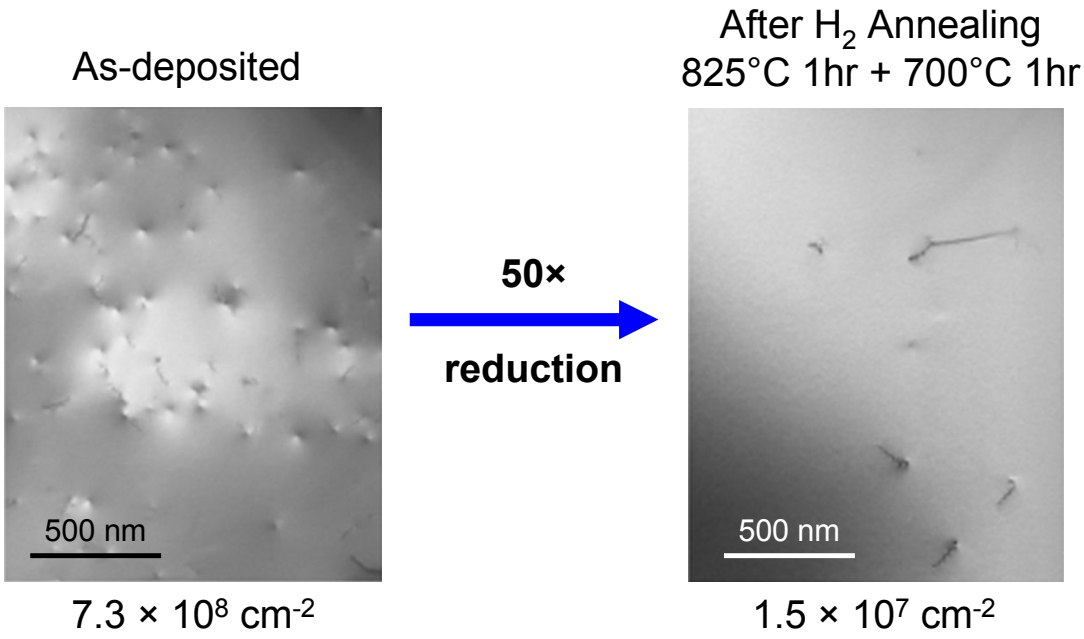

Fig. 4.11 Plan-view TEM image of as-grown and H_2 annealed Ge on Si showing 50× reduction in dislocation density. Film growth is carried out in an industry-standard epi-reactor in Canon.

4.3.2 Electrical characterization

First, individual metal-semiconductor (MS) junctions are characterized to verify Schottky behavior and assess the layer quality. Fig. 4.12(a) shows the current-voltage (I-V) characteristics of the Ti-Ge contact with very good Schottky rectification. The total area of the MS junction diode is 1.25×10^{4} μm^2, which yields a reverse saturation current density of 32 mA/cm^2 at 5 V reverse bias. Both decent rectification behavior of the MS diodes and very low reverse saturation current density are indications of excellent electrical quality of the Ge films. These measurements are obtained from vertical MS junctions. A schematic of the measured structure is illustrated in Fig. 4.12(b)

accompanied with the energy band diagram of the system in Fig. 4.12(c). It should be noted that the grown Ge film is intrinsic since no dopant gases are introduced during the epitaxy. The underlying Si substrate does not influence the current flow in the reverse bias operation. Furthermore, in the forward bias region, the flow of holes is impeded by the potential barrier due to valence band offset between Si and Ge and the resulting potential step. The energy band diagram argument signifies that the on-state-current of the MS diode is underestimated and the MS junction rectification is even stronger than reported.

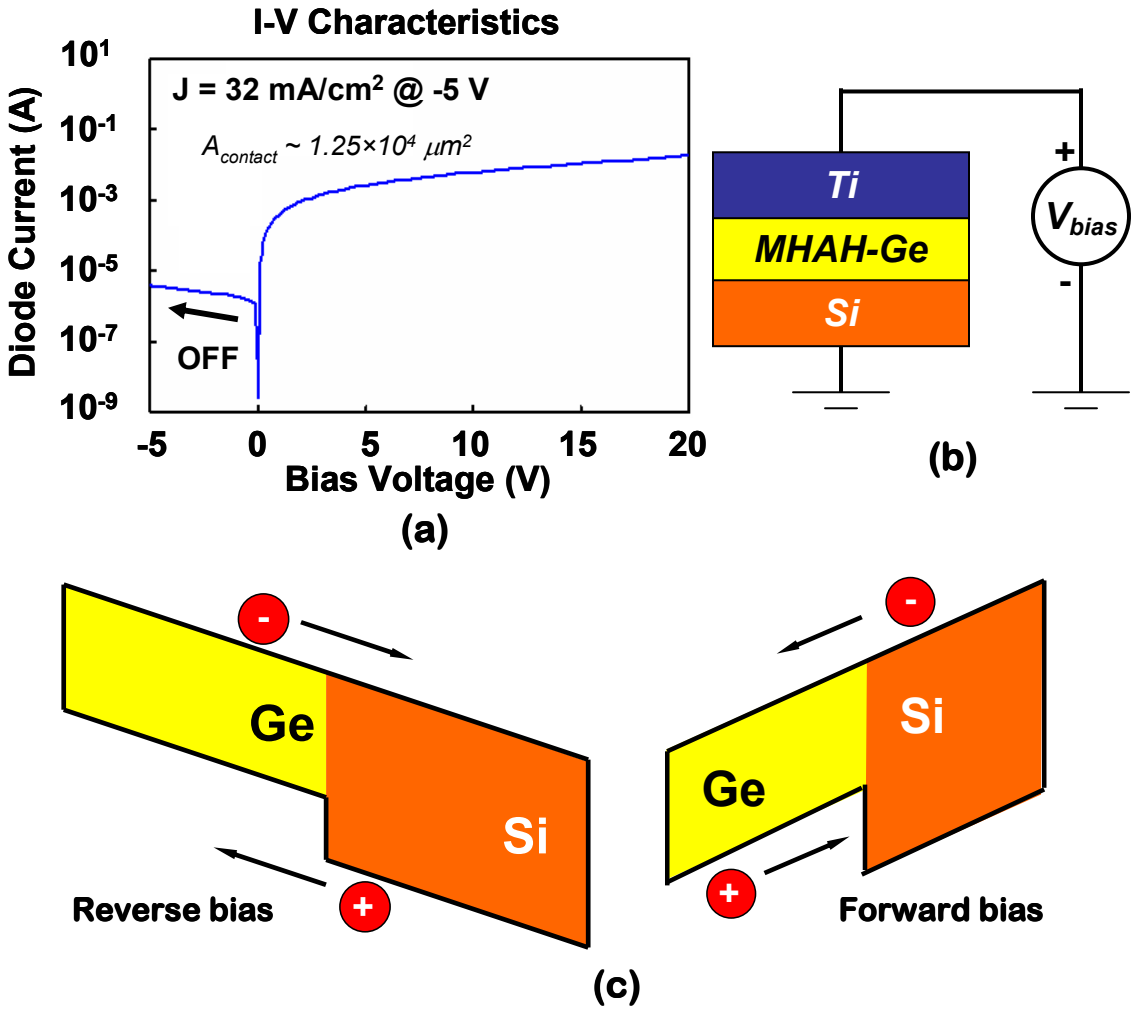

Fig. 4.12(a) Measured I-V characteristics of the Ti-Ge Schottky diode. Decent rectification obtained with low reverse saturation current density.
(b) The schematic of the measured MS diode structure and applied bias.
(c) Energy band diagram of the measured MS diode.

Next, back-to-back MS diodes are characterized. The measured I-V characteristics of such MSM structures with 5 μm electrode width and spacing are shown in Fig. 4.13. Ti-Ge-Ti symmetric MSMs have lower dark current (I_{dark}) than the Ni-Ge-Ni symmetric case. This is because the Ti workfunction (4.3 eV) is around the midgap energy level of Ge providing a high injection barrier for both electrons and holes as discussed in Chapter 3. On the other hand, the Ni workfunction (5.2 eV) is close to the valence band energy of Ge resulting in a small barrier for hole injection. Cr-Ge-Cr symmetric photodetectors yield dark current values similar to the Ti-Ge-Ti case owing to similar workfunctions of Cr and Ti. The dark current densities extracted for these structures are ~ 100 mA/cm^2 at 1 V reverse bias. This is attributed to the planar structure of the MSMs and hence an increased surface leakage due to lack of good passivation of Ge surface, as discussed previously. It should also be noted that the MSM photodetector structure employed here has not been optimized for I_{dark} suppression. For instance, the large probing pads were in intimate contact with the Ge film together with the interdigitated fingers.

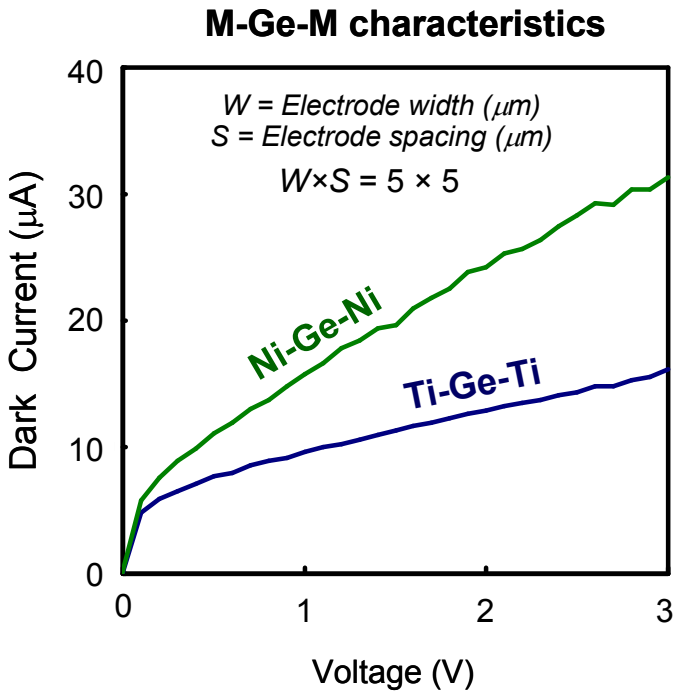

Fig. 4.13 Experimental I-V characteristics of back-to-back MS diodes. Interdigitated MSM with electrode width and spacing 5 μm. Ti-Ge-Ti and Ni-Ge-Ni symmetric detectors.

Measured I-V characteristics of interdigitated MSMs with different finger spacing are plotted in Fig. 4.14. The finger width is fixed at 1 μm and the finger spacing is varied from 3 μm to 5 μm. As the finger spacing is increased, dark current at a given bias is reduced due to reducing electric field. This is another indication of high electrical quality of the Ge layers grown using the MHAH technique.

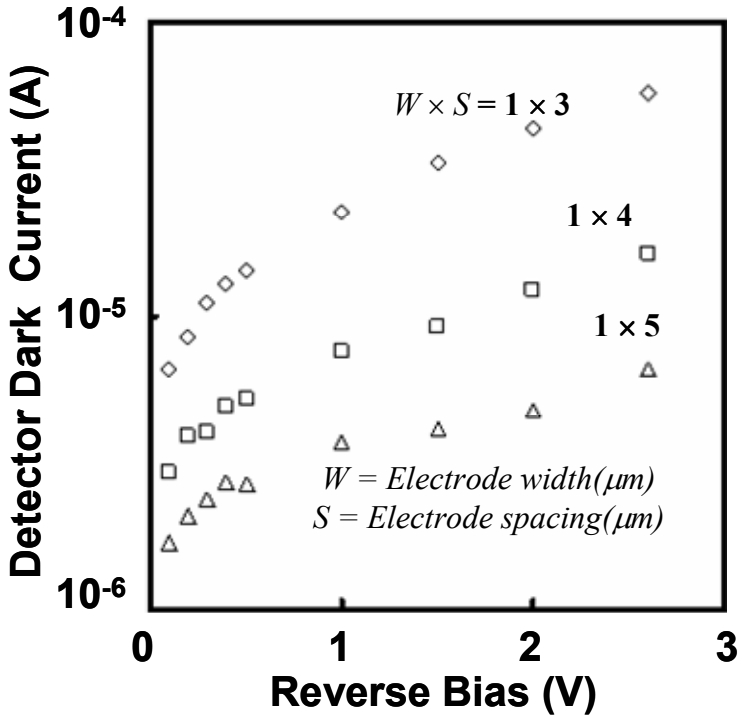

Fig. 4.14 Experimental I-V characteristics of Ti-Ge-Ti interdigitated MSM with electrode width 1 μm and spacing 3,4, and 5 μm.

4.3.3 Optical characterization

The photoresponse of the MSM detectors is obtained using 1550 nm laser illumination. At a specific reverse bias, the laser power is increased while recording the resultant dc current through the MSM. This is repeated for a range of reverse bias voltages, and the obtained data points are fitted with linear approximations. The optoelectronic quality of the Ge film can also be investigated by measuring the dependence of the photocurrent on the applied electric field (E) and the intensity of light impinging on the sample. The measured photocurrent I_{photo} versus E is found, for weak

fields, to exhibit a linear relation as described by the Hecht formula [70] but saturates for large values of E, as shown in Fig. 4.15. Moreover, the photocurrent remains linear for over an order of magnitude in light intensity for various applied voltages. A typical set of data points with corresponding linear fit are plotted in Fig. 4.16. The photocurrent is linear over an order of magnitude in light intensity verifying excellent optical quality of the Ge layer.

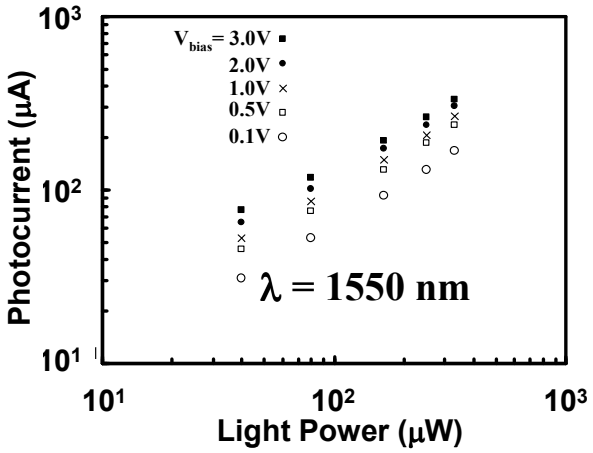

Fig. 4.15 Photocurrent versus light intensity at different applied reverse bias for Ti-Ge-Ti MSM with electrode width and spacing 5 μm.

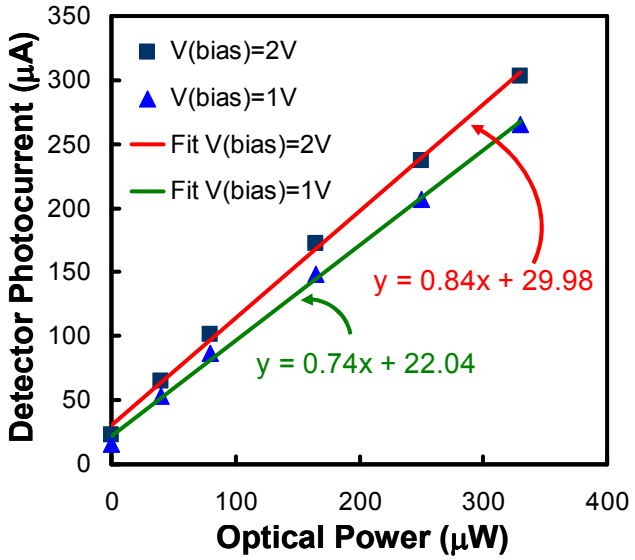

Fig. 4.16 Detector current vs. input optical power (λ = 1550 nm) for MSM with electrode width and spacing 5 μm. The points are measured data and the lines are theoretical fit.

The slopes of the linear fitting curves in Fig. 4.16 have the units of A/W which is responsivity ($\Re$). For each reverse bias condition, the slope of the linear fit is used to extract the responsivity and the resulting curve for the Ti-Ge-Ti photodetector operated at 1550 nm is plotted in Fig. 4.17(a). The active absorption area of the device is 10^4 μm^2 with 5 μm electrode width and spacing. We observe $\Re$ of 0.74 A/W under 1 V reverse bias, corresponding to 61% external quantum efficiency (η_{ext}). The highest $\Re$ at 2 V reverse bias is 0.84 A/W, corresponding to η_{ext} ~ 68%, is observed from a detector with 5 μm electrode width and spacing. This value is among the highest reported so far in the literature.

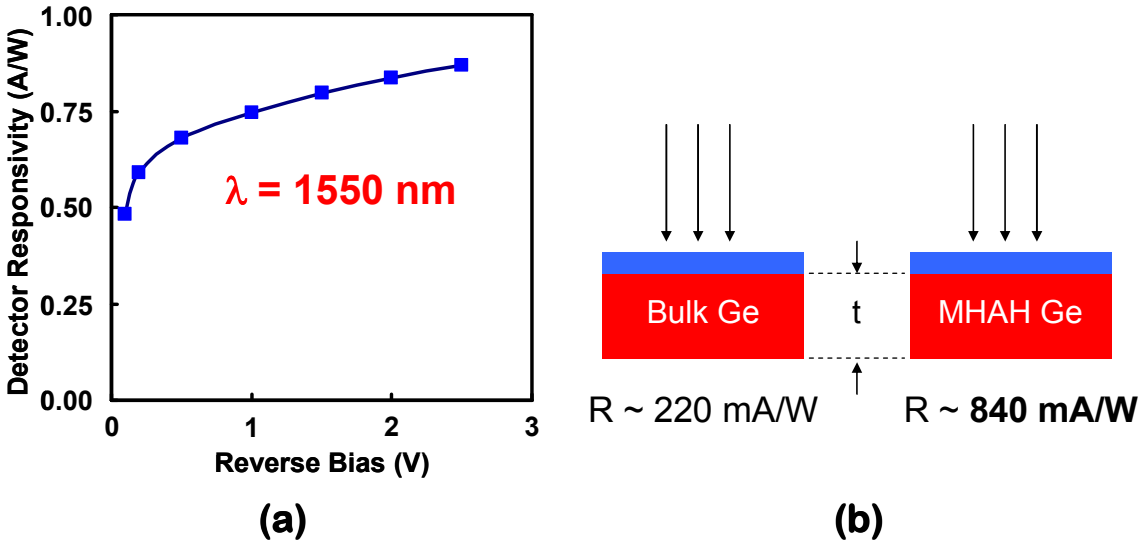

Fig. 4.17(a) Measured responsivity of Ti-Ge-Ti MSM with electrode width and spacing 5 μm. At every bias point, responsivity is extracted from the slope of the linear fit in the previous figure.
(b) Comparison of theoretical vs. experimental responsivity.

The responsivity of a photodetector can be calculated by

$$\Re = (e\lambda / hc)(1 - R_{refl})[1 - \exp(-\alpha_{Ge} t_{Ge})](\eta_{int}) \qquad (4.1)$$

where R_{surf} accounts for losses due to surface reflections, α is the absorption coefficient in inverse distance, t_{film} is the absorbing film thickness and η_{int} is the internal quantum

efficiency. The schematic in Fig. 4.17(b) compares the experimental results with the theoretical expectations. The absorption coefficient of bulk Ge (α_{Ge}) at 1550 nm is ~ 490 cm^{-1} [71]. The refractive index of the deposited 300-nm-thick CVD SiO_2 (n_{oxide}) is ~ 1.7 and n_{Ge} is ~ 4. The calculated surface reflection at λ = 1550 nm is 13% [72]. Assuming 100% internal quantum efficiency, the theoretical maximum $\Re$ for 4.5-μm-thick Ge layer at this wavelength is ~ 220 mA/W. The experiments yield that measured $\Re$ (~ 840 mA/W) is roughly 4× higher than the maximum theoretical expectation. A detailed explanation of this phenomenon is presented in the following section.

In high performance applications, it is desirable to deplete the semiconductor region completely to achieve highest internal quantum efficiency. The grown Ge layers reported here are intrinsic in order to achieve total depletion at small bias voltages. Assuming a doping density for as-grown undoped Ge, to be ~ 10^{14} cm^{-3} for instance, the extent of depletion layer is 4.2 μm and 5.9 μm for 1 V and 2 V reverse bias, respectively. It is evident from these calculations and Fig. 4.17(a) that the MSM detectors are fully depleted even at small reverse bias voltages.

The detectors were not optimized for fast response because of lithographic limitations. Simulations show time response ~ 350 psec at a reverse bias of 2 V, corresponding to a frequency cutoff higher than 1 GHz. Detector bandwidth could be further improved by submicrometer film thickness [46] in a trade-off for reductions in $\Re$. The performance of the photodetectors can be optimized by incorporating different metals to provide work-function asymmetry. This may be helpful in obtaining a built-in E-field, such as in p-i-n detectors, to facilitate low-voltage bias operation [73].

4.4 STRAIN AND STRESS IN MHAH-GROWN GE LAYERS

The difficulty of direct epitaxy of Ge on Si stems from the lattice mismatch between the two material systems. The lattice constants for Si and Ge are a_{Si} = 5.43105 Å, and a_{Ge} = 5.65785 Å, respectively [74]. The lattice mismatch can be calculated by

$$\frac{a_{Ge} - a_{Si}}{a_{Si}} \times 100 = 4.1759\% \qquad (4.2)$$

As Ge is epitaxially grown on Si, the first few monolayers of Ge conform to the lattice constant of the underlying Si substrate. As a result, this ultra-thin Ge layer is compressively strained because Si lattice constant is smaller than that of Ge. This situation is illustrated in Fig. 4.18(a), noting that the thin Ge layer is defect-free. At a critical thickness during further growth, it becomes energetically more favorable to relieve the strain by forming misfit dislocations at the Ge/Si interface as depicted in Fig. 4.18(b). It has been shown that this critical thickness is around 4-10 nm [75]. In addition to misfit dislocations, islanding can occur as an additional means of reducing the elastic strain energy of the film. Therefore, thick Ge layers grown on Si will be relaxed through defects and dislocations [18]. In the next section, detailed examination of the lattice and stress/strain state of the MHAH-grown Ge on Si layers is presented. It was found that the grown Ge films are not fully relaxed as predicted by [18], but rather they are under residual tensile strain. The origin of the tensile strain and its effects on the photodetector performance will be explained in the subsequent sections.

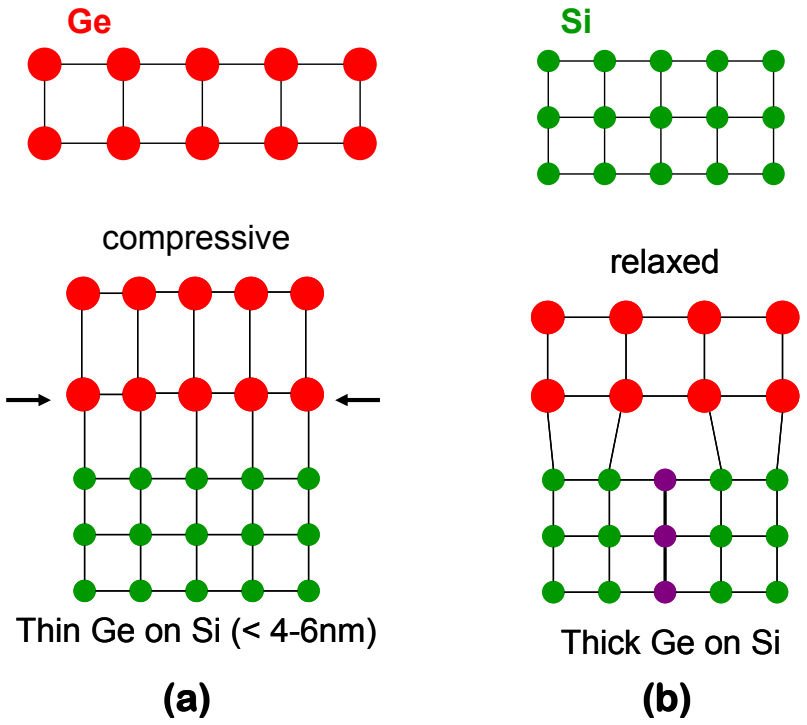

Fig. 4.18(a) Ultra-thin Ge grown on Si is under compressive strain. No defects are introduced until critical thickness is achieved (~ 5 nm).
(b) Thick Ge layer grown on Si. The stress is relieved by forming dislocations and Ge attains the relaxed lattice constant.

4.4.1 Residual tensile strain in Ge layers

X-ray diffraction analysis (XRD) is a tool that can be used to analyze the crystal lattice. The X-ray probe interacts with the periodic crystal lattice resulting in a diffraction pattern. The intensity of reflected waves is counted over a range of reflection angles. The lattice parameters can be extracted using Bragg angles from diffraction peaks and Bragg's law [76,77]

$$2d_{hkl}\sin\theta = \lambda \tag{4.3}$$

where d_{hkl} is the spacing between atomic planes, θ is the half angle of the peak position and λ is the wavelength of the incident radiation (Cu $K_{\alpha 1}$ line, λ = 1.5406 Å). Starting from a standard (004) Ω–2θ scan such as the one plotted in Fig. 4.19, it is possible using Bragg's law to extract the lattice parameter of Ge layer in the growth direction, $a_{Ge}^{\perp}$, from the associated angular position ω_{Ge}^{004} of the peak. Indeed, it is given by [78]

$$a_{Ge}^{\perp} = \frac{2\lambda}{\sin(\omega_{Ge}^{004})} \tag{4.4}$$

Knowing the relationship linking the Ge layer in-plane ($a_{Ge}^{\parallel}$) and perpendicular ($a_{Ge}^{\perp}$) lattice parameters to the bulk, unstrained Ge lattice parameter (a_{Ge} = 5.65785 Å), i.e.,

$$a_{Ge} = \left(\frac{1-\nu}{1+\nu}\right)a_{Ge}^{\perp} + \left(\frac{2\nu}{1+\nu}\right)a_{Ge}^{\parallel} \tag{4.5}$$

ν=0.271 being the elastic modulus of Ge, it is possible to extract the degree of strain relaxation Θ of our Ge layers, given by

$$\Theta = \left(\frac{a_{Ge}^{\parallel} - a_{Si}}{a_{Ge} - a_{Si}}\right) \tag{4.6}$$

a_{Si} = 5.43105 Å, being the lattice parameter of our Si substrates [78]. The sample plotted in Fig. 4.21 has a degree of strain relaxation Θ = 104%. This means that the Ge layer is in

a tensile-strain configuration onto Si(001) substrates. This translates into ~ 0.168% residual tensile strain.

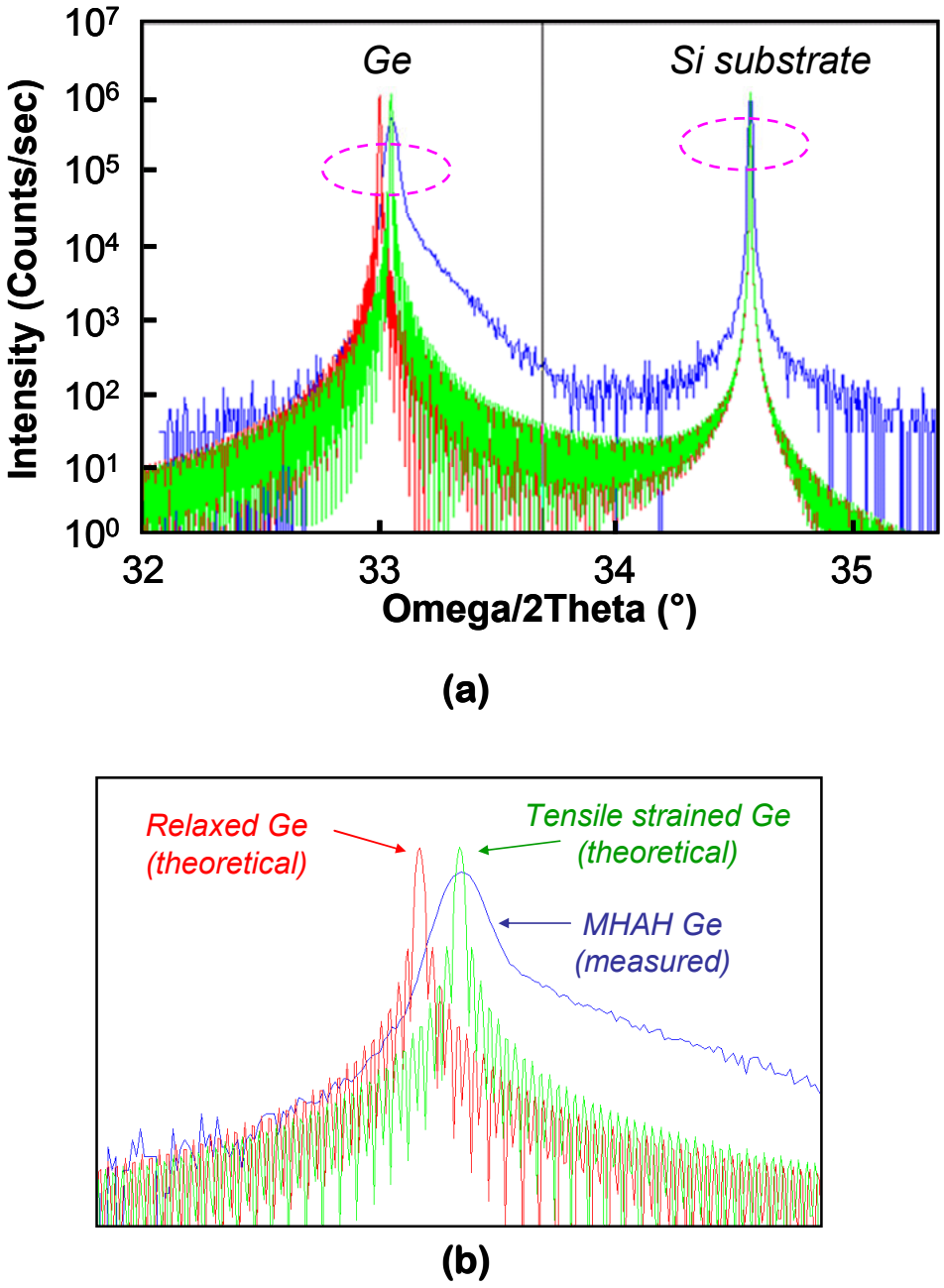

Fig. 4.19(a) (004) Ω–2θ XRD scan of MHAH-Ge grown on Si. The peak on the right is from the Si(001) substrate and the one on the left is Ge lattice.
(b) Magnified view of the Ge peak. The blue curve is the measured signal, the red and green curves are calculated curves for relaxed and tensile strained Ge, respectively.

A similar tensile strain configuration has been reported by MIT researchers [79] for 1-μm-thick, UHV-CVD grown Ge thick layers on Si(001) that have subsequently been submitted to some 700-900°C cyclic thermal anneal. Hartmann and co-workers have also observed a similar tensile strain configuration in Ge grown on Si(001) using a low-temperature/high-temperature approach [74].

4.4.2 Origin of the residual tensile strain

The Ge thick layers are relaxed on Si at the growth/anneal temperature. However, there is a difference between the linear coefficients of thermal expansion of Si and Ge Indeed, $\Delta a/a(Ge) = 5.8\times10^{-6}\ \Delta T\ (°C)$, vs $\Delta a/a(Si) = 2.6\times10^{-6}\ \Delta T\ (°C)$ [80]. This translates into a lattice mismatch between Si and Ge which increases from 4.18% at room temperature up 4.38% at 600°C and 4.45% at 850°C. The Ge thick layer, which is nearly fully lattice-matched to the Si substrate at the growth temperature or at the annealing temperature, finds itself in a tensile strain configuration at room temperature, as illustrated in Fig. 4.20. The as-grown Ge layer on Si is relaxed through defects and dislocations. Our films are annealed in hydrogen ambient between 825-850°C followed by cooling down to room temperature. During this cool down, due to the mismatch between the coefficients of thermal expansion of Si and Ge, the latter tries to contract faster than Si. However, the Ge layer has to comply with the Si substrate, and hence it undergoes residual tensile strain. It has been suggested that this phenomenon occurs most probably because the perpendicular lattice parameter of our Ge layers shrinks more easily during the cooling-down phase than the in-plane one, whose temperature behavior is somewhat influenced by the Si substrate underneath.

What can also be noticed from X-ray diffraction profile in Fig. 4.19 is that the Ge peak is broadened compared to the theoretical estimates, with a quite definite tail towards the high incidence angles. This would mean that either some parts of the Ge layer are in a tensile strain configuration even more severe than the average 104% or more plausibly that some Si has diffused from the Si(001) substrate into the Ge layer during thermal annealing. Si inter-diffusion is separately verified by Rutherford back-scattering (RBS) showing 91% Ge in a 200-nm-thick Ge film and 96% Ge in a 400-nm-thick Ge film [18].

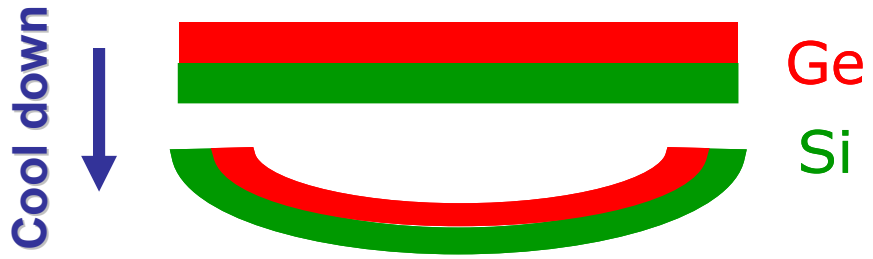

Fig. 4.20 Schematic illustration of mismatch between coefficients of thermal expansion between Si and Ge. Ge tries to contract faster than Si on cooling down from the annealing temperature (825-850°C).

4.4.3 Effects of strain on Ge band structure

The energy vs momentum (E-k) diagram for relaxed Ge is plotted in Fig. 4.21. The relaxed-state bands deform with the introduction of stress/strain in the Ge layer. Our films are under 0.168% residual biaxial tensile strain.

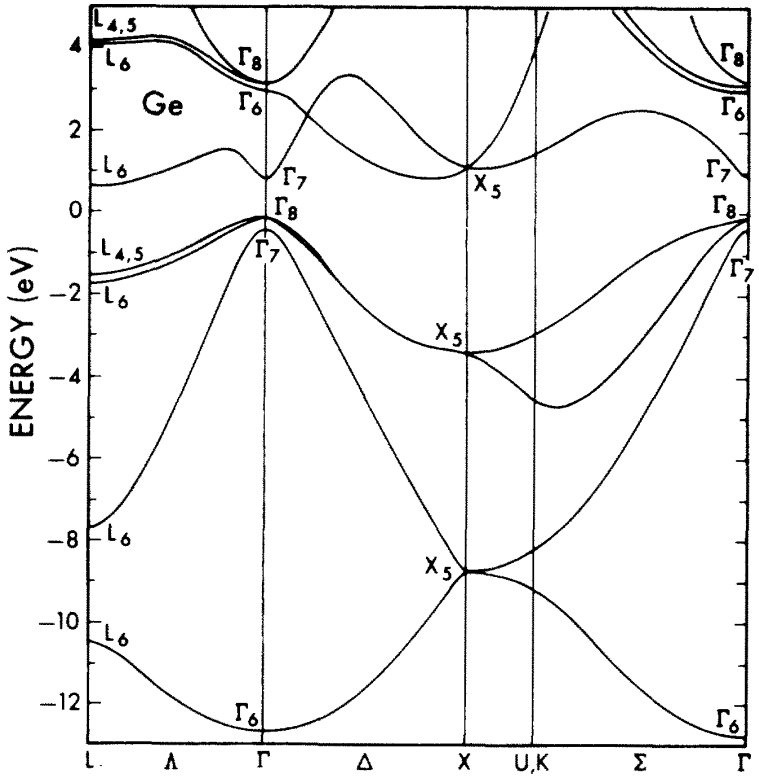

Fig. 4.21 Band structure of Ge calculated by Chelikowsky and Cohen [81].

The calculated valence and conduction band shifts at various symmetry points in Ge as a function of in-plane biaxial strain are plotted in Fig. 4.22 [82] using the deformation potentials from [83]. The conduction band minimum at the zone center is denoted by $\Gamma_{7,c}$. The valence band maxima for light holes and heavy holes are denoted by $\Gamma_{8,v1}$ and $\Gamma_{8,v2}$, respectively. The direct bandgap of Ge, which is the energy difference at the zone center between the minimum of the conduction band and the maximum of the valence band, is highlighted in Fig. 4.22. With increasing tensile strain, the direct energy band gap of Ge is shrinking. The minimum of the conduction band is moving down while the maximum of the valence band is moving up, as illustrated in Fig. 4.23. Furthermore, the effective masses are also slightly modified due to biaxial strain in the films [82].

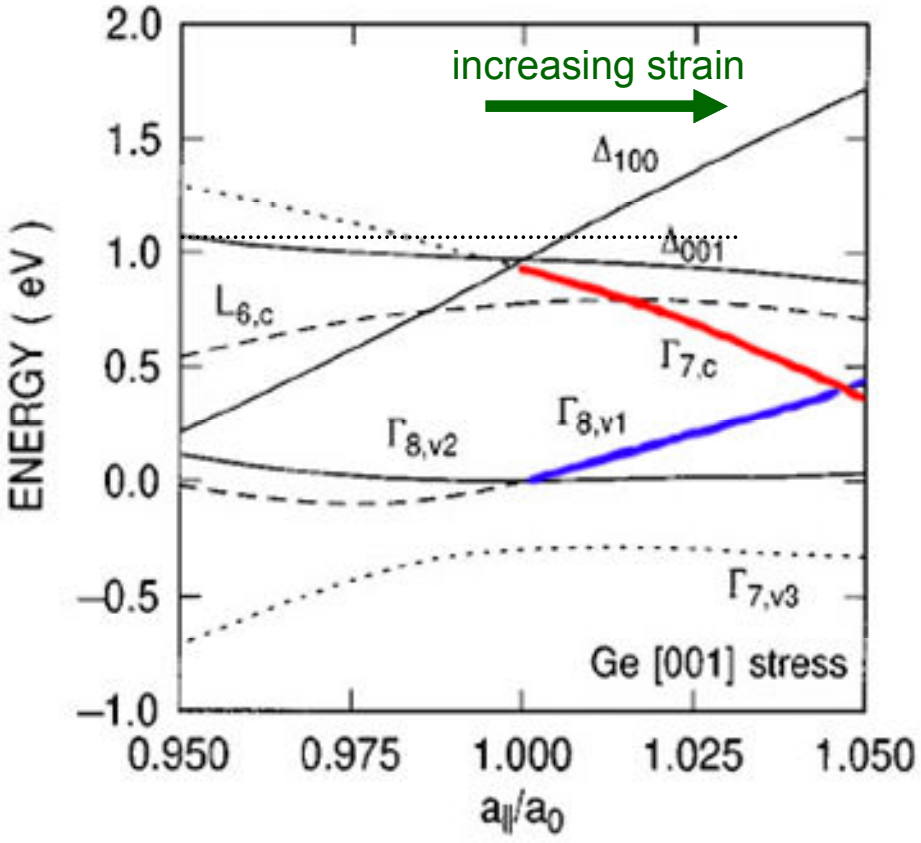

Fig. 4.22 Deformation of band structure of Ge with biaxial strain calculated by Fischetti [82]. The change in the conduction band minima at the zone center and the valence band maxima for light holes with increasing biaxial tensile strain are highlighted by red and blue, respectively.

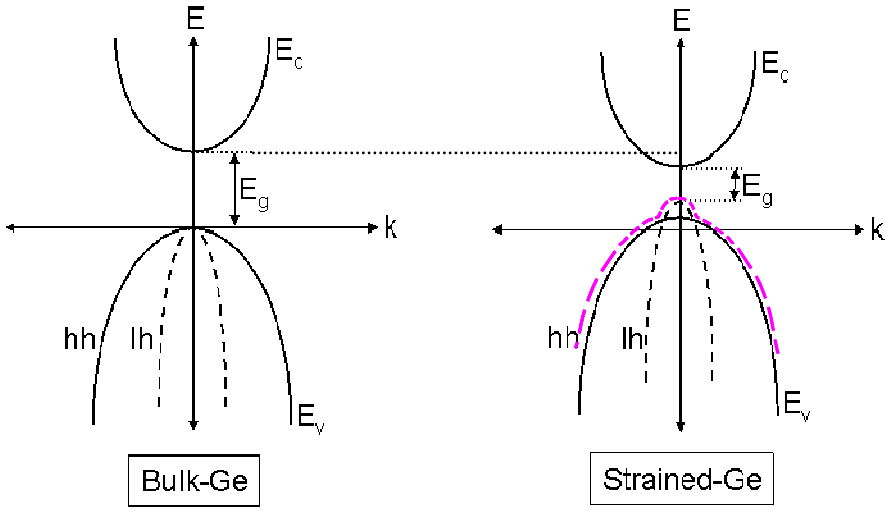

Fig. 4.23 Illustration of the change in the bands with biaxial tensile strain in the Ge film. The minimum of the conduction band at the zone canter moves down while the maximum of the valence band for heavy and light holes move up. The direct band energy is reduced due to tensile strain.

It is clear that, with the introduction of tensile strain in the Ge films, the direct bandgap is shrinking. This translates into an increase in the absorption strength of the strained layers compared to relaxed Ge, owing to an increase in the available density of states around the band edge. Furthermore, photons with lower energies than the band energy of relaxed Ge can be absorbed in these strained layers. Fig. 4.24 plots the calculated change in the direct gap energy of Ge (ΔE_g) as a function of biaxial strain [79].

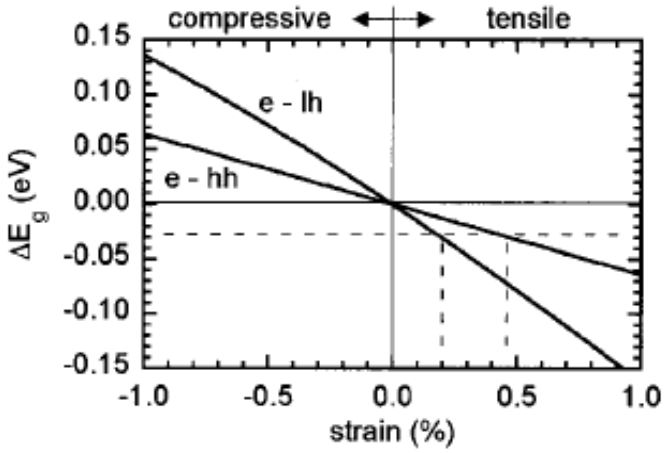

Fig. 4.24 The change in the direct gap energy of Ge calculated by [79].

Using the results of X-ray measurements and the approach in [79,82], the theoretical estimate of reduction in the direct gap energy in our MHAH-grown Ge films is calculated to be ~ 24 meV. This result has great implications on the absorption characteristics of MHAH layers which are elaborated in the following section.

4.4.4 Red shift of Ge absorption edge

In order to confirm theoretical predictions, wavelength spectral measurements are taken on MSMs on MHAH-grown Ge layers. The measured detector responsivity versus the wavelength is plotted in Fig. 4.25. The primary observation from this figure is that the absorption edge of Ge is at a longer wavelength than 1550 nm.

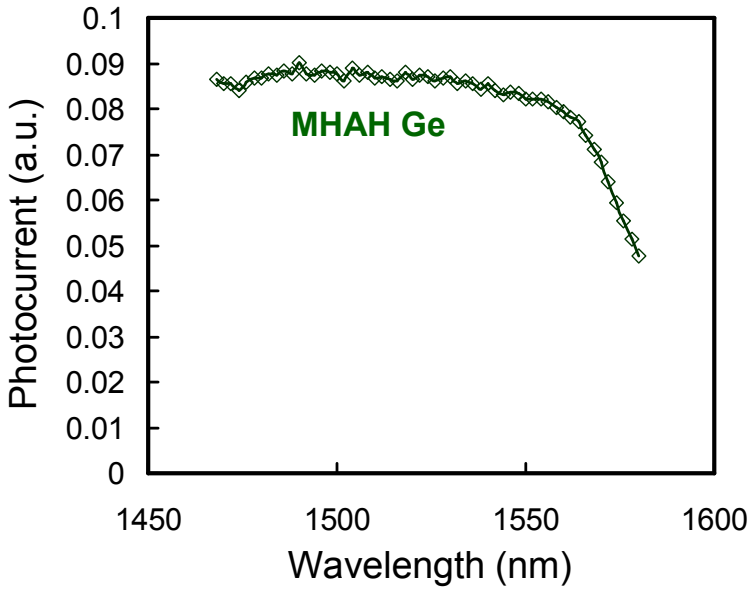

Fig. 4.25 Measured responsivity vs wavelength of Ti-Ge-Ti MSM with electrode width and spacing 5 μm.

The absorption curve of MHAH Ge layers can be extracted from the measured responsivity values and back-calculating the absorption coefficient using the relation in (4.1). The surface reflections are calculated for each photon wavelength, and a 300-nm-thick CVD SiO_2 anti-reflection layer. The internal quantum efficiency is assumed to be 90%, a reasonable estimate for the dislocation density present in the grown film [79]. The extracted absorption coefficient values are plotted in Fig. 4.26 versus photon energy. For

comparison, the absorption curve for relaxed Ge [71] is also shown in the same plot. It is clear that the absorption edge of strained-Ge has shifted towards longer wavelengths. We record almost a 47 nm red shift of the absorption edge corresponding to ~ 24 meV of bandgap shrinkage. This is in very good agreement with theoretical predictions in the previous section.

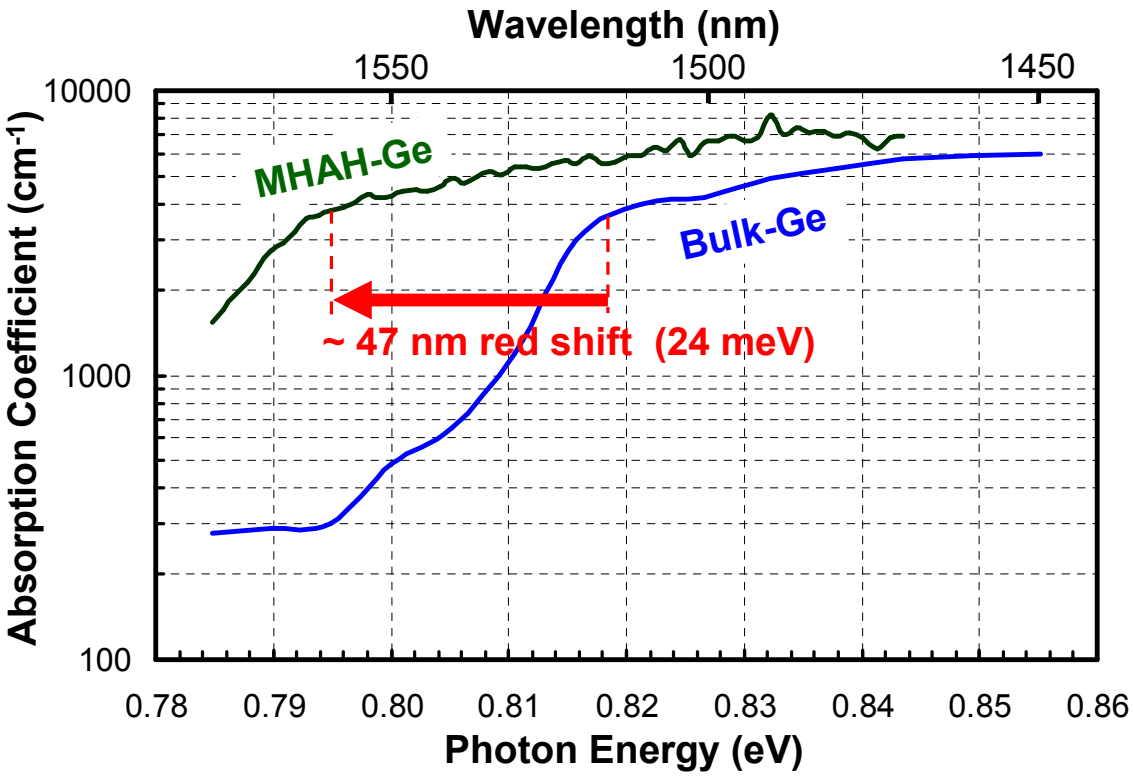

Fig. 4.26 Experimental absorption coefficient vs photon energy for MHAH-grown Ge layers. α_{Ge} is extracted from measured responsivity correcting for surface reflections and assuming 90% internal quantum efficiency. The absorption curve for relaxed Ge is also plotted for reference purposes. A 47 nm red shift of the absorption edge is recorded due to tensile strain.

In addition to the red shift of the absorption edge, the absorption strength around the band edge has dramatically increased. As explained earlier, this is due to the increased density of states available for valence-to-conduction band transitions. A very striking outcome of the residual tensile strain in the films is the greatly enhanced absorption strength of Ge at 1550 nm, from 490 cm^{-1} for relaxed layers up to ~ 4240 cm^{-1} for strained films. The roughly 4× higher experimental responsivity values at 1550 nm

compared to theoretical predictions originates from the enhancement in α_{Ge}. With increasing photon energy, the absorption coefficient for relaxed and strained Ge layers becomes comparable. This is attributed to a diminishing difference in the available density of states with increasing photon energy.

4.5 CONCLUSIONS

In summary, we have successfully demonstrated MSM photodetectors in Ge grown directly on Si by using a novel technique that allows growth of high quality thick heteroepitaxial-Ge layers on Si. Up to 68% quantum efficiency photodetectors with 0.85 A/W responsivities are achieved at 2 V reverse bias and λ = 1550 nm. Residual tensile strain in the grown layers is verified by X-ray diffraction analysis and separately confirmed by wavelength spectral measurements. The origin of the strain is explained due to thermal expansion mismatch between Si and Ge. We recorded a 47 nm red shift of the absorption edge by experiments corresponding to ~ 24 meV bandgap shrinkage, in good agreement with theoretical predictions. Exceptionally high efficiency of the photodiodes at this wavelength also reveals the high quality of the grown MHAH-Ge layers, making this technology a very promising candidate for monolithic integration of Ge and Si optoelectronics.

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CHAPTER 5: INTEGRATION OF OPTICAL POLYMER PILLAR WAVEGUIDES WITH MSM PHOTODETECTORS

This chapter describes the experimental study of optical polymer pillar waveguides integrated with photodetectors. We demonstrate the process integration and characterization of mechanically compliant optical polymer pillar chip I/O interconnections with group-IV metal-semiconductor-metal photodetectors (MSM-PDs). Some of the key performance metrics of the MSM-PDs before and after the process integration are reported. This is a collaborative effort between Stanford University and Georgia Institute of Technology (GATECH). Fabrication of photodetectors was carried out in Stanford University followed by deposition of polymer pillars in GATECH. The completed samples were characterized in Stanford University. Polymer waveguide processing was done by Muhannad S. Bakir under the supervision of James Meindl in GATECH. Detector fabrication, electrical and optical characterization measurements, and the relevant data analysis were primarily conducted by Ali K. Okyay under the supervision of Krishna C. Saraswat. Parts of this chapter have already been published in *IEEE Trans. Electron Dev.* Vol. 51, 7, 1084, (2004) [22].

5.1 INTRODUCTION

There is a critical need for highly integrated wafer-level optical and electrical input–output (I/O) interconnections at the die-to-module/board level [1-4]. The use of microphotonic interconnects technology for chip-to-chip communication offers potential advantages over electrical communication. I/O interconnections between die and board have traditionally been provided by metallic conductors. Electrical interconnects, however, have inherent limitations which include high noise, high drive power, impedance matching requirements, tradeoff between data rate and distance, insufficient densities/data rates, and expensive redesign. Optical interconnects, on the other hand, have the potential for low noise, low drive power, high density, high data rates, simplified design, and redesign. Due to the performance limitations of electrical interconnects, not

only have optical interconnects replaced electrical interconnects for long distance communication, but optical interconnects are also being developed for chip-to-chip communication [5-15]. To this end, it is essential to develop optical devices that are compatible with Si CMOS process technology. It is essential to develop optical chip-to-chip waveguide technologies as well as optical I/O interconnections to interconnect the chips together at the board level. Interconnecting and maintaining the alignment between the chip-level optical sources and detectors with board-level planar waveguides is challenging when the board and the chip have a different coefficient of thermal expansion (CTE).

A particularly promising optical I/O technology is the recently developed sea of polymer pillars (SoPPs) [16-22]. It potentially has all of the above favorable optical-interconnect characteristics with the additional desirable features of low cost, high tolerance to coefficient of thermal expansion (CTE) mismatches, accommodation of wafer-level testing, and low-temperature processing compatibility with semiconductor manufacturing. Polymer pillars have also been fabricated with surface metallic conductors on them allowing simultaneous dual-mode electrical and optical interconnects [17,18]. Furthermore, SoPPs have been fabricated at very high densities ($> 10^5$ cm^{-2}).

SoPP is a chip I/O interconnection technology that enables the batch fabrication of high density and mechanically compliant electrical and optical I/O interconnections at the wafer level [19-22]. SoPP is advantageous over conventional packaging because the I/O interconnections are designed to minimize the stresses induced at the die pads, and, thus, the low interlayer dielectric, during thermal cycling by undergoing strain. Simultaneously, they maintain optical alignment between the optical elements on the die and on the board. Through the use of a mirror or a grating couple, light can be coupled between a polymer pillar and a board-level polymer waveguide, as previously described [19,20]. The polymer pillars were shown to act as precision waveguides, thus verifying the cross-sectional uniformity, smoothness of surfaces, endface flatness, and optical quality of the material [21]. A representative polymer pillar of Avatrel 2000P (from Promerus LLC) [23] in an array of polymer pillars made by the procedure described below is shown in Fig. 5.1.

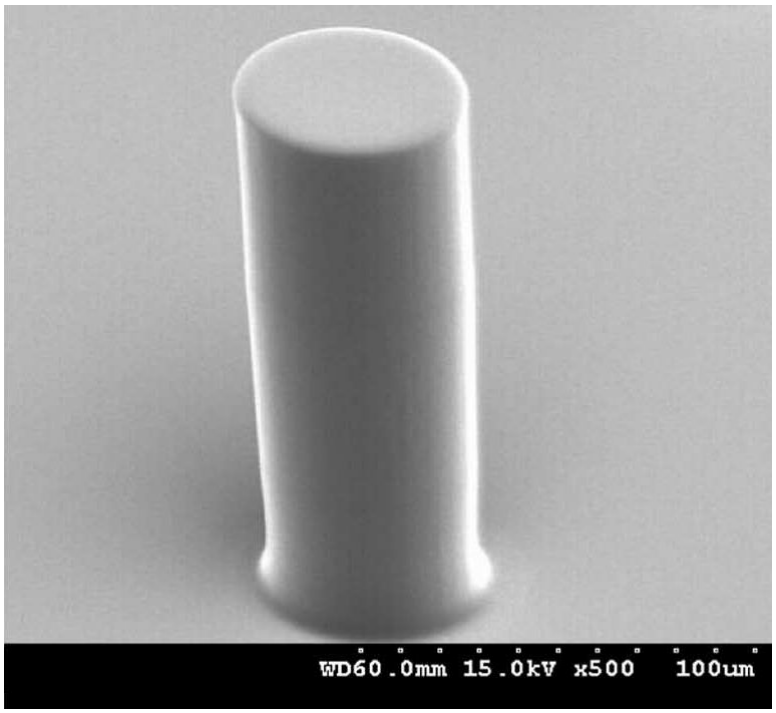

Fig. 5.1 SEM micrograph of a polymer pillar that is ~ 180 μm tall and 55 μm wide.

The MSM-PD technology described in this chapter was used to demonstrate very low dark current as introduced in Chapter 3. Coupled with their ease of fabrication, such MSM-PDs are promising for integration with Si CMOS technology. The integration of the detectors and the optical I/O interconnections at the wafer level represents the demonstration of an optoelectronic subsystem that is necessary for Si CMOS chip-to-chip optical communication.

In this chapter, we describe the process integration and testing of sea of polymer pillars (SoPP) with chip-level metal–semiconductor–metal photodetectors (MSM-PDs) at the wafer level. The details of the fabrication are presented in Section 5.2. Section 5.3 describes the layout design and demonstrates the integrated structures. Some of the key performance metrics of Si MSM-PDs with and without polymer pillars are reported in Section 5.4. The primary metrics in this analysis are the dark current and the photo-to-dark current ratio normalized to input optical power (NPDR) [24,25]. Finally, Section 5.5 is the conclusion.

5.2 EXPERIMENTAL PROCEDURE

For optical interconnect applications, the polymer pillars are fabricated directly on semiconductor chips. The polymer pillars may be integrated with passive devices such as mirrors or grating couplers [26] or with active devices such as photodetectors or lasers. In this work, we study the integration of polymer pillars with photodetectors.

A schematic of the complete fabrication process is shown in Fig. 5.2.

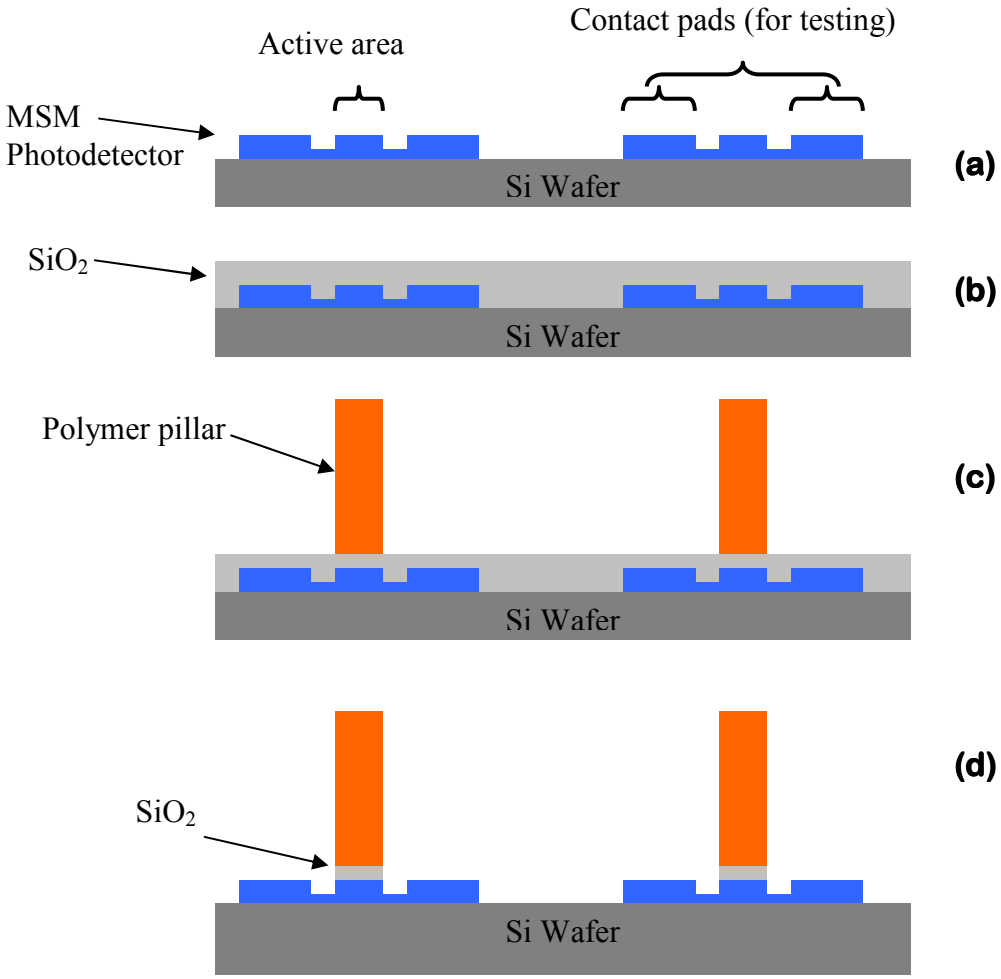

Fig. 5.2 A schematic of the process used to fabricate polymer pillars on MSM-PDs.

(a) Wafer with prefabricated MSM-PDs.
(b) SiO_2 is deposited on the wafer to enhance adhesion between the polymer film (subsequent step) and the substrate.
(c) Polymer pillars are fabricated above the active area of the MSM-PDs.
(d) Using the polymer pillars as an etch mask, the SiO_2 film was etched using BOE. This process step exposed the contact pads of the detectors to facilitate electrical testing.

Starting with the wafer containing the prefabricated MSM-PDs [Fig. 5.2(a)], which are fabricated through a liftoff process, less than a 1-μm–thick layer of SiO_2 was deposited, as shown in Fig. 5.2(b). The SiO_2 film was deposited using a PlasmaTherm plasma-enhanced chemical vapor deposition at a temperature of 150°C. This layer enhances the adhesion of the polymer to the surface. Next, a 50-μm-thick film of the polymer Avatrel 2000P was spin coated on the wafer. After a soft bake on a 100°C hotplate, the wafer was transferred to a mask aligner. The cross-sectional geometries of the polymer pillars on the mask were aligned with respect to the wafer such that the active area of the detectors was centered within the cross-sectional geometry of the polymer pillars. Following ultraviolet (UV) irradiation, hard bake, and spray developing, the polymer pillars were in place [Fig. 5.2(c)]. Next, the wafer was placed in a nitrogen-purged furnace (1 h at 200°C) for a cure. Finally, it was important to etch the SiO_2 on the MSM-PD contact pads to facilitate electrical testing. Using the polymer pillars as an etch mask, the substrate was immersed in buffered oxide etchant (BOE) to etch the SiO_2 film [Fig. 5.2(d)]. Finally, the wafer was ready for testing. A schematic illustration of the proposed device is shown in Fig. 5.3.

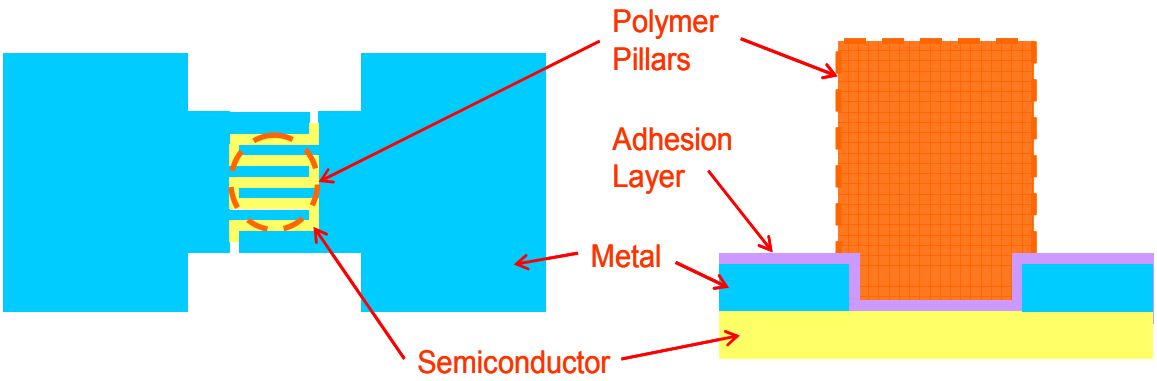

Fig. 5.3 Schematic illustration of the proposed integration scheme. The MSM photodetector is fabricated followed by the deposition of the polymer. Pillars of different size and geometry are defined using lithography.

5.3 GEOMETRICAL DESIGN AND IMAGES OF COMPLETED DEVICES

In order to investigate the effects of polymer pillar geometry and size (cross section) on the characteristics of the MSM-PDs, the layout was designed as shown in Fig. 5.4.

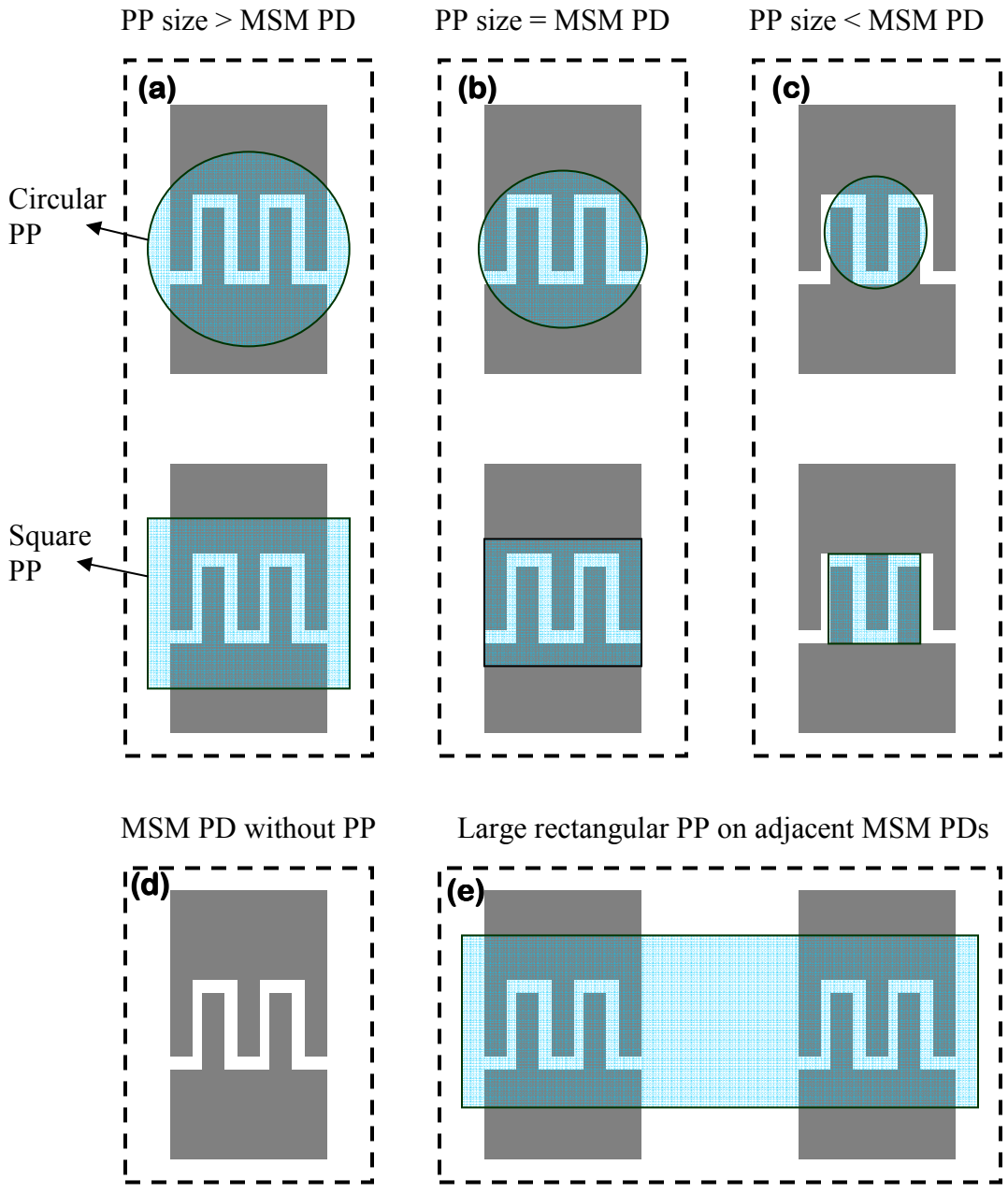

Fig. 5.4 Schematic illustrating how various size and shape polymer pillars (PP) were fabricated on identical MSM-PDs. Through measurements, such a layout design will ultimately provide insight into how the polymer pillars affect the characteristics of the MSM-PDs.

For each MSM-PD size, circular and square shaped polymer pillars with sizes larger than [Fig. 5.4(a)], equal to [Fig. 5.4(b)], and smaller than [Fig. 5.4(c)] the size of the active area of each PD were designed. Moreover, polymer pillars were omitted on some detectors to benchmark the measurements. This is schematically illustrated in Fig. 5.4(d). Finally, few polymer pillars were designed in the layout such that they covered more than one PD, as shown in Fig. 5.4(e).

Figs. 5.5 and 5.6 illustrate a set of circular polymer pillars with an aspect ratio greater than two fabricated above MSM-PDs. Fig. 5.7 is a scanning electron microscope (SEM) micrograph illustrating two circular polymer pillars with different diameters and aspect ratios fabricated on two similar MSM-PDs.

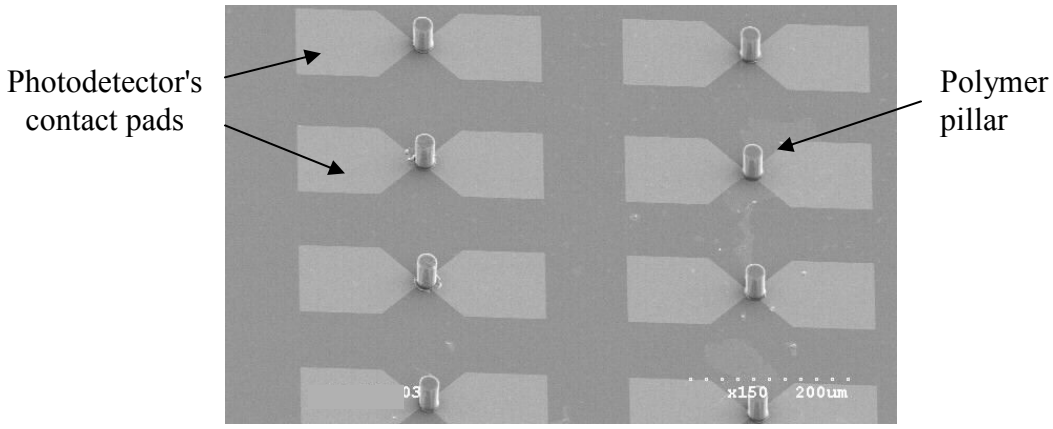

Fig. 5.5 SEM micrograph of a set of polymer pillars fabricated on Ti-Si-Ti MSM-PDs. The large pads on either side of the active area are used to facilitate electrical measurements.

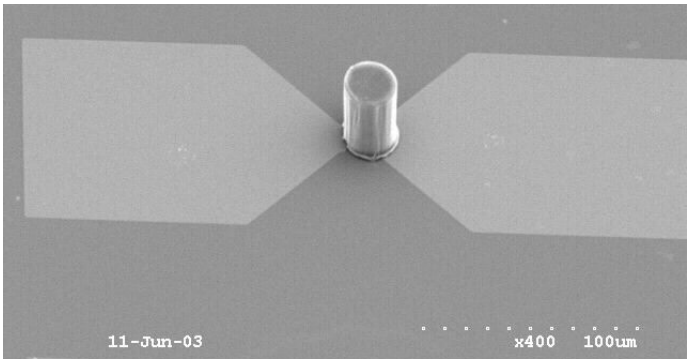

Fig. 5.6 A higher magnification SEM micrograph of previous figure illustrating a polymer pillar on an MSM-PD.

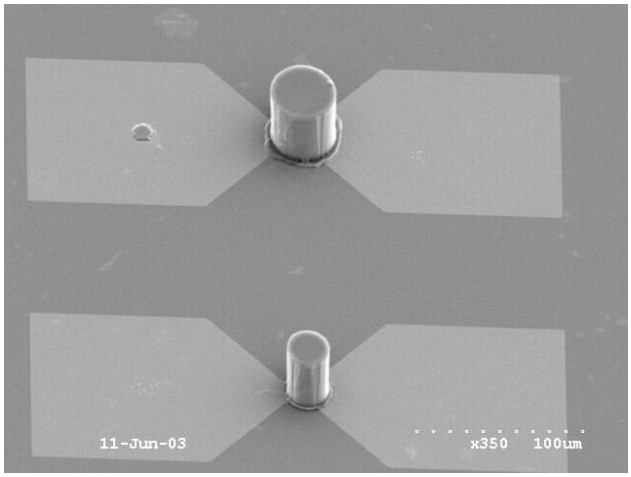

Fig. 5.7 SEM micrograph illustrating two polymer pillars with different aspect ratios fabricated on two similar MSM-PDs.

Fig. 5.8 illustrates a square-shaped polymer pillar above a MSM-PD with a large active area. An optical micrograph of a set of square-shaped polymer pillars that are larger than the active area of the MSM-PDs is shown in Fig. 5.9. Fig. 5.10 illustrates a pair of similar MSM-PDs with and without a circular polymer pillar. In this case, the size of the circular polymer pillar is equal to the size of the active area of the MSM-PD. Finally, Fig. 5.11 is a micrograph illustrating MSM-PDs with small active areas and the fabrication of equally small cross section circular polymer pillars above them.

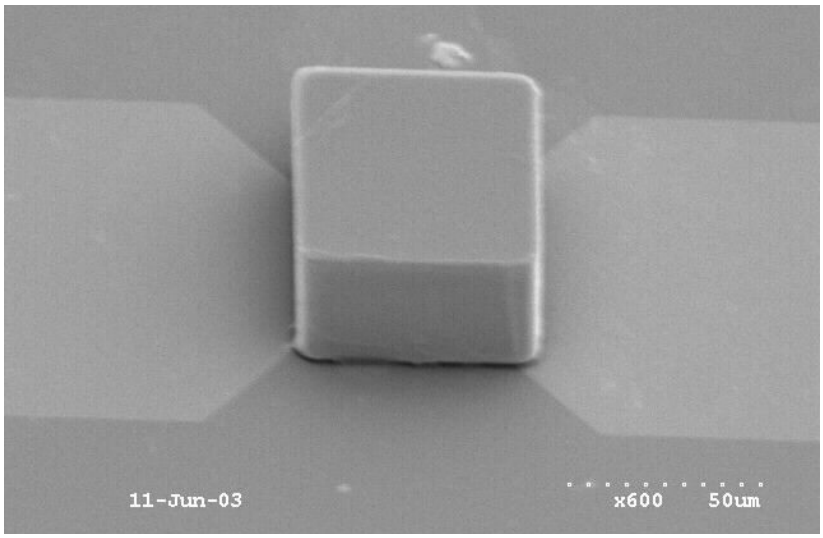

Fig. 5.8 SEM micrograph of a very low aspect ratio square-shaped polymer pillar on a large MSM-PD.

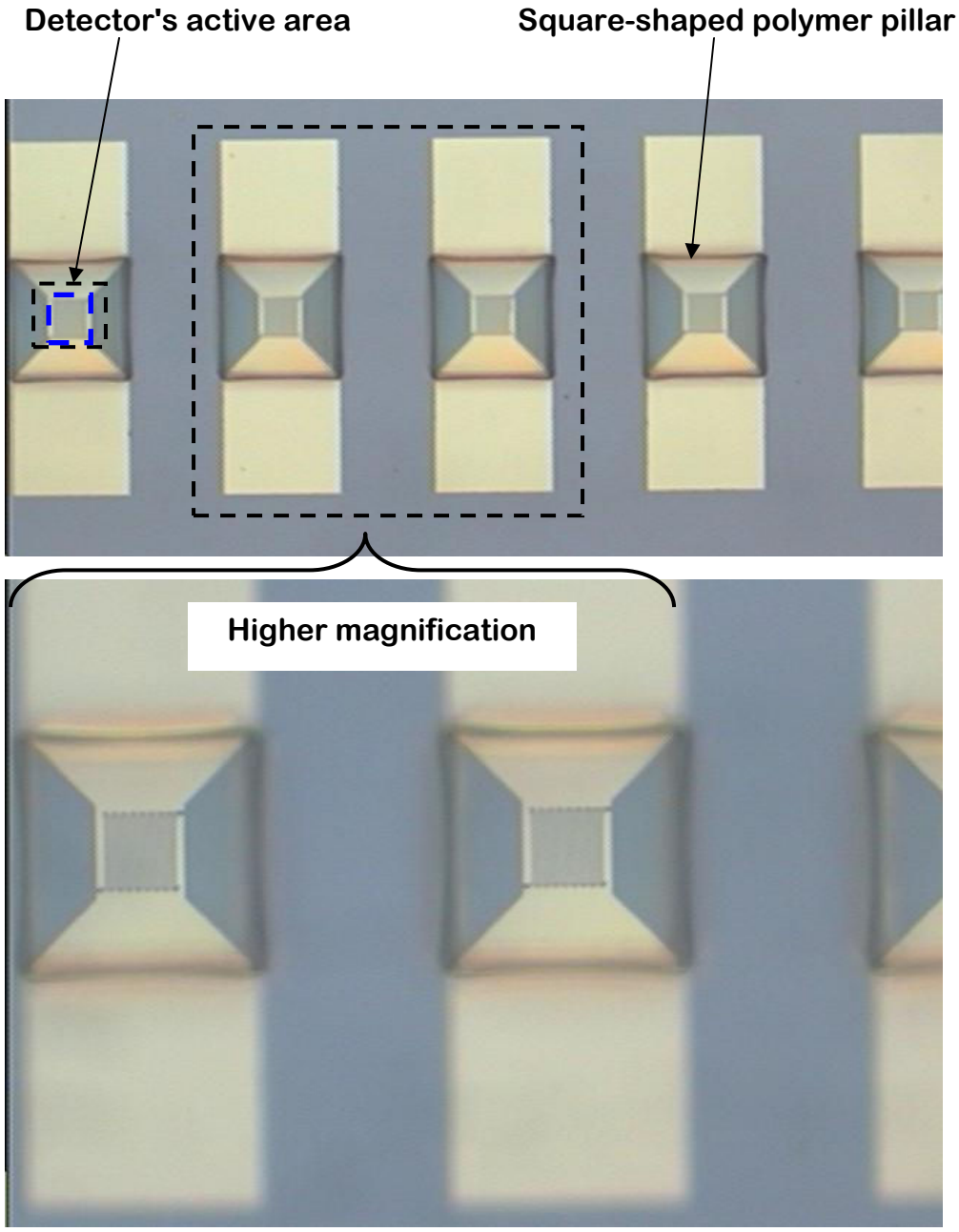

Fig. 5.9 Optical micrographs of a set of square-shaped polymer pillars fabricated above the active area of MSM-PDs. The size of the pillars is much larger than the size of the PDs.

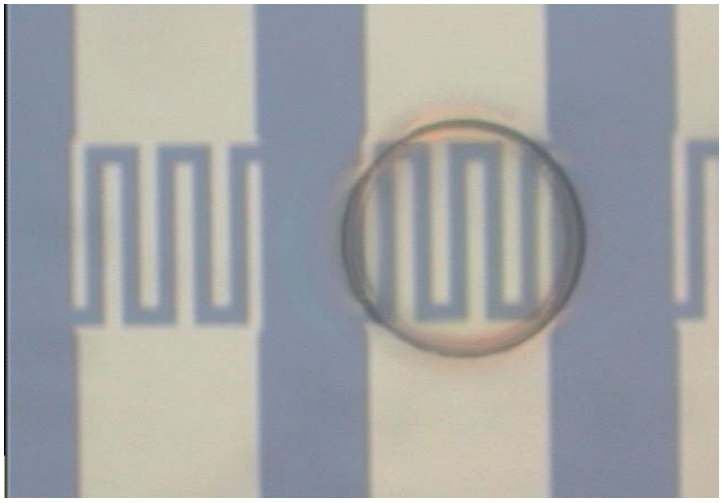

Fig. 5.10 Optical micrograph of a MSM-PD with and without a polymer pillar. The cross-sectional area of the pillar is equal to the size of the active area.

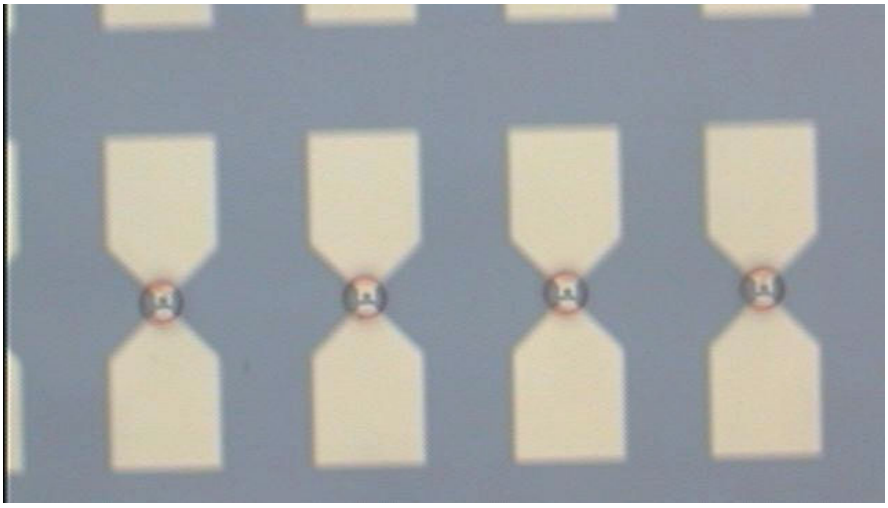

Fig. 5.11 Optical micrograph illustrating small diameter and high aspect ratio circular polymer pillars fabricated above relatively small MSM-PDs.

5.4 RESULTS AND DISCUSSION

The polymer pillar is illuminated by a collimated linearly polarized light of free space wavelength λ = 790 nm at normal incidence. Under ideal circumstances, the large-diameter circular cross-sectional pillar of refractive index n_p will act like a multi-mode circular waveguide. It would be similar to an optical fiber with the pillar acting as the core and air acting as the cladding. It differs from a single-mode optical fiber in that the

diameter is much larger and that the cladding is air (n = 1) rather than glass of slightly lower refractive index than the core.

As stated in Chapter 3, the two performance metrics of interest are the dark current and the NPDR. The measured dark current as a function of bias and finger width and spacing for a set of symmetric Si MSM-PDs with an active area of 1156 μm^2 is shown in Fig. 5.12. The four samples plotted in the figure are detectors prior to fabrication of the polymer pillars (labeled "No Process"), detectors that went through the polymer pillar processing but did not have polymer pillars (labeled "None"), detectors with circular polymer pillars that are smaller than the size of the active area (labeled "Small Circle"), and detectors with circular polymer pillars that are equal to the size of the active area (labeled "Circle").

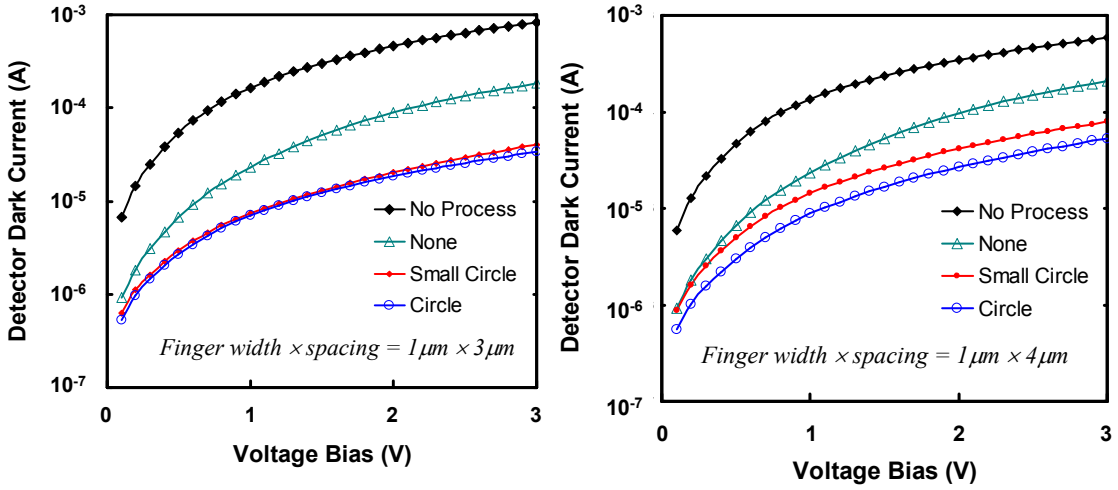

Fig. 5.12 Measured dark current as a function of bias for a set of Ti-Si-Ti MSM-PDs with and without polymer pillars. The plots are for detectors with a 1 µm x 3 µm and 1 µm x 4 µm finger width and spacing. The active area of the detectors is 1156 μm^2.

The data suggests that the MSM-PDs with polymer pillars consistently demonstrated one to two orders of magnitude reduction in the dark current. This is primarily due to the SiO_2 passivation, which was used as an adhesion layer between the pillars and the Si surface. Comparing the two types of MSM-PDs without the resultant polymer pillar and SiO_2 above the active area ("No Process" and "None"), the one that went through the polymer pillar processing exhibited lower leakage than the one without. It can possibly be

explained by the fact that the residual photoresist after liftoff, which had remained on the finished MSM structure, was removed by the polymer pillar processing and, thus, minimized any potential surface leakage. The reduction of dark current with the passivation oxide and the polymer pillar is consistently observed over different size detectors.

Fig. 5.13 illustrates the dark current measurements when performed on a set of symmetric Si MSM-PDs with an active area of 10,000 μm^2. The measurements are plotted for the following samples: detectors prior to the fabrication of the polymer pillars (labeled "No Process"), detectors that went through the polymer pillar processing but did not have polymer pillars (labeled "None"), detectors with square-shaped polymer pillars that are smaller than the size of the active area (labeled "Small Square"), detectors with square-shaped polymer pillars that are equal to the size of the active area (labeled "Square"), detectors with circular polymer pillars that are equal in size to the active area (labeled "Circle"), and detectors with wide rectangular polymer pillars that cover multiple detectors (labeled "Cont Rect").

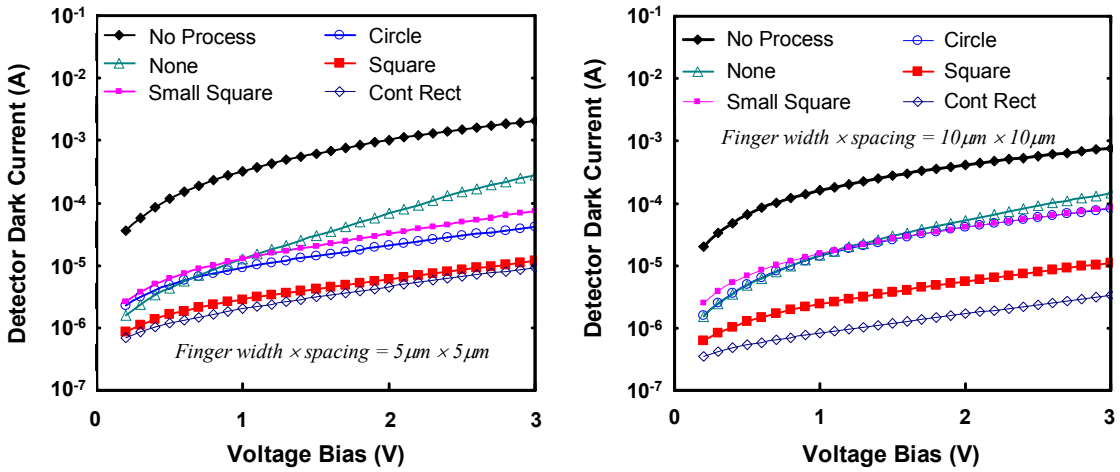

Fig. 5.13 Measured dark current as a function of bias for a set of Ti-Si-Ti MSM-PDs with and without polymer pillars. The plots are for detectors with a 5 μm x 5 μm and 10 μm x 10 μm finger width and spacing. The active area of the detectors is 10,000 μm^2.

The trend in the results is similar to that of the 1156 μm^2 large MSM-PDs. In addition, the continuous coverage of the wide rectangular polymer pillars yielded the

lowest dark current. Also, the same active area detectors with smaller finger width and spacing have higher I_{dark}. This is attributed to the fact that under the same voltage bias, the electric field is stronger for shorter electrode spacing. Moreover, as the finger width is reduced, the overlap between opposite polarity electrodes increases, yielding a higher perimeter leakage. The above figures also illustrate that the PDs with pillars smaller than the active area attained higher dark current than the PDs with pillars that are equal to or larger than the active area. This is an expected result because the better passivation coverage provides further I_{dark} reduction. Finally, a cross-over in I_{dark} at low voltage bias (~ 1 V) is consistently observed between the "None" PDs and PDs with active areas that were not completely covered with polymer pillars and SiO_2 ("Small Square" and "Circle"). This phenomenon could be accredited to the presence of the polymer pillar edge above and within the MSM active area where this edge-generated leakage is dominated at lower voltage bias.

All the integrated MSM-PDs with and without polymer pillars were illuminated with 790 nm, 1–1.5 mW laser excitation. The laser beam was collimated and focused on the sample with free space optics. Laser power level was separately recorded for each measurement to account for input optical power variations with time. The light beam was centered on the detectors visually via an infrared camera. Before taking each measurement, the coupling from the input optical beam to the integrated MSM-PD was spatially fine tuned to maximize the resultant photocurrent. Fig. 5.14 plots the NPDR as a function of bias voltage (linear scale) for the same samples listed in Fig. 5.12. Similarly, Fig. 5.15 plots the NPDR as a function of bias for the same samples listed in Fig. 5.13. As expected, the NPDR is higher for the detectors with larger electrode spacing and better surface passivation coverage because of their lower I_{dark} as discussed above. In other words, if the I_{dark} level of all these samples is equalized, the sample that shows the highest NPDR will deliver the highest responsivity and external quantum efficiency and exhibit the minimum noise-equivalent power [25].

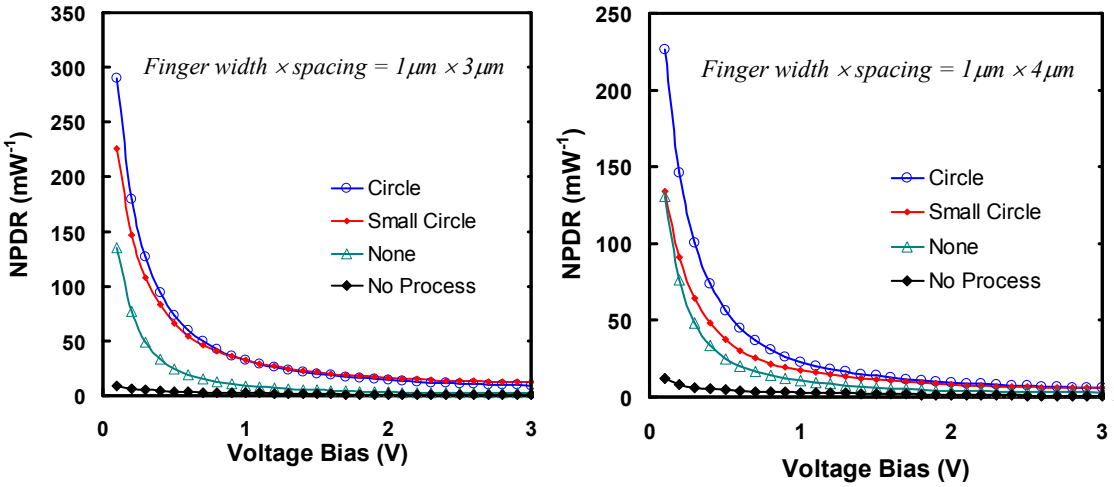

Fig. 5.14 Normalized photo-to-dark current ratio (NPDR) as a function of bias for a set of Ti-Si-Ti MSM-PDs (Fig. 5.12) with and without polymer pillars. The plots are for detectors with a 1 μm x 3 μm and 1 μm x 4 μm finger width and spacing. The active area of the detectors is 1156 μm^2. The measurements were made with a 790 nm and 1-1.5 mW laser.

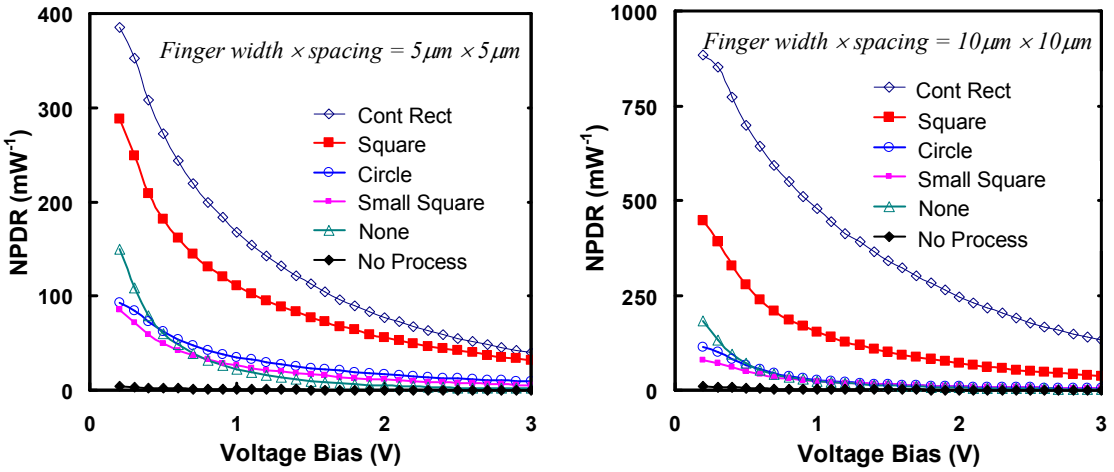

Fig. 5.15 Normalized photo-to-dark current ratio (NPDR) as a function of bias for a set of Ti-Si-Ti MSM-PDs (Fig. 5.13) with and without polymer pillars. The plots are for detectors with a 5 μm x 5 μm and 10 μm x 10 μm finger width and spacing. The active area of the detectors is 10,000 μm^2. The measurements were made with a 790 nm and 1-1.5 mW laser.

The dark current of the stand-alone MSM-PDs without going through the polymer pillar process does not degrade significantly when these PDs are thermally cured. To emulate the effect due to different processing thermal budgets on the I_{dark} of MSM-PDs, a set of MSM-PDs that have an active area of 10,000 μm^2 and finger width and spacing of

5×5 μm was cured with either 1 or 2 h at 200°C as illustrated in Fig. 5.16. For an additional 1 h cure at 200°C compared to our actual experimental condition, the I_{dark} of MSM-PDs increased only slightly due to enhanced metal–silicon interaction or intermixing.

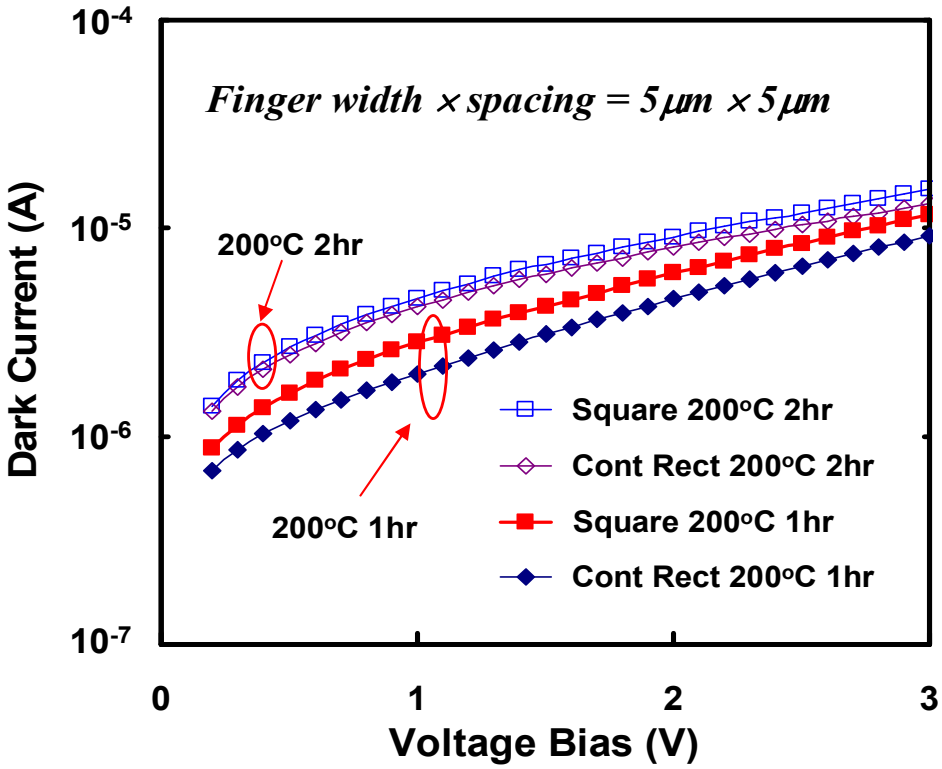

Fig. 5.16 Dark current as a function of bias voltage for a set of MSM-PD that have an active area of 10,000 μm^2 and finger width and spacing of 5 μm x 5 μm.

Finally, we investigated the effects of MSM-PD sizing using the I_{dark} and NPDR measurements. For the fixed PD active area of 10,000 μm^2, the MSM finger width and spacing was varied from 5 to 10 μm apiece. As obvious from the trends in Fig. 5.17 and consistent with the aforementioned principles, the I_{dark} reduces with increasing finger spacing. The tendency is also directly reflected in the NPDR behavior, which also suggests that these resultant MSM-PDs are not adversely affected by the polymer pillar processing. All measurements reported in this section were the average value of several measurements.

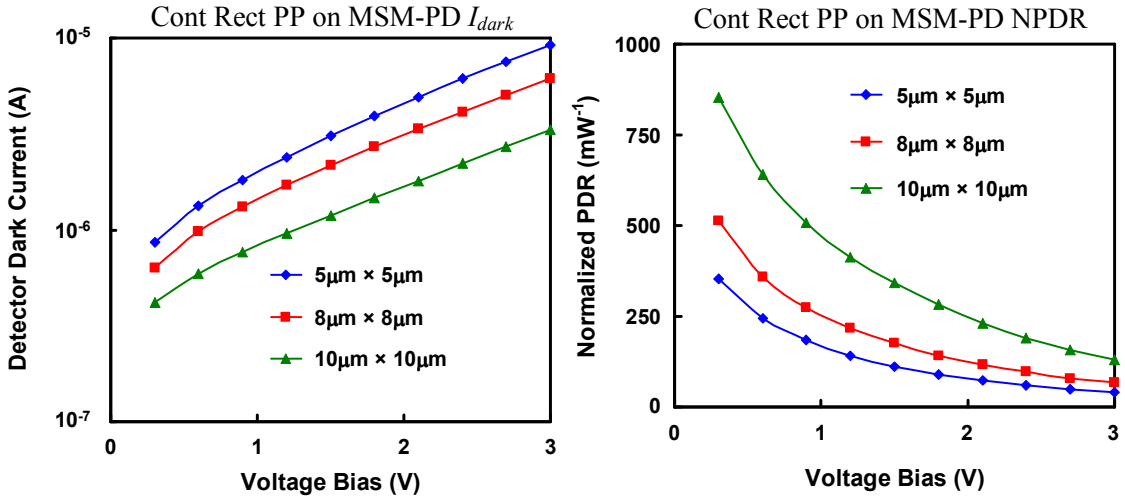

Fig. 5.17 Dark current and NPDR as a function of bias voltage for a MSM-PD of the configuration shown in Fig. 5.4(e) that have an active area of 10,000 μm^2.

5.5 CONCLUSIONS

In a typical optical interconnect, the signal will be routed to the receiver via the waveguide which will subsequently couple it into the photodetector. We have process-integrated surface-normal mechanically flexible polymer pillar optical waveguides with Group IV (Si) MSM-PDs. This technology is promising for efficient integration of waveguides and photodetectors on a chip. Polymer pillars with various cross-sectional geometry, size, and aspect ratio were fabricated on detectors with various active area and metal finger spacing. The different polymer pillar and PD configurations enabled us to quantify the impact of pillars on the PDs. Results indicate that the characteristics of the PDs do not degrade as a result of the pillar fabrication. Moreover, measurements indicate that the thermal cure process that is required for the pillar fabrication does not degrade the performance of the PDs. Such a scheme of a detector coupled with a waveguide can be used to distribute light to photodetectors built on a chip for optical interconnections.

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CHAPTER 6: A NOVEL CMOS COMPATIBLE SEMICONDUCTOR OPTOELECTRONIC SWITCHING DEVICE: BRINGING LIGHT TO LATCH

All truth passes through three stages. First, it is ridiculed. Second, it is violently opposed. Third, it is accepted as being self-evident.
Arthur Schopenhauer

In this chapter we introduce a novel semiconductor optoelectronic switch that is a fusion of an optical detector and a MOSFET (metal-oxide-semiconductor field-effect-transistor). The device operation principle is investigated and the performance is explored by simulations. In addition, we report experimental proof-of-principle demonstration of the OE switch. Detailed device fabrication process and results of optical and electrical measurements are presented. Experimental device fabrication, electrical and optical characterization measurements, and the relevant data analysis together with the theoretical study of the physics of the proposed device along with the optoelectronic simulations were primarily carried out by Ali K. Okyay under the supervision of Krishna C. Saraswat. Parts of this chapter have already been published in *Optics Lett.* Vol. 32, No. 14 (2007) [83].

6.1 INTRODUCTION

The universal goal of a device and circuit design for digital operation is to obtain the highest possible switching speed for the lowest overall static and dynamic power dissipation in a cost-effective way. As the speed of electronic circuits approaches 10 Gbps and beyond, the volume of chip-to-chip and on-chip communication skyrockets. Traditional copper wires are efficient at short distances, but they suffer excessive power dissipation and delay in global lines, and cannot cope with the ever growing bandwidth demand [1-3]. Moreover, with the microprocessors evolving towards multi-core architectures, the requirements for increased bandwidth density further strain the electrical interconnects [4,5]. The idea of bringing high speed optical signals directly to CMOS (complementary metal-oxide-semiconductor) chip offers opportunities for using light to aid electrical functions in novel ways. This seems increasingly imminent as

optical interconnects are promising to alleviate problems faced by copper wires [6-10]. Compound semiconductors have been the forerunner in optoelectronic applications, but their integration with Si is expensive and hindered by parasitics [11,12]. Recently, it has been demonstrated that incorporation of Ge into Si is a promising approach that can enable the design of low-cost modulators [13-18] and optical detectors [19-32] on Si with potentially higher efficiencies than their hybrid counterparts. This technology is fast approaching to replace the conventional building blocks of the transmitter end in an optical link operating at telecommunication standard wavelengths.

Traditional optical receivers are composed of a photodetector that feeds a TIA (trans-impedance amplifier) stage which converts the current from the photodetector to a voltage signal, as illustrated in Fig. 6.1. This voltage signal is then amplified by a cascade of size-matched amplification and buffering stages and finally it is used to drive the next-stage-logic, where the signal was initially intended for.

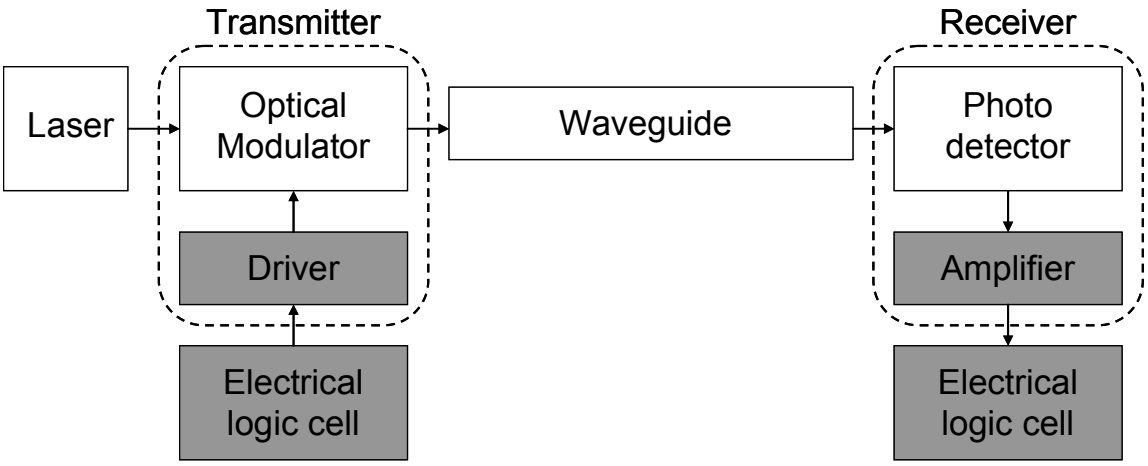


Fig. 6.1 A block diagram illustration of an optical link in which the light from a continuous wave laser is modulated and transmitted. The waveguide carries the optical signal to the receiver which is converted to electrical current by the photodetector. The trans-impedance amplifier converts current to a voltage signal and the subsequent buffer stages amplify the voltage to the logic level.

Inevitably, this scheme generates a large overhead in power consumption and chip real estate, besides raising a serious scalability question for large scale integration.

Moreover, increasingly stringent power requirements on a chip limit the total number of receivers, hence the number of links. The influence of detector capacitance on system level performance of optical interconnects was recently analyzed by Cho et al. for chip-to-chip links [33]. Fig. 6.2 plots the critical length above which optical links become more power efficient compared to their electrical counterparts. The critical length reduces as the detector capacitance is lowered. Haurylau and co-workers have reported similar findings for on-chip interconnects [9]. It is imperative to lower the detector capacitance in facilitating the insertion of optical interconnects into VLSI domain.

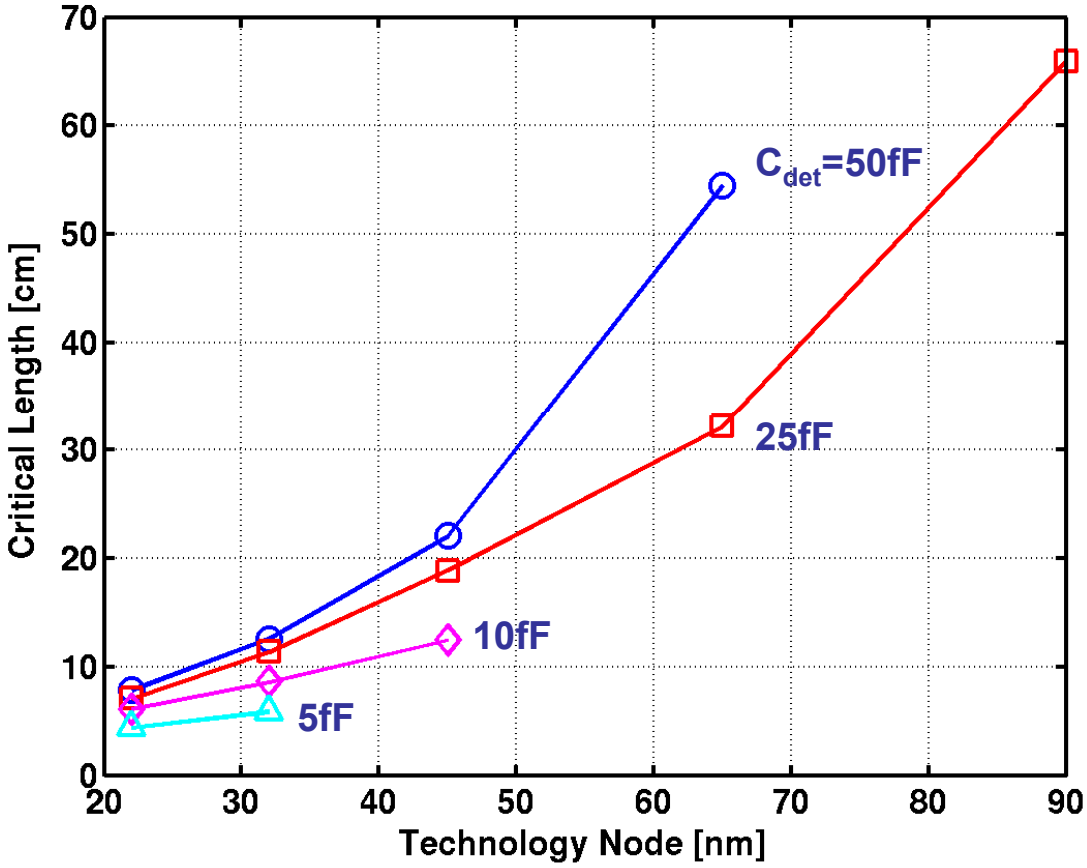


Fig. 6.2 Family of curves corresponding to different detector capacitances plotting critical length as a function of technology scaling. Technology scaling incorporates both transistor performance improvement and higher bit rate demand. After Cho *et al*. [33].

Some research has focused on eliminating the bulky receiver circuitry and replacing it with back-to-back photodetectors [34-36]. Fig. 6.3 depicts such a configuration with cascaded photodiodes directly driving a next stage logic. Successful operation was demonstrated with such totem-pole configuration with < 6 psec rms jitter. This scheme, on the other hand, requires two consecutive optical signals, precisely separated in time, arrive at the detectors, all over the chip. Furthermore, very low capacitance detectors are essential from the required optical energy perspective.

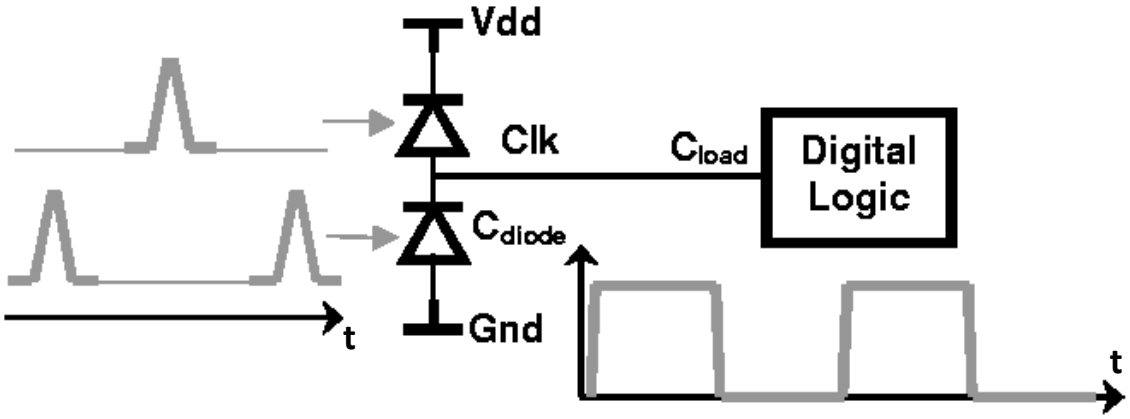


Fig. 6.3 Schematic view of the receiver-less direct clock injection. Two photodiodes are connected on top of each other in a *totem-pole* scheme. Light pulses delayed in time are incident on the diodes. At every cycle, the upper diode charges the load capacitor followed by discharging by the lower one. After Debaes *et al*. [34].

Optical interconnects can have great impact on inter-chip links and on-chip signaling and clocking applications. We introduce a novel optoelectronic switch for such applications. The building block for the switch is an optoelectronic MOSFET. The device scales with the technology and can be made extremely compact with very low capacitance and small footprint area. In the context of optical integration, such a detector based on a MOSFET structure would represent a highly practical and uniquely scalable optoelectronic component. By such a design, light can be introduced at the latch level eliminating the ever so power-hungry electrical interconnection hierarchy of clock distribution networks as well as the conventional high capacitance optical detectors for optical interconnects. In this chapter, we explore the operation of the proposed device by simulations and experiments.

6.1.1 Literature review of phototransistors

The idea of photo-transistor was introduced soon after the demonstration of the first transistor in 1947. The term "phototransistor" was first coined [37] for a point contact Ge photoconductive device that bore a little resemblance to the bipolar structures to which the term is usually applied today. Shockley and co-workers first proposed the use of the bipolar configuration (*n-p-n* or *p-n-p*) as a phototransistor [38]. They correctly described the operation of a transistor with an optically generated base current. The first demonstration of this type of photodetector was reported two years later with an *n-p-n* Ge phototransistor that exhibited optical gain in excess of 100 [39]. A common phototransistor differs from a standard bipolar transistor by omitting the base contact, and by having much larger base and collector areas compared to the emitter as illustrated in Fig. 6.4. The work of Ryvkin and later Tsyrlin provided a detailed description of the dc gain characteristics and the frequency response of phototransistors [40,41]. Using integrated circuit technology, arrays of Si phototransistors were fabricated in the late 1960s for solid-state imaging applications. The development of charge-coupled devices pushed this technology to the background.

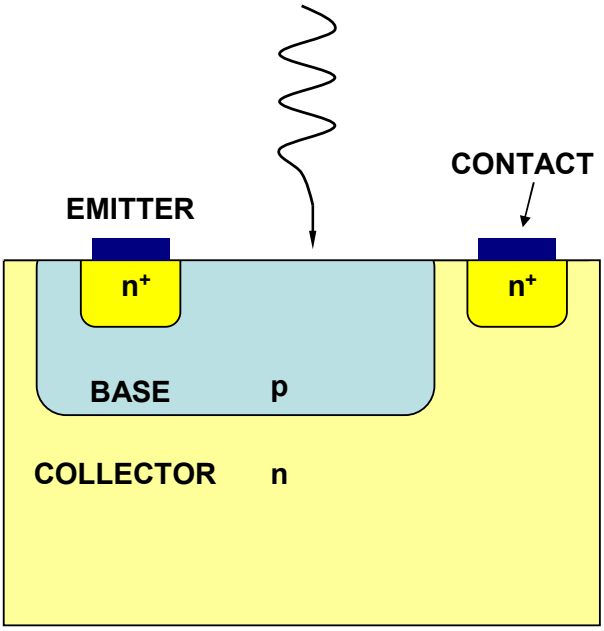


Fig. 6.4 Schematic illustration of a common phototransistor which is a modified version of a classical bipolar transistor.

The advent of heteroepitaxy of crystal systems with lattice-matched structures brought about a revived interest in phototransistors in the 1980s with the prospect of application in optical fiber telecommunication systems [42-49]. A key factor in obtaining improved performance from phototransistors has been the use of heterostructures with a wide bandgap emitter [50]. The availability of high-quality heterojunctions has made the wide-bandgap-emitter configuration a practical concept as illustrated in Fig. 6.5. The idea of using an emitter having a wider bandgap than that of the base to improve the emitter injection efficiency (hence gain) of a bipolar transistor was analyzed by Kroemer [51,52] and first applied by Alferov and co-workers [53]. Even better characteristics can be achieved by taking advantage of the avalanche multiplication in the base-collector junction of the phototransistor to enhance current amplification [54,55].

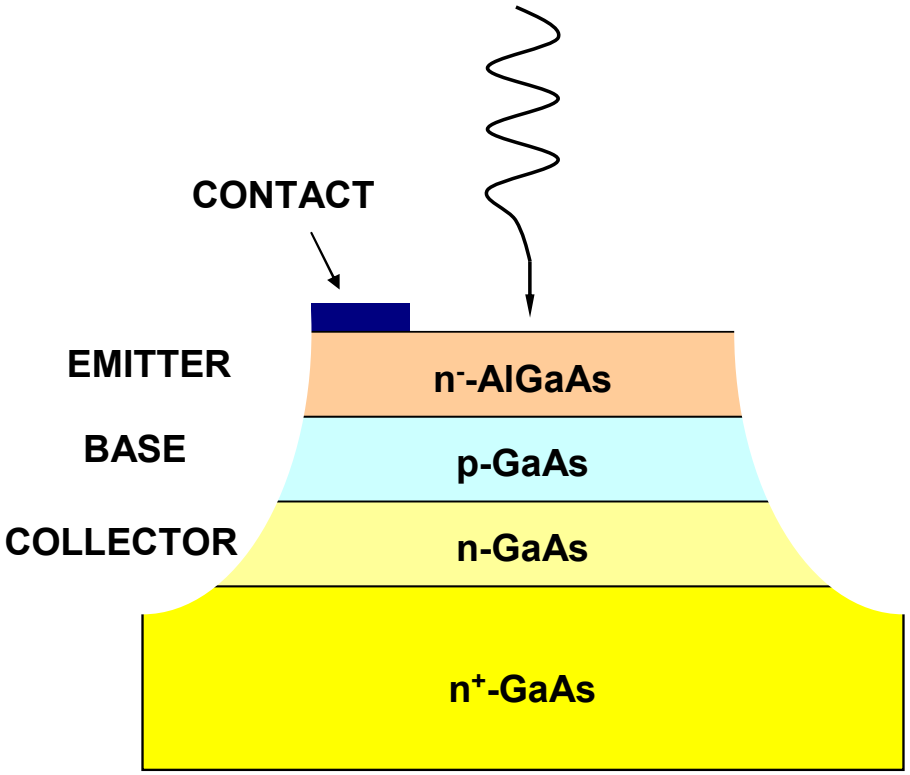


Fig. 6.5 A typical heterojunction phototransistor with a wide bandgap emitter configuration. The emitter does not absorb the incident light due to high bandgap, hence increasing the efficiency in addition to the improved emitter injection efficiency.

A qualitative energy band diagram illustrating the response of a phototransistor to light is shown in Fig. 6.6. Photo-generated holes flow to the energy maximum and they are trapped in the base. This accumulation of positive charge lowers the base energy (raises the potential), and allows a large flow of electrons from the emitter to the collector. The result of a much larger electron current caused by a small hole current is the consequence of emitter injection efficiency γ. The speed of a phototransistor is limited by the charging times of the emitter and collector. In practical homojunction devices, the response time is very long. The frequency of heterojunction phototransistors can go beyond 2 GHz [55-57]. Despite their improved speed and higher gain, heterojunction phototransistors are too costly to be commercially feasible.

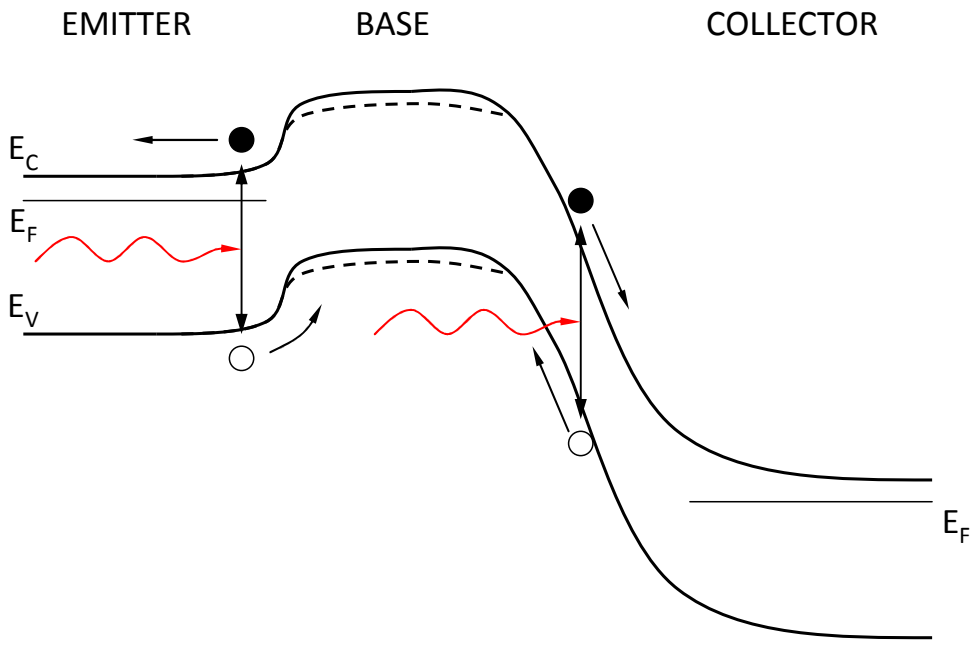


Fig. 6.6 Energy band diagram of a phototransistor. The dashed lines indicate the change of the base potential caused by the accumulation of photo-generated holes.

Until the late 1980s, bipolar structures were the subject of the most of the research on phototransistors, after which a great deal of attention was directed towards the photosensitivity of field-effect transistors (FET). The photosensitive FET covers a class of FETs that combine high-impedance amplifiers with built-in photodetectors [58-69]. The advantages of this type of photodetector are very fast response and high optical gain.

The photo-FETs studied include JFET (junction FET), MESFET (metal-semiconductor FET) and MOSFET. Fig. 6.7 illustrates a typical photosensitive MESFET where light is absorbed in the channel region modifying its characteristics. Baack and co-workers first demonstrated the use of an FET as a high-speed photodetector [59]. Using a GaAs MESFET to detect an optical pulse, they observed a pulse width of 73 psec, which compared favorably with a pulse width of 178 psec obtained with a high-speed avalanche photodetector (APD).

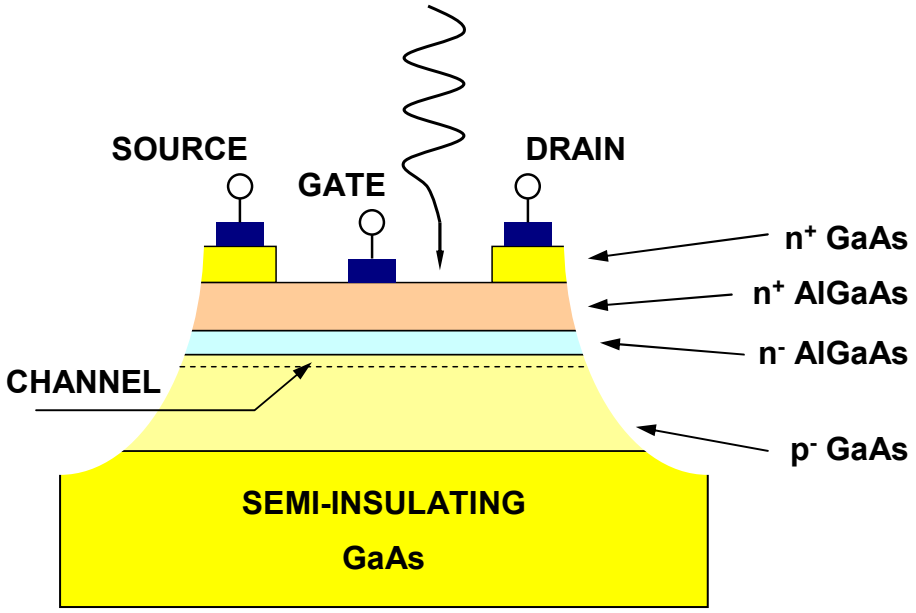


Fig. 6.7 Illustration of a typical photosensitive heterojunction field-effect transistor. The MESFET is configured as a modulation-doped transistor.

Although there has been little doubt regarding potential operation of FETs as photodetectors at gigabit data rates, the origin of the gain has been the subject of some debate. The simplest model is based on photoconductivity [57]. Experimental evidence indicates that the phenomena of photosensitivity and gain in FETs is a complex combination of several mechanisms, including photoconductivity with gain [60-62]; changes in the source-drain current resulting from photovoltaic response of the gate junction [63,64] or the substrate-channel junction [65]; and electric-field-aided diffusion of photo-generated carriers from the substrate to the channel [66].

Past research on FET-based optical detection has focused primarily on compound semiconductor technologies which lack the vital cost-effective integration capacity with advanced Si VLSI technology. We have recently introduced a novel FET photodetector based on Si MOS scheme which provides optical gain at high bit rates. The proposed device is a Si MOSFET with a photosensitive Ge gate. Such a structure uniquely enjoys the potential of monolithic integration with the standard CMOS while promising to tackle scaling challenges of high-end computation systems.

6.2 DEVICE DESCRIPTION AND OPERATION

6.2.1 Device structure

The schematic structure of the proposed device is shown in Fig. 6.8. It is an integrated structure analogous to a Si MOS transistor with an absorption region on the gate of the transistor.

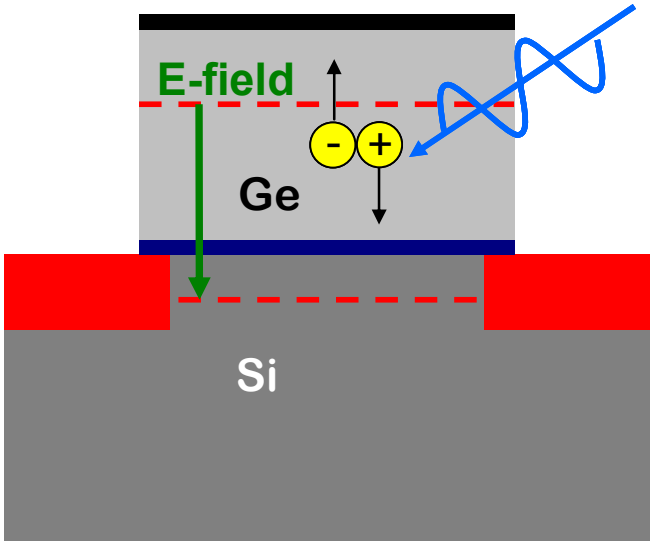


Fig. 6.8 Schematic of the optoelectronic MOSFET – cross section. Source/drain and channel regions are formed in Si. Ge gate is deposited and it is isolated from the channel by thermally grown SiO2. Light can be coupled by normal incidence or by a through waveguide scheme. Light in the 1.3-1.55μm window is absorbed in Ge gate only. Due to large bandgap energy of Si, no absorption takes place in the channel; hence the surrounding Si circuit is noise immune.

The body and the channel of the OE MOSFET are formed in Si while the gate is made of Ge. The gate absorbs near infrared light at longer wavelengths compared to Si channel. The absorbing gate is separated from the channel by the gate insulator. The upper photodetector part absorbs the optical input power and the lower FET part modulates the electric current through the potential applied to the FET. The source and drain regions can be formed by conventional implantation of the Si body. In short, the device is a Si MOSFET with a Ge gate. Light can be coupled into the device from the top surface as well as through a waveguide scheme in a fully integrated system.

6.2.2 Principle of operation

The signal is generated remotely and is transmitted in the form of optical energy in the 1330-1550 nm window where Ge is a strong absorber. When the light enters the absorption region, part of the input light is absorbed and electron-hole pairs are generated. Incoming photons are absorbed only by the Ge gate because Si is transparent at these wavelengths [70]. Optically generated carriers then move within the gate in an electric field caused by band bending and the applied gate bias, as shown in Fig. 6.9(a). For the case illustrated in this figure, the optically generated electrons drift away from the SiO_2 interface while the holes drift towards this interface. This constitutes a net current in the gate terminal (I_{GATE}) resulting in accumulation of electrons and holes at either side of the gate insulator. Consequently, the electric field from the applied gate voltage is screened by the field due to the optically generated charge. The band bending and the quasi-Fermi levels for electrons (Q_{fn}) and holes (Q_{fp}) are modified owing to the new charge distribution, as indicated with the dashed lines in Fig. 6.9(b). Hence the original electric field in the gate is reduced while the potential across the gate insulator and the channel rises. The electric field distribution across the gate stack with and without illumination are plotted in Fig. 6.10, demonstrating the increased potential in the channel region. This performs as the gate voltage control, so the drain-to-source current will be modulated as an amplified version of the gate current due to increased carrier density in the channel.

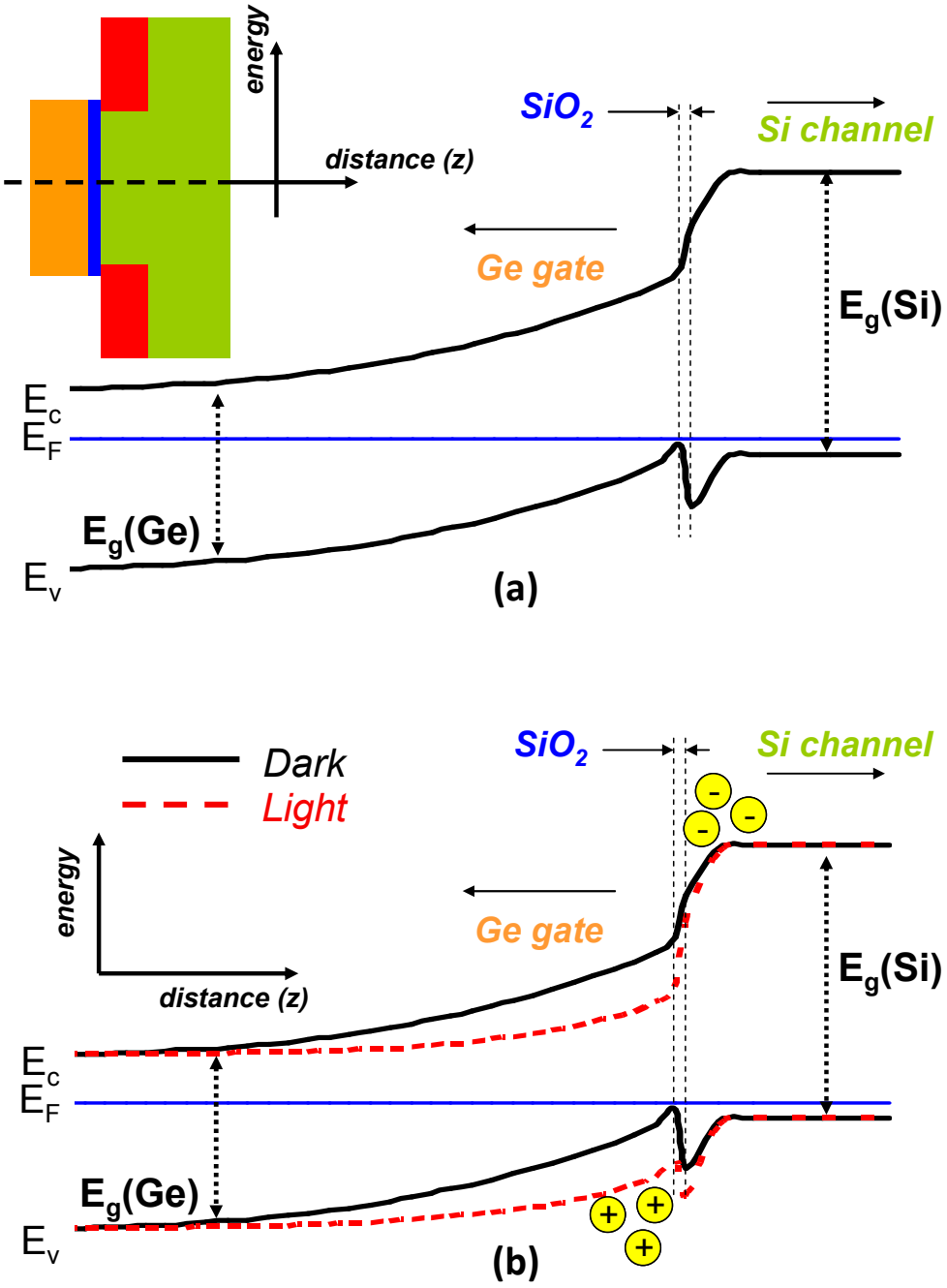


Fig. 6.9 (a) Energy band diagram of Ge-SiO_2-Si stack under equilibrium. (b) Band bending under steady state illumination is shown with the dotted lines. Optically generated carriers accumulate at either side of the gate dielectric. This photo-excited charge modifies the electric field across the stack. In the case illustrated here, holes accumulate at the Ge-SiO_2 interface, while the electrons are swept towards SiO_2-Si interface inducing a channel.

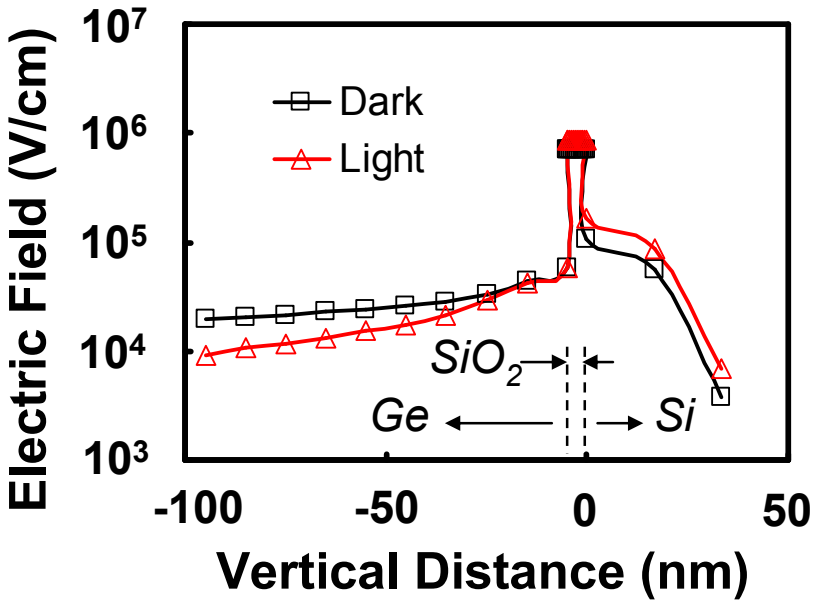


Fig. 6.10 Vertical electric field across the Ge-SiO_2-Si stack with and without light. Voltage distribution across the structure is modified by redistribution of optically generated carriers.

Under steady state, the sum of recombination and diffusion of excess carriers is equal to the photogeneration which replenishes the excess carriers. The recombination rate, however, is significantly higher than its equilibrium value due to the presence of excess carriers. Fig. 6.11 plots the simulated carrier recombination rate versus physical distance in the MOS structure, comparing steady state illumination with the thermal equilibrium. The recombination rate under steady state illumination is much higher, specifically at the gate insulator interface, where most of the excess carriers are accumulated. When light is turned off, the gate oxide capacitance discharges through both increased recombination in the gate depletion region and diffusion due to the gradient in the carrier concentration. The speed of the turn-off mechanism can be controlled by carrier lifetimes and thickness of the gate region as well as the applied gate bias. Furthermore, it is possible to tailor the built-in band bending using a graded SiGe gate region. Owing to the unique band offsets between Si and Ge, the valence band can be engineered for more efficient removal of excess carriers.

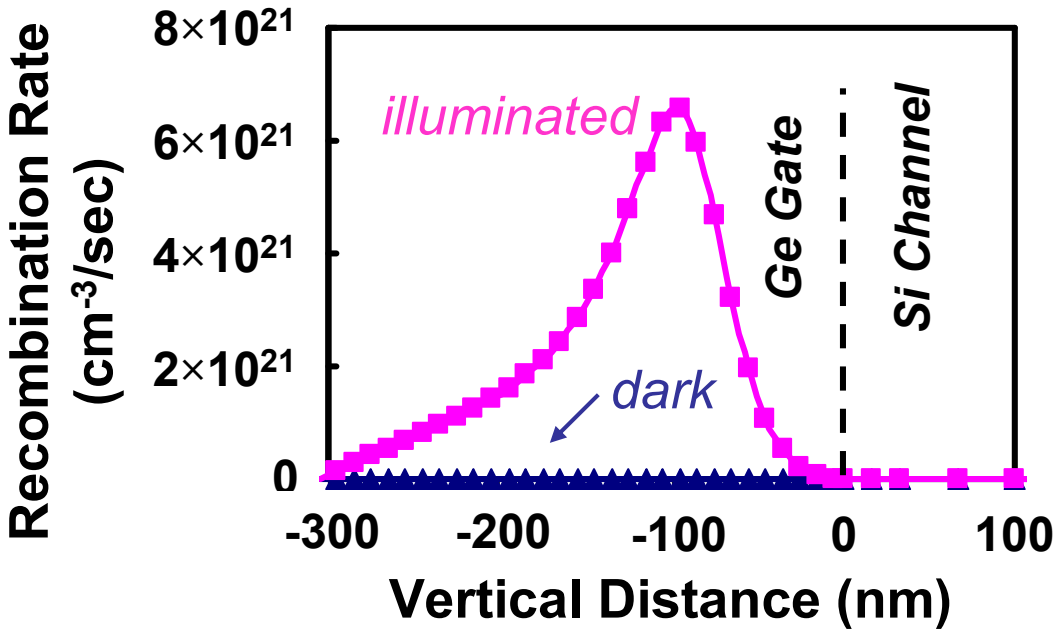


Fig. 6.11 Net recombination rate in the Ge-gate region under illumination. Recombination is negligible when there is no light. When the light turns off, excess carriers in the gate recombine which is one of the mechanisms responsible for device turn-off.

In this device, the absorbing Ge gate and the Si FET region are electrically isolated by a high quality insulator such as thermally grown SiO_2. The current of the FET is modulated, not by the optically generated carriers, but by the electric field due to these carriers. Furthermore, the bandgap energy of the Ge absorption region is lower than that of Si FET regions. Hence, there is no significant generation of carriers in the Si channel when light enters the body of the transistor. In a classical optical FET however, the channel is illuminated directly and photo-excited carriers are generated in the channel. The diffusion of these carriers limits the speed of such a device. Moreover, other Si channels in the vicinity would be prone to suffer from light-induced noise generation. On the contrary, in this device, high speed optical to electrical conversion is possible while the surrounding Si circuitry is noise free, providing noise immunity from signaling and clocking.

6.2.3 The MOS capacitor

An alternative way to model the operation of the device is to consider the capacitive voltage division in the Ge-SiO_2-Si gate stack which governs the operation of the device. Three capacitors in series – gate depletion, C_{Ge}, insulator, C_{ox}, and channel depletion, C_{Si} – divide the potential difference across the gate stack, as illustrated in Fig. 6.12. The equivalent capacitance, C_{TOTAL}, of the capacitors in series is given by (6.1)

$$\frac{1}{C_{TOTAL}} = \frac{1}{C_{Ge}} + \frac{1}{C_{ox}} + \frac{1}{C_{Si}} \tag{6.1}$$

The value of the equivalent capacitance is dominated by the smallest capacitance among the three, which in turn depend on the device structure and operating bias.

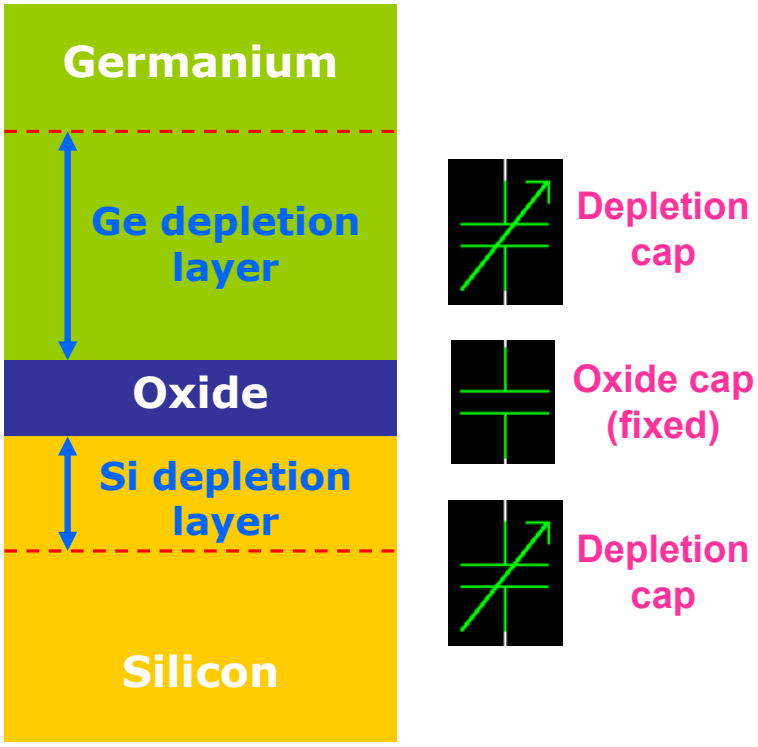


Fig. 6.12 The series combination of the oxide capacitor and the two semiconductor depletion layer capacitances. The oxide capacitance is fixed while the Ge and Si depletion capacitance vary with the bias. The equivalent capacitance is dictated by the smallest among the three. Therefore, it is desirable to have the oxide capacitance much larger compared to the Ge capacitance.

MEDICI^{TM} was used for 2-D electrostatic and transient device simulations to analyze the gate stack [71]. The simulated structure is a stack of 300 nm Ge with 10^{18} cm^{-3} *p*-type doping, 5 nm SiO_2 on *p*-type Si with 10^{16} cm^{-3} impurity concentration. C_{TOTAL} versus gate voltage (V_{GATE}) curves with varying light intensity are plotted in Fig. 6.13. For $V_{GATE} < -1V$, the Si channel is accumulated hence C_{TOTAL} is equivalent to C_{Ge} and C_{ox} in series. Incident light with $\lambda = 1320$ nm is absorbed in the Ge gate increasing the stored charge, hence increasing C_{Ge}. The film thicknesses are such that $C_{ox} >> C_{Ge}$ so C_{TOTAL} increases with C_{Ge}. The capacitance is modified by light because the optically generated carriers in the gate depletion region act as an extra source of charge. Due to capacitance change, $Q_{inversion}$ is also modulated with incoming light.

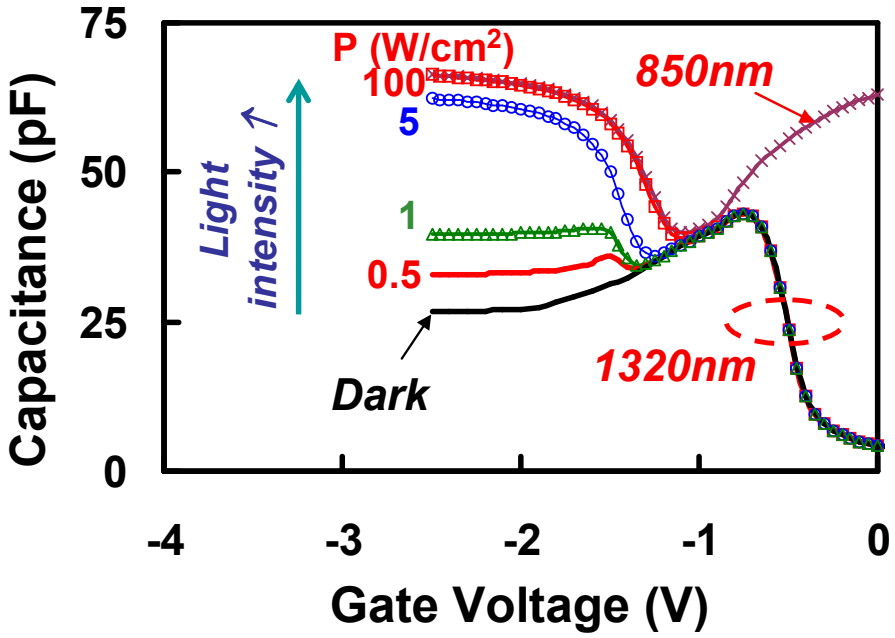


Fig. 6.13 Simulated C_{gate}-V_{gate} with varying light intensity of Ge-SiO_2-Si stack. Only Ge depletion capacitance is modulated by 1320 nm light. Si also absorbs at 850 nm, hence Si depletion capacitance is also modulated with light at this wavelength.

For $V_{GATE} > -1V$, Si is depleted and finally inverted, while the gate is accumulated. Since Ge region is accumulated, C_{TOTAL} is equivalent to C_{Si} and C_{ox} in series, and cannot be modulated by absorption in the gate. Moreover, Si is transparent at $\lambda = 1320$ nm, so C_{TOTAL} is unchanged with incoming light intensity at this wavelength. A single curve is

plotted for incident light with λ = 850 nm which is absorbed by Si. C_{TOTAL} increases with C_{Si} as the stored charge increases due to absorption in Si depletion region.

6.2.4 Small signal FET gain

The origin of the built-in gain in the OE-MOSFET can be understood by investigating the transistor frequency response. A simplified way of modeling a MOSFET can be a voltage controlled current source. The small signal equivalent circuit of a MOSFET is schematically illustrated in Fig. 6.14 [72] where the subscripts *G*, *D* and *S* denote gate, drain and source terminals, respectively.

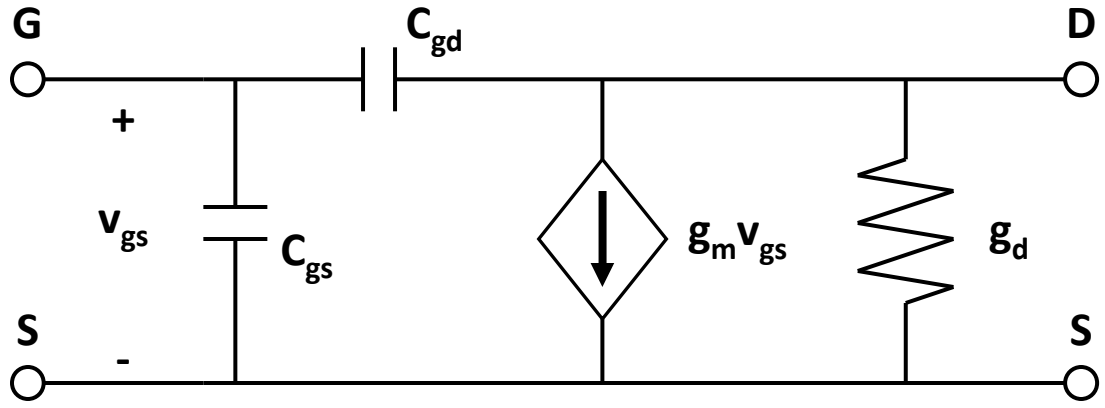


Fig. 6.14 Schematic illustration of the small signal ac equivalent circuit of a MOSFET. The MOSFET is modeled as a voltage controlled current source. The gate voltage is amplified at the drain terminal by the transconductance and the drain conductance. Similarly, the drain current is an amplified version of the gate current due to the FET gain.

The transconductance, g_m, is given by

$$g_m = \frac{W_G \times \mu \times C_o}{L_G} V_D \tag{6.2}$$

where W_G and L_G are gate width and length, respectively, μ is the effective mobility in the channel, C_o is the gate capacitance per unit area, V_D is the dc drain voltage at the bias

point and g_d is the output conductance. The small signal current gain, β, of the transistor can be defined as the ratio of the drain current to the gate current. This term indicates the current amplification by the MOSFET, similar to that in a bipolar transistor. When the output of the transistor is shorted, the ac drain current, i_d, is given by,

$$i_d = g_m v_g \tag{6.3}$$

where v_g is the ac gate voltage. Similarly, gate current, i_g, can be expressed as [73]

$$i_g \approx j\omega \times C_o \times v_g \tag{6.4}$$

Therefore, combining (6.3) and (6.4) the magnitude of the current gain, β, becomes

$$\beta = \frac{i_d}{i_g} \approx \frac{g_m \times v_g}{\omega \times C_{gs} \times v_g} \tag{6.5}$$

Substituting g_m from (6.2), $C_{gs} = C_o \times W \times L$ and $\omega = 2 \times \pi \times f$, (6.5) can be further simplified

$$\beta \approx \frac{\mu \times V_D}{2 \times \pi \times f \times L^2} \tag{6.6}$$

where f is the frequency of operation. Therefore, shrinking the gate length of the MOSFET quadratically enhances the current amplification factor. This is extremely promising especially from scalability perspective. It is also worth noting that the unity-gain frequency, f_{max}, (or sometimes called the cut-off frequency, $f_{cut\text{-}off}$) defined as the frequency at which the absolute value of the ratio of the output current to the input current is unity when the output of the transistor is short circuited. At this frequency $\beta = 1$ and the transistor is no more amplifying the gate current, but merely replicating it at the output terminal. Therefore,

$$f_{\max} \approx \frac{\mu \times V_D}{2 \times \pi \times L^2} \tag{6.7}$$

6.3 DEVICE FABRICATION

6.3.1 Ge-SiO_2-Si capacitor fabrication

To verify simulation results, we fabricated Ge-SiO_2-Si structures. The starting substrates were (100) oriented *p*-type 4" Si wafers with resistivity in the range of 1-5 Ω-cm (~10^{15} cm^{-3}). An ultra-clean surface is essential in order to ensure good interface quality between Si channel and the gate insulator. This is achieved using a standard clean consisting of two main steps to remove organic and metallic contaminants. The organic and gross contaminants such as scribe dust are removed using a 4:1 volume ratio mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) at 90ºC for 10 minutes. A thin chemical oxide is formed on the surface of Si substrate due to oxidizing nature of H_2O_2 and this can be removed by a dilute hydrofluoric acid (HF). Following the removal of organics, the wafers are cleaned in a 5:1:1 volume ratio mixture of de-ionized (DI) water, hydrochloric acid (HCl) and H_2O_2 at 70ºC for 10 minutes in order to remove alkali ions and other trace metallic contaminants. H_2O_2 oxidizes the surface while HCl reacts with most metals to form soluble chlorides. Similar to the previous step, a chemical oxide forms on the surface during this clean. This chemical oxide and any native oxide on the surface of the wafer will prevent good interface quality, hence they need to be removed. A 30 sec etch in 50:1 diluted HF solution is used to remove the oxides from the surface.

To ensure no native oxide grows on the surface, wafers are loaded into oxidation furnaces immediately after the cleaning. Two samples were fabricated with 3.5-nm-thick (sample CA) and 6-nm-thick (sample CB) SiO_2 layers thermally grown at 900°C followed by 240 nm polycrystalline Ge deposition. No intentional impurity was introduced during or following Ge deposition. The gate regions were patterned by photolithography and dry etched. Finally, both samples were annealed at 400°C in forming gas ambient for 45 min.

Fig. 6.15(a),(b) plots the measurement results for sample CA and CB respectively, showing capacitance changing with light as predicted by simulations. Due to experimental difficulties, visible light was used in capacitance measurements. When V_{GATE} < -1V, Si channel is accumulated while Ge gate is inverted. In this region, total

capacitance, C_{TOTAL}, is roughly equal to C_{Ge} because C_{ox} is considerably high. Light absorbed in the space charge region modifies the depletion width in the gate changing C_{TOTAL} and hence the stored charge. The accumulation and inversion conditions for Si and Ge swap when $V_{GATE} > 0V$. Similarly, equivalent capacitance is now dominated by C_{Si} and the light absorbed in the channel modifies C_{TOTAL}. The modulation of measured capacitance in sample CA is stronger than that in sample CB owing to thinner oxide in sample CA.

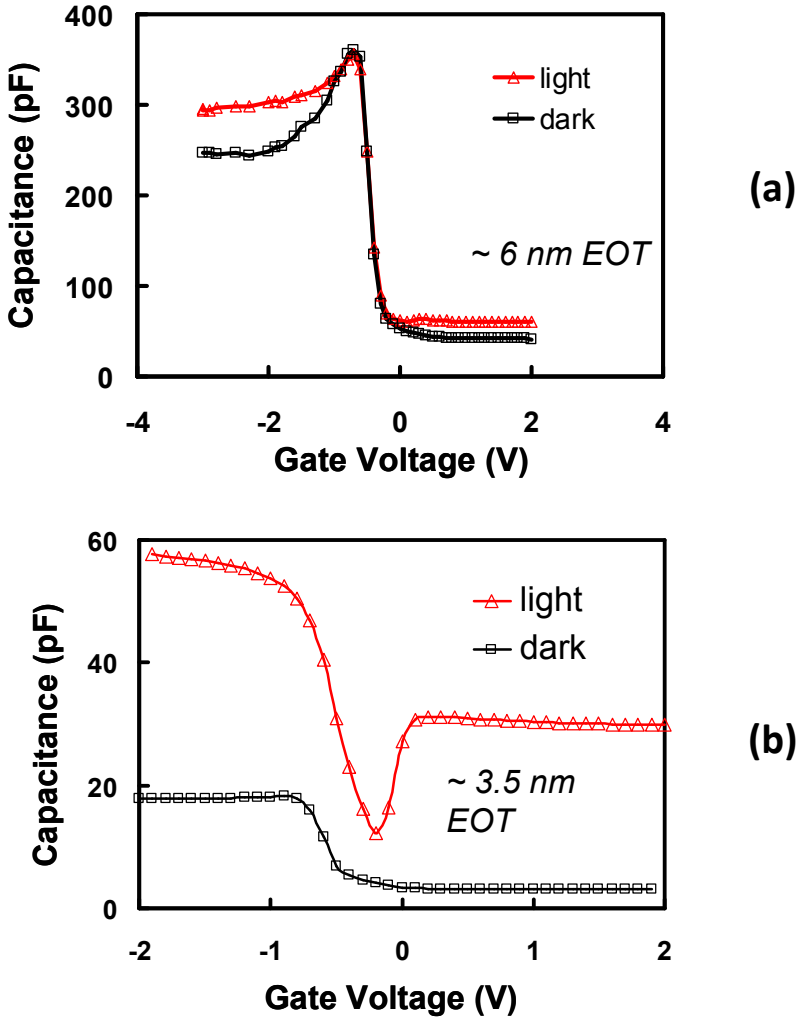


Fig. 6.15 Experimental high frequency (100kHz) C_{GATE}-V_{GATE} results. SiO_2 thickness (a) 6 nm and (b) 3.5 nm. Due to experimental difficulties, visible microscope light is used in measurements. Si also absorbs at this wavelength and hence Si depletion capacitance, dominant when $V_{GATE}>0$, is also modulated.

6.3.2 Optoelectronic transistor fabrication

The fabrication process of optical transistors is similar to that of the capacitors with additional steps to define the source and drain regions and contacts. The complete process flow is provided in Table 6.1 with each step outlined. The optoelectronic MOSFETs were fabricated on (100) oriented *p*-type (~10^{15} cm^{-3}) Si substrates. The wafers were initially cleaned similarly by the standard clean (SC), 10 min in 4:1 H_2SO_4:H_2O_2 and 10 min in 5:1:1 H_2O:H_2O_2:HCl to remove organics and trace metals, respectively. Following the standard clean, the wafers were dipped in 50:1 H_2O:HF for 30 sec to remove the chemical oxide that formed on the surface of Si. Immediately after the HF clean, the wafers were loaded to the oxidation furnace to grow 500 nm of SiO_2 at 1000°C in steam ambient. This growth was sandwiched between two steps of high quality thin SiO_2 for 10 min each in dry ambient within the same atmospheric furnace. This oxide layer is used as field isolation (FOX) of individual MOSFETs to avoid parasitic electrical interaction between neighboring transistors [74]. In order to define active areas for the devices, the field oxide was then patterned by photolithography followed by wet chemical etching in 6:1 H_2O:HF buffered oxide etchant (BOE). Wet etching ensures slanted FOX sidewall in addition to minimize etch damage to the active area that will become the channel of the transistor.

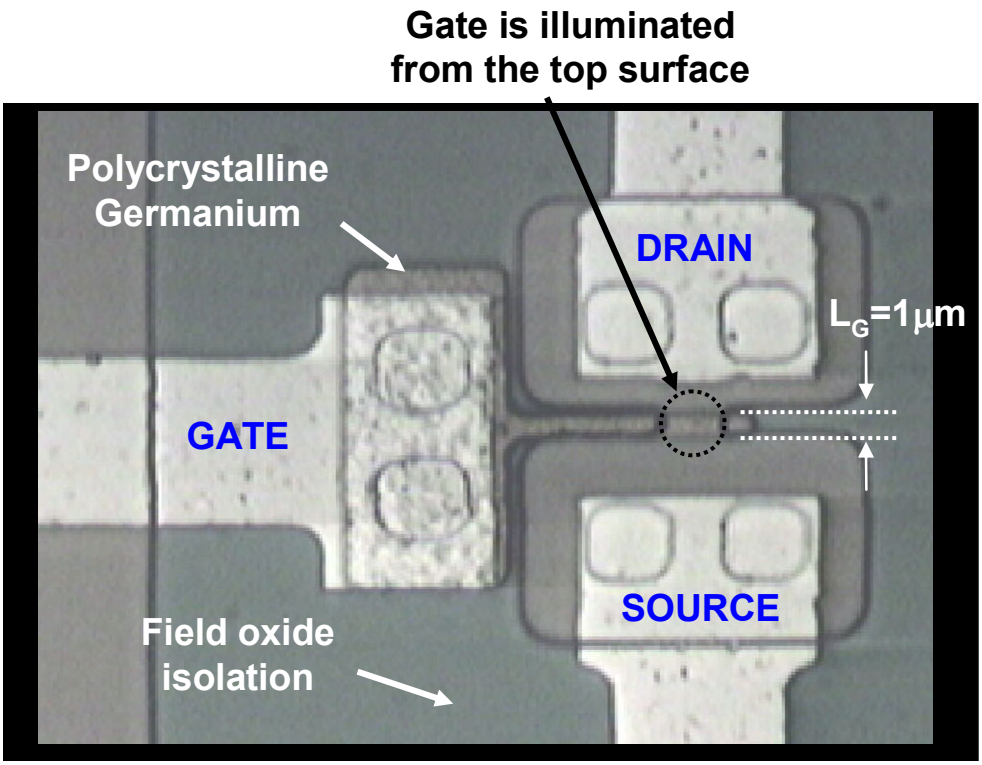
Photoresist was removed by hot sulfuric acid and the wafers were again cleaned by SC followed by 30 sec HF dip. A 40 nm sacrificial SiO_2 layer was thermally grown in order to reduce the ion implant damage to the surface and to avoid dopant out-gassing during subsequent anneal steps. The samples were then doped with Boron. A double implant was performed, the first with 180 keV B11 with a dose of 5×10^{12} cm^{-2} to form a p-well and the second more shallow 50 keV B11 with a dose of 1.4×10^{12} cm^{-2} to adjust the threshold voltage. The samples were cleaned by SC following the implantation and annealed for 1 hr in inert ambient at 1000°C in order to diffuse and activate the doped regions [74,75]. After the activation of *p*-type dopants, the wafers were implanted by 100 keV 5×10^{15} cm^{-2} As75 using photoresist as the masking layer. This step was followed by source/drain activation anneals for 15 min at 1000°C in inert N_2 ambient. The sacrificial SiO_2 layer prevents dopant out-diffusion from the source/drain regions [75].

Step	Description	Process Details
0	Starting substrate	4” (100) *p*-type 1-5 Ω-cm Si wafers
1	Field isolation (FOX)	Standard clean (SC) → Thermal oxidation at 1100°C, oxide thickness ~ 5000Å
2	Active area definition	Lithography → Wet chemical etching of FOX by 6:1 Buffered HF
3	Sacrificial oxidation	Resist strip → SC → Thermal oxidation at 900°C, oxide thickness ~ 400Å
4	Double p-well implant	180 keV B11 at 5×10^{12} cm^{-2} 50 keV B11 at 1.4×10^{12} cm^{-2}
5	Annealing and dopant activation	SC → 1 hour furnace anneal at 1000°C in inert N_2 ambient
6	Gate lithography	Photoresist patterned to mask the gate
7	Source/Drain implant	100 keV As75 at 5×10^{15} cm^{-2}
8	Annealing and dopant activation	SC → 15 min furnace anneal at 1000°C in inert N_2 ambient
9	Sacrificial oxide removal and gate oxidation	SC → wet etching in 50:1 HF → Thermal oxidation at 900°C, oxide thickness ~ 57Å
10	Gate deposition	LPCVD Ge deposition at 450°C 240 nm → CVD SiO_2 deposition at 400°C
11	Gate patterning	Lithography → Dry etching with RIE
12	Contact definition	280 nm CVD SiO_2 deposition at 400°C → Contact-via lithography → Wet SiO_2 etching in 6:1 Buffered HF
13	Metallization	Titanium (<20Å) followed by Aluminum (2500Å) deposition by sputtering
14	Metal patterning	Lithography → wet Al etching → 5 sec HF
15	Forming gas anneal	400°C for 45 min

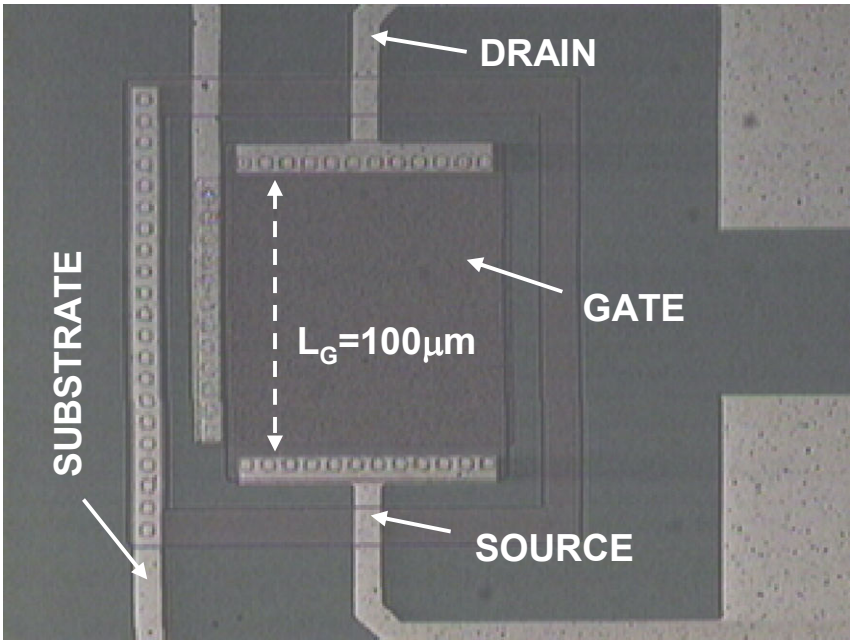
Table 6.1 Optical MOSFET process flow and details

The wafers were then cleaned with SC, this time followed by a longer 50:1 HF etching to remove the sacrificial oxide. Immediately after the sacrificial oxide strip, 5.7 nm high quality SiO_2 was grown as gate oxide at 900°C in dry ambient. It is crucial to minimize time delays between gate oxide growth and the deposition of the gate to avoid incorporation of impurities that may degrade the quality of the gate insulator. 240 nm Germanium gate was deposited by chemical vapor deposition (CVD) at 450°C immediately following the thermal oxidation step. When Ge is deposited directly on SiO_2, the reactions favor the etching of oxide instead of Ge deposition [76]. Therefore, a very thin (< 20 A) layer of Si "seeding" layer is first deposited. It is difficult to remove contaminants on Ge surface, so the Ge film was capped with a thin (< 40 nm) LTO (low temperature oxide) layer right after deposition. Various techniques have been demonstrated to obtain single crystal Ge on SiO_2 such as lateral overgrowth (necking) [77,78], rapid melt crystallization [79,80] and metal induced crystallization [81]. The crystallinity of Ge layer will affect the lifetime of optically generated carriers, and hence will influence the overall sensitivity and speed of the device. In this experiment, polycrystalline Ge is used for proof of concept owing to ease of deposition.

Transistors with gate lengths (L_G) and widths (W_G) ranging from 1-100 μm were patterned by photolithography and dry etched by RIE (reactive ion etching) using HBr chemistry to achieve straight side walls. A 280 nm LTO layer was deposited to protect the surface. Contact-via holes were opened into this LTO followed by 250 nm Al deposition. When annealed following this step, the gate electrode is significantly disfigured due to the very high tendency of Al to diffuse in Ge even at low temperatures. Therefore, it is essential to use a barrier to avoid Al diffusing into Ge and spiking in Si source/drain [75]. A thin layer of Ti (< 20 nm) was deposited first, as a barrier for Al diffusion into Si and Ge. Aluminum was patterned and etched to form the electrical probing pads. Finally, the samples were annealed at 400°C in forming gas ambient for 45 min. Fig. 6.16 shows a series of images of the completed devices with different gate lengths.



(a)



(b)

Fig. 6.16 Optical micrograph of the completed OE MOSFET with (a) 1 μm and (b) 100 μm gate length.

6.4 DEVICE CHARACTERIZATION

Electrical and optical characteristics of the optoelectronic MOSFET were both simulated and measured from experimental samples. Typical I_{DRAIN}-V_{DRAIN} results obtained by MEDICI^{TM} simulations are shown in Fig. 6.17(a). The plotted characteristics are for an L_G = 1 μm transistor formed on *p*-type Si with an acceptor concentration of 10^{18} cm^{-3} and *n*-type Ge gate with a donor concentration of 10^{16} cm^{-3}. I_{DRAIN} values are shown with and without light illumination of 1 μW/μm^2 intensity. From this figure, the *I-V* characteristics are comparable to that of a conventional MOSFET, regardless of whether or not light was input. The incident light acts as an additional gate bias modifying the conductivity of the Si channel.

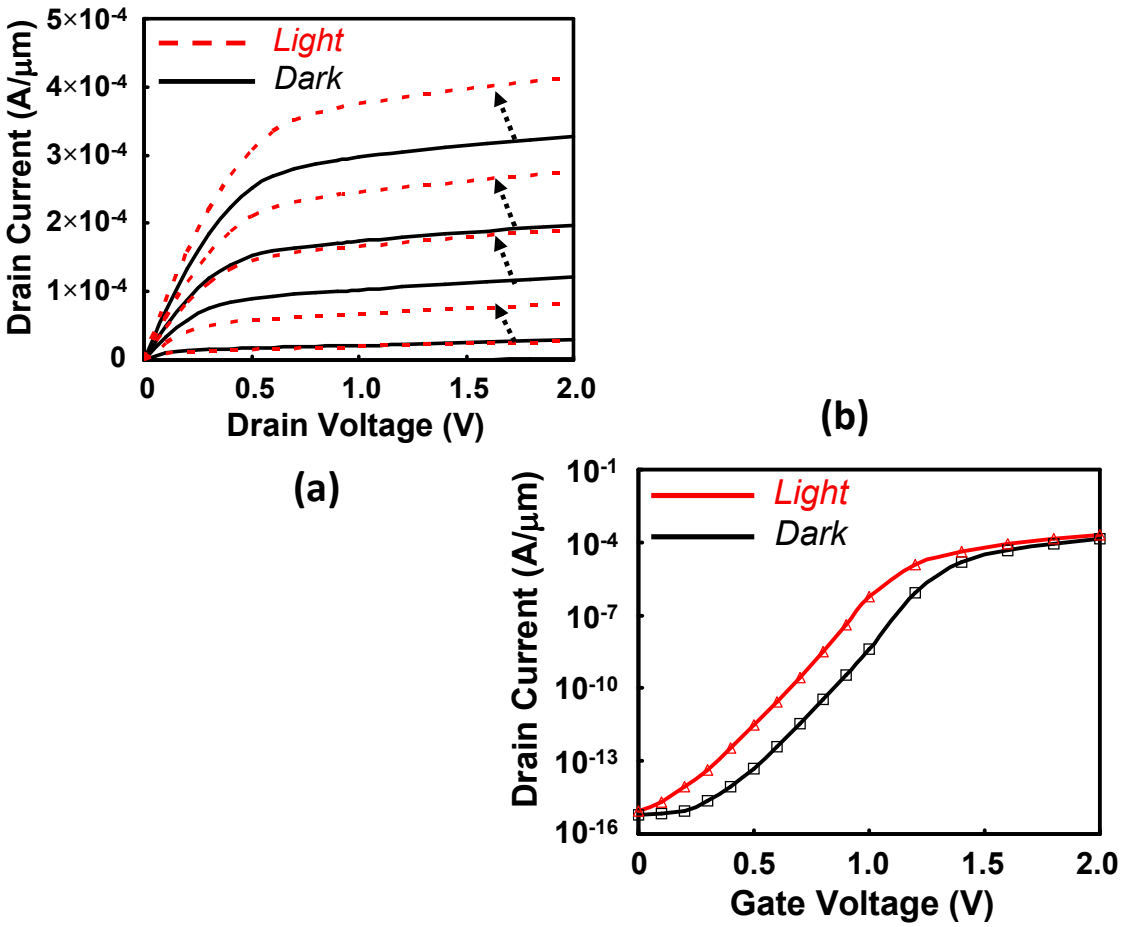


Fig. 6.17 (a) Simulated I_{DRAIN}-V_{DRAIN} results of a 1μm gate length transistor with n-doped Ge (10^{16}cm^{-3}) and p-doped Si (10^{18}cm^{-3}). Incident light (1μW/μm^2 in this case) constitutes a gate signal. (b) I_{DRAIN}-V_{GATE} characteristics of the same device. The curve is shifted due to the incident light.

Similary, I_{DRAIN}-V_{GATE} results are shown in Fig. 6.17(b) with and without illumination. A clear shift of the *I-V* curve is observed similar to a change in the threshold voltage or gate workfunction.

6.4.1 Experimental setup and characterization

The schematic of the measurement setup is shown in Fig. 6.18. The optical characteristics of the device were measured using an internally modulated semiconductor laser with a wavelength of 1.55 μm, which was coupled to a single-mode optical fiber. The light from the end of the fiber was irradiated onto the device via an optical setup such that the beam and the sample could be monitored simultaneously on an infrared camera. The light was coupled into the gate from the top surface. No attention was paid to anti-reflection coating as this can be separately designed for improved coupling efficiency.

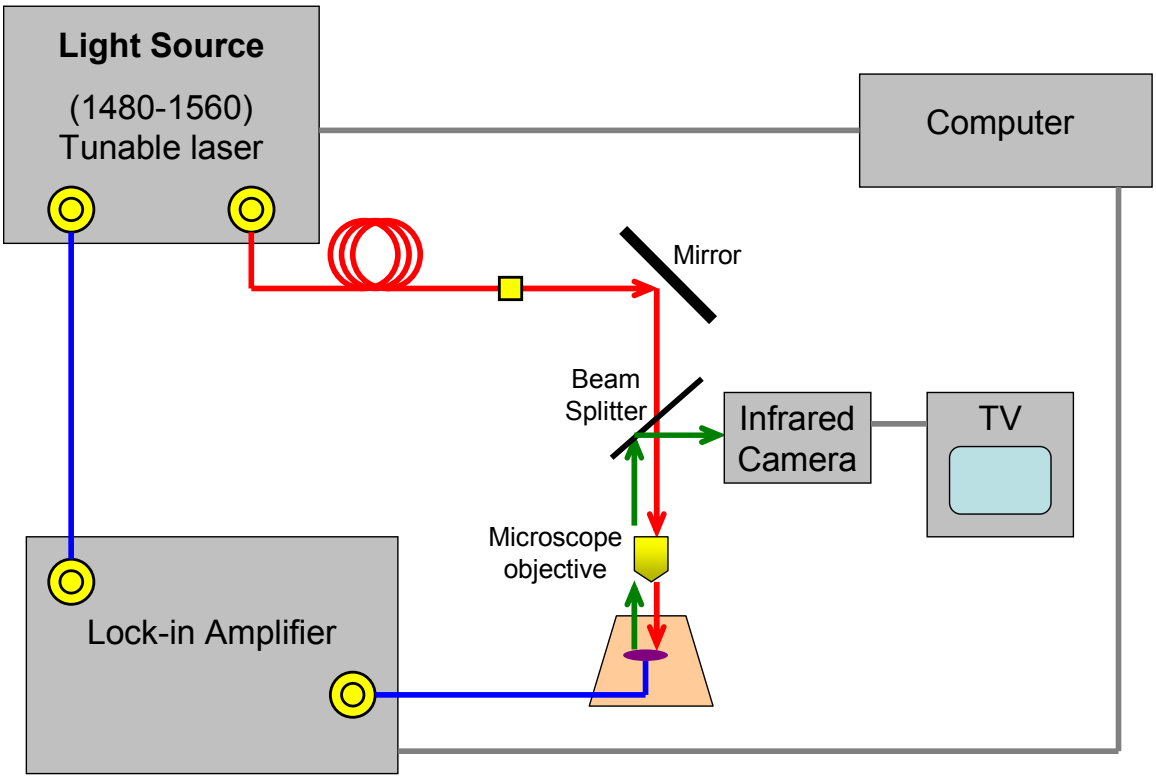


Fig. 6.18 Schematic of the experimental measurement setup.

There is no dc gate current (within measurement noise) due to the insulating SiO_2 layer. A synchronized lock-in amplifier was used to precisely extract the photocurrent component of the measured signal. Fig. 6.19 plots the measured optical gate and drain currents versus the gate voltage for $V_{GATE}=V_{DRAIN}$. The observed drain current is up to 3 orders of magnitude larger than the gate current, which can be attributed to the built-in gain of the transistor [82].

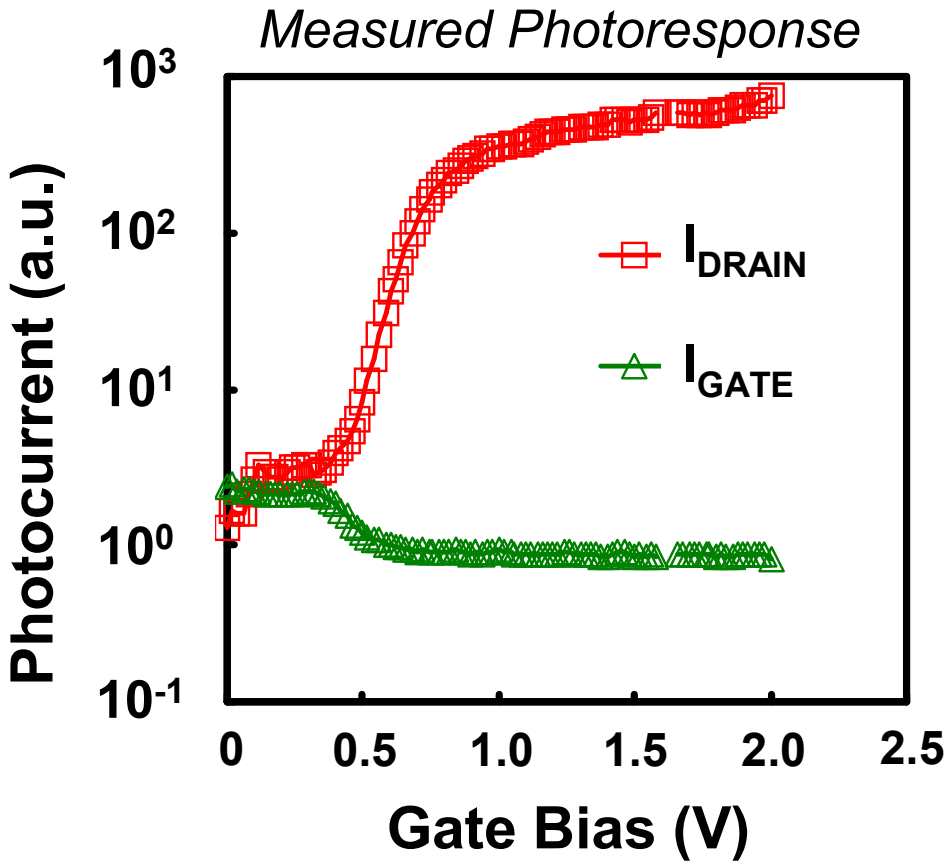


Fig. 6.19 Measured photocurrent at the gate and drain terminals when $V_{GATE}=V_{DRAIN}$. The dc current is below measurement noise limit. The flow of optically generated carriers in the gate constitutes a gate current, I_{GATE}, which is amplified by the transconductance of the FET at the drain terminal, I_{DRAIN}. Lock-in technique was used to precisely extract the optical currents.

6.4.2 Temporal response

The response speed of the OE MOSFET is limited by the FET cutoff frequency, f_{cutoff}, the drift speed of the photogenerated carriers in the absorption region and the *RC* time constant of the absorption region. The FET cutoff frequency is determined by the gate length and the carrier mobility in the channel. To increase f_{cutoff}, it is necessary to shorten the length of the FET channel and to use high mobility material for the channel. The *RC* time constant is determined by the dimension of the absorption region and lifetime of carriers. By reducing the dimension of the absorption region, the *RC* time constant will be decreased, and the cutoff frequency will be increased. When the channel is long, the overall cutoff frequency is determined by f_{cutoff}. When the length of the channel is shortened, the drift velocity or the *RC* time constants limit the cutoff frequency.

The intrinsic speed of the device is obtained by impulse response simulations. Ge is assumed single crystal in the simulations because there are no existing models for the polycrystalline grain boundaries. The grain boundary influence is predicted to reduce the carrier lifetime thus further increasing the device speed, trading off with sensitivity. The intrinsic speed increases with shrinking gate length. The calculated full-width half-maximum from impulse response simulations are < 1 nsec and < 100 psec for $L_G = 1$ μm and L_G = 100 nm, respectively. The high-speed performance of the OE-MOSFET is benchmarked against that of a traditional photodetector. The response of a classical MSM photodetector to a train of optical pulses is plotted in Fig. 6.20. The simulated MSM has 100 nm electrode spacing on 100-nm-thick Ge layer. In comparison, transient response obtained from the OE-MOSFET with identical 100×100 nm slab of Ge in the gate is also plotted in Fig. 6.20. This device provides significantly higher photocurrent (~ 3.5×) for identical optical energy in addition to lower off-state leakage (~ 4×) [83].

The speed of response of classical bipolar (FET) phototransistors is dominated by the capacitance of the collector-base junction (gate-drain) due to the Miller effect which multiplies the value of the *RC* time constant by the current gain of the phototransistor. Since there is no base (gate) connection in traditional phototransistors, when the collector (drain) terminal tries to rise in voltage, there is no source for the charge to come from to go onto the base (gate) end of the capacitor. The impact of the Miller effect is often

reduced by utilizing phototransistors in a cascode circuit. In the OE MOSFET structure, however, the detection region is electrically isolated from the transistor region and the charge can flow from the gate terminal. The output capacitance of the device, C_{switch}, is dominated by the gate-to-drain overlap and it is ~ 0.02 fF for an OE MOSFET with 100 nm gate length and width. Therefore, the *RC* limited bandwidth is very large. With proper scaling and band engineering, the device can operate in excess of 10 GHz.

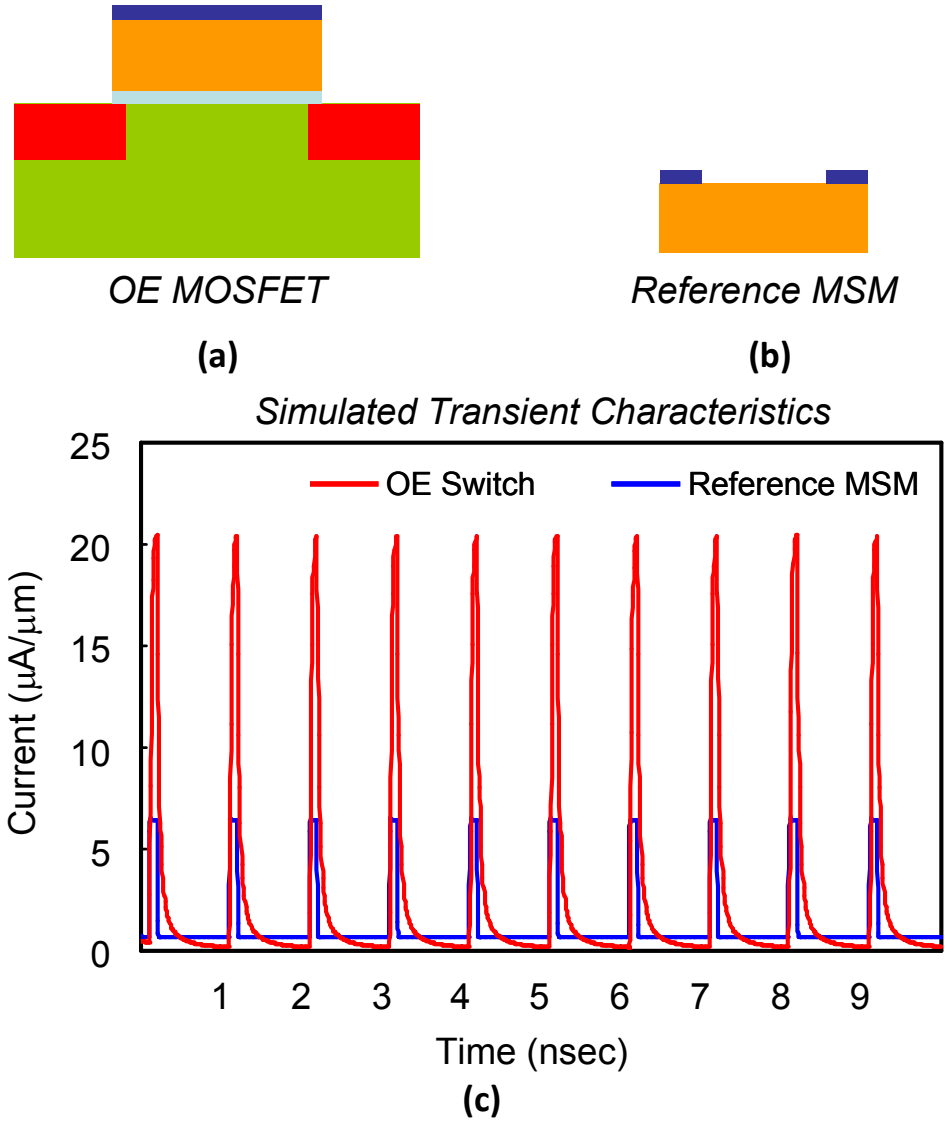


Fig. 6.20 Schematic illustration of (a) OE-MOSFET (b) traditional Ge MSM photodetector. The slab of Ge is identical in both structures. (c) Simulated transient response comparing the classical detector in (b) and the proposed device in (a). The input is a pulse train, each pulse delivering 1 fJ optical energy.

Another scheme we employed to compare the performance of the device is the totem-pole style [35,36] receiver-less operation. The simulated response from two back-to-back MSM detectors driving a capacitance (0.5 fF in 150 nm technology node [84]) is plotted in Fig. 6.21 together with that from two OE MOSFETs connected in a similar fashion and driving an identical capacitance. Two short pulses carrying 10^{-17} J each, and delayed in time by 100 psec are incident in both cases. The OE MOSFET provides significantly higher voltage swing with same input optical energy [85]. This essentially means less number of post amplification stages are required to raise the voltage level to the logic rail, reducing excess power dissipation, delay and area.

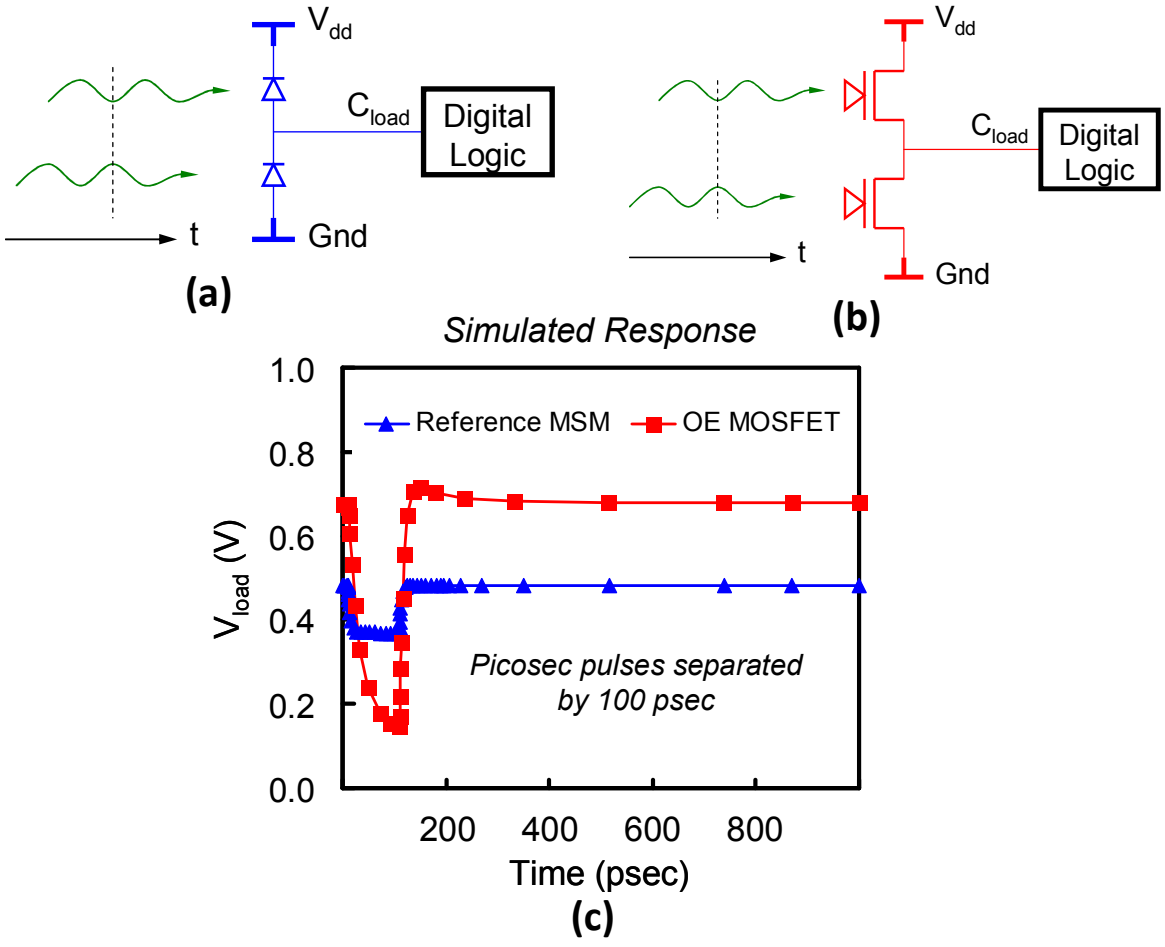


Fig. 6.21 Schematic illustration of totem pole circuit using (a) traditional Ge MSM photodetector (b) OE MOSFET. (c) Simulated transient response. In each case, the input is two short optical pulses delayed by 100 psec and delivering 10^{-17} J optical energy. The OE MOSFET provides > 4× voltage swing with identical input optical energy, driving identical capacitors.

The proposed device essentially is an optical detector with a built-in gain mechanism. In comparison, avalanche photodiodes (APD), for instance, provide gain by impact ionization. However, APDs require high bias voltages (20 V/μm) to achieve desired ionization rates, an increasingly difficult challenge to meet at operating temperatures of today's high-end processors. In contrast, the OE switch allows low voltage operation suitable for on-chip applications and potentially a better noise performance due to the separation of absorbing and conduction regions.

6.5 COMPLEMENTARY OPERATION

6.5.1 More light, less conduction

Unlike classical optical receivers, complementary operation is also attainable by this device scheme. The doping in the Ge gate and Si channel regions can be tailored such that the MOSFET drain-to-source current is reduced with the incident light. In other words, it is possible to configure a device that becomes less conductive as it absorbs more light. Such a device would be similar to a *depletion-mode* MOSFET (or *p*-MOSFET) and presents a complementary function to the enhancement-mode operation (or *n*-MOSFET). To simulate this concept depletion mode device with $L_G = 1$ μm channel was defined on *n*-type Si with an acceptor concentration of 10^{18} cm^{-3} and *p*-type Ge gate with a donor concentration of 10^{16} cm^{-3}. Fig. 6.22 compares simulated I_{DRAIN}-V_{GATE} characteristics of "enhancement mode" and "depletion mode" of operation with and without light. The enhancement mode device turns on with incident light, as described in section *6.4*. The depletion mode device, however, is normally on, and turns off when illuminated with light. The optoelectronic *n*-MOSFET and *p*-MOSFET devices can be connected as a CMOS inverter to create an optoelectronic latch with light as the input signal.

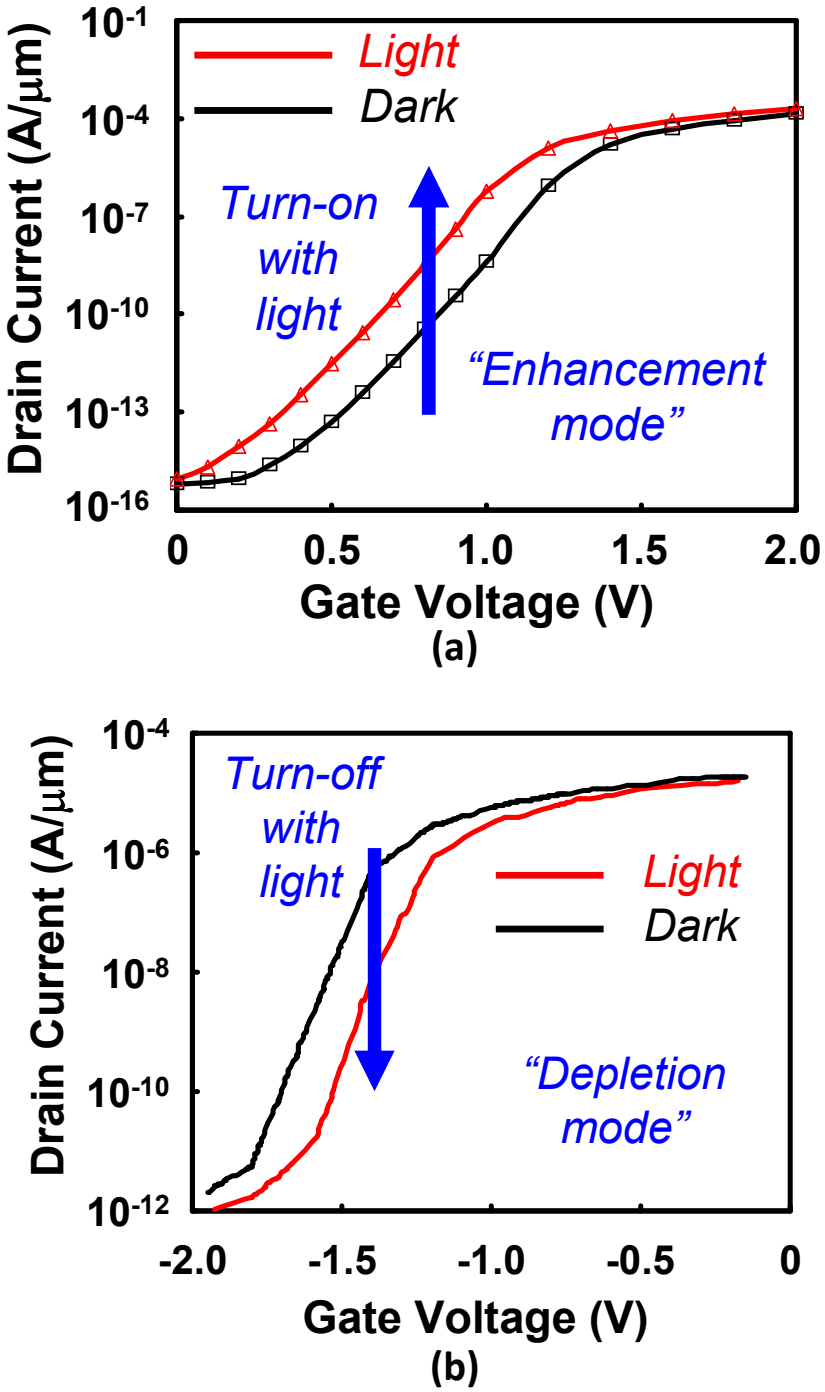


Fig. 6.22 (a) Simulated I_{DRAIN}-V_{GATE} show the effective gate signaling by incoming light. The device is normally off and turns on when illuminated with light, hence "enhancement mode" switch. (b) I_{DRAIN}-V_{GATE} characteristics of a normally on device. When illuminated, the device turns off (depletion mode). Gate and channel doping types are switched to achieve this behavior; p-doped Ge ($10^{16}cm^{-3}$) and n-doped Si ($10^{18}cm^{-3}$)

6.5.2 Optically controlled electrical inverter: Paving the way to bring light to latch

The arrangement, as described in section *6.5.1*, is illustrated in Fig. 6.23(a), in which, an optical signal irradiates the pair of complementary optoelectronic MOSFETs. The pair then drives the next stage logic, represented by the gate capacitance, C_{LOAD}. The characteristics for the optically controlled electrical inverter are obtained by MEDICI^{TM} transient device and circuit simulations. The simulated structure and mesh are shown in Fig. 6.23(b). No accurate models exist for polycrystalline Ge, so the gate is assumed to be crystalline Ge during the simulations. The channel lengths are chosen to construct a minimum size inverter in the 150 nm technology node [84]. For circuit operation, it is desirable to design the channel widths of the *n*-MOSFET and *p*-MOSFET independently. However, MEDICI^{TM} is a 2D simulator, so the channel widths are assumed identical, as the simulations were done along the channel depth and length. The next stage logic is chosen to be a minimum size inverter, which is one of the building blocks of the electrical logic, in the same technology node. When there is no optical input, the *p*-MOSFET is turned on while the *n*-MOSFET is off. The output capacitor is charged up to V_{dd}, hence it is at logic-high state. This could be considered as the initial condition. The input optical signal is a short pulse that excites the pair of complementary optoelectronic MOSFETs simultaneously. Upon arrival, the optical pulse turns the *n*-MOSFET on and the *p*-MOSFET off. The next-stage logic gate is discharged through the *n*-MOSFET during the optical pulse, pulling the output voltage down to logic-low. As the photo-excited carriers are removed, the pair recovers to initial state, charging C_{LOAD} back to V_{dd}. Therefore, an electrical 1-to-0 followed by a 0-to-1 logic transition is attained with the incident optical pulse.

The simulated temporal response of the optically controlled inverter is shown in Fig. 6.24, which plots the output voltage, V_{LOAD}, versus time. The speed of output high to low transition is in the order of 10-20 psec and depends strongly on the thickness of the absorbing layer. The width of the electrical pulse is determined by the low to high transition, which is governed by the *RC* time in the absorbing layer. Switching times as short as 100 psec are achieved corresponding to bit rates of ~ 10 Gbps.

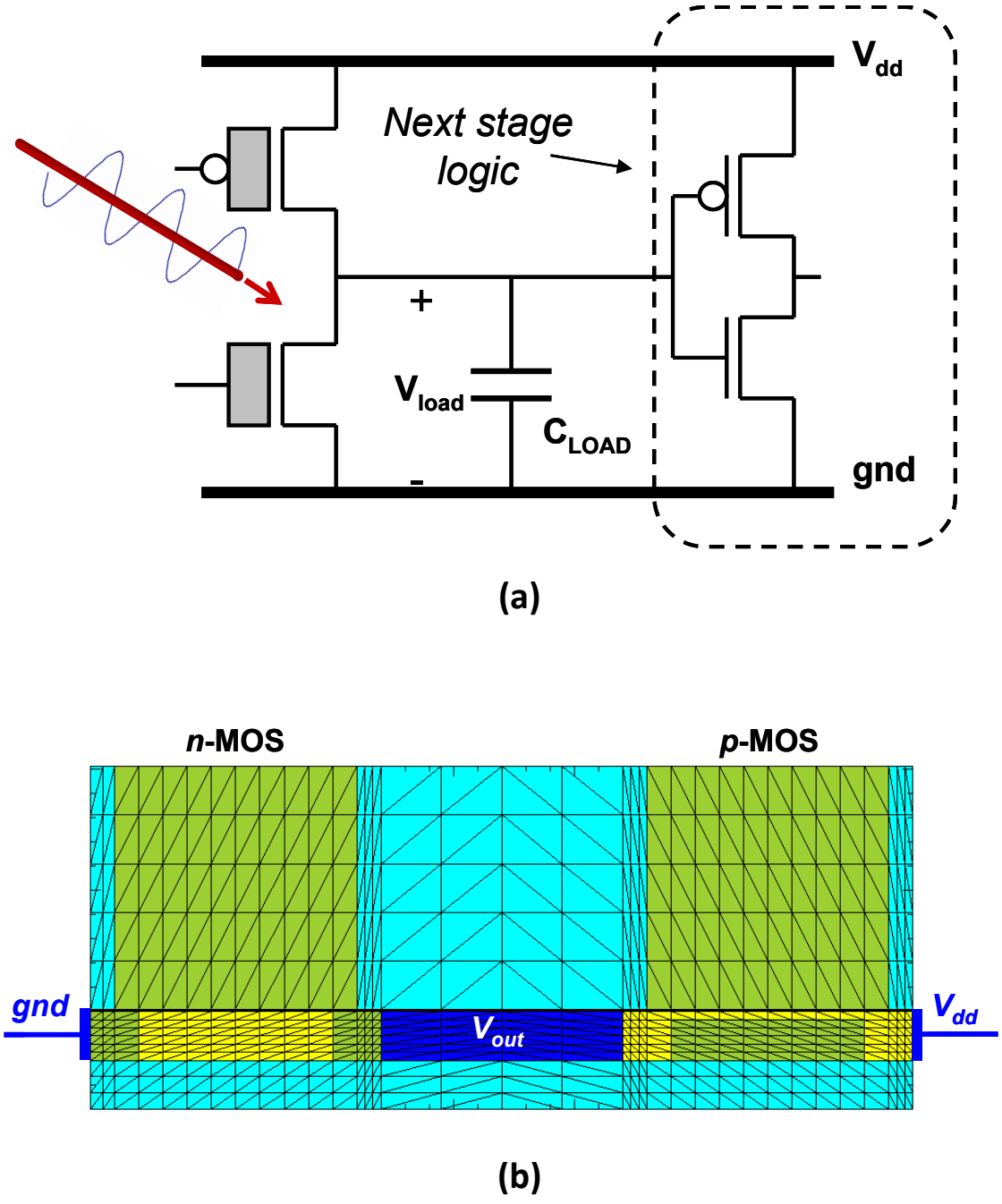


Fig. 6.23 (a) The complementary optical MOSFET pair connected as an inverter. The next stage logic is resented with a load capacitor. The capacitance is equal to that of a minimum sized inverter in 150 nm technology node. (b) The simulation mesh structure of the complementary pair forming an optically controlled electronic inverter.

This could be further improved by designing a thinner absorbing region and with shorter carrier lifetimes such as in polycrystalline Germanium [86], with the trade-off of reduced sensitivity. As mentioned above, the *p*-MOSFET and *n*-MOSFET channel widths can be independently tailored to "match" the complementary couple. In other words, by designing the relative channel widths, the pull up and pull down strengths of the pair can be balanced. Furthermore, the transistor channels can be scaled down for faster speeds.

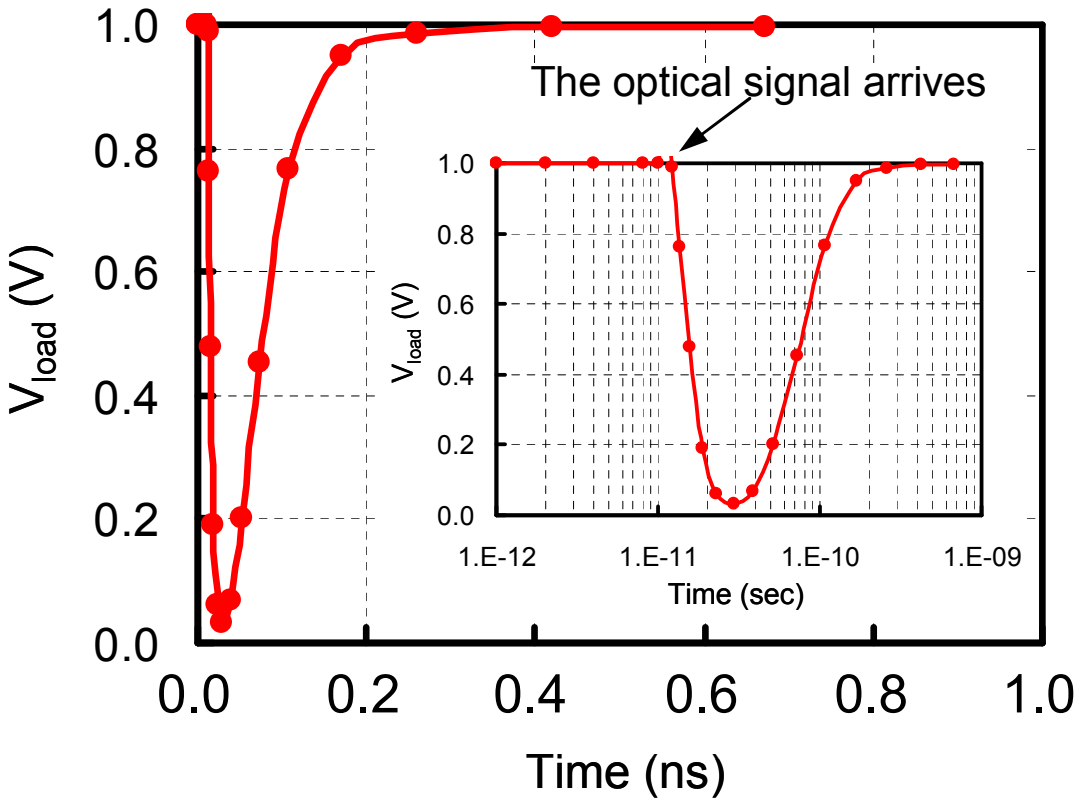


Fig. 6.24 Simulated transient response of the complementary optical MOSFET pair. The optically controlled electronic inverter is driving a minimum sized inverter as the next stage. Light pulse arrives at 10 psec. The output voltage is plotted vs time. It is possible to achieve very fast rail-to-rail swing even with no amplification stages.

6.6 OPTOELECTRONIC MOSFET AND THE TRADITIONAL RECEIVER

In this section we will present a qualitative argument about the comparison of the OE switch with a photodiode directly interconnected to a MOSFET, as illustrated in Fig. 6.25(a) and (b). Such a monolithic integration of the detector has many advantages in the traditional receiver design. As discussed above, this provides reduced detector capacitance and parasitic effects. The OE switch is advantageous compared to the direct connection scheme in a number of ways.

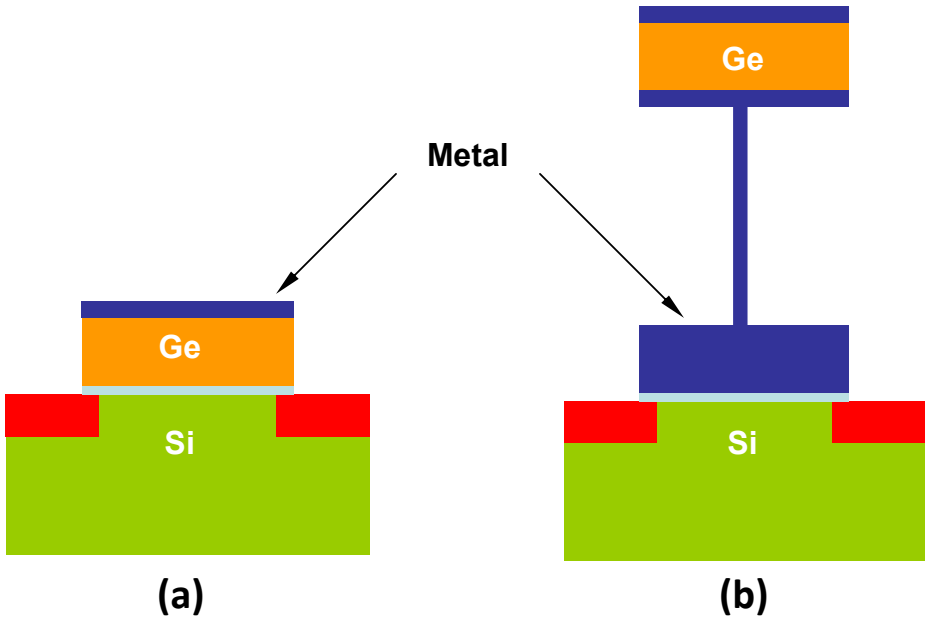


Fig. 6.25 (a) The OE MOSFET (b) Photodiode interconnected with a MOSFET.

The most obvious advantage can be expressed as the parasitic effects of the electrical connection. All electrical wires have resistance representing the ability of the wire to carry the charge flow. Similarly, all wires have capacitance representing the charge that must be added or removed to change the electrical potential on the wire. This situation is depicted in Fig. 6.26, which implies that the photo-generated charge will be shared between the line and the MOS gate. Therefore, sensitivity will be reduced. With the scaling of the technology, this problem is also magnified. Table 6.2 lists a number of critical technology design parameters [84]. The capacitance of the CMOS gate is decreasing with scaling technology nodes from 0.53 fF in the year 2000 down to less than 0.01 fF in the year 2007. The capacitance of the electrical wires, on the other hand, is

around 0.2 fF/μm and no longer scaling [87]. Fig. 6.27 plots simulation results of the transient response of OE MOSFET simultaneously with that of identical photodetector and MOSFET interconnected with 1 μm electrical wire. The input is a light pulse with identical energy and the wire resistance is ignored. OE MOSFET provides a significantly higher voltage swing.

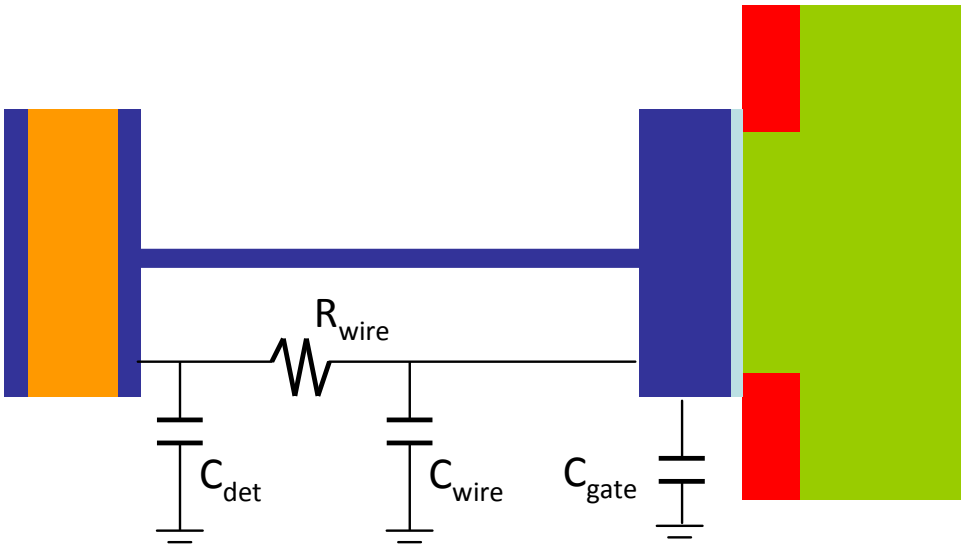


Fig. 6.26 Photodiode interconnected with a MOSFET. The wire capacitance and resistance as well as the detector and gate capacitances are indicated.

Year	***2000***	***2001***	***2002***	***2003***	***2004***	***2005***	***2006***	***2007***
Technology node (nm)	150	130	115	100	90	80	70	65
Physical gate length (nm)	100	90	75	45	37	32	28	25
Gate oxide thickness (nm)	2	2	1.5	1.3	1.2	1.1	1	1
C (minimum inverter) (fF)	**0.53**	**0.43**	**0.40**	**0.17**	**0.12**	**0.10**	**0.08**	**0.07**
Local wiring pitch (nm)					214	190	170	152
RC delay 1 mm line (psec)					304	395	502	553

Table 6.2 The ITRS technology design parameters.

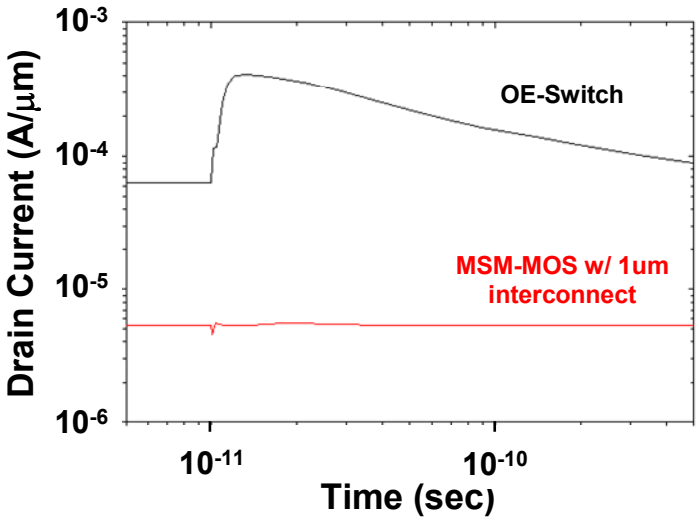


Fig. 6.27 Transient simulation results comparing OE-switch with a photodiode directly connected to a MOSFET with 1 μm electrical interconnect. The wire capacitance is assumed to be 0.2 fF and the wire resistance is ignored.

Another potential drawback of the configuration in Fig. 6.25(b) stems from the metal-semiconductor (M-S) junction. The M-S injection barrier will significantly reduce the speed of the device. When the light is turned off, the accumulated carriers in the gate electrode will have to be injected over a potential barrier from the metal into the semiconductor region. Furthermore, the potential application of complementary operation of the OE switch provides a promising scheme for the direct injection of light into the logic circuitry.

6.7 PERFORMANCE IMPROVEMENT AND SCALABILITY

6.7.1 Tunnel-FET

The physical thickness of the gate insulator decreases with the scaling technology. In the OE switch, electrons and holes accumulated on either side of the gate insulator, as illustrated in Fig. 6.9(b). The probability of carriers tunneling through such a narrow potential barrier can no longer be ignored in future technology nodes. This introduces an alternative mechanism for the removal of excess carriers when the light signal turns off. Therefore, the response speed of the transistor is expected to improve with the tunneling mechanism. In order to investigate the influence on the sensitivity, it is helpful to

consider a relatively old scheme, the MIS (metal-insulator-semiconductor) diode scheme. Fig. 6.28 shows the energy band diagram of a classical tunnel-emitter phototransistor that is based on MIS tunnel diode [57,88]. In contrast to thick insulator structures, MIS diodes with very thin insulating layers allow appreciable tunnel current flow between the metal and the semiconductor causing the semiconductor to depart significantly from the thermal equilibrium conditions when the diode is biased. In response to light, photogenerated holes accumulate at the semiconductor surface, and voltage is redistributed between the layers as shown with dotted lines in Fig. 6.28. The electron tunneling current is largely increased due to (1) the field across the tunneling layer is increased and (2) the barrier thickness is reduced since conduction band edge at the surface is below E_{Fm}. Under such conditions, multiplication of minority current may occur in the contact region. Shewchun and co-workers have explained in detail this multiplication process by driving analytical expressions and extensive numerical analysis [88,89]. They showed that small signal multiplication factor in the range of 10^2-10^3 can be obtained with appropriately designed diodes. The OE switch can be properly designed to take advantage of the tunnel mechanism in order to further improve its performance.

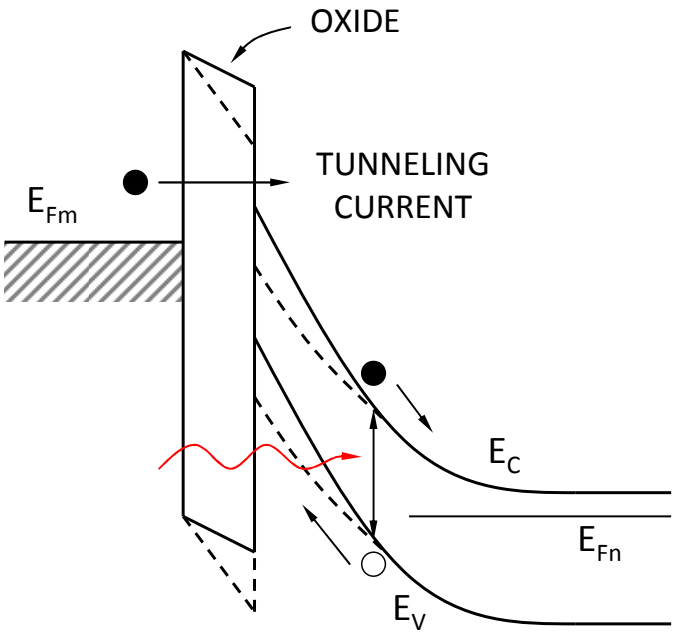


Fig. 6.28 Energy band diagram of the metal-insulator-semiconductor tunnel diode. Dashed lines indicate the response to light.

6.7.2 Photo-MOSFET

As an optoelectronic transformer the photodiode (MSM, PIN, APD) is studied as part of optoelectronic-integrated-circuits (OEIC). As discussed in the introduction, many photodetectors using FET have also been investigated because of their high speed response and the potential of integration. In these devices, photogenerated carriers are directly used to modulate the channel current. Unlike these devices, the OE switch introduced in this study, employs the change of the potential, not the change of the carriers. By making use of the third dimension in the design of the OE switch, the design space can be expanded even further. This section briefly describes a three-dimensional (3-D) OE switch structure, the *photo-MOSFET*. The schematic of the device structure is illustrated in Fig. 6.29(a) and (b) for 2-D and 3-D schemes, respectively.

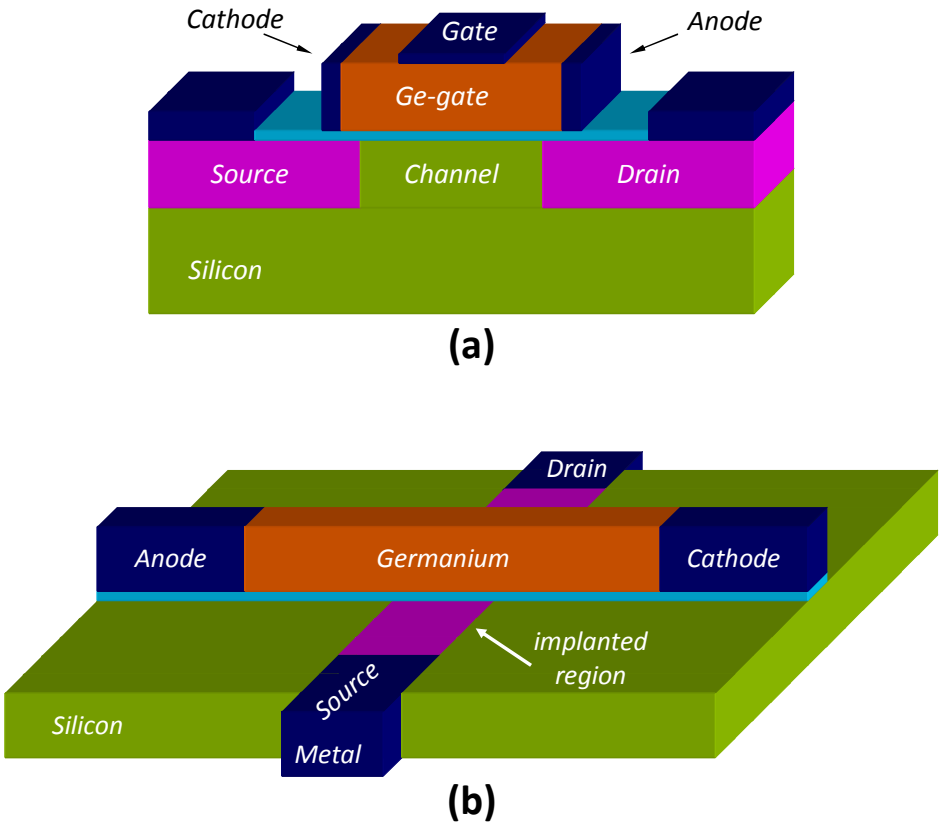


Fig. 6.29 Schematic illustration of (a) 2-D and (b) 3-D photo-FET. The switching speed is limited by the carrier transit time in the upper photodiode. A p-i-n or a planar MSM configuration can be used. Light can be coupled from the top or in a waveguide scheme.

The photo-MOSFET and the OE switch are alike except for the additional pair of metal contacts in the overlaid photodiode on the FET. Similar to the OE MOSFET, the upper photodiode part absorbs the optical input power and the lower FET part modulates the electric current via the potential applied to the FET. When light enters the absorbing gate region, part of the optical energy is absorbed and electron-hole pairs are generated. These electrons and holes drift to the opposite sides of the gate due to the external applied electric field. The excess charge in the gate modifies the potential distribution, similar to the OE switch case, which in turn modulates the gate voltage of the FET.

The analysis can be simplified if we ignore the influence of the gate voltage. This assumption is true when there is no gate voltage applied and it provides a general idea of device characteristics. The carrier transport in the intrinsic region of the overlaid photodiode is governed by the continuity equations given by [90-92],

$$\frac{\partial n}{\partial t} = -\left[\frac{n - n_o}{\tau_n}\right] + g + \frac{1}{e}\frac{\partial}{\partial x}J_n \tag{6.8a}$$

$$\frac{\partial p}{\partial t} = -\left[\frac{p - p_o}{\tau_p}\right] + g - \frac{1}{e}\frac{\partial}{\partial x}J_p \tag{6.8b}$$

where n and p are the carrier concentrations of the electrons and holes, g is the rate of generation of carriers, n_o and p_o are the equilibrium concentrations, t_n and t_p are the lifetime, and J_n and J_p are the current densities of the electrons and holes, respectively. With the uniform absorption of the input optical energy in the volume of the photodiode, the generation rate becomes,

$$g = \frac{\eta \times P_{optical}}{(h \times \nu)(L \times W \times H)} \tag{6.9}$$

Where η is the external quantum efficiency, $h\nu$ is the photon energy, and L, W and H are the dimensions of the gate as shown in Fig. 6.29. The recombination term and the diffusion current in the intrinsic region can be ignored if the length of this region is much shorter than the diffusion length of the carriers [73,90-92]. In addition, if the drift

velocity of the carriers is assumed to be constant at the saturated values, v_p for holes and v_n for electrons, (6.8) can be simplified as,

$$\frac{\partial n}{\partial t} = g + v_n \frac{\partial n}{\partial x} \tag{6.10a}$$

$$\frac{\partial p}{\partial t} = g - v_p \frac{\partial p}{\partial x} \tag{6.10b}$$

Under steady state conditions, the electric field and the carrier densities can be obtained by solving (6.10) and Poisson's equation simultaneously. The new charge distribution causes a reduction in the original applied electric field. There is a voltage drop due to this screening field which was driven by integrating the screening field in the intrinsic region [68,90,92].

A simplified analytical argument of the photo-FET is provided in this section. The underlying gain mechanisms in the OE switch and the photo-FET are similar and are based on a secondary photoconductivity. When biased properly, an electron traverses the FET channel for as long as a hole is present in the gate, resulting in more than one unit of current for a single photo-generated charge. The switching speed of this device is no longer dictated by carrier diffusion or recombination, but basically limited by the transit time of the carriers. Therefore, it is promising to attain very high switching speeds. This implies a trade off with sensitivity due to the nature of the gain mechanism in the FET device. Further investigation and a more detailed analysis of the photo-FET including the gate voltage are suggested in the *Future Work* section in the last chapter.

6.7.3 Nano-metallic light concentrators

Nano-metallic structures can be used to concentrate optical energy to a very small scale exploiting surface plasmonic waves. An illustrative schematic is shown in Fig. 6.30 integrating a photo-FET with metallic nano-structures. Experimentally, a factor of 5× enhancement in optical absorption has been demonstrated in [93-95], and in principle, it is possible to further increase this factor. Researchers have proposed other structures including bow-tie antenna [96] and bull's eye antenna [97]. The performance of the

optoelectronic switch can be improved by concentrating light on such small dimensions as the gate of the optical MOSFET pair. The switching speed can be increased by shrinking the thickness of the absorbing layer. Moreover, by squeezing more light into the volume of the absorbing gate region, the required optical energy for switching at a particular frequency could be reduced.

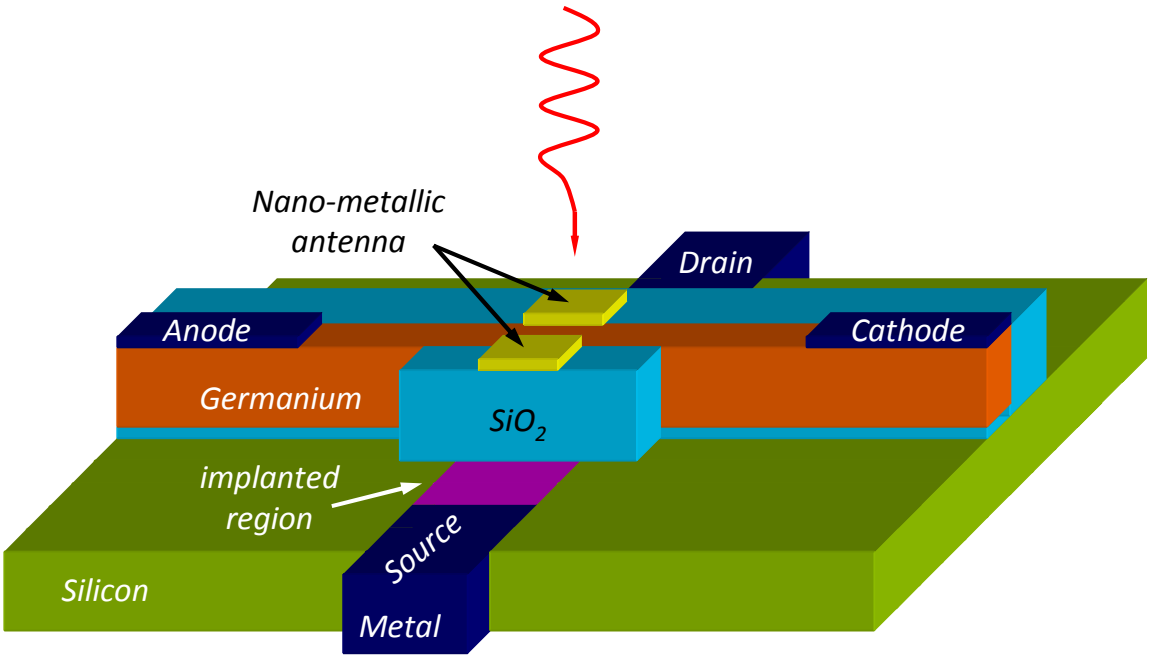


Fig. 6.30 Schematic illustration of integrated nano-metallic antenna with the OE switch. The plasmonic antenna can enhance the field around the absorbing gate region hence increasing the total absorbed optical power. Parts of the device are bisected and labeled ease of illustration. Anode and cathode collect the photo-generated carriers from the gate.

6.8 CONCLUSIONS

We have introduced a SiGe switching device that can perform optoelectronic conversion at the nanoscale. The OE MOSFET exhibits gain owing to a secondary photoconductive effect based on the current amplification of the FET. The switch is composed of a pair of complementary optical MOSFETs. The operation principle of the individual optical MOSFET is demonstrated by proof of concept experiments. The circuit performance of the complementary pair connected in an inverter fashion is investigated across various design parameters. Simulations show that it is possible to achieve 100 psec

cycling times by devices designed in the ITRS 150 nm technology node. The switching device can be fabricated along with deeply scaled conventional MOSFETs using advanced Si technology. Such a device is extremely compact and has very small capacitance. This is especially promising for on chip clocking applications, which require a synchronizing signal to be distributed to a large number of nodes. This scheme offers the ability to perform optoelectronic conversion at the latch level, facilitating optical clock distribution on the chip. This eliminates the power dissipation and area due to electrical H-tree networks. Plasmonic coupling could be used to concentrate light on such dimensions by nano-metallic structures to further enhance device performance. This design facilitates the insertion of optics at shorter distances in the chain of digital communication bringing light one step closer to the latch level.

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CHAPTER 7: CONCLUSIONS

To laugh often and much;
To win the respect of intelligent people and the affection of children;
To earn the appreciation of honest critics and endure the betrayal of false friends;
To appreciate beauty, to find the best in others;
To leave the world a bit better…
To know even one life has breathed easier because you have lived.
This is to have succeeded.
Ralph Waldo Emerson

Due to fundamental physical limitations and manufacturing complexity, it is becoming clear that alternative technologies are vital to mitigate communication problems in electronic information processing systems. Optics offers a range of features to overcome limitations of intrer-chip and intra-chip interconnections that are becoming increasingly attractive at higher bit rates and interconnection densities. Nevertheless, optics has to meet power, delay and cost requirements in order to be competitive with electrical wires. Monolithic integration of optical components with silicon electronic circuitry is critical to satisfy these requirements as well as novel device schemes that can exploit the physical advantages offered by optics. Germanium based optoelectronics has gained considerable attention thanks to its compatibility with the Si processing technology and strong optical absorption. Among photodetector schemes, metal-semiconductor-metal (MSM) optical detectors are attractive owing to their low detector capacitance, high speed and ease of integration. On the other hand, MSMs suffer from relatively higher leakage currents.

We have proposed a scheme to reduce the leakage of MSM photodetectors by using asymmetric metal electrodes. This method allows simultaneous engineering of the metal-semiconductor contacts. Using this technique, we have experimentally demonstrated an order of magnitude and two orders of magnitude reduction of dark current in Ge and Si MSM detectors, respectively (Chapter 3). To satisfy the cost and performance requirements, it is crucial to integrate photodetectors with silicon electronics. However, Ge growth on Si is hampered by the large lattice mismatch (4.2%) between the two material systems. The large mismatch results in extremely rough films high in defect

density. The performance of optical detectors built on such layers is significantly degraded. We have discussed a recently introduced technique to grow high quality Ge directly on Si. It consists of multiple steps of growth and annealing in hydrogen ambient. Such grown layers were shown to have low dislocation densities. Very high efficiency photodetectors were demonstrated using these Ge films grown on Si. In such detectors, recorded responsivities were as high as 0.85 A/W and up to 68% external quantum efficiency at 1550 nm wavelength (Chapter 4). Further physical investigation gave insight on the stress-strain levels of the grown Ge layers. X-ray diffraction analysis yielded a residual tensile strain which was verified by wavelength spectral measurements. The origin of the strain was explained by the mismatch in coefficients of thermal expansion of Si and Ge. A 47 nm red shift of the absorption edge was recorded corresponding to ~ 24 meV bandgap shrinkage.

For optical interconnects, a waveguide is the medium in which the signal propagates from the transmitter to the receiver. We have experimentally demonstrated the integration of Si-based optical detectors with optical waveguides (Chapter 5). The polymer-based waveguide technology was introduced earlier by other researchers. Polymer pillars with various cross-sectional geometry, size, and aspect ratio were fabricated on detectors with various active area and metal finger spacing. Results indicate that the characteristics of the photodetectors do not degrade as a result of the pillar fabrication.

Finally, we have introduced a novel SiGe optical to electronic transformer based on MOSFET scheme (Chapter 6). The device exhibits internal amplification owing to FET current gain based on a secondary photoconductivity. The proof of concept for the individual optical MOSFET was demonstrated by experiments and current amplification up to 1000 was recorded. We investigated a complementary scheme using the optical MOSFET as the building block. Simulations result 100 psec cycling times by devices designed in the ITRS 150 nm technology node. The switching device can be fabricated along with deeply scaled conventional MOSFETs using advanced Si technology. This is especially promising for on chip clocking applications, which require a synchronizing signal to be distributed to a large number of nodes. This scheme offers to perform optoelectronic conversion at the latch level.

RECOMMENDATIONS FOR FUTURE WORK

1. *Integrated waveguide photodetector:* In this work, we demonstrated very high efficiency Ge optical detectors based on SiGe. This technology can be further exploited in conjunction with the SOI or polymer based waveguide scheme to realize a waveguide photodetector integrated on a Si chip. Further integration with silicon CMOS can be a framework to asses the impact of integration on individual transistor performance.

2. *On-chip optical link:* The suggestion above can be extended to a full-scale optical link integrated on a chip by using the recently introduced SiGe electro-optic modulator technology. Such an integration is extremely interesting to become the first demonstration of fully compatible on-chip optical interconnect. Moreover, it opens the possibility to comparatively study the performance of traditional copper interconnects and optical interconnects on a chip simultaneously.

3. *Integrated CMOS receiver:* The very high efficiency Ge detectors can be integrated with Si receiver circuits for high performance classical receivers.

4. *Complementary function and analytical modeling:* Simulations show very promising results for complementary function of the optoelectronic MOSFET. Experimental verification of the concept is essential to build a complementary pair. Furthermore, the current study offers a rather qualitative explanation of the operation of the device. Application dependent optimization requires more detailed analytical models based on first principles. It is also desirable to have a circuit model for the device (such as a SPICE model) which can significantly benefit the simulation and optimization studies.

5. *Tunnel-FET:* Turn-off can be a potential bottleneck for the OE-MOSFET high speed operation due to the need to remove the accumulated carriers at either side of the gate insulator. The properties of the gate dielectric can be engineered to allow tunneling of the accumulated carriers hence increasing the speed of operation with a trade-off in the sensitivity.

6. *Photo-MOSFET:* The photo-generated carriers in the gate of the OE MOSFET can be collected by a traditional scheme of a photodetector. In such a device, the speed of operation can be very high because the carriers are swept out of the gate region. The gain is still related to the number of times a carrier traverses the channel until the photo-generated charge in the gate is removed. For highly scaled transistor dimensions, the MOSFET provides the current amplification at such high speeds.

7. *Optoelectronic memory:* The communication bottleneck between the processor and the memory on future tera-scale CPUs is looming as a show-stopper. In applications such as computer vision, the memory bandwidth is already well above traditional requirements, reaching 100's of GB/s. The need for large bulk memory capacity and bandwidth is seen as a great challenge with increasingly more stringent power requirements. The OE MOSFET can be studied as a direct-write optical memory. The absorbed optical signal generates carriers in the gate of the MOSFET. This corresponds to a threshold change of the MOSFET, hence toggling its storage status (e.g. from logic zero to logic 1). The "read" operation can be similar to that used in flash memory units, as the storage is similarly based on threshold voltage change with electronically injecting carriers into a floating gate. For use as a volatile-memory, the OE MOSFET can be designed to retain the gate charge for relatively longer times with less frequent refresh requirements.

8. *Nano-metallic light concentrators:* Today, the dimensions of the gate of a transistor are less than 100 nm. The OE MOSFET is promising many benefits, however, coupling of light into such nano-scale dimensions is a significant challenge. Plasmonic antennas were demonstrated elsewhere using nano-metallic concentrators. Integration of such an "antenna" with the proposed OE MOSFET can address the problem of light-coupling into the device.

APPENDIX A: POLYCRYSTALLINE GERMANIUM BASED DETECTORS

In this appendix, the growth of polycrystalline Germanium films for the purpose of optical detectors is discussed. Physical characterization results of the grown films together with measured photodetector characteristics are presented.

A.1 FILM GROWTH

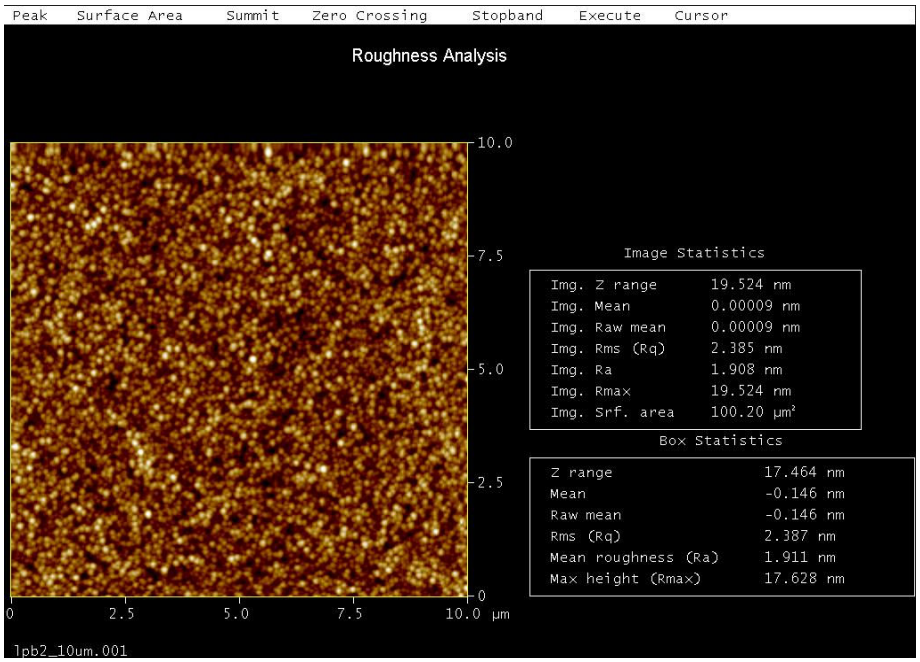
Germanium films were grown in a low pressure chemical vapor deposition (LPCVD) furnace using germane (GeH_4) species. The growth mechanism is similar to the epitaxial growth described in Chapter 4. The reaction furnace used is a multi-wafer, hot-wall quartz tube heated by coils. Hydrogen is used as the carrier gas. Germanium is deposited as either an amorphous or polycrystalline phase depending on the reaction conditions.

A.2 PHYSICAL CHARATERIZATION

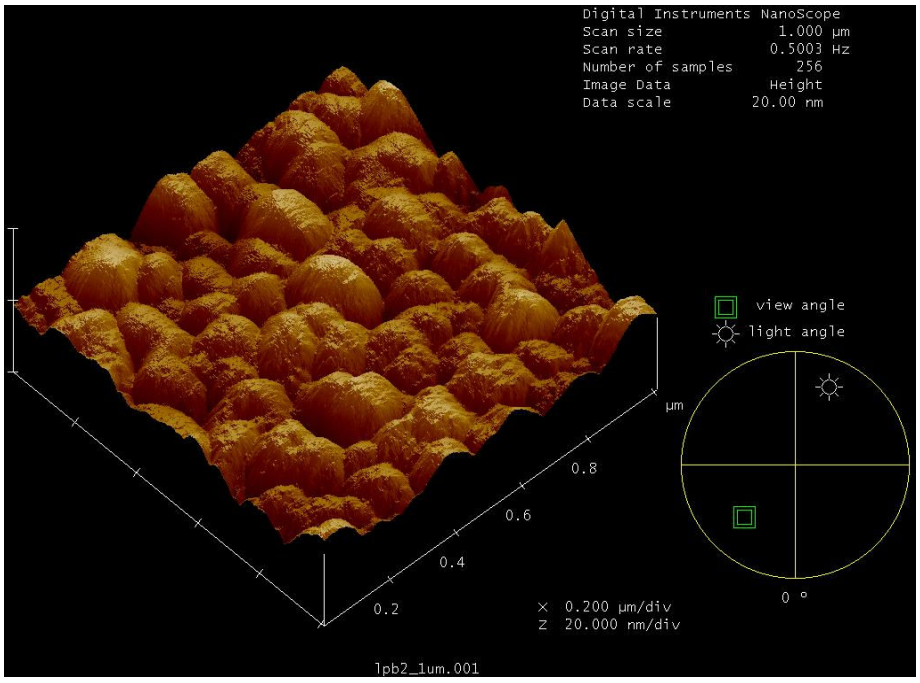
Atomic force microscope (AFM) analysis of the films were conducted for amorphous and polycrystalline phases. Typical AFM scans show that amorphous films are relatively flat with root-mean-square (rms) surface roughness 1 nm. For annealed and as-deposited polycrystalline samples rms surface roughness is in the range of 2-5 nm. Fig. A.1 shows the results of 1 μm and 10 μm AFM scans of a typical sample.

Scanning electron microscope (SEM) image of amorphous Germanium deposited on Silicon wafer is shown in Fig. A.2(a). The layer is very smooth and conformal. The film is crystallized by thermal annealing after which it was patterned by photolithography followed by dry etching. SEM images of the resulting mesas are shown in Fig. A.2(b) and (c). The Ge layer formed into grains and the surface roughness of the film has significantly increased. The average grain size is in the order of 100 nm.

SEM image of as-deposited polycrystalline films are shown in Fig. A.3. Similar to the re-crystallized case, the Ge layers exhibit granular structure with a rough surface. The grains, however, are formed in a columnar behavior as a consequence of the growth condition. The next section discusses the electrical properties of such films.



(a)



(b)

Fig. A.1 Typical (a) 10 µm and (b) 1 µm AFM surface scan of polycrystalline Ge layers grown on Si.

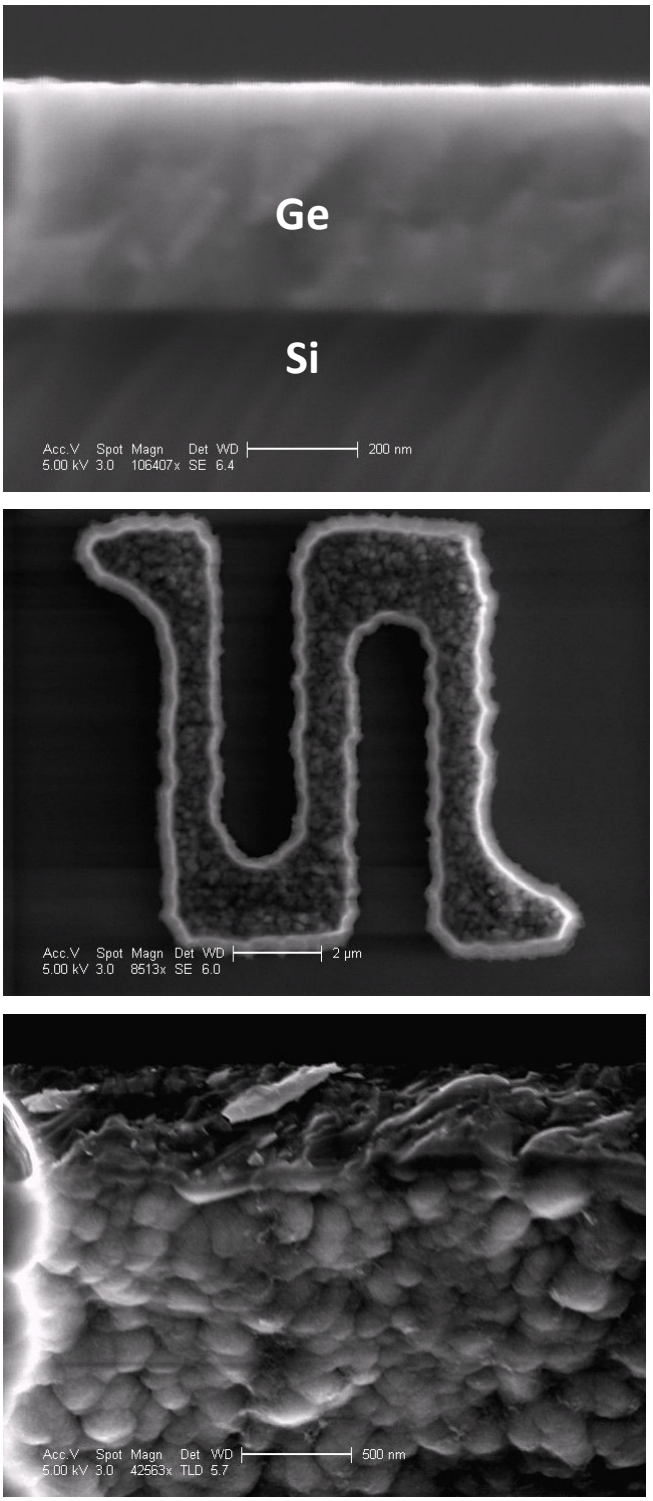
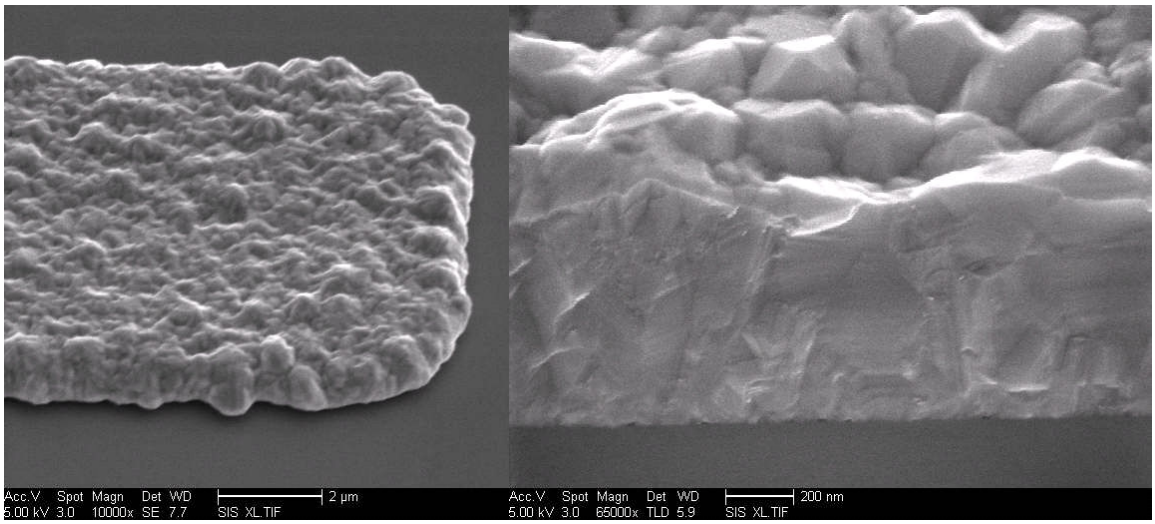
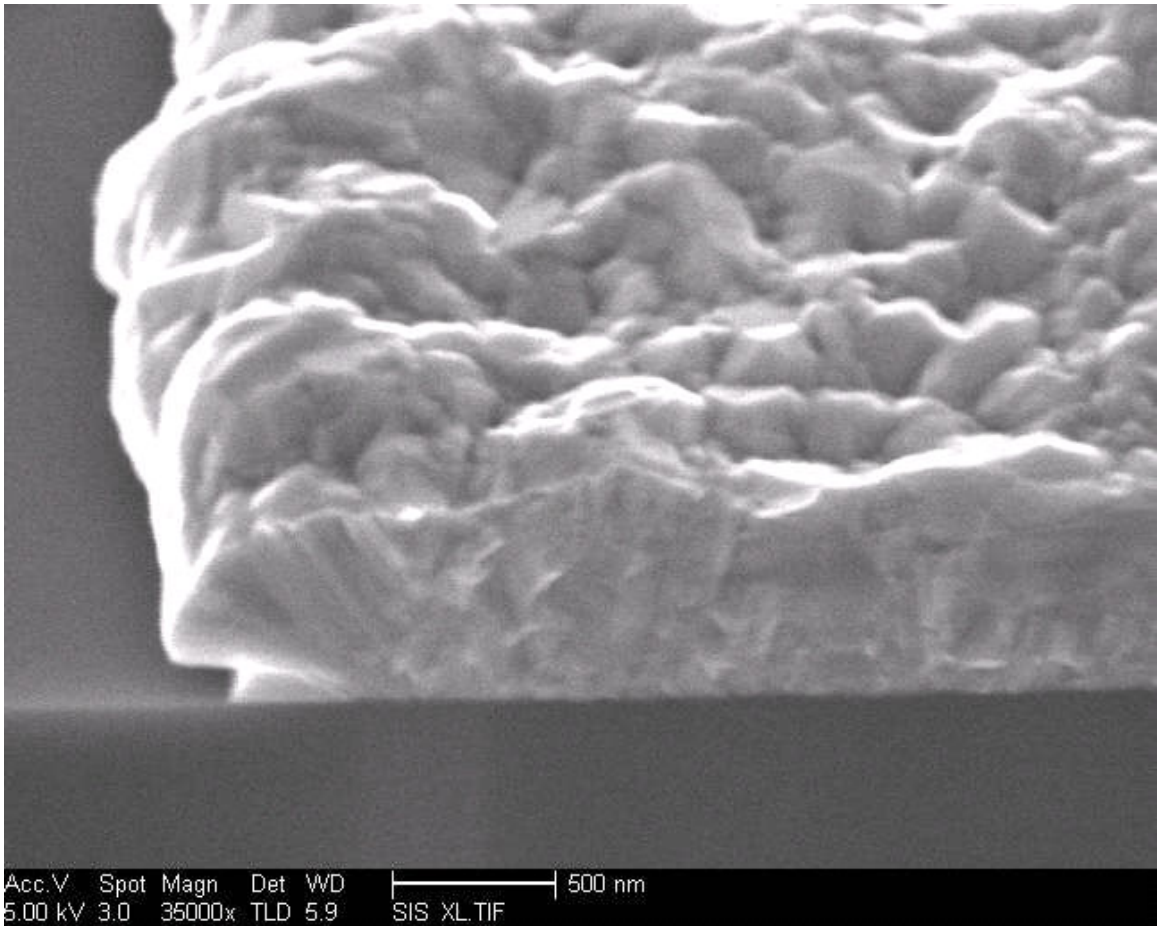


Fig. A.2 SEM images of (a) amorphous Ge film on Si (b) and (c) granular structure of the layer after thermal crystallization.



(a) **(b)**



(c)

Fig. A.3 SEM images of as-deposited polycrystalline Ge layers on Si.

A.3 ELECTRICAL CHARACTERIZATION

Interdigitated MSM photodetectors were fabricated on the deposited Ge layers using lift-off technique. The measured current-voltage characteristics from such detectors resulted in ohmic behavior. The polycrystalline Ge layers became simple resistors instead of diodes. The resistance of the films varies only slightly with changing deposition and post annealing conditions. There were no intentional impurities introduced during the growth or post annealing conditions. Four point probe measurements were used to determine the effective doping concentration of the films. The results show that the deposited layers behave p-type with an effective doping concentration around 10^{18} cm^{-3}. This is similar to that observed by [1-3] and was explained by the electrically active grain boundaries in the polycrystalline Ge films. Due to this high electrical concentration, the films became highly conductive causing an intolerably high dark current for photodetector purposes.

A.4 SI CAP

A Silicon capping layer was deposited followed by the deposition of Ge to circumvent the high dark current associated with the grain boundary conduction. Fig. A.4 shows an SEM image of such a stack of layers. Electrical measurements showed improvement in the electrical characteristic of the device showing reduced leakage. For our purposes, polycrystalline Ge based detectors did not show promise. Single crystal Ge based photodetectors using direct epitaxial growth as described in Chapter 4 were pursued.

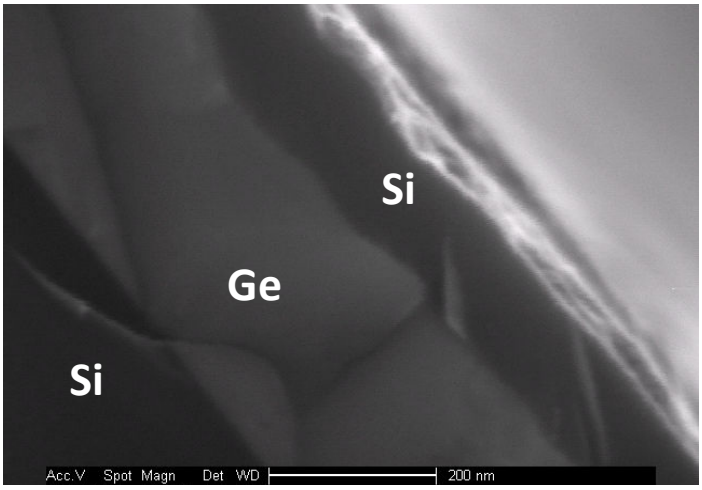


Fig. A.4 SEM image of a Si cap layer on polycrystalline Ge film deposited on Si.

A.5 SUMMARY

In conclusion, polycrystalline Ge layers can be obtained by LPCVD directly on Si or SiO_2. However, these films have high surface roughness. Photodetectors fabricated on such layers exhibit ohmic behavior with high dark currents. This is attributed to very high electrical activity of the grain boundaries. A mechanism that can passivate the grain boundaries can be extremely useful to eliminate this problem and pave the way for decent photodetectors on such layers.

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APPENDIX B: A TYPICAL MHAH RECIPE

Everything should be made as simple as possible, but not simpler.
Albert Einstein

In this appendix, the growth conditions of the MHAH technique are provided in a typical recipe.

Step No	Step name	Time	Center	Dep/ Vent	N2H2	Rot	HClHi	HCl	SiH_4	GeH_4	P
1	START	0.1	1170	VENT	20H	0	0V	0V	0	0	ATM
2	HEAT 1	30	1170	VENT	10HR	25RU	0V	0V	0	0	ATM
3	HEAT 2	45	1170	VENT	10H	25U	20ER	0V	0	0	ATM
4	ETCH1	10	1170	VENT	10H	25U	20E	0V	0	0	ATM
5	ETCH2	30	1170	VENT	80HR	25D	20E	500E	0	0	ATM
6	ETCH3	45	1170	VENT	80H	25D	20E	500E	0	0	ATM
7	COOL	60	800	VENT	80H	10RD	0V	0V	0	0	ATM
8	HOMESUS	60	800	VENT	40HR	0	0V	0V	0	0	ATM
9	TEMP CK	0.1	850S	VENT	20H	0	0V	0V	0	0	ATM
10	LOAD	0.1	800	VENT	10H	0	0V	0V	0	0	ATM
11	RAMP	0.1	950S	VENT	42H	35R	0V	0V	0	0	ATM
12	BAKE	30:00	950	VENT	50HR	*SAME	0V	0V	0	0	80
13	TEMP CK	300	432S	VENT	22H	*SAME	0V	0V	0	0	80
14	STABDEP	90	432	VENT	22H	*SAME	0V	0V	0	30	10
15	DEPOSIT	15:00	432	DEPOSIT	22H	*SAME	0V	0V	0	30	10
16	TEMP CK	300	800S	VENT	22H	*SAME	0V	0V	0	0	80R
17	BAKE	60:00	800	VENT	50HR	*SAME	0V	0V	0	0	80
18	TEMP	300	432S	VENT	22H	*SAME	0V	0V	0	0	80
19	STAB	90	432S	VENT	22H	*SAME	0V	0V	0	30	10
20	DEPOSIT	15:00	432	DEPOSIT	22H	*SAME	0V	0V	0	30	10
21	TEMP	300	800S	VENT	22H	*SAME	0V	0V	0	0	80R
22	BAKE	60:00	800	VENT	50HR	*SAME	0V	0V	0	0	80
23	TEMP	300	462S	VENT	22H	*SAME	0V	0V	0	0	80
24	STAB	90	462	VENT	22H	*SAME	0V	0V	0	30	10
25	DEPOSIT	15:00	462	DEPOSIT	22H	*SAME	0V	0V	0	30	10
26	TEMP	300	800S	VENT	22H	*SAME	0V	0V	0	0	80R
27	BAKE	60:00	800	VENT	50HR	*SAME	0V	0V	0	0	80

28	TEMP	300	502S	VENT	22H	*SAME	0V	0V	0	0	80
29	STAB	90	502	VENT	22H	*SAME	0V	0V	0	30	10
30	DEPOSIT	15:00	502	DEPOSIT	22H	*SAME	0V	0V	0	30	10
31	TEMP	300	800S	VENT	22H	*SAME	0V	0V	0	0	80R
32	BAKE	60:00	800	VENT	50HR	*SAME	0V	0V	0	0	80R
33	POSTPRG	45	800	VENT	20H	10R	0V	0V	0	0	ATM
34	HOMESUS	15	800	VENT	10HR	0	0V	0V	0	0	ATM
35	UNLOAD	0.1	795	VENT	10H	0	0V	0V	0	0	ATM
36	TMP RMP	30	800	VENT	20H		0V	0V	0	0	ATM
37	END	1	800	VENT	20H		0V	0V	0	0	ATM

Table B.1 Typical MHAH recipe.