Error-Free Operation of an All-Silicon Waveguide Photodiode at 1.9 μm

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***Abstract*— Error-free detection at 1 Gb/s is experimentally demonstrated with an all-Si ion-implanted p-i-n waveguide photodetector operating at 1.9 μm, and the receiver sensitivity is measured. The responsivity of the device is compared between operation at 1.9 and 1.55 μm, and a 5 dB drop in responsivity is observed. Simulations show that nearly 25% of this drop is due to the lower confinement of the 1.9 μm wavelength. Theoretical analysis of the waveguide structure optimized for operation at 1.9 μm shows that data rates of 10 Gb/s are possible with a loss in sensitivity of only 3 dB compared with operation at 1.55 μm.**

***Index Terms*— Optoelectronic devices, optical receivers, photodiodes, silicon.**

I. Introduction

HIGH-TRAFFIC networks and telecommunication systems requiring increased optical-link capacity have propelled the search for ways to increase link aggregate bandwidth. Techniques utilizing advanced modulation formats, massive wavelength parallelism, and spatial parallelism have led to demonstrations exceeding 100 Tb/s [1]–[4]. A complementary approach for increasing bandwidth is to utilize wavelengths beyond the standard communications band [5]. Recently, a 10 Gb/s data transmission rate at 1884 nm was demonstrated with Si photonics, opening up the possibility of telecom channels out to 2 μm [5]. However, these long-wavelength (>1.7 μm) signals pose an inherent challenge for on-chip detection due to the fact that they are beyond the band edge of Ge, the material most often used for integrated Si photonic receivers [6]. Bandgap engineering using super-lattices [7] and bonding of III-V materials [8] can achieve detection at these longer wavelengths, but require processing beyond standard Complementary Metal-Oxide-Semiconductor (CMOS) practices. An alternate approach for long-wavelength data reception beyond the U-band (1625 nm–1675 nm) is to utilize extrinsic photodectors (PDs), where sub-bandgap absorption in Si waveguides is induced *via* ion implantation. This additional fabrication step is fully compatible with standard CMOS technology [9].

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One structure that has shown promise is based on Si^+ ion implanted waveguide PDs with the primary defect responsible for absorption believed to be the Si interstitial cluster [10]. These devices have been shown to have absorption coefficients up to 20 dB/cm, bandwidths of >35 GHz, and internal quantum efficiencies (IQE) up to 0.8 A/W at 5 V for an operating wavelength at 1.55 μm [10]. Error-free data transmission of 10 Gb/s operating at 1.55 μm wavelength was recently demonstrated with performance comparable to that of Ge detectors [11]. Alternatively, these same devices can be operated utilizing absorption from the Si-divacancy defect, caused by the dislocation of lattice atoms during ion implantation [9], [12], [13]. Each of these two devices (interstitial and divacancy) have different post-implantation maximum processing temperatures. The interstitial devices are processed at 475 °C or higher, whereas the divacancy devices are processed at below 300 °C [12]. Although the IQE of the divacancy defect is lower (0.2 A/W at 5V [9] compared to 0.5–0.8 A/W for interstitial clusters [9], [10]), it has a waveguide absorption coefficient ranging from 100 to 200 dB/cm [9], [12], [13]. The increase in absorption offsets the lower quantum efficiency and affords for shorter devices, resulting in higher responsivities for devices of >250 μm in length. In the original research from Fan and Ramdas on deuteron-irradiated Si, a peak in absorption around 1.8 μm was observed for Si divacancy defects [14]. Thus by utilizing devices implanted with Si ions and processed at temperatures below 300 °C, detection and data transmission can be achieved at wavelengths up to 1.9 μm [15].

In this letter, we demonstrate error-free operation (Bit Error Rate (BER) $<10^{-9}$) of a 2-mm-long Si^+ ion implanted waveguide PD with 1 Gb/s data rates at 1.9 μm. The sensitivity of this divacancy device is calculated from the measured data; the responsivity is measured and compared to operation at 1.55 μm. The device structure is then optimized using Finite Element Method (FEM) analysis and compared to previous devices based on the interstitial clusters. Theoretical analysis suggests operation at 10 Gb/s is possible with only a 3 dB loss in sensitivity compared to operation at 1.55 μm. To the best of our knowledge, this is the first systems-level demonstration of a monolithic Si waveguide PD operating at wavelengths beyond 1.8 μm.

II. Measurements and Results

A. Experimental Setup

The Si^+ implanted Si waveguide *p-i-n* PDs were fabricated on the CMOS line at MIT Lincoln Laboratory, as described

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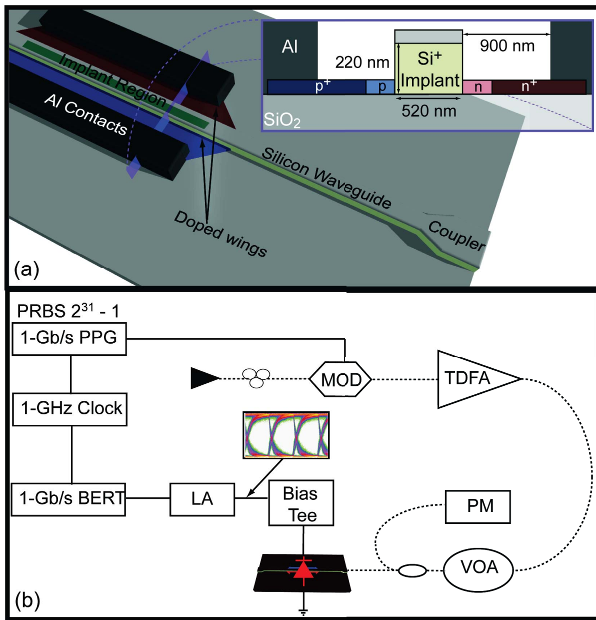

Fig. 1. (a) Device cartoon indicating waveguide, contacts, wings, implant region, and adiabatically tapered coupler, with inset giving cross-sectional dimensions. The waveguide implant region is doped with a dose of 10^{13} cm^{-2} Si^{+} ions. The "wings" are 50 nm high with the heavily doped regions concentration of 10^{19} cm^{-3} and lower doped regions concentration of 10^{18} cm^{-3}. The contacts are formed with deposited Al and a 10 nm Ti adhesion layer. (b) Experimental setup for measuring BER, with solid lines representing electrical connections, and dashed lines representing fiber.

in [11], with dimensions given in Fig. 1(a) and a Si^{+} implantation energy of 195 keV. As shown in Fig. 1(b), 1 Gb/s non-return-to-zero (NRZ) data is generated by a pulse pattern generator (PPG), and used to drive a $LiNbO_3$ modulator, which imparts the signal onto a 1.9 μm carrier. The modulated optical signal is then sent to a thulium-doped fiber amplifier (TDFA), and a variable optical attenuator (VOA) is used to control the power being launched on-chip for BER measurements. A 1% power tap after the VOA diverts a portion of the signal to an optical power meter (PM) for input-power monitoring. The optical signal from the VOA is coupled to the waveguide fan-out taper shown in Fig. 1(a). The PD is contacted with electrical probes rated for 40 GHz operation, and a bias tee is used to apply a DC bias. The electrical data signal is connected to a Limiting Amplifier (LA) and sent to either a bit-error-rate tester (BERT) or digital communications analyzer (DCA) for eye diagram measurements [Fig. 2(a) inset]. A C-V analyzer (not shown) is used to measure PD capacitances.

B. Results

The Si^{+} implanted Si waveguide receiver sensitivity curve for a 2 mm PD is shown in Fig. 2(a) at a 25 V reverse bias, with the power shown giving the off-chip launched power measured using a 1/99 tap. Total input and output facet loss is measured to be 27 dB utilizing transmission tests through straight waveguides at 1.55 μm. Photocurrent is then measured after alternating the side of the input. Since the measured difference in photocurrent is less than 1 dB, the loss from each facet is taken to be equivalent, resulting in an $\approx$13.5 dB facet loss. An additional 3 dB of loss is assumed due to an on-chip power splitter prior to the PD.

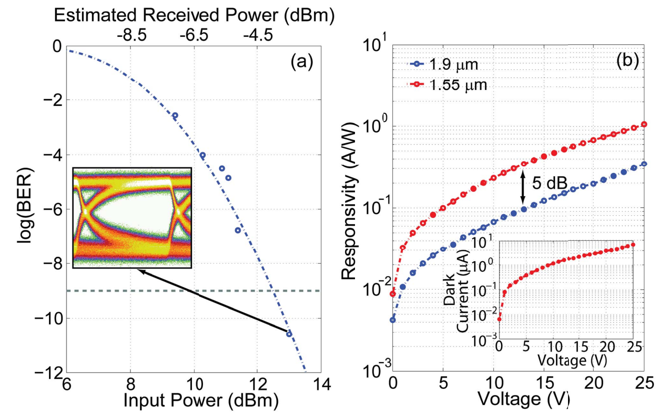

Fig. 2. (a) Sensitivity curve for a 2 mm-long PD operating with a 25 V reverse bias at 1 Gb/s. Input power shown is the input power prior to coupling into chip. The received power is 16.5 dB down due to coupling and on-chip power splitter losses. (Inset) Eye diagram for a 13.5 dBm input power. Eye is clearly open both horizontally and vertically corresponding to error-free operation. (b) Calculated responsivity versus voltage based on measured coupling loss, splitter loss, and 100% absorption. A $\approx$5 dB penalty was seen between 1.9 μm and 1.55 μm operation. (Inset) Dark current vs reverse bias for device.

Error-free operation is demonstrated at 1 Gb/s for the 2 mm device at a 25 V bias. The 25 V reverse bias provides enough current gain to drive the LA, overcoming significant optical losses of the non-optimized device. It is believed the device is operating in avalanche mode at this high bias similar to devices in [12]. The measured data is fit with a complimentary error function using nonlinear least-squares curve fitting, in order to attain a sensitivity estimate for the device [16]. Sensitivity is measured to be 12.4 dB for the 2 mm PD. The eye diagram measured prior to the LA for an error-free case is inset in Fig. 2(a), and shows data rate is limited by frequency response. Measured dark current (inset of Fig. 2(b)) is nearly two orders of magnitude less than the photocurrent, having negligible impact on device sensitivity.

Responsivity at both 1.9 μm and 1.55 μm is measured and shown in Fig. 2(b). The photodetector operation at 1.9 μm shows an $\approx$5 dB loss in responsivity throughout the reverse bias range measured. Improved on-chip performance can be achieved by redesigning the waveguide and photodiode for operation at 1.9 μm instead of 1.55 μm.

III. Discussion

A. Responsivity

In [14] the divacancy defect showed peak absorption strength at 1.8 μm with a measured absorption coefficient at 1.9 μm averaging 1.75 dB higher compared to that at 1.55 μm for both implanted doses of deuterium. Based on previous measurements of the absorption coefficient at 1.55 μm being $\approx$100 dB/cm [11], the absorption coefficient at 1.9 μm is assumed to be $\approx$145 dB/cm. With $>99\%$ of the power absorbed in the 2 mm device at 1.55 μm and 1.9 μm, the measured responsivity at 1.9 μm is expected to be equivalent to the responsivity at 1.55 μm, assuming that all other parameters are equal. To account for the difference between measured and expected responsivity values, Finite Element Method (FEM) analysis is utilized to determine the confinement factor, Γ, and the parasitic loss per unit length, α_{pl},

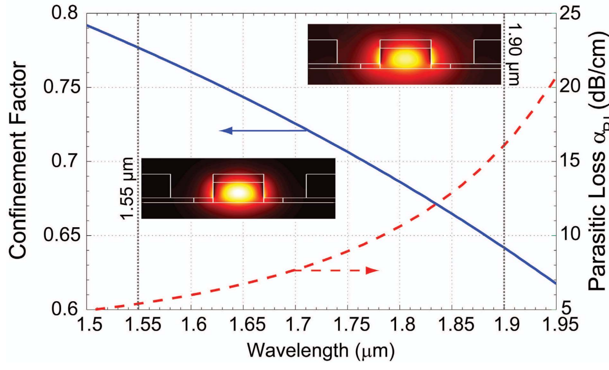

Fig. 3. Confinement factor (red - dashed) and parasitic loss (blue) as a function of wavelength. Insets show guided mode at 1.55 μm and 1.9 μm.

as a function of wavelength for the PD with dimensions as given in inset of Fig. 1(a). Free-carrier effects in the wings of the device are modeled using data from [17]. The Sellmeier coefficients [18] are used for the intrinsic-Si regions and for the buried oxide and SiO_2 cover layers; the coefficients for the Al contacts are from [19]. The calculated Γ and α_{pl} are plotted as a function of wavelength in Fig. 3.

The calculated α_{pl} at 1.55 μm is found to be 5.5 dB/cm, matching well with previous measurements of 8 dB/cm [10] for the same PD structure. The parasitic loss is increased significantly as Γ is decreased due to the increased overlap of the field with the doped wings. This increase in overlap results in an α_{pl} at 1.9 μm of 16 dB/cm as Γ decreased to 0.637.

The responsivity, $\Re$, is calculated assuming $> 99\%$ absorption and using the expression

$$\Re = \Gamma \cdot \zeta \cdot \alpha_{abs}/(\alpha_{abs} + \alpha_{pl}) \quad (1)$$

where ζ is the IQE, and α_{abs} is the absorption coefficient. The ratio between α_{abs} and α_{pl} is considered separate from IQE to account for the percentage of power absorbed versus loss due to varying α_{pl}. The increase in α_{pl} and decrease in Γ leads to a calculated loss in photocurrent between 1.9 μm and 1.55 μm accounts for nearly 25% of the measured difference.

The change in facet loss between the Lensed Tapered Fiber (LTF) and the waveguide fan-out taper is estimated by computing the overlap integral of the LTF with the coupler modes. The mode from the LTF is estimated utilizing a Gaussian profile with the manufacturer specified spot size at 1.55 μm of 2.5 μm [20]. The mode profile at 1.9 μm is estimated to be approximately 20% larger, matching closely with the change in mode profile in the coupler and resulting in an estimated change in coupled power of less than 0.5 dB.

The remaining difference between the theoretical and measured responsivity at 1.9 μm is either from a change in IQE at 1.9 μm compared to 1.55 μm, or due to a wavelength dependent change in the absorption coefficient under thermal annealing.

To optimize the design of the PD for operation at 1.9 μm, FEM analysis is used to examine both the confinement factor and parasitic loss as a function of waveguide height and width. Utilizing the calculated terms, the responsivity, $\Re = \Gamma \cdot \zeta \cdot \alpha_{abs}/(\alpha_{abs} + \alpha_{pl}) \cdot e^{-(\alpha_{abs}+\alpha_{pl})\cdot L}$, is maximized. A PD length of 250 μm is assumed, allowing direct comparison to the interstitial-based PD previously demonstrated for a 10 Gb/s data rate in [11]. Fig. 4 shows the surface plot of the calculated responsivity at 5 V as a function of waveguide width and height for an assumed device length of 250 μm. The maximum responsivity of 38 mA/W is generated by a device that is 0.66 μm wide by 0.24 μm high and is within 3 dB of the calculated responsivity of 72 mA/W for the tested device at 1.55 μm. Further, this 1.9 μm divacancy device compares well with calculated responsivity of between 54 to 86 mA/W at 1.55 μm of the 250 μm interstitial device in [11], based on the measured absorption coefficient and IQE [10].

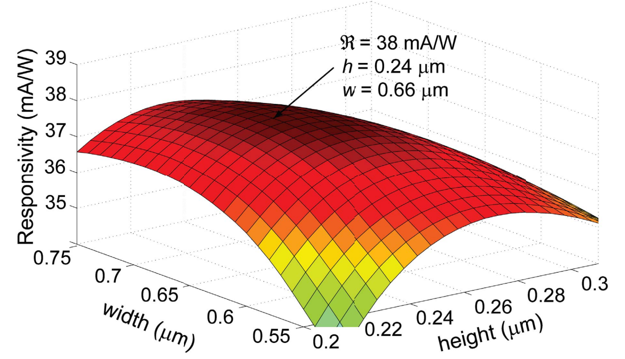

Fig. 4. Responsivity at 1.9 μm as a function of both height and width. A peak is reached for a height of 0.24 μm and a width of 0.66 μm. Expected responsivity for this device at 1.55 μm is 72 mA/W and for an interstitial device is between 54 to 86 mA/W.

B. Frequency Response

To determine the impact of optimizing the waveguide structure for operation at 1.9 μm, the individual frequency response components of the device are analyzed, focusing on carrier-transit time, optical-transit time, and device capacitance. The total frequency response of the PD is then calculated from:

$$f_{tot}^{-2} = (f_{transit}^{-2} + f_{optical}^{-2} + f_{RC}^{-2}).$$

A commercial simulation package (LaserMod [21]) is used to solve Poisson's equation and the Boltzmann transport equations for the given and optimized device structures to estimate carrier-transit time. A 0.2 ps Gaussian pulse is used to simulate the PD impulse response. The resultant current pulse is then Fourier transformed to get the estimated carrier-transit frequency response. The carrier-transit frequency response, assuming velocity saturation, for the PD with dimensions in Fig. 1(b) is calculated to be $\approx$100 GHz, matching well with previously calculated values of 95 GHz [10]. The response dropped to $\approx$78 GHz for the optimized device due to the increased aggregate transit length. Although this value is not insignificant, its impact on overall PD frequency response is shown to be minimal.

The frequency response for optical-transit time is based on device length, group velocity, and absorption coefficient, and

can be found utilizing the transfer function from [10]:

$$\frac{p(\omega)}{p(0)} = \frac{v_g^2\alpha^2}{F^2(\omega^2 + v_g^2\alpha^2)}\left[1-2(1-F)\times\cos\left[\frac{\omega\ln(1-F)}{v_g\alpha}\right] + (1-F)^2\right] \quad (2)$$

where $\omega = 2\pi f$, $\alpha =$ attenuation coefficient in cm^{-1} (including absorption and parasitic loss), v_g is the group velocity in cm/s, and F is the percentage of light absorbed by the guide. Group velocities are found through FEM analysis, with the optimized PD having a $v_g = 7.5 \cdot 10^9$ cm/s at 1.9 μm, and the tested PD having $v_g = 7.3 \cdot 10^9$ cm/s at 1.55 μm. The calculated optical-transit frequency response is 137 GHz for a 250 μm optimized PD operating at 1.9 μm and 131 GHz for a 250 μm PD with the dimensions given in Fig. 1(b) at 1.55 μm. For the interstitial device demonstrated in [11], the calculated optical-transit time is 129 GHz, with a slight decrease in frequency response due to the lower absorption coefficient. The slight differences across the devices have little impact on the final calculated frequency response below.

Frequency response due to capacitance is found based on a 50-Ω load, with the wing resistance assumed to be negligible. Capacitance is measured for several device lengths resulting in a capacitance versus length relation of $\approx$0.34 pF/mm. For the PD with width and height as tested and a length of 250 μm, the calculated frequency response is 37 GHz. To determine the impact of the optimized PD's width and height, capacitance is calculated for the diode by using LaserMod simulation software and for the contact structure and wings by using conformal mapping technique [22]. The calculated capacitance for the PD with dimensions as tested is found to be 0.27 pF/mm, matching within 20% of the measured values. Utilizing the same technique on the modified structure resulted in an approximate 4.5% decrease in capacitance. Decreasing the measured capacitance values by 4.5% results in an estimated frequency response of 39 GHz for the optimized PD dimensions.

The total frequency response for the optimized PD and the tested PD of 250 μm length is calculated to be 33.8 GHz and 33.5 GHz, respectively. The decrease in response due to an increase in transit time is offset by a slightly lower capacitance and slightly higher v_g.

IV. Conclusion

An all-Si ion-implanted waveguide PD has been demonstrated with 1 Gb/s error-free data reception at 1.9 μm. To the best of our knowledge, this is the first demonstration of a monolithic Si waveguide PD operating at wavelengths beyond 1.8 μm. Responsivity at 1.9 μm was found to be 5 dB less than at 1.55 μm, with nearly 25% of the penalty coming from an increase in parasitic loss and a decrease in modal confinement.

A theoretical analysis optimized the waveguide for operation at the longer wavelength. The modified PD was compared to a previously demonstrated interstitial-based PD, with the new structure showing near identical frequency response and a 3 dB penalty in responsivity. Based on this analysis, 10 Gb/s error-free data reception is theoretically achievable for this modified device operating with wavelengths from 1.55 μm to 1.9 μm and with an estimated loss in sensitivity at 1.9 μm of only 3 dB, enabling high-data-rate long-wavelength communications on-chip.

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