A New Family of Single-Stage Isolated Power-Factor Correctors with Fast Regulation of the Output Voltage

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Abstract - **A new family of single-stage isolated power-factor correctors features fast regulation of the output voltage, one or two power switches operated in unison, a single control loop, and automatic shaping of the line current. We give topologies, steady-state analysis, design considerations, and experimental results.**

I. INTRODUCTION

IEC 555-2 and several national standards require that the harmonics of the line current of an electronic equipment stay below certain specified levels. To meet the requirements, it is customary to add a power-factor corrector ahead of the isolated dc/dc converter section of the switching power supply. The electrical performance can be acceptable, but the power-factor corrector increases the size and cost of the power supply. In order to keep the size and cost increase within acceptable limits, designers have attempted to integrate the functions of power-factor correction and isolated dc/dc conversion into a single power stage (see, e.g. [1–7]). Unfortunately, all of the proposed solutions suffer from one or more of the following drawbacks:

- large low-frequency ripple at the output [1–2]
- slow regulation of the output voltage [1–2]
- complexity of the circuit topology [3]
- complexity of circuit operation [6]
- complexity of the control [2–7]
- large increase of the voltage across the storage capacitor at light load [4–5], [7]
- large energy stored in the leakage inductance [1–2], [4–5], [7]
- low exploitation of the power transformer due to transmission of pulsating power [1–2]
- low efficiency, due to i^2R losses associated with large circulating current [6]

The large increase of the storage-capacitor voltage can be eliminated by increasing the switching frequency at light load [7] but that causes other problems, e.g. reduced light-load efficiency and interfering with the distortion-reducing frequency modulation [4–5].

In this paper we introduce a new family of isolated power-factor-corrected switching power supplies, which is free from all of the above-listed drawbacks. The family name is Single-Stage Isolated Power-factor-corrected Power supply; its acronym is SSIPP or S^2IP^2. We present the topologies and operation of the S^2IP^2 family, the steady-state analysis, practical design considerations, and experimental results.

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II. TOPOLOGIES AND OPERATION

A. Topologies

The topologies of the members of the new family can be derived from the general structure shown in Figure 1.

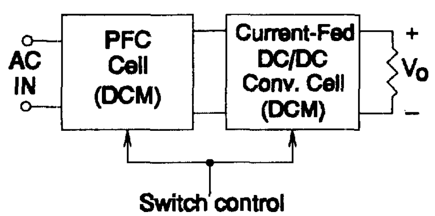

Figure 1. General structure of the new family of power-factor-corrected switching power supplies.

The power-factor-corrected switching power supply comprises a power-factor-corrector ("PFC") cell followed by a current-fed dc/dc converter cell. (In most practical applications the dc/dc converter cell is isolated.) Both cells operate in discontinuous mode ("DCM"). The controlled switches of both cells receive the same control signal, yielding economical control circuitry.

Figure 2 shows some of the practical PFC cells. Figure 3 shows some of the practical isolated current-fed dc/dc converter cells based on the buck-boost converter. Figure 4 shows some of the practical isolated current-fed dc/dc converter cells based on the buck converter.

In all figures in this paper we use the following conventions: flyback transformers (i.e. transformers with intentional energy storage) and inductors are drawn with a thick line representing the core; transformers for buck-derived converters (i.e. transformers without intentional energy storage) are drawn with a thin line representing the core; capacitors with significant low-frequency energy-storage capacity are drawn with polarity indication, and capacitors with negligible low-frequency energy-storage capacity are drawn without polarity indication. Also, for clarity, we do not show the reset and clamp circuits of the single-switch and two-switch flyback and forward converter cells.

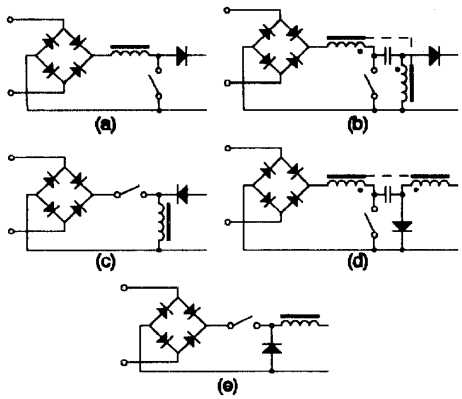

Figure 2. PFC cells: (a) boost, (b) SEPIC, (c) buck-boost, (d) Ćuk, (e) buck.

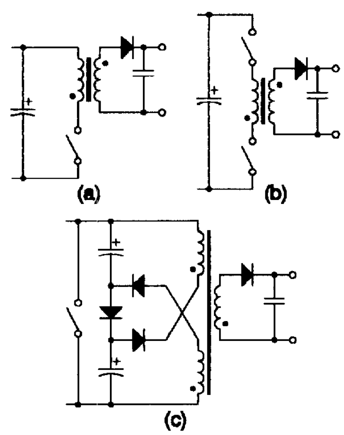

Figure 3. Current-fed isolated dc/dc converter cells based on the buck-boost converter: (a) single-switch flyback, (b) two-switch flyback, (c) series/parallel flyback.

Note that in our definition of the PFC cell the low-frequency energy-storage capacitor is not part of that cell; rather it is part of the cascade-connected current-fed dc/dc converter cell. Note also that with the exception of the "series/parallel" (the two energy-storage capacitors are charged in series and discharged in parallel) flyback or forward cells, all other dc/dc converter cells can be either current-fed or voltage-fed. The series/parallel cells can be fed only with current (e.g. with an inductor in series with the rectified line).

Figures 2b and 2d show the coupled-inductor versions of the SEPIC and Ćuk converters. Naturally, the versions with two independent inductors can also be considered; similarly other extensions of the PFC or dc/dc converter cells are conceivable (e.g. tapped inductors or the two-transformer versions of the series/parallel cells).

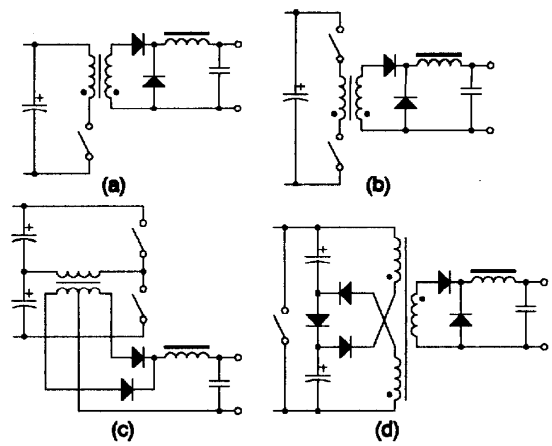

Figure 4. Current-fed isolated dc/dc converter cells based on the buck converter: (a) single-switch forward, (b) two-switch forward, (c) half-bridge, (d) series/parallel forward.

In several combinations of the PFC and dc/dc converter cells, the switch in the PFC cell is referenced to the same point as one of the switches in the dc/dc converter cell. Taking into account that the switches are controlled in unison, this makes it possible to combine them into a single switch, using one or two diodes if necessary, as shown in Figure 5. (No such diodes are needed if the off voltages of the two switches are equal.)

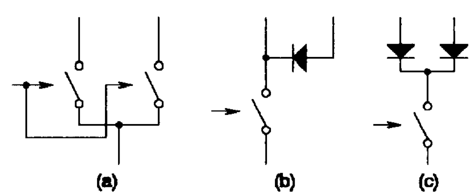

Figure 5. (a) Two switches with unison control and common reference point; (b) combination when the left switch always has a higher off voltage; (c) combination when the off voltage of the left switch can be lower or higher than that of the right switch.

Figure 6 shows how to combine the switch of a boost PFC cell with the switch of the series/parallel forward converter cell. As can be seen, the boost switch, the boost diode, and the switch of the series/parallel converter cell (inside the dashed box of Figure 6a) can be combined into a single switch (dashed box of Figure 6b).

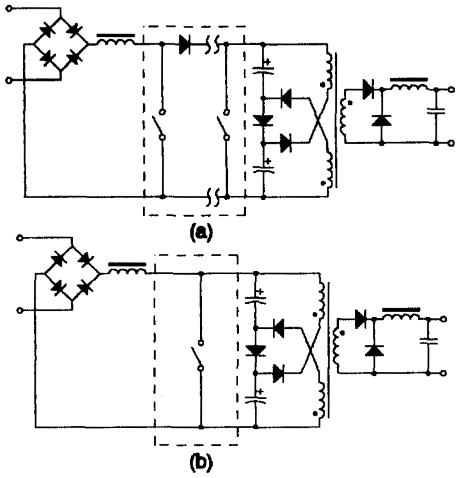

Figure 6. Combining the switches of the boost PFC cell and the series/parallel forward converter cell.

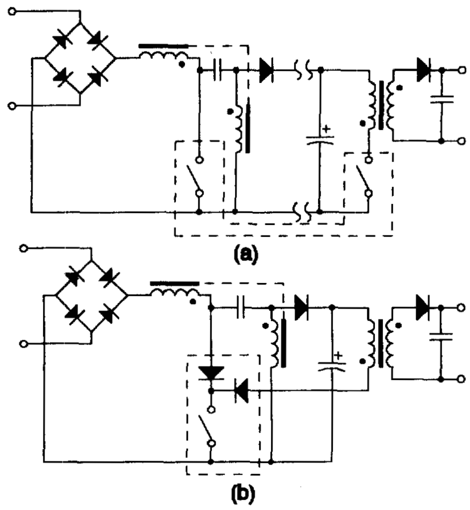

Figure 7. Combining the switches of the SEPIC PFC cell and the single-switch flyback converter cell.

Figure 7 shows the case when the SEPIC PFC cell is combined with a single-switch flyback cell. That combination is an example where the two ground-referenced switches can be combined only by using two diodes. The reason is that close to the zero-crossing of the ac-line voltage, the off voltage of the SEPIC switch is smaller than that of the flyback switch; but close to the peak of the line the SEPIC switch is likely to have a higher off voltage than the flyback switch.

Figure 8 shows some of the practical combinations of the boost PFC cell and various dc/dc converter cells. Similar combinations can be generated with all other PFC cells shown in Figure 2.

It is interesting to note that the average current (averaged over a switching cycle) of all PFC and dc/dc converter cell combinations is continuous, except for the combinations of the buck PFC cell and those dc/dc converter cells where there is a storage capacitor (or two storage capacitors in series) directly in parallel with the input terminals of the dc/dc cell. (Those cells include the ones in Figures 3a, 3b, 4a, 4b, and 4c.) In those configurations, no current can flow in the ac line when the instantaneous line voltage is below the voltage across the storage capacitor(s). The two buck-PFC based circuits of Figure 9, however, have continuous (average) current down to zero instantaneous line voltage. ("Continuous average current" means that the average current, averaged over a switching cycle, is different from zero.)

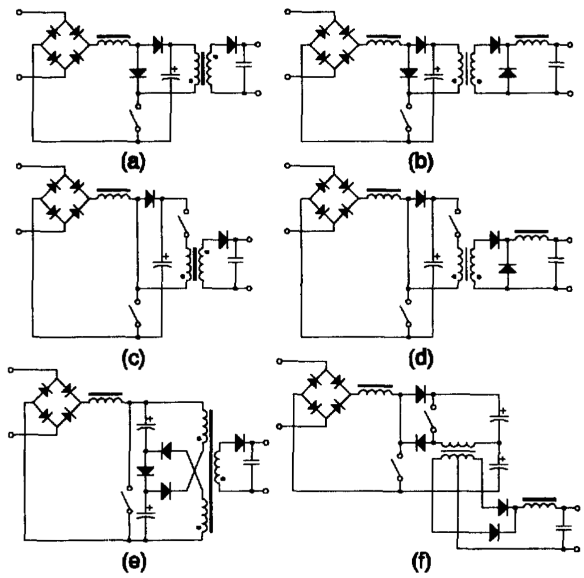

Figure 8. S^2IP^2 topologies based on the boost PFC cell.

B. Operation

Optimally, in all members of the S^2IP^2 family, both the PFC section and the dc/dc converter section operate in discontinuous conduction mode (DCM). In topologies where a section contains only one inductive energy-storage component, DC means that by the end of

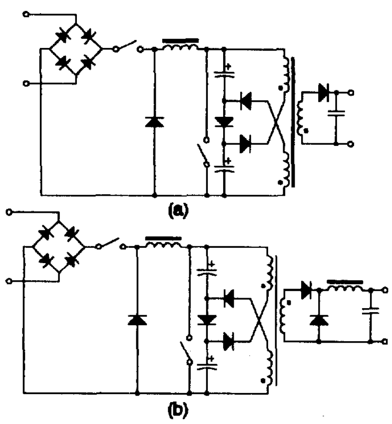

Figure 9. S^2IP^2 topologies combining a buck PFC and a series/parallel flyback (a) or forward (b) converter cell.

the switching cycle the inductor delivers all of its stored energy to the next stage or to the load. (All topologies shown in this paper, including topologies containing the coupled-inductor SEPIC and Ćuk PFC cells, have only one inductive energy-storage component per section.) In topologies where a section contains two inductive energy-storage components (e.g. the uncoupled-inductor versions of the SEPIC or Ćuk cells, not shown in the paper) DCM means that the free-wheeling diode of the cell stops conducting at some point within the switching cycle. That happens when the currents in the two inductors of the cell become equal.

All members of the S^2IP^2 family are controlled with a single fast control loop; that control loop keeps the output voltage constant by monitoring it and correcting it as needed, using some sort of pulse-width modulation. As in any ordinary switching regulator, the pulse-width modulation can be based on voltage-mode control or one of the several types of current-mode control (either constant-frequency or variable-frequency). If current-mode control is used, the inner current-controlling loop must be based on the current flowing in the dc/dc converter section of the S^2IP^2 cell because the current in the PFC section is fluctuating according to the instantaneous ac-line voltage. This means that it is not acceptable to monitor only the current of the switch that carries the currents of both sections. A signal corresponding to the current in the output section can be generated by using a current transformer in series with the primary winding of the power transformer or by sensing both the total switch current and the current in the PFC section and subtracting the PFC current signal from the switch current signal.

Operating both sections in DCM eliminates a major drawback of other single-stage isolated power-factor-corrected power supplies with fast regulation. Those power supplies [4–7] were designed for operation with continuous conduction mode (CCM) of the inductor in the dc/dc converter and DCM of the inductor in the PFC section. With that combination of operating modes, the voltage across the storage capacitor becomes a function of the load current. The physical explanation for that dependence is as follows. Assuming constant duty ratio, the charge, and also the energy, removed from the storage capacitor in a switching period is proportional to the load current. But the charge, and also the energy, transferred from the source to the storage capacitor in the same switching period remains constant. The energy unbalance between energy added to the capacitor (from the source) and withdrawn from the capacitor causes a change in the storage-capacitor voltage. At reduced load, the change is positive, and the capacitor voltage increases. The increasing voltage leads to a decrease in the switch duty ratio, via the feedback control loop. The end result at the lower load current is a new energy equilibrium, at an increased storage-capacitor voltage and reduced duty ratio. (Note: In power-factor-corrector applications, the energy equilibrium is valid only over a half-cycle of the ac-line voltage.) Simple mathematics shows that, as a first approximation, the storage-capacitor voltage depends on the load current as $1/\sqrt{I_{LOAD}}$. The large variation of voltage with load current has several undesirable effects, including reduced hold-up time at heavy load, reduction of the useful line-voltage range, and requirement for transistors, diodes, and capacitors with increased voltage rating.

By design, in the S^2IP^2 family both sections of the circuit operate in DCM. It is not necessarily harmful if the dc/dc converter section slips into CCM at, or close to, full load, but for reduced variation of the storage-capacitor voltage it is desirable that it does not move into deep CCM. DCM of both sections ensures an inherent energy balance at varying load, and the voltage across the storage capacitor becomes independent from the load current. The penalty to pay for DCM operation is only a slight increase in the conduction losses; the switching losses associated with hard turn-off of the output rectifier diodes are, however, eliminated.

III. ANALYSIS

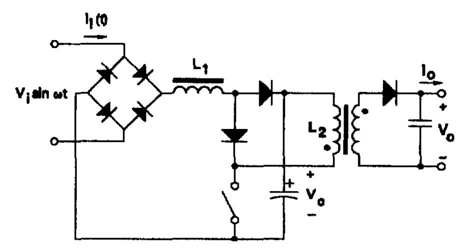

Figure 10. Boost/single-switch flyback combination circuit.

A. Steady-State Analysis

The steady-state analysis of the S^2IP^2 family is demonstrated on the circuit of Figure 10: a boost PFC circuit combined with a single-switch flyback dc/dc converter. One of the essential quantities of the circuit is the voltage V_c across the storage capacitor. That voltage can be determined by equating the energy absorbed from the ac line during a line half-cycle with the energy delivered to the load during the same half-cycle. The energy equality can be written as follows:

$$\int_0^{T/2} v_i(t)\, i_i(t)\, dt = \frac{T}{2} V_o I_o \qquad (1)$$

where T is the line period and V_o and I_o are the output dc voltage and current. Substituting the circuit parameters and the time function of the line voltage, we obtain the following equation for the voltage V_c:

$$\frac{2}{T}\,\frac{V_i^2}{V_c}\,\frac{L_2}{L_1}\int_0^{T/2}\frac{\sin\omega t}{V_c - V_i\sin\omega t}\,dt = 1 \tag{2}$$

where L_1 is the inductance of the boost inductor and L_2 is the inductance of the primary winding of the flyback transformer.

Equation (2) does not have a closed-form solution but it is easy to solve it numerically. Figure 11 shows the voltage V_c as a function of the rms line voltage, with L_1/L_2 as the parameter. It can be seen that the voltage across the storage capacitor increases with increasing line voltage and with decreasing ratio of the boost and flyback inductances. When the inductance ratio is 0.55, the voltage stays between 380 and 550 V over a line voltage range of 180 to 260 Vrms. Note that the storage-capacitor voltage does not depend on the load current.

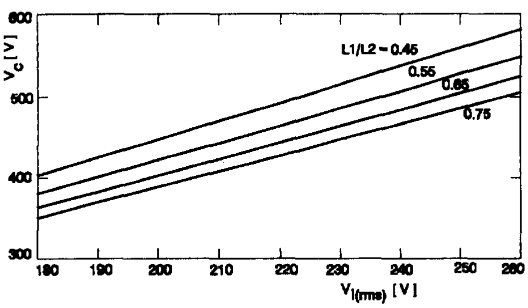

Figure 11. The voltage across the storage capacitor in function of the rms line voltage; parameter: ratio of boost and flyback inductances.

Figure 12 shows a period of the calculated averaged line-current waveform when $L_1/L_2 = 0.55$. (The line current is averaged by the high-frequency EMI filter not shown in the schematic in Figure 10). As can be seen, there is a discernible distortion in the current. In general, the distortion is a function of the ratio of the storage-capacitor voltage and the line voltage. The larger the voltage ratio, the smaller the distortion will be. Because the voltage ratio is a function of the inductance ratio, the distortion itself also becomes a function of the inductance ratio. Here we have a trade-off possibility: Low distortion can be achieved at the expense of the increased value of the voltage V_c, and vice versa.

The line-current harmonics and the total harmonic distortion can be determined using numerical Fourier transform. With an inductance ratio of 0.55, the calculated total harmonic distortion is about 20.9% and the ratio of the third harmonic to the fundamental of the line current is 20.8%, indicating that most of the distortion is due to the third-harmonic current.

As does the distortion, the power factor depends on only the ratio of L_1 and L_2. Table 1 shows the power factor as a function of the inductance ratio.

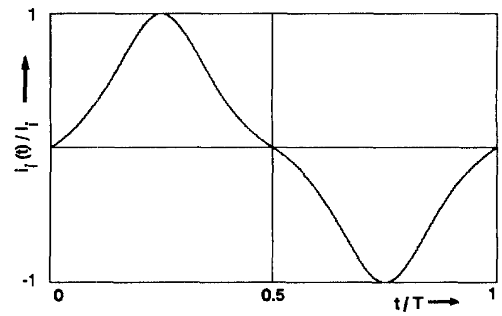

Figure 12. Line-current waveform when $L_1/L_2 = 0.55$.

TABLE 1.

POWER FACTOR AS A FUNCTION OF THE INDUCTANCE RATIO L_1/L_2

L_1/L_2	0.45	0.55	0.65	0.75
PF [%]	98.3	97.9	97.5	97

The rms current in the switch is calculated using the method given in [9]. The result is

$$I_{sw(rms)} = \sqrt{\frac{D^3T_s^2}{3}\left(\frac{V_i^2}{2L_1^2} + \frac{V_c^2}{2L_2^2} + \frac{4V_iV_c}{\pi L_1L_2}\right)} \tag{3}$$

where D is the switch conduction duty ratio and T_s is the switching period. The duty ratio can be determined from the storage-capacitor voltage, the inductance of the primary winding of the flyback transformer, the output power P, and the switching period. Its value is

$$D = \frac{1}{V_c}\sqrt{\frac{2L_2P}{T_s}} \tag{4}$$

Inserting (4) into (3) yields the switch rms current as a function of the storage-capacitor voltage and the output power. The value of the switch rms current can then be obtained by inserting values of the ac-line voltage and the corresponding storage-capacitor voltage from Figure 11.

Similar analyses can be carried out for all other members of the S^2IP^2 family. Note that the family members that incorporate the flyback, SEPIC, or Ćuk PFC cell, and also the combination of the buck PFC cell and the series/parallel flyback or forward dc/dc converter cell, theoretically produce zero distortion of the filtered ac-line current.

B. Small-Signal AC Analysis

The small-signal ac analysis of the members of the S^2IP^2 family can be carried out by considering the two sections (PFC and dc/dc) of the circuit as the cascade connection of two converters. The method of characteristic coefficients discussed in [10] is eminently suited for the analysis. In most practical applications, the two sections are essentially decoupled by the large energy-storage capacitor; for that reason, some of the transfer functions of the PFC section and the dc/dc converter section can be analyzed without needing of taking the influence of the other section into account. It is interesting to note that due to the instantaneous power balance that inherently exists in the system, the transfer function of control voltage to storage-capacitor voltage is zero; that means that a change in the control voltage will not change the storage-capacitor voltage. (The power balance is instantaneous on the time scale of the ac-line half-cycle, but not on the time scale of the switching cycle.)

IV. DESIGN CONSIDERATIONS

A. Line-Current Distortion

The line-current distortion of the circuits with boost PFC section depends on the ratio of the voltage across the storage capacitor and the line rms (or peak) voltage. The voltage ratio, in turn, depends on the ratio of the boost inductance and the inductance in the dc/dc converter section. A small inductance ratio yields a high voltage ratio and a filtered line current waveform that is of low distortion. Consequently, a direct trade-off exists between the distortion and the voltage across the storage capacitor.

Circuits with buck-boost, SEPIC, or Ćuk PFC cell (and also with buck PFC cell combined with series/parallel dc/dc-converter section) have theoretically zero line-current distortion, independent of the inductance ratio.

The buck PFC cell terminated with a dc/dc cell having a capacitor in parallel with its input terminals cannot draw current from the line when the instantaneous line voltage is below the storage-capacitor voltage. This leads to a large distortion.

B. EMI

Due to the DCM of the PFC cells, members of the S^2IP^2 family have a differential-mode EMI current that is somewhat larger than that of the boost power-factor corrector operating in CCM. Depending on the design, the typical difference is in the range of 10 to 20 dB. S^2IP^2 circuits with SEPIC or Ćuk PFC cells are somewhat better than circuits with a boost PFC cell because current is flowing in the input inductor even in DCM. Circuits with buck-boost or buck PFC cells are somewhat worse than circuits with a boost PFC cell because of the lack of an inductor directly in series with the ac-line.

In principle, by coupling the two inductors of the SEPIC or Ćuk PFC cells, complete ripple-current cancellation could be achieved. Unfortunately, in practice it is not easy to reduce the ripple current significantly by coupling the inductors, because of the effect of the large ac voltage across the coupling capacitor [11]. That ac voltage is applied directly across the leakage inductance of the coupled-inductor structure and generates an extra ripple current. Another problem with the coupled-inductor scheme is the high-Q resonance between the leakage inductance and the coupling capacitance. That resonance injects a large amount of current in the ac line at the resonant frequency. To control the resonance, a series RC damping circuit must be connected in parallel with the coupling capacitor [11].

C. Start-Up

At start-up or at programming the output voltage from zero to a nominal voltage, the storage capacitor must be charged up from the peak value of the line voltage (at boost PFC cells) or from zero (at all other PFC cells) to the operating voltage. This means that an inherent delay of a few tens or hundreds of milliseconds is present in the system under those conditions.

D. Current-Mode Control and Overload Protection

The members of the S^2IP^2 family have two quasi-independent sections, with different currents flowing in them. In many cases, however, there is only one switch in the circuit. If current-mode control is used, only the current in the output (i.e. dc/dc-converter) section must be controlled, otherwise the system does not behave the way it is expected. Although during nominal operation or at overload it is not necessary to control the current of the input (PFC) section, it is still desirable to include a second current sensor that senses either the input current or the total switch current. The signal from the second current sensor provides an additional input to the overload protection circuit of the switch. The second current signal is used at start-up or at a surge in the line voltage.

E. Operation Over a Wide Line-Voltage Range

With the proposed operating mode of the S^2IP^2 family (DCM for both sections), the voltage across the storage capacitor becomes a proportional function of the line voltage. This means that the storage-capacitor voltage varies over a three-to-one range when the line voltage varies between 90 and 270 Vrms. It is straightforward to design the power supply to accommodate that variation. Reduced variation in the storage-capacitor voltage is achievable, however, if the ratio of the inductances of the PFC and dc/dc-converter sections is set according to the ac-line voltage. Satisfactory results can be achieved if we reduce the PFC inductance by a factor of four for 115-Vrms ac-line voltage operation. The simplest way to implement this is by placing two windings with equal numbers of turns on the PFC inductor and connecting the two windings in series at 230-Vrms line and in parallel at 115-Vrms line.

F. Leakage-Inductance Energy

Unlike several other single-stage isolated power-factor correctors [1–2], [4], [5], [7], members of the S^2IP^2 family do not need to handle a leakage inductance energy in excess of that customarily present in similar switching converters. Therefore the usual simple RCD or low-loss snubbers or clamps suffice.

G. Continuous Conduction Mode

The advantages of the S^2IP^2 family over other approaches are most explicit when both sections of the circuit operate in DCM. It is not harmful, however, to operate the power supply such that the dc/dc converter section works in CCM (assuming that the design has taken this into account). The main negative effect of CCM is a load-dependent variation of the storage-capacitor voltage.

H. Rectifier Diodes

In some circuits (e.g. in the circuits in Figures 6b, 8c, 8d, 8e, and 8f) the rectifier diodes in the bridge rectifier are turned off with the rather high *di/dt* that exists in the boost inductor during the decaying part of the current. In practical realizations, it might be necessary to place a high-frequency diode either in series with the boost inductor or in some other suitable current path.

V. EXPERIMENTAL RESULTS

Two experimental 100-W (50-V/2-A) circuits have been built and tested to verify the theoretically predicted behavior. The first circuit is a single-switch boost/flyback combination (Figures 8a and 10), the second is a single-switch coupled-inductor SEPIC/flyback combination (Figure 7b). Both circuits are modifications of an existing switching power supply and were not optimized for 230-Vrms operation. Therefore, for safety, the ac-line voltage was reduced to about 180 Vrms throughout the experiments. The L_1/L_2 inductance ratio of the boost/flyback circuit is 0.6, the inductance ratio of the SEPIC/flyback circuit is unity. Both circuits are controlled with a UC3843 IC, using peak-current control in the flyback section; the switching frequency is 100 kHz.

Figure 13 shows the filtered line current of the boost/flyback circuit at full load. As can be seen, the waveform is very close to the predicted waveform in Figure 12.

Figure 14 shows the transient response of the line current (top trace) of the same circuit to a step change in the load current from 25 to 100% and back. (Note: The bottom trace is the control signal for the load switch.) Clearly, the line current resumes the required new value without noticeable delay.

Figure 15 shows the line current (top trace) and the voltage across the storage capacitor (bottom trace) when the load changes from 25% to 100% and back. The only effect of the increased load on the voltage of the storage capacitor is an increase in the ripple voltage.

Figure 16 shows the response of the output voltage (top trace) of the circuit to a step change in the load current from 100% to 25% and back. (The bottom trace is the control signal for the load switch.) The response is very fast because it is determined solely by the dc/dc converter section with its wide-band voltage-regulating loop.

Figure 17 shows the filtered line current of the SEPIC/flyback circuit. As expected, the waveform is nearly ideally sinusoidal with very little distortion.

Figure 18 shows the transient response of the line current (top trace) of the SEPIC/flyback circuit to a step change in the load current from 25 to 100% and back. (The bottom trace is the control signal for the load switch.) Similarly to the boost/flyback circuit, the line current resumes the new value without noticeable delay.

Figure 19 shows the response of the output voltage (top trace) of the SEPIC/flyback circuit to a step change in the load current from 25% to 100% and back. (The bottom trace is the control signal for the load switch.) Again, the response is very fast.

Figure 13. Filtered line current of the 100-W boost/flyback experimental circuit. Scales: 0.4 A/div., 5 ms/div.

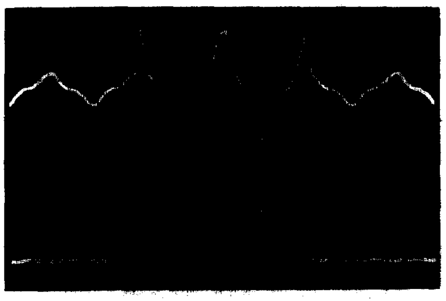

Figure 14. Transient response of the line current of the boost/flyback circuit to a step change in the load from 25% to 100% and back. Scales: 2 A p-p (top trace), 100 ms (full scale).

Figure 15. Transient response of the line current (top trace) and storage-capacitor voltage (bottom trace) of the boost/flyback circuit to a step change in the load from 25% to 100% and back. Scales: 2 A p-p (top trace), 4 V p-p (bottom trace), 100 ms (full scale).

Figure 16. Transient response of the output voltage (top trace) of the boost/flyback circuit to a step change in the load from 100% to 25% and back. Scales: 0.2 V/div. (top trace), 1ms/div.

Figure 17. Filtered line current of the SEPIC/flyback experimental circuit. Scales: 0.4 A/div., 5 ms/div.

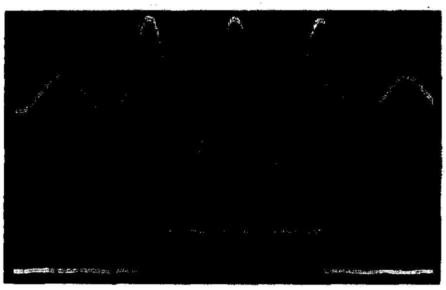

Figure 18. Transient response of the line current of the boost/flyback circuit to a step change in the load from 25% to 100% and back. Scales: 1.6 A p-p (top trace), 100 ms (full scale).

Figure 19. Transient response of the output voltage (top trace) of the SEPIC/flyback circuit to a step change in the load from 25% to 100% and back. Scales: 0.2 V/div. (top trace), 1ms/div.

VI. SUMMARY

In the paper we introduced a new family of single-stage isolated power-factor-corrected power supplies (S^2IP^2). The family members feature fast regulation of the output voltage, one or two power switches controlled in unison, a single PWM control loop, and automatic shaping of the line current. When the inductors of the S^2IP^2 circuits operate in DCM (the preferred operating mode), the voltage of the storage capacitor becomes independent from the load. The S^2IP^2 family represents a low-cost alternative to the traditional two-stage PFC power supplies and is free from the disadvantages of other single-stage circuits. We presented topologies, steady-state analysis, and practical design considerations. Experimental waveforms taken from a boost/flyback circuit and a SEPIC/flyback circuit show excellent agreement with the theoretical predictions.

VII. LEGAL NOTICE

The technology described in this paper is the subject of a patent application by author Redl. His employer is willing to issue licenses for the use of this technology. Interested parties can contact Dr. Redl at the address given at the beginning of this paper.

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