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The Impact of Self-Heating and SiGe Strain Relaxed Buffer Thickness on the Analog Performance of Strained Si nMOSFETs

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Abstract- **The impact of the SiGe strain relaxed buffer (SRB) thickness on the analog performance of strained Si nMOSFETs is investigated. The negative drain conductance caused by self-heating at high power levels leads to negative self-gain which can cause anomalous circuit behavior like non-linear phase shifts. Using ac and dc measurements, it is shown that reducing the SRB thickness improves the analog design space and performance by minimizing self-heating. The range of terminal voltages that leverage positive self-gain in 0.1 µm strained Si MOSFETs fabricated on 425 nm SiGe SRBs is increased by over 100% compared with strained Si devices fabricated on conventional SiGe SRBs 4 µm thick. Strained Si nMOSFETs fabricated on thin SiGe SRBs also show 45% improvement in the self-gain compared with the Si control as well as 25% enhancement in the on-state performance compared with the strained Si nMOSFETs on the 4 µm SiGe SRB. The extracted thermal resistance is 50% lower in the strained Si device on the thin SiGe SRB corresponding to a 30% reduction in the temperature rise compared with the device fabricated on the 4 µm SiGe SRB. Comparisons between the maximum drain voltage for positive self-gain in the strained Si devices and the ITRS projections of supply voltage scaling show that reducing the SiGe SRB thickness would be necessary for future technology nodes.**

Index Terms- **Analog MOSFET, Self-heating, Silicon-Germanium, Strained Silicon, self-gain.**

I. INTRODUCTION

Tensile strained silicon (Si) enhances electron mobility by lifting the conduction band degeneracies, reducing carrier scattering and increasing the population of carriers in sub-bands with lower transverse effective mass [1]. Strained Si implemented in radio frequency complimentary metal oxide on semiconductor (RFCMOS) shows good prospects for mixed signal solutions. The epitaxial deposition of Si on silicon-germanium strain relaxed buffers (SiGe SRBs) generates biaxial tensile strain in the Si layer with a strain magnitude that is proportional to the degree of lattice mismatch. Manufacturing difficulties such as the production cost of graded buffers, process optimization, silicidation chemistry, yield and device issues such as germanium (Ge) out diffusion, oxide interface properties and self-heating, have made uniaxial (or process induced) strain preferable to biaxial strain. Uniaxial strain induced by silicon nitride (Si_3N_4) contact etch stop layers and source/drain silicon-germanium (SiGe) selective epitaxial growth have made inroads into industrial CMOS processes [2, 3]. The stress magnitude predicted by simulations of such devices is as high as 600 MPa [4]. This is less than what is obtainable on biaxial strained substrates, where stress magnitudes in excess of 1.4 GPa can be realised, corresponding to strained Si epitaxially grown on a $Si_{0.8}Ge_{0.2}$ SRB. Since much larger values of strain can be realized, it is worthwhile to investigate some of the challenges that arise from strained layer heteroepitaxy. This investigation addresses one such challenge, namely, self-heating and its impact on analog metal oxide on semiconductor field effect transistor (MOSFET) performance.

Self-heating arises from the lower thermal conductivity of SiGe relative to Si, which means that the MOSFET is less capable of dissipating heat as the channel current is increased since the channel is separated from the substrate by a low thermal conductivity SRB layer [5, 6]. The consequence is increased carrier scattering that lowers the drain current in saturation as the drain voltage is increased. This effect is more pronounced in short channel devices

where the power levels are higher. Self-heating is important in analog devices where the duty cycle is higher (the MOSFET is on for longer periods of time) and the drain conductance behaviour of the MOSFET is important because of its relationship with the output resistance and self-gain. Self-heating is most observable in the MOSFET output characteristics where the reduction in the drain current from its saturation magnitude is obvious as the drain voltage is increased. This amounts to a negative drain conductance which causes a negative self-gain and thus renders the circuit behaviour anomalous by causing non-linear operation and phase shift [7]. Simulations of the frequency response of high gain amplifiers using bipolar junction transistors showed that self-heating can cause serious errors in the small signal parameters and affect the compensation of such circuits [8]. Self-heating was reported to exacerbate current mismatch due to localized temperature differences which affect the performance of circuits such as current mirrors and digital-to-analog converters that strongly depend on current matching [9]. It was also shown that small signal amplifier characteristics displayed visible anomalies due to self-heating. Hence, circuit designers using strained Si technology on SiGe SRBs must be careful to ensure that the bias terminals of the MOSFET are such that the drain conductance is not negative. This implies limitations in the range of gate and drain voltages caused by the possibility of negative drain conductance.

Thin SiGe SRBs have been proposed as a method of reducing self-heating in strained Si MOSFETs [10, 11]. Conventional graded buffers have thicknesses that are normally on the order of one or several micrometers thick however literature shows that progress has been made on the reduction of buffer thicknesses. Some studies on thin SiGe SRB technology focus on materials growth and characterization [12-14] whereas others focus on self-heating in devices [10, 11, 15-21]. The introduction of point defects during the growth of the SRB has been demonstrated as a method of fabricating thin SiGe SRBs [13]. $Si_{0.6}Ge_{0.4}$ SRBs with thicknesses as low as 40 nm to 60 nm were achieved by MBE grown on Si substrates with

point defect supersaturation at low growth temperatures [14]. Thicknesses below 100 nm were achieved for SiGe SRBs with Ge percentages as high as 70% [13]. 500 nm thick $Si_{0.56}Ge_{0.44}$ SRBs prepared by low energy plasma enhanced chemical vapour deposition (PECVD) with acceptable defect density magnitudes were reported but were used in fabricating modulation doped field effect transistors (MODFETs) [20]. Olsen *et al* used 200 nm SiGe SRBs to demonstrate that some of the performance enhancement lost to self-heating at high terminal voltages in thick SRB devices can be recovered by scaling the buffer thickness [10]. Strained Si pMOSFETs on a 400 nm $Si_{0.8}Ge_{0.2}$ SRB were demonstrated by Lei *et al* [18] with on-state enhancements of 25%. Sawano *et al* achieved 100 nm SRB thickness with 17% Ge content and full relaxation using ion implantation [21].

There has been no reported investigation on the impact of SiGe SRB scaling on the analog performance of strained Si MOSFETs. This investigation for the first time shows the impact of self-heating on the analog performance of strained Si MOSFETs and how thin SiGe SRBs can be used to limit the deleterious nature of self-heating by relaxing the limitations imposed on the design space.

II. DEVICE FABRICATION

A Si control wafer, a wafer with strained Si grown on a conventional thick SiGe SRB and a wafer with strained Si on a thin SiGe SRB were co-processed. The device on the thick 4 μm SiGe SRB comprised a 2.5 μm graded buffer, a 1.5 μm constant composition $Si_{0.8}Ge_{0.2}$ layer and a 10 nm tensile strained Si layer. In the case of the thin SiGe SRB devices, a layer of SiGe:C was used to achieve high strain relaxation. The total thickness in the thin SRB was 425 nm. The MOSFETs underwent an identical MOSFET process fabrication flow. A 1.4 nm gate oxide was thermally grown followed by 100 nm pre-doped poly deposition. Next was gate definition, source/drain shallow implants, halo implants to control short channel effects,

sidewall spacer formation, source/drain deep implants, nickel silicidation and aluminum metallization. A variety of gate lengths were fabricated with 10 µm gate widths. Fig. 1 shows the cross-sectional TEM of the thin and thick SiGe strain relaxed.

III. ELECTRICAL RESULTS AND DISCUSSION

Using the split CV technique with series resistance correction [22], the effective mobility was extracted from 1 µm gate length devices. Fig. 2 shows the effective electron mobility as a function of the vertical effective field. The thin and thick SRB devices both exhibited 100% mobility enhancement compared with the Si control device. This result shows that the effective strain in the thin and thick SiGe SRB devices is equivalent and that buffer scaling has not adversely affected mobility enhancement.

A model was developed in [23] for small signal output admittance parameters in silicon-on-insulator (SOI) MOSFETs and was used to show the non-linear behaviour of CMOS inverters and cascode amplifiers with self-heating taken into account [7]. Using this model, the DC self-gain of the MOSFET can be expressed as

$$A_V = \frac{g_m}{g_{DS} + R_{TH}\theta I_{DS}} \quad (1)$$

where A_V is the self-gain, g_m is the transconductance, g_{DS} is the drain conductance, R_{TH} is the thermal resistance, θ is the temperature sensitivity of the mobility and I_{DS} is the drain current. From equation (1), it is apparent that a high R_{TH} will have a negative impact on the A_V of the MOSFET. Due to the lower thermal conductivity of SiGe, the thermal resistance of SiGe buffers is higher than that of Si and increases with the buffer thickness. Fig. 3 (a) and Fig. 3(b) shows the MOSFET A_V as a function of the drain voltage (V_{DS}) for the 1 µm and 0.1 µm

gate length Si control nMOSFET and the strained Si nMOSFETs on the thin and thick SiGe SRBs. Since future deep submicrometer technology nodes (0.022 µm and below) will have non-minimum length (NML) analog MOSFETs with gate lengths of about 0.1 µm designed for delivering high A_V, the results in Fig. 3(b) are representative of state-of-the-art devices and show that self-heating is an important factor in NML MOSFETs. It can be seen in Fig. 3(a) that the 1 µm gate length strained Si nMOSFETs have significant self-gain enhancement compared with the Si control device for V_{DS} less than 1 V. At V_{DS}= 0.5 V, the self-gain of the strained Si nMOSFETs is an order of magnitude higher than the Si control device. As V_{DS} is increased, the percentage enhancement in the self-gain is reduced particularly for the strained Si nMOSFET on the thick SiGe SRB where the self-gain becomes higher in Si. The reduction in the self-gain at high V_{DS} is due to self-heating and it can be seen from Fig. 3(a) that the effect is ameliorated in the strained Si nMOSFET on the thin SiGe SRB. The problem of negative self-gain is however not exhibited for the 1 µm gate length devices. Fig. 3(b) shows the same A_V vs. V_{DS} characteristics for the 0.1 µm gate length devices where a discontinuity can be observed in the characteristic of the thick SiGe SRB device at a V_{DS} of approximately 1 V. This discontinuity occurs when the denominator in (1) crosses the zero mark and the self-gain rises infinitely. It can be seen from Fig. 3(b) that the problem of the negative self-gain evident in the strained Si nMOSFETs on the thick SiGe SRB is eliminated in the thin SiGe SRB. In addition, the self-gain of the strained Si nMOSFETs on the thin SiGe SRB also shows up to 45% improvement compared with the bulk Si nMOSFET. The self-gain improvement in the strained Si nMOSFET on the thin SiGe SRB evident in Fig. 3 is due to improved on-state performance (higher g_m) while maintaining similar drain conductance (g_{DS}).

The problem of negative self-gain due to self-heating in the strained Si nMOSFET on the thick SiGe SRB imposes limits on the range (i.e. design space) of drain and gate voltages

(V_{GS} & V_{DS}) useable in analog circuits designed for high gain. To best illustrate the impact of the buffer thicknesses on the design space, two-dimensional contour plots are used as shown in Fig. 4a and Fig. 4b. Fig. 4a and Fig. 4b show the self-gain contours as functions of the V_{GS} and V_{DS} for the 0.1 μm strained Si nMOSFETs on the thick and thin SRB respectively. In Fig 4a, approximately 40% of the design space area is comprised of negative self-gain, which imposes very rigid limitations on the bias potentials available for delivering positive self-gain. Drain voltages above 1.1 V for all gate voltages yield negative self-gain with the strain Si nMOSFETs on the thick SiGe SRB. In Fig. 4b, the percentage area of the design space comprised of negative self-gain is reduced to 15% because the potentials that cause negative drain conductance are higher in magnitude thereby demonstrating the effectiveness of thin SiGe SRBs in reducing the impact of self-heating. Hence, reducing the buffer thickness from 4 μm to 425 nm reduces the percentage area of negative self-gain on the contour maps from 40% to 15%. These plots indicate that the use of thin SiGe SRBs relax the restrictions that self-heating imposes on the design space if normal analog circuit operation is to be ensured.

Self-heating also has a deleterious impact on the cut-off frequency of the device which is another important analog metric. The cut-off frequency of the MOSFET is proportional to the drain current and the transconductance. The performance enhancement in the drain current of the strained Si device, which is reduced by self-heating at higher power densities, can be recovered by thinning the SiGe buffer. The performance enhancement is dependent on the terminal voltages of the MOSFET since the self-heating is a function of the power levels. Fig. 5a shows the contour map of the performance enhancement in the 0.1 μm gate length strained Si device on the thick SiGe SRB compared with the Si control whereas Fig. 5b shows that of the strained Si nMOSFET on the thin SiGe SRB. Fig. 5a and Fig. 5b show that the area with performance enhancement is approximately 25% and 90% for the strained Si nMOSFETs on the thick and thin SiGe SRB respectively. In the strained Si

nMOSFET on the thick SiGe SRB, performance enhancement is evident only for small gate overdrives and drain voltages because of self-heating at high power levels. This shows that much of the performance enhancement lost to self-heating in the strained Si devices on the thick SRBs is recovered in the strained Si devices on the thin SRBs. This is important for high speed analog devices where the mobility enhancement due to strain can be manifested as higher cut-off and maximum oscillation frequencies.

AC conductance measurements have been performed on the strained Si devices so as to remove the effects of self-heating and extract the intrinsic device characteristics [24, 25]. The thermal resistance is also extracted from these measurements. The output characteristics derived from the AC conductance technique is shown in Fig. 6 where the reduction in the drain current characteristics due to self-heating has been removed by the high frequency measurements. Fig. 7 shows the self-gain for 0.1 μm and 1 μm gate length nMOSFETs using the high frequency (10 MHz) drain conductance measurements. Negative self-gain is absent in the 0.1 μm gate length strained Si nMOSFET on the thick SiGe SRB and the intrinsic performance of the device shows that the self-gain compared with Si control is improved by mobility enhancement due to strain. Since the device under real circuit operation will not be biased with a high frequency AC drain signal, the high frequency measurements of Fig. 6 and Fig. 7 show the potential performance if the challenge of self-heating is solved.

The impact of self-heating on the cut-off frequency is also ascertained by measuring the maximum cut-off frequencies, f_t^{MAX}, of the devices at DC and at 10 MHz at a drain voltage of 2 V. Fig. 8 shows the percentage enhancements in f_t^{MAX} for the strained Si devices on the thick and thin SiGe SRBs as functions of the gate length with and without self-heating. The percentage enhancement of f_t^{MAX} compared with the Si control extracted with self-heating present reduces from 30% at 1 μm to -15% at 0.1 μm in the thick SRB device and from 30% at 1 μm to 10% at 0.1 μm in the thin SRB device. This is expected since self-heating increases

as the gate length is reduced. By reducing the thickness of the SiGe SRB from 4 μm to 425 nm, 25% of the f_t^{MAX} enhancement lost to self-heating at 0.1 μm gate length is recovered thereby demonstrating the effectiveness of thinning the SiGe buffer. In the absence of self-heating, Fig. 8 shows that the percentage enhancement of f_t^{MAX} reduces from 30% at 1 μm to approximately 20% at 0.1 μm for both devices. Since 10% of the f_t^{MAX} enhancement is still lost with self-heating removed, other factors such as series resistance and mobility degradation (due to the higher channel doping in the strained Si devices) may be present.

The thermal resistance is a measure of the heat conduction efficiency and can be used to evaluate the amount of self-heating in the respective devices. The thermal resistances of the strained Si devices have been calculated using (2) below which is a semi-empirical MOSFET model with the temperature dependencies of the threshold voltage and effective mobility taken into account. It was first derived for SOI MOSFETs in [25] and later used for strained Si MOSFETs on SiGe SRBs in [11, 26].

$$g_{DS} = g_{DST} + (T - T_O)\left(\frac{1}{V_{DS}} + \frac{g_{DS}}{I_{DS}}\right)\left[\frac{\beta_O \chi V_{DSAT}(1+\lambda V_{DS})\left(\frac{T}{T_O}\right)^{-k}}{\left(1+\frac{V_{DSAT}}{LE_{SAT}}\right)} - \frac{kI_{DS}}{T} - \frac{I_{DS}V_{DSAT}}{LE_{SAT}+V_{DSAT}}\left\{\frac{0.8\exp\left(\frac{T}{600}\right)}{600\left[1+0.8\exp\left(\frac{T}{600}\right)\right]} - \frac{k}{T}\right\}\right] \quad (2)$$

where g_{DS} is the drain conductance at low frequencies, g_{DST} is the drain conductance at high frequencies, T_O is the ambient temperature, T is the device temperature, V_{DSAT} is the saturation drain voltage, λ is the channel length modulation factor, L is the MOSFET gate length, E_{SAT} is the critical electric field, χ is the temperature threshold coefficient, k is the mobility temperature exponent, β_O is the transconductance factor and V_{DS} is the drain voltage. The temperatures of the 0.1 μm gate length strained Si nMOSFETs are calculated in

(2) using measured values of the MOSFET parameters shown in table 1. The calculated temperatures are shown as functions of the DC power, which is calculated as $I_{DS}.V_{DS}$ for the 0.1 μm gate length strained Si nMOSFETs. Fig. 9 shows the rise in the device temperature as a function of the DC power level where the higher temperatures are evident in the strained Si nMOSFETs on the thick SiGe SRB. It is also observed that reducing the thickness of the SiGe SRB from 4 μm to 425 nm reduces the temperature rise in the device by 30% which is responsible for higher drive current and higher self-gain in the thin SiGe SRB device. The thermal resistance, which is calculated as $(T - T_O)(V_{DS}I_{DS})^{-1}$, is extracted from the slope of the line of best fit in Fig. 9. The thermal resistances of the 0.1 μm gate length strained Si nMOSFETs on the thick and thin SiGe SRB were 30.5 $K.mW^{-1}$ and 16.6 $K.mW^{-1}$ respectively. This amounts to approximately 50% reduction of the thermal resistance in the strained Si device on the thin SiGe SRB.

Due to the fact that heat dissipation in strained Si nMOSFETs is not only dependent on the thickness of the SiGe SRB, it is difficult to make comparisons of thermal resistances between devices that are not co-fabricated. The gate length has an impact on the thermal resistance. The thermal resistance is known to increase as the gate length is reduced because the smaller cross-sectional area of the MOSFET reduces the heat conduction efficiency to the Si substrate [27]. The strained layer thickness also affects the thermal resistance since the typical strained Si thickness is much lower than the room temperature phonon mean free path (200 nm to 300 nm at 300 K in Si) and phonon scattering at the Si/SiGe heterointerface will contribute to the thermal resistance [27]. Other parameters such as the source/drain extension and the sidewall spacer width will also affect the thermal resistance. The thermal resistance values calculated here are comparable to what has been published in literature for strained Si MOSFETs on SiGe SRBs [10, 26]. This reduction in thermal resistance and temperature rise in the strained Si device on the thin SiGe SRB reveals the importance of buffer scaling if

globally strained Si devices are to be implemented in mixed-signal applications.

Knowing the maximum drain voltage (V_{DS}^{MAX}) allowable for positive self-gain at a particular gate length and SiGe buffer thickness is important for mixed signal design in strained Si technology due to the fact that there are limits to how much SiGe buffers can be scaled. The onset of negative g_{DS} was at V_{DS}=1.0 V and 1.25 V for the 100 nm L_G strained Si nMOSFET on the thick and thin SiGe SRB respectively. Hence, there is a fundamental trade-off between V_{DS}^{MAX} and the maximum buffer thickness for positive self-gain. i.e. V_{DS}^{MAX} decreases for thicker SiGe SRBs and increases for thinner SiGe SRBs. Since there are challenges in scaling SiGe SRB thicknesses due to strain relaxation and threading dislocation density requirements, circuit designers can scale V_{DS} as an alternative so as to ease the burden on the device fabricators. However, there are also limits to V_{DS} scaling and other design parameters may affect the choice of the drain bias. The choice of V_{DS} depends on the application. For example, laterally diffused power MOSFETs comprising of low doped drain extensions are typically used for high power amplification in telecommunications base stations. These devices are usually biased at drain voltages of about 28 V [28]. The gate length of the device will also affect V_{DS}^{MAX}. V_{DS}^{MAX} reduces with the gate length which is expected since the power density, hence self-heating increases with gate length reduction. Fig. 10 shows the drain conductance as a function of the drain voltage for 1 μm, 0.5 μm, 0.35 μm and 0.1 μm gate length strained Si nMOSFETs on the thick SiGe SRBs at a gate voltage overdrive of 1.5 V. At the inset of the Fig. 10 is a magnified illustration of how V_{DS}^{MAX} is read-off from the drain voltage axis by taking the V_{DS} point at which g_{DS}=0. As the gate length of the MOSFET is reduced from 1 μm to 0.1 μm, V_{DS}^{MAX} reduces from 1.2 V to 0.9 V, which illustrates that fact that the design space becomes more rigid as for short channel MOSFETs.

There is already a long-term expectation in the semiconductor industry for scaling the power supply voltages (V_{DD}) [28, 29], a trend that can alleviate the problem of self-heating

in highly scaled analog MOSFETs as V_{DS} may be reduced below V_{DS}^{MAX}. Scaling V_{DD} is essential in CMOS because the high lateral electric field caused by aggressive gate length scaling has a negative impact on device reliability and also because of the rapidly increasing power density in very large scale integration applications [30]. Power supply scaling is even more important in some mixed signal wireless circuits where battery life is critical. However, since V_{DD} is not being scaled as aggressively as the MOSFET gate length, the problem of self-heating still persists for now. The international technology roadmap for semiconductors (ITRS) "RF and analog/mixed signal" guide [28] as well as the "Process Integration, Devices and Structures" guide [29] is used to show the interplay between projected power supply voltages and V_{DS}^{MAX} in strained Si MOSFETs at various gate lengths. Fig. 11 shows the supply voltage as a function of the gate length for ITRS long and near term projections in low standby power, high performance logic, high-speed NFET and low noise amplifier (LNA) nFET. Fig 11 also shows that the V_{DS}^{MAX} of the strained Si nMOSFETs on the thin and thick SiGe SRB. The devices on the thin SiGe SRB show greater flexibility in the design space since V_{DS}^{MAX} is higher compared with the devices on the thick SRB for all gate lengths. V_{DS}^{MAX} is improved by 30% for all the gate lengths in the strained Si nMOSFETs on the 425 nm thick SiGe SRB compared with the strained Si devices on the 4 μm thick SiGe SRB. Fig. 11 shows that SRB thinning is necessary for analog MOSFETs implemented in strained Si since the V_{DD} scaling has not gone below V_{DS}^{MAX}.

Scaling the power supply voltages has implications on the processing speed of CMOS circuits. As the drain voltage is reduced, the lateral electric field is reduced and hence, the velocity of the electrons entering the drain is also reduced. Higher drain voltages therefore translate to shorter gate delay however, at the cost of higher power dissipation and self-heating. This trade-off between the on-state speed and the power dissipation is well known to CMOS circuit designers. Hence, as progress is made on the ITRS initiative of

power supply scaling, the importance of high mobility channels becomes more apparent as technologists seek to maintain circuit speed at reduced power supplies. The low V_{DS} performance of the Si control and strained Si devices under investigation is assessed by calculating the minimum gate delay as a function of V_{DS}. The minimum gate delay, t_D^{MIN}, is calculated from the maximum transconductance, g_m^{MAX}, extracted from the gate transfer characteristics (I_{DS} vs. V_{GS}) by

$$t_D^{MIN} = \frac{2\pi C_{OX}}{g_m^{MAX}} \quad (3)$$

where C_{OX} is the gate dielectric capacitance per unit area. The percentage improvement in t_D^{MIN} for the strained Si nMOSFETs on the thick and thin SiGe SRB is calculated. The results of the calculations are shown in Fig. 12 where the percentage improvements in t_D^{MIN} compared with the Si control are shown for the 0.1 μm gate length strained Si nMOSFETs as functions of the drain voltage. It can be seen from Fig. 12 that the improvement in t_D^{MIN} remains positive for the strained Si device on the thick and thin SiGe SRB up to 0.5 V and 0.8 V respectively. The performance reduction at high drain voltages is due to self-heating and does not occur for longer gate length devices where power densities are lower. That performance reduction occurs at a higher drain voltage for the thin SiGe SRB is indicative of the fact that self-heating is reduced in the device by virtue of lower thermal resistance. Fig. 12 shows that the improvements in the on-state performance increases as the drain voltage is reduced and is 15% higher for the strained Si nMOSFET on the thin SiGe SRB at V_{DS}=0.5 V. This is encouraging since Fig. 11 shows V_{DD} could be scaled to 0.5 V in the near future. Hence, the reduction in on-state performance from V_{DS} scaling is replenished by the performance enhancement from tensile strain. The results here indicate that the ITRS

projection of supply-voltage scaling is promising for the prospects of strained Si nMOSFETs on thin SiGe SRBs since higher performance enhancement compared with the Si control is obtainable at lower V_{DS}. As V_{DD} is scaled below V_{DS}^{MAX}, which is 30% higher for the thin SiGe SRB, the problem of negative self-gain is diminished and better on state performance enhancement is obtained.

IV. CONCLUSIONS

Analog circuit designers using strained Si/SiGe technology must be careful not to bias MOSFETs in the design space of negative drain conductance otherwise the circuit may produce negative gain and anomalous non-linear phase shift. It has been shown that reducing the thickness of the SiGe SRB improves the design space of analog MOSFETs by reducing the impact of self-heating. Measured data shows that the drain conductance in 425 nm thick SiGe SRB devices is improved by 40% compared to the 4 μm thick SiGe SRB devices. A 45% improvement in self-gain compared with bulk Si was also obtained using thin SiGe SRBs. AC conductance measurements were used to extract the thermal resistance of the strained Si devices which was 50% lower in the strained Si nMOSFETs on the 425 nm thick SiGe SRB where the temperature rise in the device was reduced by 30% compared with the strained Si nMOSFETs on the 4 μm thick SiGe SRB. The intrinsic drain current was used to compute the true self-gain of the MOSFETs, which showed over 100% enhancement in the strained Si nMOSFETs. Measured data shows that thinner buffers are required to mitigate self-heating in short channel devices and the maximum drain voltage for positive self-gain is improved by 30% in the strained Si devices on the 425 nm thick SiGe SRB compared with the 4 μm thick SiGe SRB. Since there are limits to how thin SiGe SRBs can be and how small the drain voltage can be scaled, the application requirements will determine which parameter will be addressed more aggressively to ensure positive self-gain.

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TABLE. 1. MOSFET PARAMETERS USED IN CALCULATING THERMAL RESISTANCE AND CHANNEL TEMPERATURE.

Parameter	0.1 μm		1 μm		Units
	Thin SRB	Thick SRB	Thin SRB	Thick SRB	
g_{DS}	-1.66	-2.53	-0.09	-0.13	mS
g_{DST}	1.73	1.72	0.05	0.045	mS
V_{DS}	1	1	1	1	V
V_{DSAT}	0.95	0.95	0.95	0.95	V
I_{DS}	17.89	17.23	3.02	2.85	mA
λ	0.01	0.01	0.01	0.01	V^{-1}
k	1.5	1.5	1.5	1.5	
E_{SAT}	0.07	0.07	0.07	0.07	$MVcm^{-1}$
χ	1	1	1	1	mVK^{-1}
μ_{EFF}	271	263	271	263	$cm^2V^{-1}S^{-1}$
β_O	62.39	61.53	6.24	6.15	mAV^{-2}

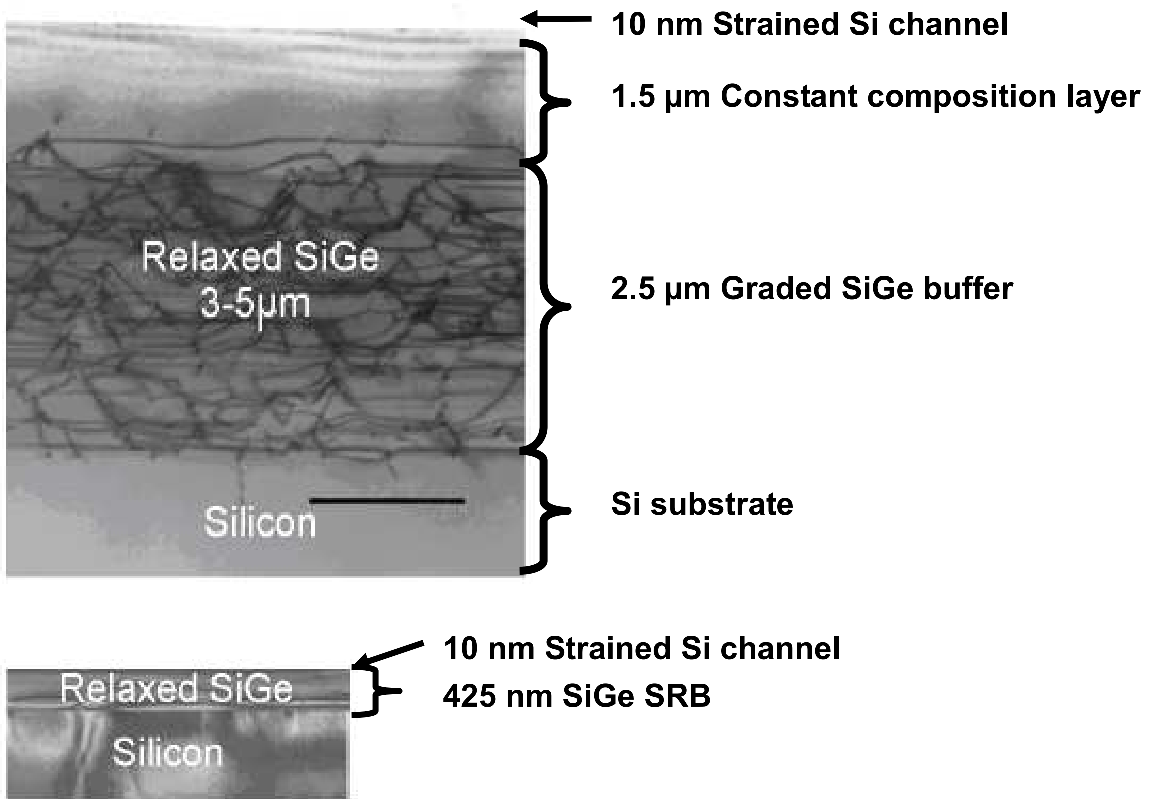

Fig.1. TEM images of the thin and thick SiGe SRB devices under investigation.

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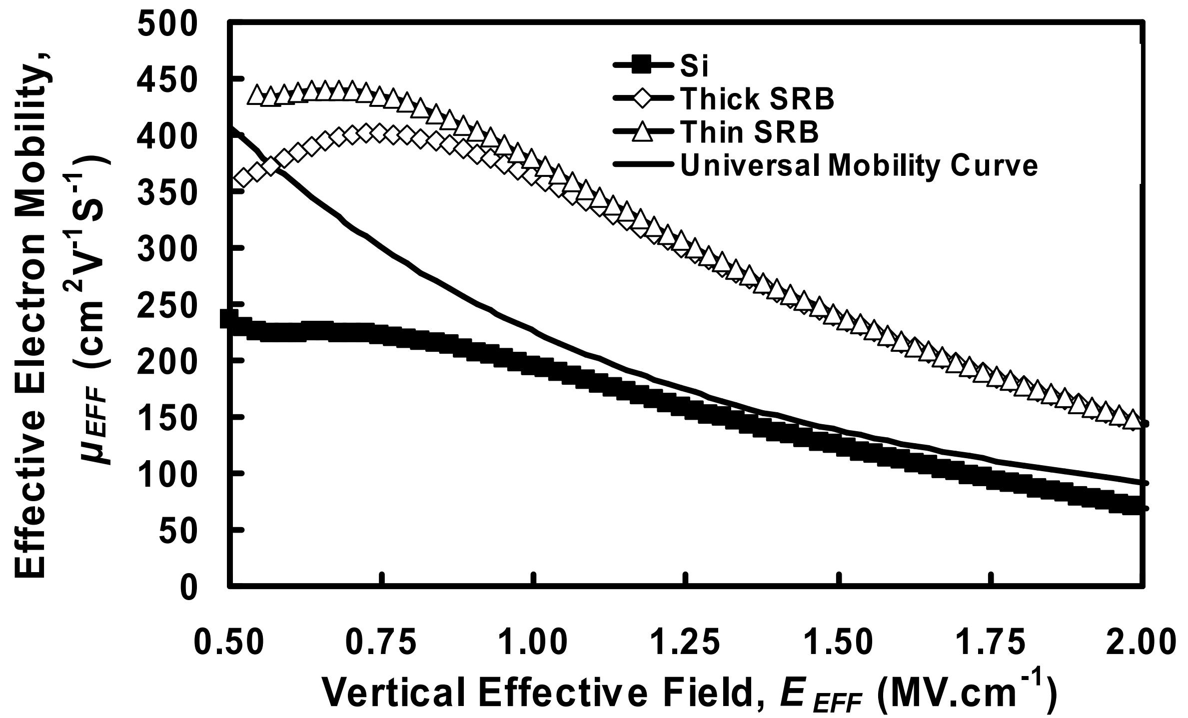

Fig. 2. The effective electron mobility as a function of the vertical effective field for the Si control and strained Si devices on the thin and thick SiGe SRBs. There is 100% mobility enhancement in the strained Si devices compared with the Si control. Full strain relaxation is achieved in the strained Si device on the thin SiGe SRB.

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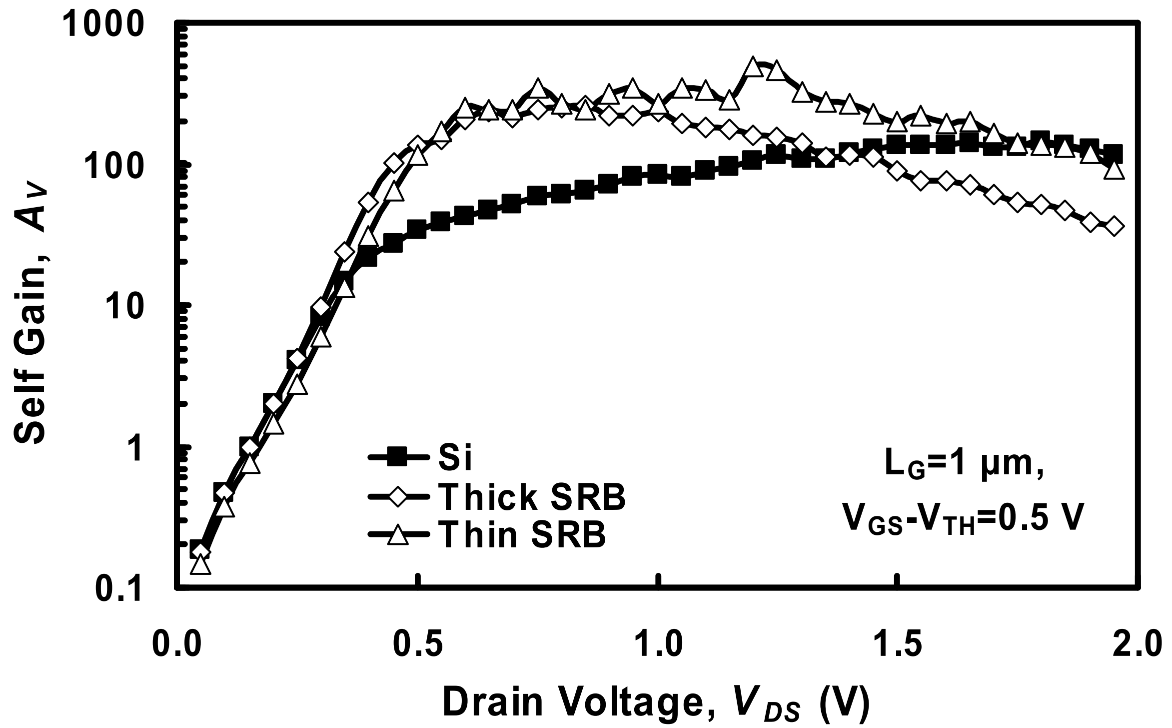

Fig. 3(a). Self-gain as a function of drain voltage for the 1 µm gate length strained Si and bulk Si MOSFETs measured at V_{GS}-V_{TH}=500 mV. High A_V enhancement is evident in the strained Si nMOSFETs compared with the Si control at V_{DS} less than 0.5 V. As V_{DS} is increased, A_V reduces in the strained Si nMOSFETs due to self-heating. A_V reduction is less in the strained Si nMOSFET on the thin SiGe SRB.

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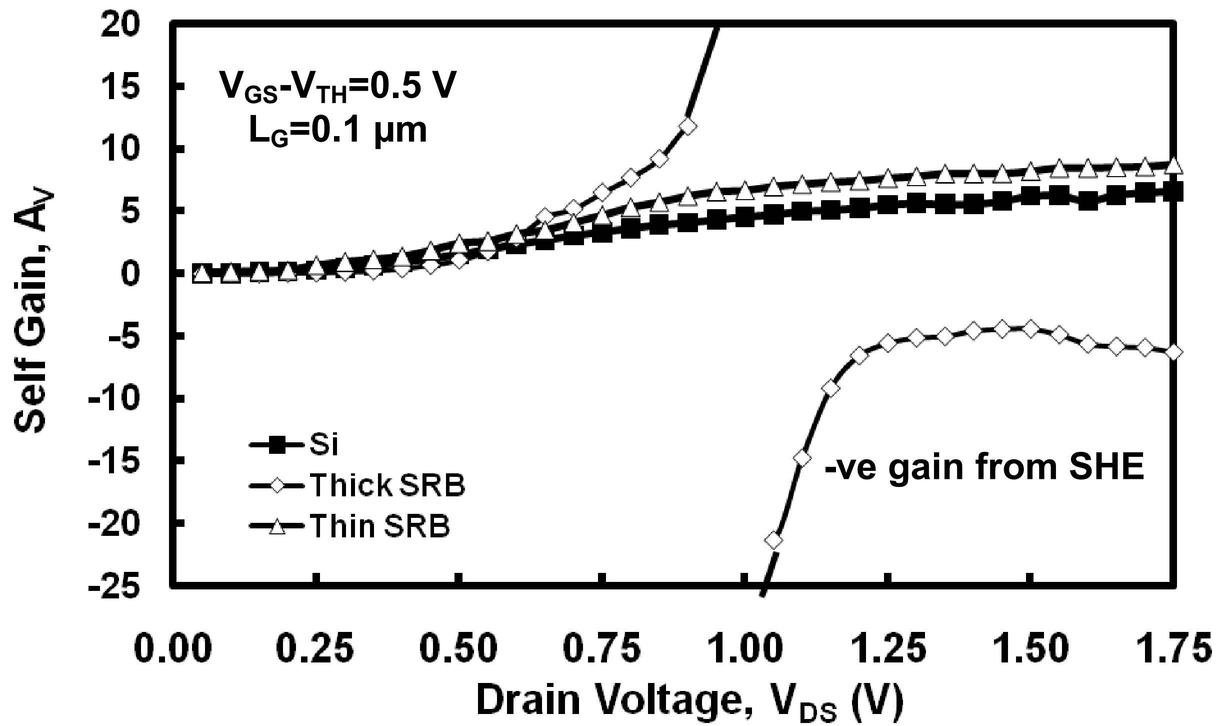

Fig. 3(b). Self-gain as a function of drain voltage for the 100 nm gate length strained Si and bulk Si MOSFETs measured at V_{GS}-V_{TH}=500 mV. Negative drain conductance due to self heating effects (SHE) causes negative self-gain for the thick SiGe SRB devices at high V_{DS}. This problem is eliminated by the thin SRBs.

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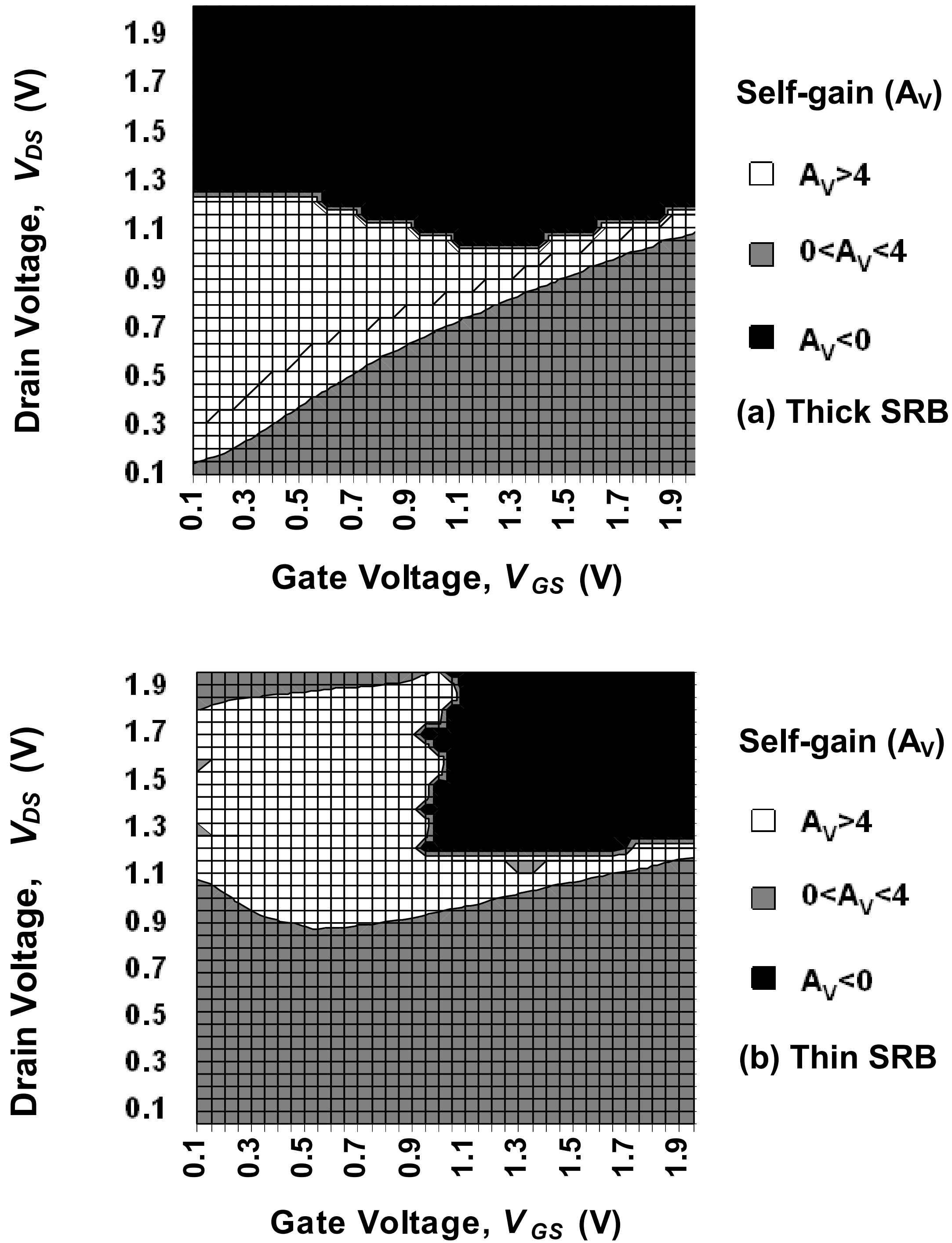
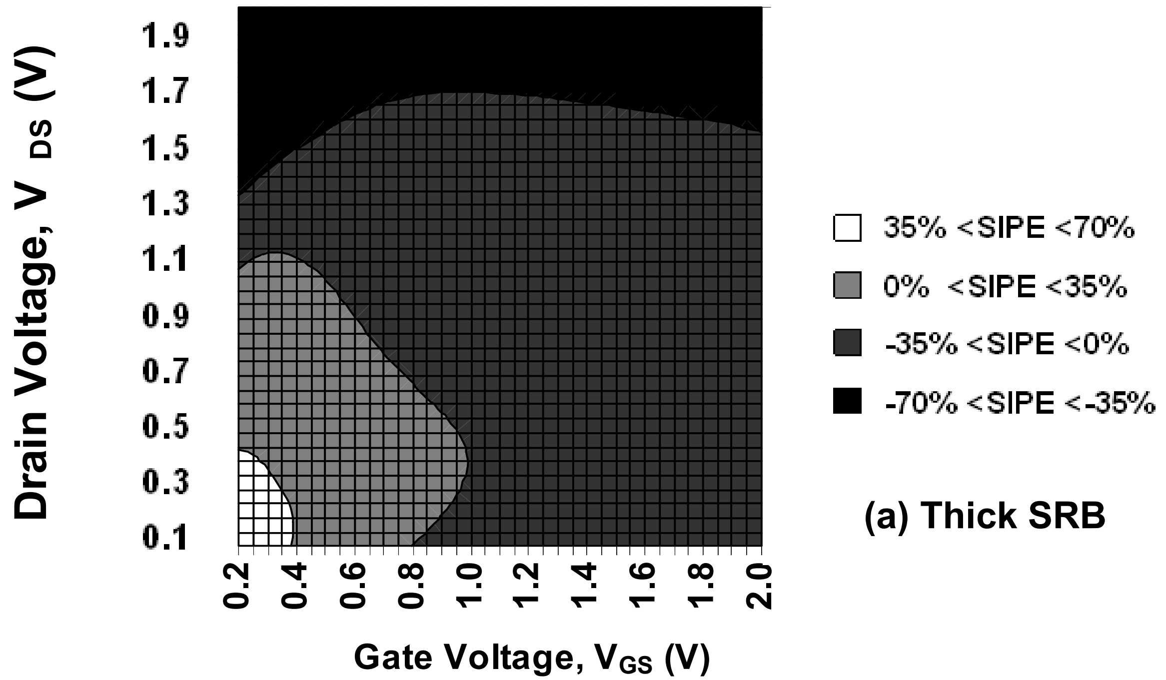


Fig. 4. Self-gain contour plots for (a) thick (b) thin SiGe strain-relaxed buffer. The negative gain space is halved using thin SRB technology enabling greater design flexibility.



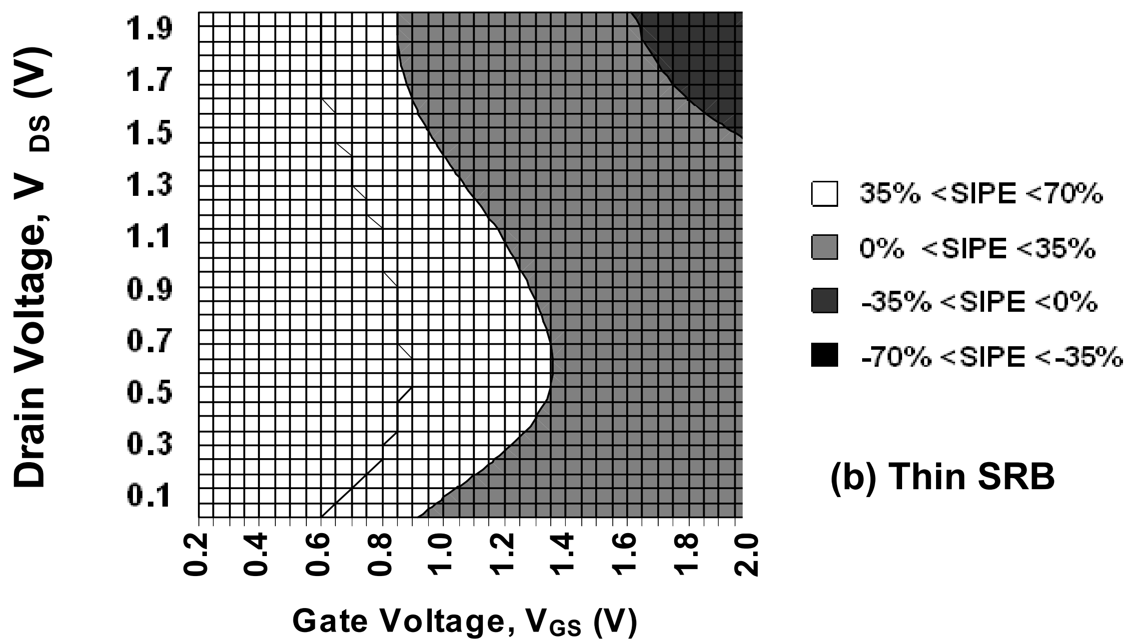


Fig. 5. SIPE contour plots for (a) thick (b) thin SiGe strain-relaxed buffer. SIPE is significantly better in the thin SRB devices due to reduced self heating.

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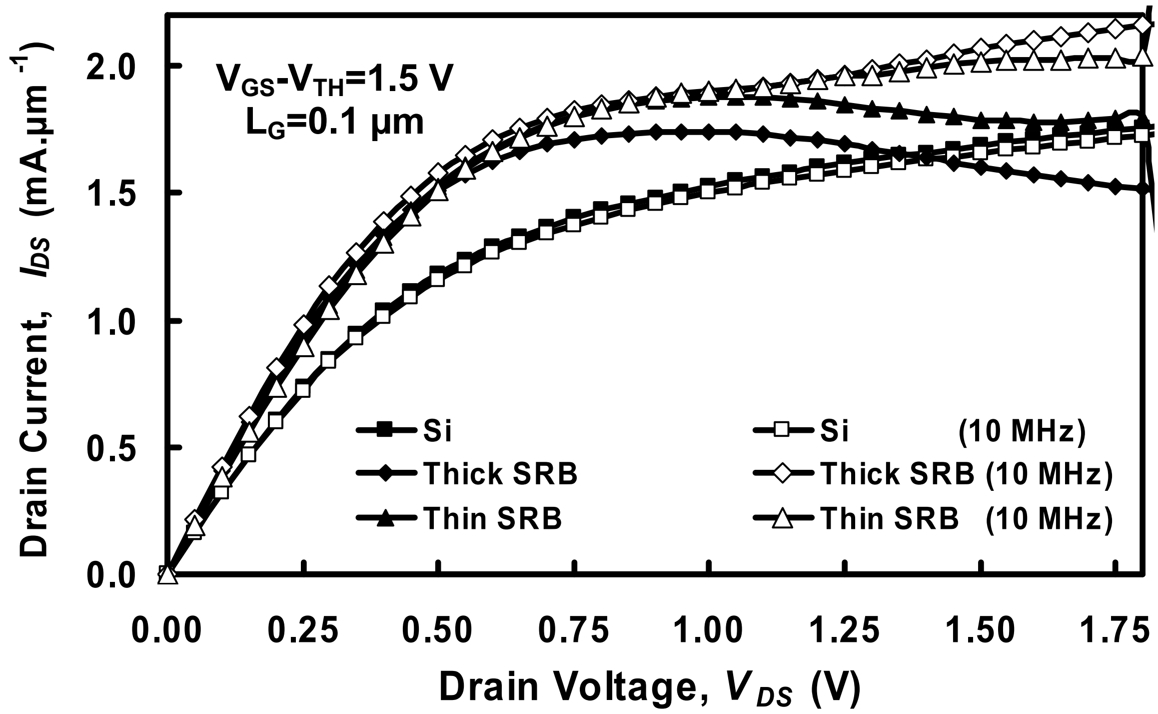

Fig. 6. Drain current as a function of drain voltage with and without self heating effects on 0.1 µm gate length MOSFETs at a gate overdrive V_{GS}-V_{TH} of 1.5 V.

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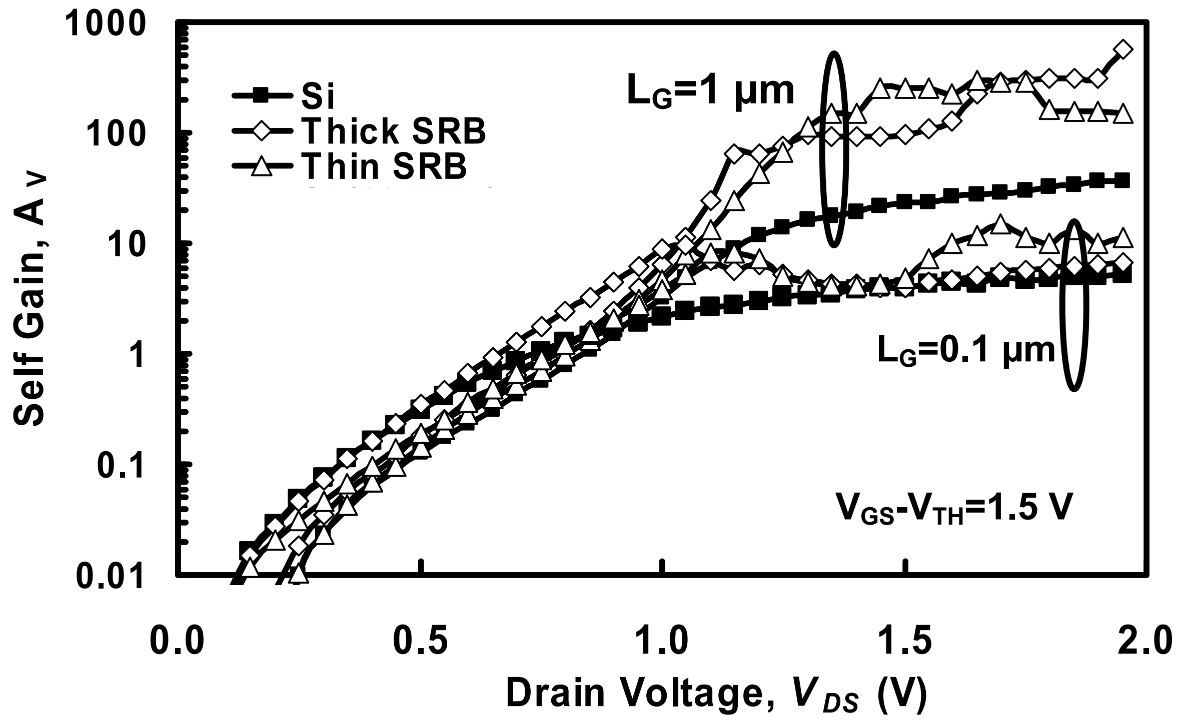

Fig. 7. Self-gain as a function of drain voltage with the self heating effect removed by drain conductance measurements at 10 MHz. There is an enhancement in the self-gain in the strained Si devices compared with the bulk Si device.

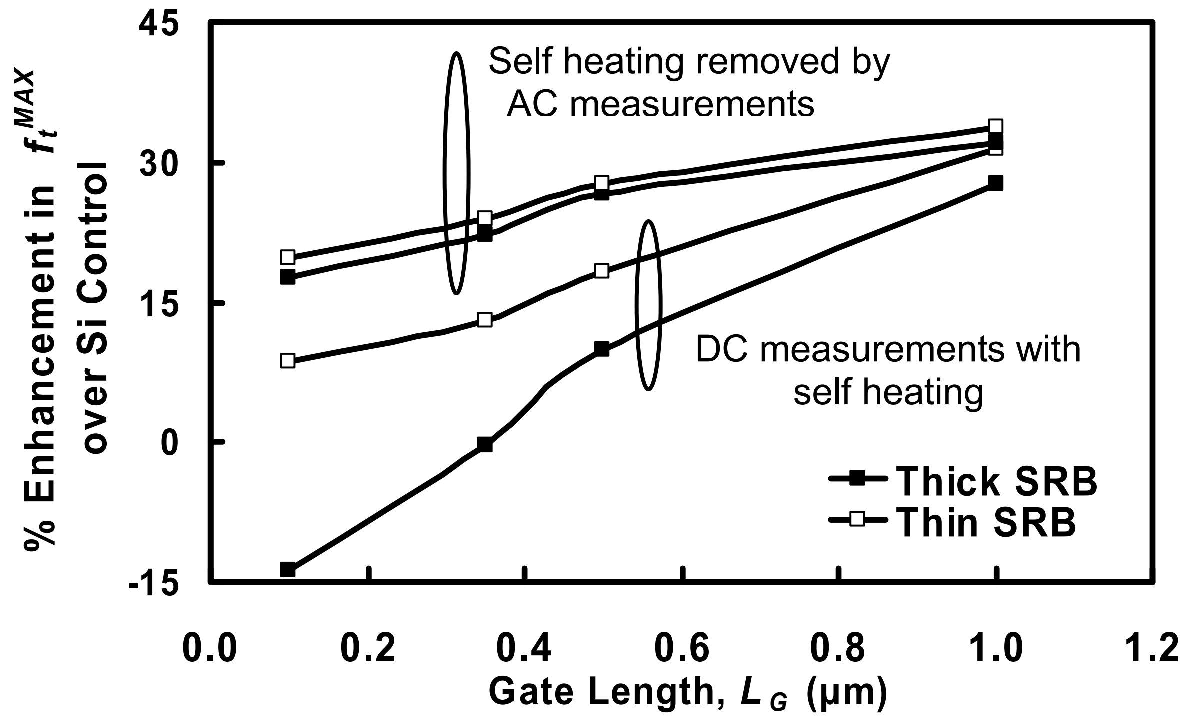

Fig. 8. The percentage enhancement of the maximum cut-off frequency compared with Si control as a function of the gate length for the strained Si devices on the thick and thin SiGe SRBs at a drain voltage of 2 V.

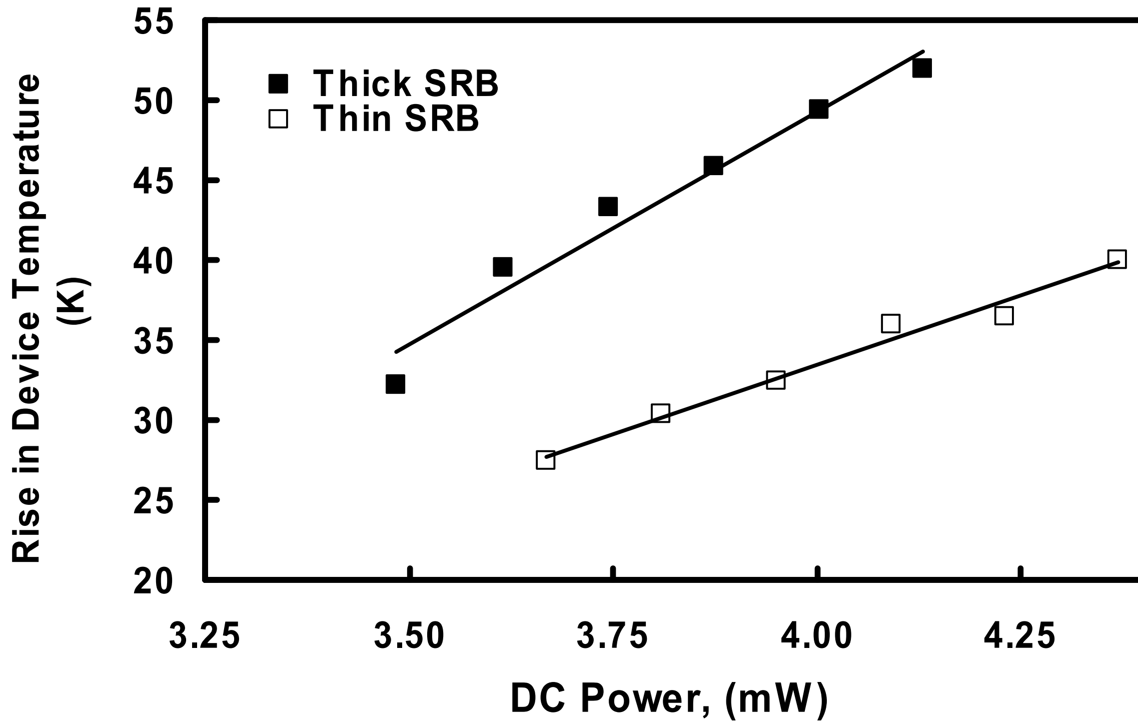

Fig. 9. The rise in device temperature due to SHE as a function of the dissipated power using data from AC and DC measurements. The results show a 30% higher temperature rise in the thick SRB devices compared with the thin SRB devices. The average thermal resistance is calculated by determining the slope of the line of best fit.

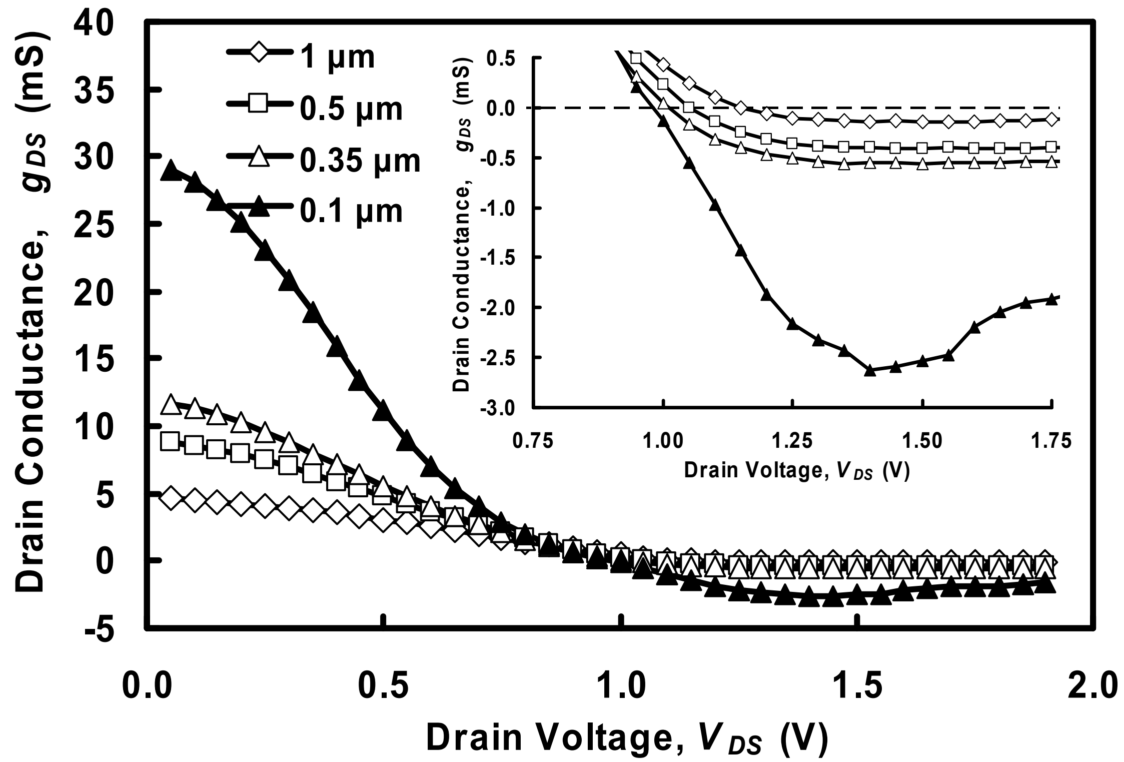

Fig.10. The drain conductance as a function of the drain voltage for the 1 µm, 0.5 µm, 0.35 µm and the 0.1 µm strained Si nMOSFETs on the thick SiGe SRB at a gate voltage overdrive of 1.5 V.

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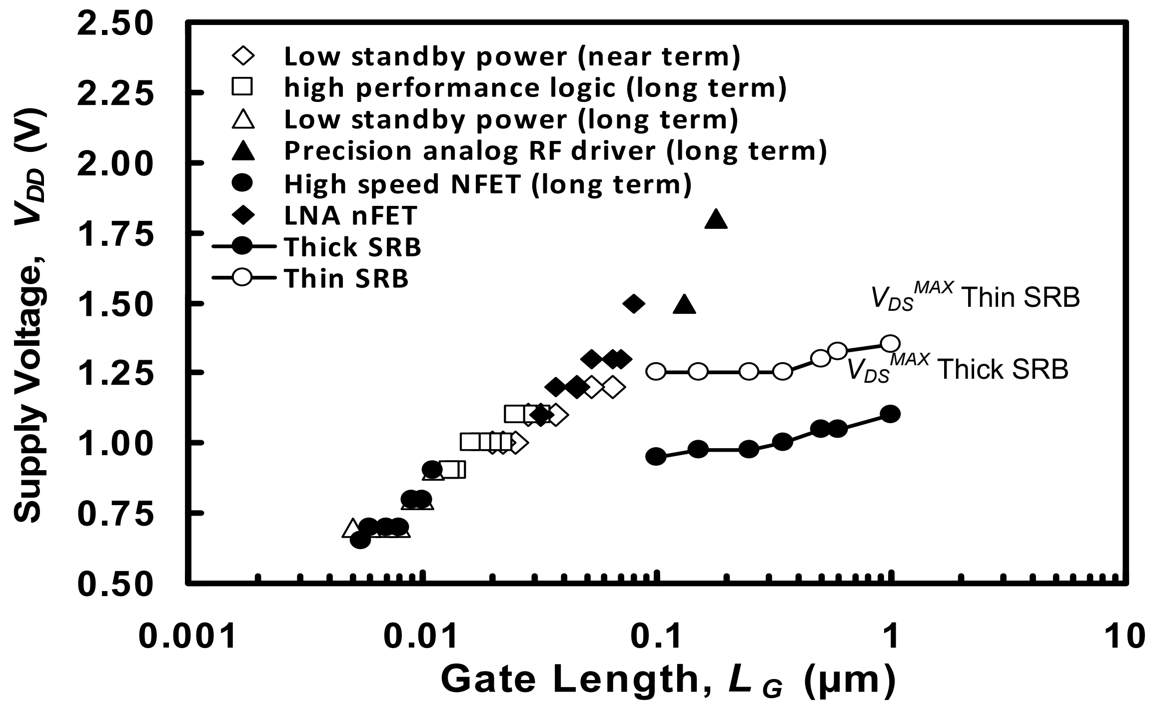

Fig. 11. The power supply voltage for various gate lengths as mandated by the ITRS. The maximum allowable drain voltage for positive self-gain for both the strained Si devices on the thin and thick SiGe SRB is shown as a function of the gate length.

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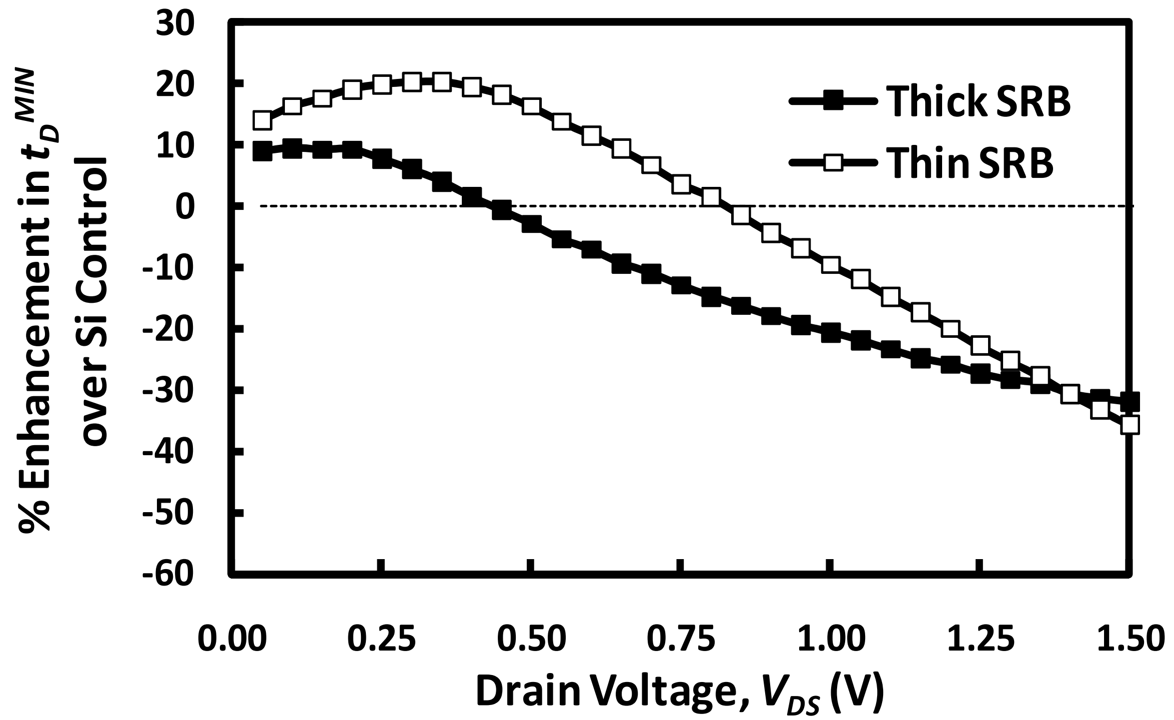

Fig. 12. The percentage enhancement in the minimum delay as a function of the drain voltage for the 100 nm strained Si nMOSFETs on the thick and thin SiGe SRBs.

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