Static-Noise Margin Analysis during Read Operation of 6T SRAM Cells

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Abstract

SRAM cell stability analysis is typically based on Static Noise Margin (SNM) investigation when in hold mode, although many memory errors may occur during read operations. Given that SNM varies with each cell operation, a thorough analysis of SNM in read mode is required. In this paper we investigate the SRAM cell SNM during read operations analyzing various alternatives to improve cell stability in this mode. The techniques studied are based on transistor width, and word- and bit-line voltage modulations. We show that it is possible to improve cell stability during read operations while reducing current leakage, as opposed to current methods that improve cell read stability at the cost of leakage increase.

1. Introduction

During the past decades CMOS IC technologies have been constantly scaled down aggressively entering in the nanometer regime during this decade. Among the wide variety of circuit applications, integrated memories – and specially SRAM cell layout – has been significantly improved. It is well known that critical dimension (CD) reduction entails an increase in physical parameters variation, which among other effects has a direct impact on SRAM cell stability. Polysilicon and diffusion CD together with implant variations are the main causes of mismatch in SRAM cells. Current System on Chip (SoC) trends result in a significant percentage of the total die area being dedicated to memory blocks, thus making SRAM parameter variations dominate the overall circuit parameter characteristics, including leakage, process variation effects, etc. Therefore, a deep knowledge and analysis about the stability of the SRAM cells and the impact of physical parameters variation is becoming a must in modern CMOS designs.

The stability and robustness of a given SRAM cell is usually evaluated analyzing both its dynamic and static behavior during the typical operations: write, read and hold periods. According to this, the memory cell stability can be estimated from the Static Noise Margin analysis. SNM is defined as the minimum DC noise voltage needed to flip the cell state [1], and is used to quantify the stability of a SRAM cell using a static approach. A significant effort has been devoted to explore the impact of process variations, temperature, etc., using the SNM as a metric. In this paper we present a detailed analysis about 6T SRAM cells static stability during read, and compare the differences between SNM during hold- and read-mode. The read-mode is usually identified as the cell weakest mode. We investigate the impact of corner analysis to determine the worst-case using a commercial 65nm CMOS technology. The impact on SNM when voltage operations, temperature and power supply vary, is analyzed.

The rest of the paper is organized as follows: the next section provides a SRAM cell stability background introducing the SNM parameter in detail. Section 3 explores the impact of variations on read-mode SNM. The section introduces a new approach that improves the cell stability by adjusting the nominal values of internal voltages during read operations. Some new ideas of increasing SNM during read operations are proposed and the relationship between cell stability and current behaviour are determined. Finally Section 4 points out the main conclusions of this work.

2. 6T CMOS SRAM STABILITY

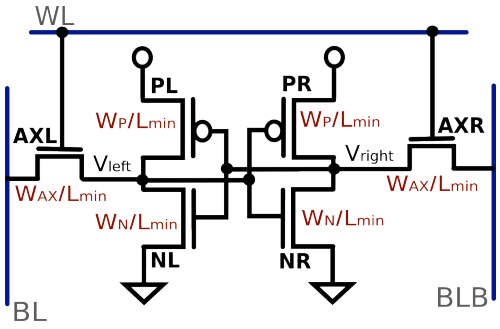

Figure 1. 6T SRAM cell schematic.

The conventional 6T SRAM memory cell is composed of two cross-coupled CMOS inverters with two pass transistors connected to complementary bit-lines. Fig. 1 shows this well-known architecture, where the access transistors AXR and AXL are connected to the word-line (WL) to perform the access write and read operations thought the column bit-lines (BL and BLB). Bit-lines act as input/output nodes carrying the data from SRAM cells to a sense amplifier during read operation, or from write circuitry to the memory cells during write operations. All transistors have

minimum length (L_{min}), while their width are typically design parameters. The value of W_P defines all PMOS transistors width and W_N defines the NMOS driver transistors width, while W_{AX} is the access transistors width.

The SRAM cell immunity to static noise is measured in terms of SNM that quantifies the maximum amount of voltage noise that can be tolerated at the cross-inverters output nodes without flipping the cell. The graphical method to determine the SNM uses the static voltage transfer characteristics of the SRAM cell inverters.

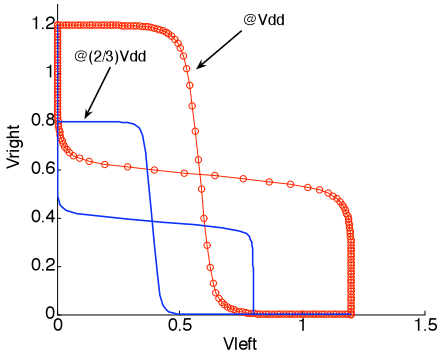

Figure 2. "Butterfly" curve during HOLD operation for two different power supply voltages.

Fig. 2 superposes the voltage transfer characteristic (VTC) of one cell inverter to the inverse VTC of the other cell inverter. The resulting two-lobed graph is called a "butterfly" curve and is used to determine the SNM. Its value is defined as the side length of the largest square that can be fitted inside the lobes of the "butterfly" curve [1]. Fig. 2 shows the variation of the "butterfly" curves for two supply voltages (V_{DDnom} and $(2/3)V_{DDnom}$) during hold operation. The Figure shows that lowering the power supply voltage reduces the static noise margin (SNM).

SNM is a key performance factor during hold and read operations, and its value changes significantly depending on the specific operation mode. It has been shown that during read the SNM takes its lowest value and the cell is in its weakest state [2]. Fig. 3 illustrates the worst-case SNM when the word-line is settled high and both bit-lines (BL and BLB in Fig. 1) are still pre-charged high. While in this situation, the SRAM cell internal node being low will be pulled up through the access transistor degrading significantly the SNM during the read operation. Fig. 3 shows an example of "butterfly" curves during read operation that illustrate the degradation in SNM during read and how lowering the supply voltage further aggravates the impact on SNM.

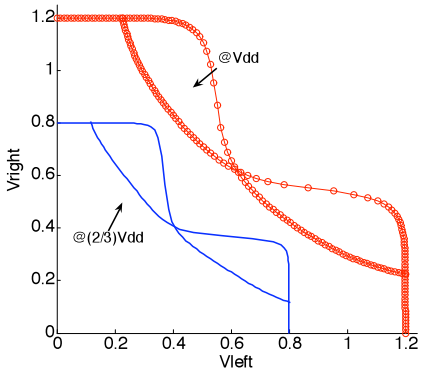

Figure 3. "Butterfly" curve during READ operation for two different power supply voltages.

Table 1 lists the SNM values during hold and read operations at two different power supply voltages corresponding to a minimum sized bit-cell. The SNM reduction during read operations with respect to hold operations is considerable at each supply voltage.

Table 1. SNM during Hold and Read operations versus Power Supply voltage

SNM (mV)	CMOS65 @ VDD	CMOS65 @ (2/3)VDD
HOLD	448.42	320.34
READ	173.49	131.88

3. SNM dependences

Given that, as shown in Table 1, the SNM is significantly degraded during read operations, we focus on analyzing the impact of some design parameters on SNM during read-mode.

3.1. Impact of transistor width modulation

We establish a metric to quantify the SNM improvement during read operations considering transistor width modulation defining the following ratios:

$$\alpha = \frac{W_N}{W_{AX}} \quad ; \quad \beta = \frac{W_P}{W_{AX}}$$

where $W_{AX} = \gamma * W_{min}$, and W_{min} is the minimum transistor width allowed by the technology. To keep cell area within reasonable values, we restrict the values of α and β ratios between the minimum, 1, and a maximum of 2.5, (i.e. $\alpha_{max} = \beta_{max} = 2.5$).

Fig. 4 plots the SNM improvements using the transistor width modulation technique computed during hold and read operations. For each W_{AX} value (corresponding to γ factors 1, 1.5, 2, and 2.5) there is a surface represented in Fig. 4. Since the SNM variation between different γ factors is negligible, we assume $\gamma = 1$ (i.e. $W_{AX} = Wmin$) during the rest of our analysis. Three main observations derive from

Fig. 4: (i) the SNM improvement during hold is negligible using this technique when comparing between hold and read modes; (ii) the SNM gain is higher when increasing the α ratio than when increasing only the β ratio, although increasing both ratios provides a higher SNM improvement, and (iii) maintaining W_{AX} at the minimum value results in similar SNM improvements compared to higher values.

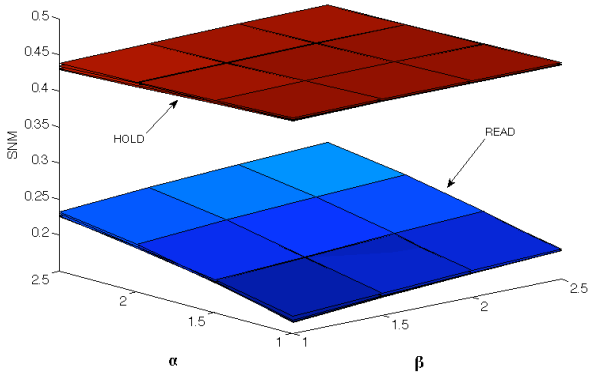

Figure 4. SNM variation applying Transistor width modulation during hold and read operations.

Although it is easy to conclude from previous analysis that increasing α and β ratios provides a better SNM, the impact on other design parameters must be considered. In this case increasing α and β will lead to higher current consumption, not only during read but also during hold due to the static consumption.

In the literature some recommendations can be found to maintain the aspect ration of cell within a certain limits. The transistors involved during read operations are the access transistor and the NMOS transistors. For this operation it is better to maintain α ratio close to or higher than 1. The transistors involved during write operations are the PMOS ones and the access transistor. In this case the β ratio is preferred near to 1, or maintaining a strong access transistor with a weaker PMOS transistor.

3.2. Impact of word-line modulation

The word-line voltage modulation is another alternative to increase the cell stability at low power supply levels compatible with recommended cell layout (α≈β≈1). This approach is based on reducing the maximum voltage swing of the word-line to maintain the cell access transistor weakly-saturated during the read operations. Fig. 5 plots the relationship between the SNM and the word-line voltage.

The word-line voltage controls the SRAM cell access state and allows two modes: hold and access operations (read and write). As shown in Fig. 5, the SNM could be improved by reducing the word-line voltage during read operations with respect to V_{DD} (world-line voltage will not be reduced during write mode). This technique may allow a substantial improvement of the SNM during read without requiring any modification of the SRAM cell array design.

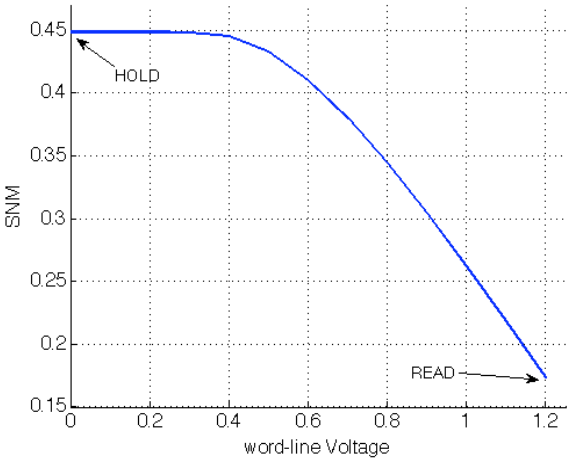

Figure 5. Impact of word-line voltage on SNM.

The strategy of reducing the power supply voltage during hold-mode is used to reduce the current leakage. Reducing the effective word-line voltage could provide an interesting technique to improve the stability of the cell during read operations.

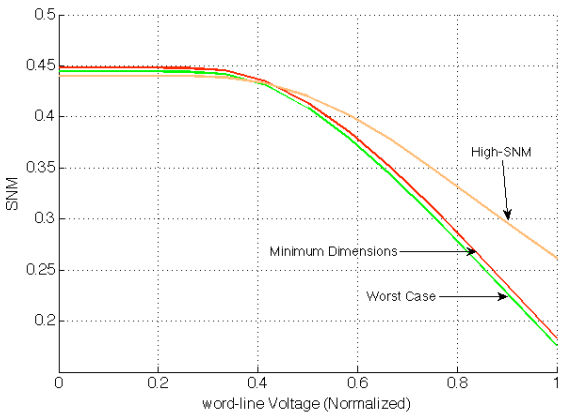

Figure 6. Impact of word-line voltage and transistor width modulation on SNM.

The overall SNM can be improved by combining both methodologies, width transistor and word-line voltage modulations,. Fig. 6 plots SNM versus word-line voltage (normalized to the nominal voltage). During Read operation, three cases are highlighted: (i) minimum sized cell where α ≈ β ≈ 1, (ii) the worst case where the SNM is minimum and, (iii) the high-SNM where the SNM increases the most. The values of α and β ratios for these three cases are summarized in Table 2.

Table 2. Significant cases

	Worst Case	Minimum Dimensions	High-SNM
α	1	1	2.5
β	2.5	1	1

The result of combining both width and voltage modulations highlights two main points: first, SNM improvement is maintained and increased and second, a different behaviour during hold and read modes is obtained. While the high-SNM curve is lower than the others in hold mode, during read mode the High-SNM curve is the top one. This indicates that the cell stability may not be well defined by SNM given its dependence on the cell mode.

3.3. Impact of Bit-line modulation

Bit-line voltage modulation is investigated to evaluate the requirement of pre-charging bit-lines at the full power supply voltage. Fig. 7 plots the relationship between the SNM and the bit-line voltage for five corners situations (T stands for typical, F for fast, and S for slow). Fig 7. Indicates that the SNM can be lightly improved by reducing below V_{DD} the bit-line voltage during read operations. This option increases the cell stability and is compatible with the voltage modulation alternatives analyzed previously. The reduced bit-line voltage swing may allow for a read-mode SNM improvement without requiring any modification of the SRAM cell array design.

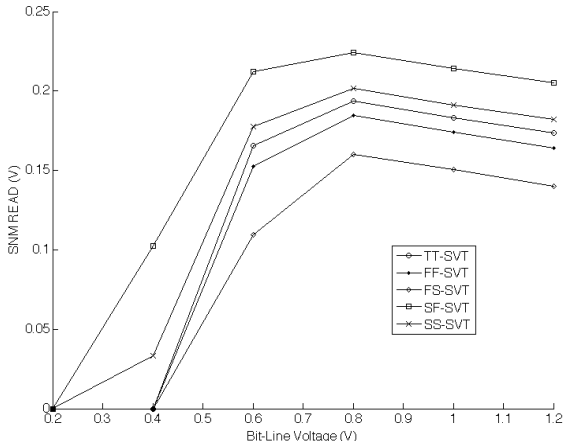

Figure 7. Impact of bit-line voltage modulation on SNM using standard V_T transistor models (SVT).

Fig. 7 shows that the SNM improvement is rapidly degraded below $(2/3)V_{DD}$, but for values between $(2/3)V_{DD}$ and V_{DD} the read-mode SNM is improved.

Fig. 8 shows the combined impact on read-mode SNM of adopting word-line and bit-line voltage modulation. The word-line voltage modulation shows a bigger impact on SNM, making the bit-line voltage modulation contribution negligible.

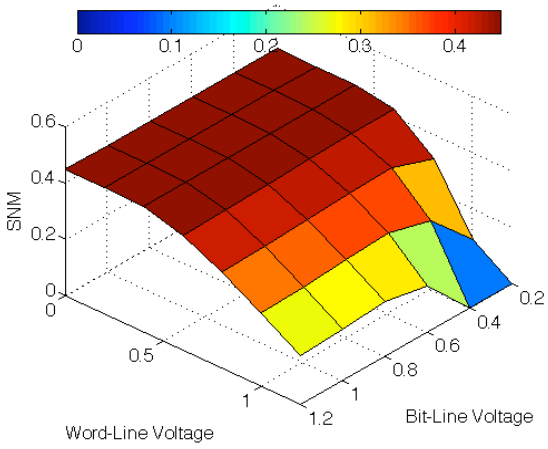

Figure 8. Impact of bit-line voltage and Word-line voltage modulations on SNM.

Moreover, word-line voltage reduction provides higher cell stability, providing margin for bit-line voltage increase to improve the overall SNM.

3.4. Impact of Power-Supply voltage modulation

The power supply voltage modulation is typically used when in hold mode to reduce power consumption and has been widely adopted in nanometer technologies for which leakage has increased dramatically. Fig. 9 shows the impact of power supply reduction during Read mode on SNM. It is clear that power supply voltage reduction during read operation is not suitable and SNM is reduced for all cases.

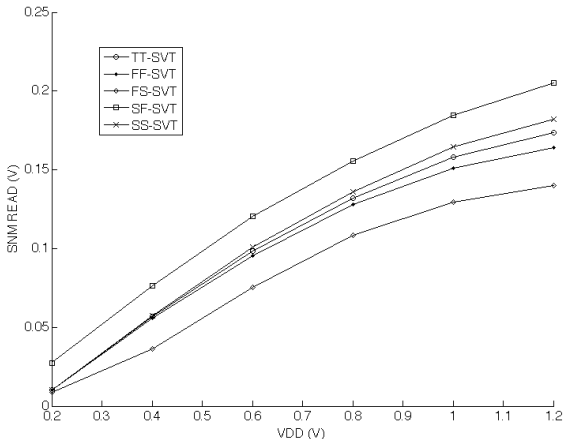

Figure 9. Impact of Power Supply voltage modulation on SNM using standard V_T transistor models (SVT).

The impact of supply voltage reduction on SNM during read operations makes it more preferable to maintain full V_{DD} when reading the memory. If the memory array is supply voltage is the same for all the cells, this implies drawing the maximum leakage over the whole memory array while accessing to a

single column. However, it is possible to maintain a reduced V_{DD} during read operation and compensate for the SNM reduction through the voltage modulation techniques described earlier.

Fig. 10 shows a comparison of the achieved SNM for various supply voltage values when modulating the word- and bit-line voltages. It is shown that word-line voltage modulation may provide a better read-mode SNM at $(2/3)V_{DD}$ by lowering the word-line voltage to about 0.6 of the nominal value.

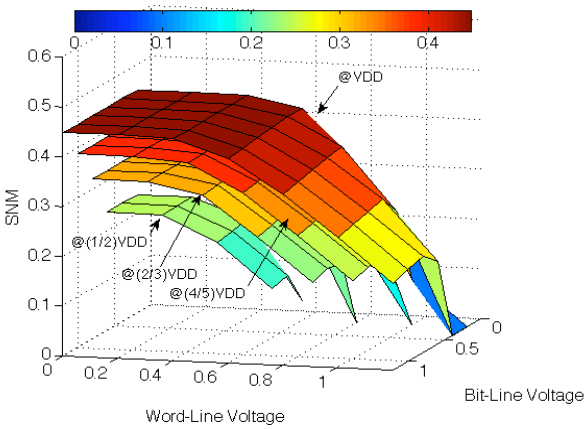

Figure 10. Impact on SNM of decreasing Power Supply voltage while word-line and bit-line modulations are used to compensate the degraded stability during Read.

Table 3 provides numerical values of the read-mode SNM for some combination of word- and bit-line voltage modulation voltages (modulated SNM) together with transistor width modulation. It is shown that the iso-supply voltage combination with 0.8 word- and bit-line voltage modulations increase the read-mode SNM more than 2X (case A), while 0.6 word- and bit-line voltage modulations together with the cell-size modulations provide 2X and 1.7X read mode SNM improvement (case B and C respectively).

Table 3. Examples of SNM_{READ} improvement with lower Power Supply voltage.

V_{DD} - case	SNM_{READ} (nominal)	WL	BL	α	β	SNM_{READ} (modulated)
1.2 –A	173.49 mV	0.8	0.8	1	1	357.0 mV
1.0 – B	158.12 mV	0.6	0.6	1	2	341.3 mV
0.8 – C	131.88 mV	0.6	0.6	2	2	231.0 mV

Table 4 provides the impact of the modulated combinations of key cell parameters like access time, leakage and area increase. Although a penalty is introduced in access time, it is shown that the overall leakage current is reduced mainly due to the power supply voltage reduction. If a layout structure containing 256 cells per column is considered, and only one cell is being access in read mode while the rest of the cells are in hold, a power reduction during read operation may reduce the total column leakage between 30% to 50%depending of modulation case considered.

Table 4. Read Time and current leakage improvement with lower Power Supply voltage for previous cases (normalized values)

VDD	Read Time (nominal)	Read Time (enhanced)	$IDDQ_{HOLD}$ (one cell)	Cell Area overhead
1.2 – A	1	3.5	1	1
1.0 – B	--	10.7	0.63	1.3
0.8 – C	--	11.0	0.48	2

3.5. Impact of Temperature

Although temperature may have a significant impact on other design parameters like access time, it is relatively insignificant for SNM analysis. The SNM variation is about ~70μV/ºC for a Typical-Typical corner, being similar for the others corners, as shown in Fig. 11. It is observed that the variation of SNM for different corners follows similar trends.

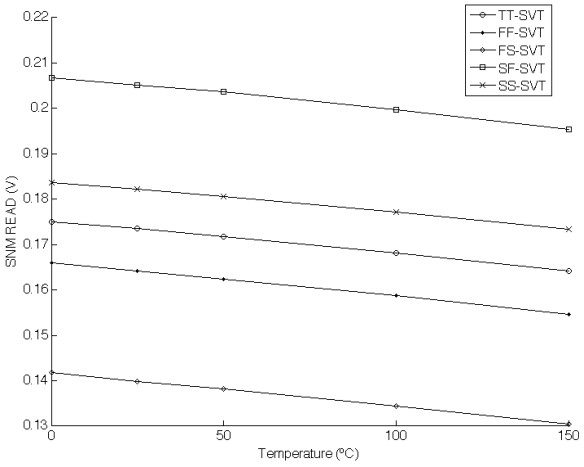

Figure 11. Impact of Temperature on SNM using standard V_T transistor models (SVT).

Such as, temperature may be considered to be a not impact on SNM during Read mode.

4. Conclusions

During a read operation, the Static Noise Margin analysis indicates that the stability of the cell is degraded, showing their lower values. Basically, three signal voltages are involved in a read operation: the world-line voltage, the bit-line voltage and the power-supply voltage. All three voltages could be used to improve the SNM. In addition, the utilization of a lower power supply may contribute to reduce the leakage current for all cells in the memory.

Three-parameter modulations have been proposed: transistor width modulation, word-line voltage modulation and bit-line voltage modulation. The different modulation effects combination has been proposed to improve the SNM during read while reducing the memory leakage current. Although a penalty is introduced in access time, it is shown that the overall leakage current is reduced mainly due to the power supply voltage reduction. As an example, if a layout structure containing 256 cells per column is considered, and only one cell is being access in read mode while the rest of the cells are in hold, a power reduction during read operation may reduce the total column leakage between 30% to 50% depending of modulation strategy considered.

The impact of SNM variation is about ~70μV/ºC for a Typical-Typical corner, being similar for the others corners, so it is expected that the impact of temperature on modulation strategy could be considered as negligible.

ACKNOWLEDGMENTS

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References

[1] Seevinck, E., List, F.J., Lohstroh, J. 1987. "Static-Noise Margin Analysis of MOS SRAM Cells". IEEE Journal of Solid-State Circuits, SC-22, 5 (Oct. 1987), 748-754.

[2] Pilo, H., Barwin, C., Braceras, G., Browning, C., Lamphier, S., Towler, F. "An SRAM Design in 65-nm Technology Node Featuring Read and Write-Assist Circuits to Expand Operating Voltage". IEEE Journal of Solid-State Circuits. 42. 4. 813 - 819 (Apr. 2007).