22nm High K Metal Gate Inverter Comparative Analysis of Substrate Biasing Effect on Low Power And High Performance Ptm Models

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***Abstract*:- This paper analysis the low power and high performance models of PTM with Hi-K metal gate cmos technology by using them in an cmos inverter. Also the effect of substrate body biasing is analysed on the output characteristics. The comparison tables are drawn on Voltage Transfer Characteristic in normal biasing as well as in nsubstrate and psubstrate biasing with input voltage sweeping from minimum to maximum voltage, at 22nm technology node. This analysis gives an insight into unusual leakages in the gate and supply terminal at 22nm node. All the simulations are being done with Hspice simulator using PTM models of 22nm cmos HiK-metal gate of Arizona state University, USA.**

Keywords:- 22nm, body biasing,BSIM473, ptm, scaling issue.

I. INTRODUCTION

There had always been requirement of high performance, low power and smaller area circuits and system. And is the reason we are moving towards higher technology nodes (scaling] and at the same time exploring other technologies such as Finfet, Silicon on Insulator, Carbon Nano Tubes etc. One is always seeking new designs, techniques, methodology etc to overcome the challenges encountered at every technology node. On scaling down to advance technology node, there are challenges related to Physics of the device, Fabrication techniques, Modeling, Scaling, Parameter and process variation. Hence there are needs of newer techniques and methodology to tackle above issues, at every node of miniaturization. Technology scaling decreases the delay and increases the frequency of Integrated circuits [1]-[5]. Number of transistor per unit area increases with scaling. At each technology node, the increased no of transistors can be utilized for new circuit techniques to improve the functionality of Integrated Circuits [1]-[7]. At the same time the bad consequences of shrinking of the chip are complexity and power consumption. For portable small size of a system, the paths of technology nodes are in the two directions of speed and lower power consumption. The group of chips with speed improvement as the main objective, employ higher clock frequency, bigger area and surplus use of circuits system requiring higher power[2], [3], [7]. This comes now with expensive cooling solutions [2]-[7]. And this may not allow chip cost to decrease further along with miniaturization. The other path of the low power chips are for the portable devices and power restrictions and limitations always have upper hand over performance [4], [6], [9]. With miniaturization/scaling of different technology nodes, the performance improvement is at a faster speed compare to lower power consumption [4], [9], and [11]. At advanced technology nodes the high performance circuit can't be used for low power applications and vice versa.

II. REVIEW OF EXISTING WORK

We have technology coming down to less than 32nm from 200nm. With this the traditional physics approaching it's final limits [23], [24] with shrinkage in feature size, the high electric fields inside the device create huge problems [25], [26], [27], [28]. And to reduce these problems, the alternatives could be to educe supply and threshold voltages in match with miniaturization factor but not possible [25], [27], [28].

The reduction in threshold voltage comes with increase in leakage current and subthreshold conduction with tremendous increase in leakage current and subthreshold conduction along with tremendous increase in noise. For the adequate noise margin Vdd should be at least 3 times the threshold voltage.

There had been vast research to know the impact of scaling on different parameters viz. leakage current, power etc along with substrate noise, incremental noise and noise in the power distribution network [29] . Also With technology scaling, these noise difficulties increases due to decrease in distance between routing layers, capacitive coupling increases [6], [8]. With scaling parasitic of interconnect increases [35], and since transistor density is increased, it results in larger substrate noise .

Power dissipation is a critical parameter for high density portable devices at advanced technology node [21, 22]. And with scaling the circuit and the chip should be able to dissipate the power generated [26].

Dynamic power is the largest amongst leakage/subthreshold power and short circuit power

P dynamic= α C V2 f (1)

C→ capacitance being switched, V→ supply voltage,

F →switching Frequency,

α→ switching activity of node

Instantaneous Power

P(t)= Vdd Iout(t) (2)

Iout(t) = CL dVout(t)/dt (3)

Threshold voltage for long channel

$$V_{th} = VFB + \Phi_s + \gamma\sqrt{\Phi_s - V_{bs}} = VTH0 + \gamma\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right)$$

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(4)

VFB→ flat band voltage
VTHO→threshold voltage of long channel device at zero substrate bias
¥→body bias coefficient

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_{substrate}}}{C_{oxe}} \quad (5)$$

Nsubstrate→uniform substarte doping condition
For short channel [44]with process variation effect

$$VTH0 = VTH0 + DELVTO$$

DELVTO→zero bias threshold voltage variation
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III. BIASING EFFECT ON 22NM HIK-METAL GATE SCMOS INVERTER PARAMETERS

3.1 VTC analysis with Vinput sweep from 0v to 1v for every sweep of psubstrate of NMOS varying from -1v to +1v and nsubstrate bias fixed at +1v.

Fig.1 below shows the characteristics of Low Power model inverter's Psub sweep -1v to +1v while input of the inverter is changing from 0v to 1v. Since nmos is responsible for zero output ,the high output remains constant inspite of psubstrate(of nmos) variations. Ideally psubstrate should be 0v. With forward biasing of psubstarte the low level of output no longer remains at 0v.

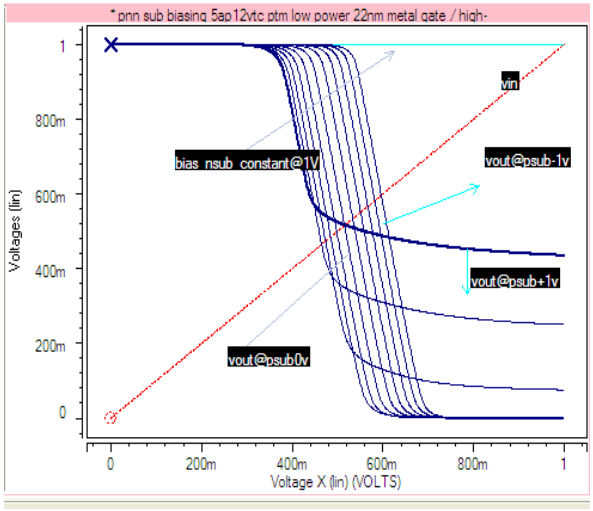

Fig. 1 Low power inverter with psubstrate variation from -1v to +1v.

Fig. 2 below shows the result of same as Fig. 1 but with high performance model. The transition slope is more steep in low power case.

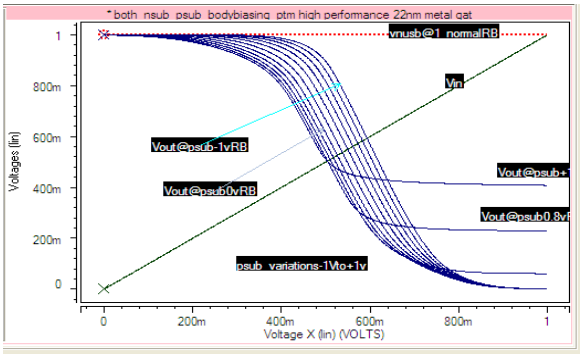

Fig. 2 high performance inverter with psubstrate variation from -1v to +1v.

Below are the graphs of low power model and High performance model inverter for current through Vdd

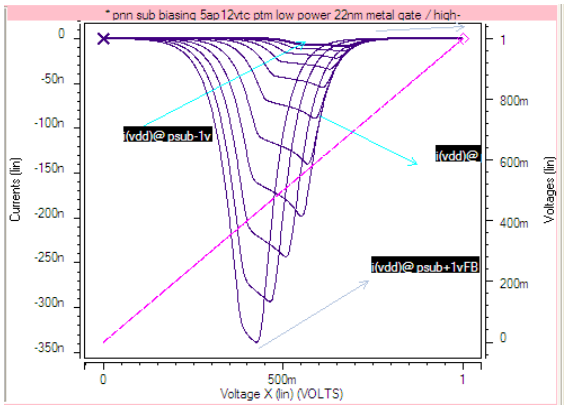

Fig.3 low power inverter's I(Vdd) with psubstrate biasing sweep

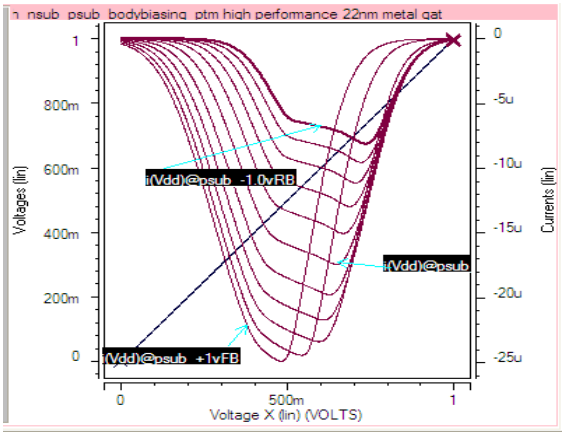

Fig. 4 High performance inverter's I(Vdd) with psubstrate biasing sweep

At the end Table I shows the VTC with psubstrate biasing sweep from -1v To +1v with Vinput sweep from 0v to 1v and nsubstrate at +1v.

3.2 VTC analysis with Vinput sweep from 0v to 1v for every sweep of nsubstrate of PMOS varying from -1v to +1v and psubstrate of NMOS bias fixed at 0v.

The graphs are shown below along with table II for comparison.

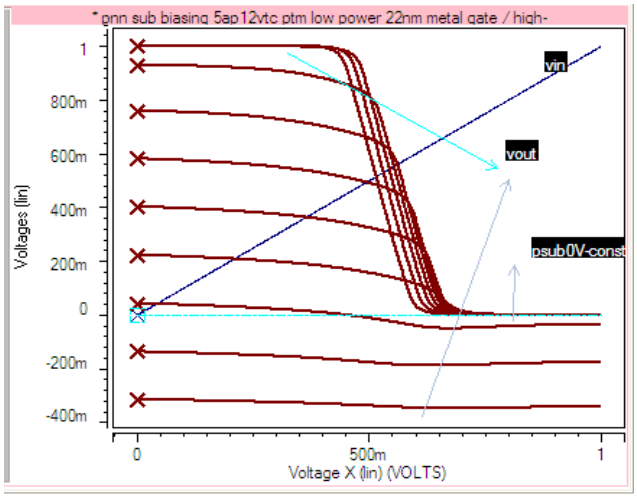

Fig. 5 LP VTC psub at 0V and PMOS nsuv varying from 1V to -1V

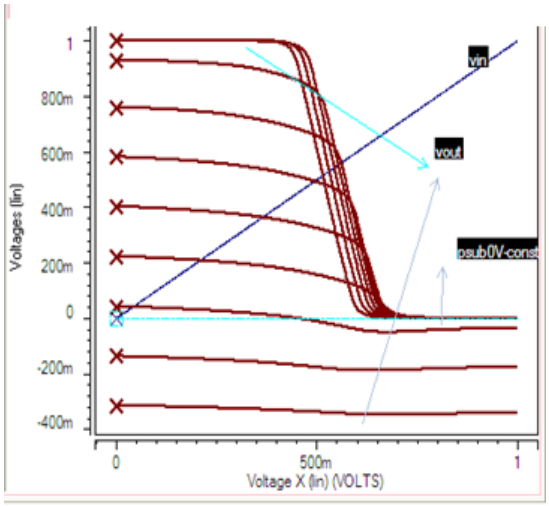

Fig. 6 HP VTC psub at 0V and PMOS nsuv varying from 1V to -1V

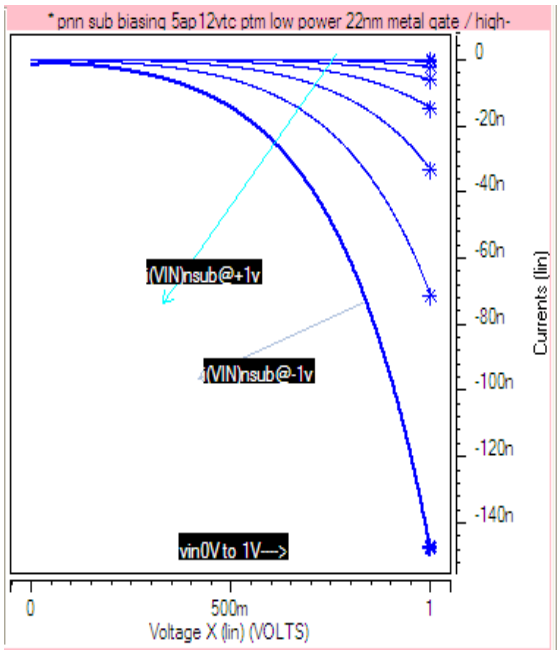

Fig 7 LP I(vin)with nsub +1v to -1V

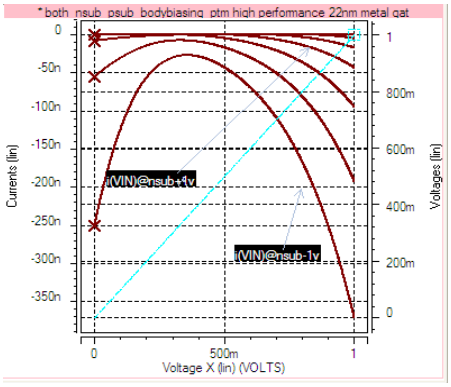

Fig. 8 HP I(vin)with nsub +1v to -1V

The above figure shows the behavior of Low power and High Performance models with nsubstrate biasing. These graphs are helpful in giving the idea of leakage at the input(and hence at the gate terminals)of an inverter with only nsubstrate biasing.

The two graphs below shows the drain currents of an inverter with two models. The drain currents of the nmos and pmos transistors of the inverter are equal and opposite and as expected , the amount of drain current is more in High performance model inverter. Higher the nsub bias in Forward Bias region ,more the drain current. Table II gives the comparative values of parameters for the two models.

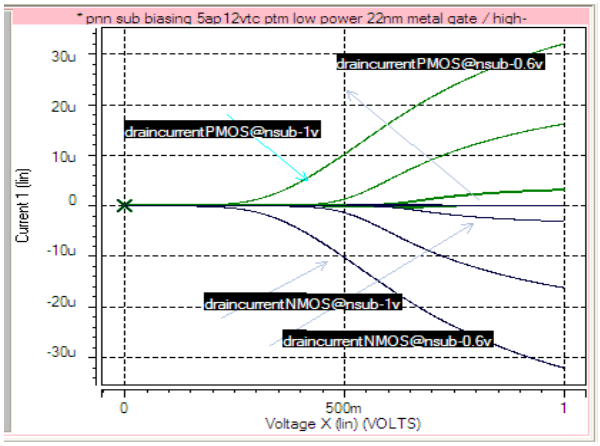

Fig 9 Lp Drain current of PMOS n nmos wid nsub biasing

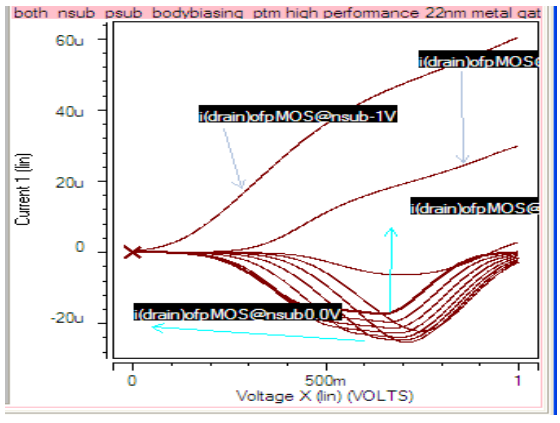

Fig 10 hp Drain I current of pmos with nsub biasing frm +1v to -1v

TABLE I

Comparison Table I VTC with substrate biasing sweep from -1v To +1v with Input sweep from 0v to 1v and substrate at +1v

		parameter	Low power CMOS HiKmG inverter Amp/Volts	Hi performance CMOS HiKmG inverter
Psubstrate sweep from -1v(reverse bias) to +1v(forward bias)	Vout	Max_@psub -1v	+1	+1
		Min @psub=-1v	0	0
	Max I@ Vin	for psub-1v to -0.6v	120P	68P
		for psub-0.8v	320p	246p
		for psub+1	920p	4.5n
	Max I@vdd 5* &6*	For psub=-1v	30n	8.09µ
		For psub=0v	70n	17.3 µ
		For psub=+1v	350n	25 µ
	Max Ipsub@psubstrate	Psub bias from -1v to 0.8v	0.2m	0.3m
		psub@+1v	10m	10ma
	Max I@gate	Psub bias from -1v to 0.6v	2p	50p
		psub@0.8v	210p	198p
		psub@+1v	800p	3250p

TABLE II

Comparison of VTC with nsubstrate biasing sweep from -1v to +1v with Vinput sweep from 0v to 1v and psubstrate at +0v

biasing	parameter	Nsub condition	LP CMOS HiKmG inverter Amp/Volts	Hi performance CMOS HiKmG inverter
Nsubstrate sweep from -1v(forward bias) to +1v(reverse bias)	Vout	Max_vout_@nsub +1v	+1	+1
		Min_vout @nsub=+1v	0	0
		Max_vout@nsub0V	0.6m	0.6
		Min_vout@nsub-1v	-0.3	-0.28
	Max I@ Vin	for nsub-1.0v	148n	371n
		for nsub-0.8v	72n	192n
		for nsub0vto +1v	0n	0n
	Max Ipsub@nsubstrate	Nsub bias from +1v to -0.8v	0m	0m
		nsub@-1v	8n	573p
	Max drain current with nsub biasing	Nsub bias=-1v	32µ	60.2 µ
		Nsub bias=-0.8v	16 µ	30 µ
		Nsub bias=+1v	0	8 µ
	Max I@gate of NMOS	Nsub bias = -1v	360p	1.51n
		Nsub bias =-0.8v	150p	240p
		nsub@+1v	50p	5.06p
	Max I@gate of PMOS	Nsub=-1	144n	.37 µ
		Nsub=-.8	68n	.192 µ
		Nsub=+1	0	0

CONCLUSION

The analysis of a 22nm Hi K-Metal Gate Technology inverter with Low power and high performance models of PTM helps us to look into the detailed behavior of the two transistors of the inverter. As expected the current and power dissipations are higher in high performance model, although they are functions of many other variables such as load capacitor, supply voltage and transistor size. The drain current increase in high performance case, for example, is almost 45%.The increase in gate leakage current is tremendous in HP model and runs into micro ampere against nano ampere as in Low power case.

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