Current Signatures: Application

Anne E. Gattiker and Wojciech Maly

Carnegie Mellon University, Pittsburgh, PA 15213

Abstract

Analysis of IC technology trends indicates that Iddq testing may be approaching its limits of applicability. The new concept of the current signature may expand this limit under the condition that an appropriate current-signature-based test methodology is developed. This paper is a first step toward such a goal. It is focused on current signature step detection in a noisy test environment. Application of current signatures in die selection and defect diagnosis is discussed as well.

1 Introduction

A great deal of attention has been devoted recently to the demise of Iddq testing. The reason is the diminishing difference between the Iddq currents of good and defective devices caused by increasing device off-current with decreasing minimum feature sizes [1]. At the same time, Iddq's ability to detect defects that are difficult to detect with voltage testing is more important than ever. For instance, gate oxide defects, known to be difficult to detect with voltage tests [2-4], are likely to become more important due to the expected decrease in gate oxide thickness.

As technology advances, defect sensitivity, such as that provided by Iddq testing in the past, is increasingly needed not only for testing, but also for defect diagnosis. The SIA-prescribed requirement to keep the cost per transistor constant while feature sizes decrease and die sizes increase make high yields a must [5,6]. The trend toward shorter windows between introductions of one new product and the next makes imperative not just high yields, but rapid yield-learning. To achieve rapid-yield learning, fast, successful defect diagnosis must be accomplished [7]. The increasing frequency of occurrence and importance of low-current-causing defects, however, makes traditional test-based techniques less and less effective. In addition, increasingly complex functions on larger chips make creating test sets for defect location more and more difficult. These facts combined indicate a need for new defect diagnosis techniques that can handle low-current defects without placing strict new requirements on diagnostic test sets.

The notion of the current signature was introduced in [8]. Current signature testing seems to be a powerful concept (especially in the presence of high IC "normal" background current) because it uses the difference between consecutive Iddq measurements rather than current values themselves to detect a defect. Consequently, even a relatively small Iddq "abnormality" can be used to indicate a defective IC even if the "normal" background current is high. Of course, the difficulty is in distinguishing between defect-generated Iddq differences and natural differences caused by measurement noise or differences which are due to normal circuit operation.

Current signatures provide insight into the physical nature of the mechanism causing elevated Iddq. In doing so they make it possible to discriminate between dies with difficult-to-detect but harmful defects from other dies that contain no such defects. They also provide a more detailed description of Iddq results than the traditional description, a pass/fail (below/above a threshold) on each test vector. This more detailed description can be used in concert with defect location methodologies, such as those described in [9-17] to improve the resolution with which defects can be diagnosed.

The current signature is a tool which has strong potential for extending the useful life of Iddq testing; however, the potential can be realized only if an appropriate current-signature-based test methodology is developed. This paper is a first step toward that goal.

The paper is organized as follows. Section 2 begins with a brief explanation of the basic current signature concept. Section 3 follows with a more detailed discussion of the potential usefulness of current signatures for die selection and defect diagnosis. Section 4 then discusses practical application of current signatures in a realistic test setting. Section 5 finishes with some conclusions.

2 Current signature concept [8]

A die's current signature uses all Iddq measurements, rather than making a comparison to a single threshold Iddq value. It is created by ordering all the Iddq measurements by magnitude. Doing so presents the Iddq results in a form that is useful for observing steps between groups of measurements of similar magnitude.

Figure 2 shows current signatures for defect-free and defective versions of the very simple example circuit shown

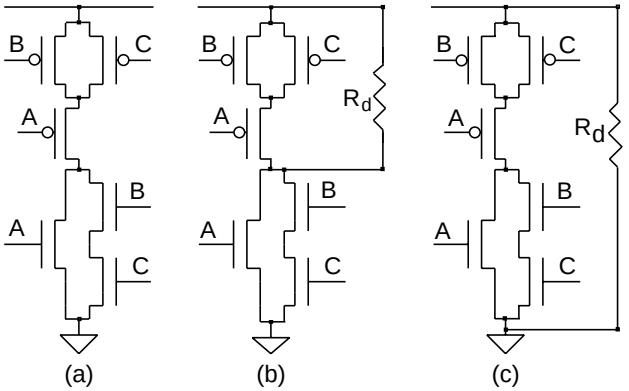

Figure 1. Defect-free (a) and defective circuits (b and c).

in Figure 1 (assumed to be built with minimum-sized transistors). The circuit in Figure 1a is defect-free and has a single-level current signature of very low magnitude. The circuit in Figure 1b has a multilevel signature, with a low level corresponding to input combinations that do not turn on the pull-down path and higher levels corresponding to input combinations that do turn on the pull-down path. The circuit in Figure 1c has a single level current signature of higher magnitude, depending on the value of the resistance of the short.

It is clear from the example circuits that key information about the defect in a static CMOS circuit is contained in the number of levels of static current and the magnitude of the levels of static current. Current signatures provide a convenient form for depicting such characteristics and, as a result, should be useful for both die selection and defect diagnosis purposes.

3 Current signature potential

3.1 Die selection

In order to support the claim that current signatures are applicable for die selection purposes, it is useful to distinguish between two types of current faults: those caused by "passive" defects and those caused by "active" defects.

We consider passive defects to be those defects that involve only non-switching nodes of the circuit. They provide a direct, static current path between Vdd and GND and produce a constant level of current on all test vectors. Examples include direct shorts between Vdd and GND and leaky non-switching reversed-biased pn junctions, such as between the well and substrate. Figure 1c shows an example of a circuit with a passive defect.

"Active defects," on the other hand, involve switching nodes of the circuit. A short between a switching node and any other node is an example of an active defect. Figure 1b shows an example of a circuit with an active defect.

Observe that because passive defects do not involve switching nodes of the circuit, they do not have a direct impact on the quality of information-carrying signals in the

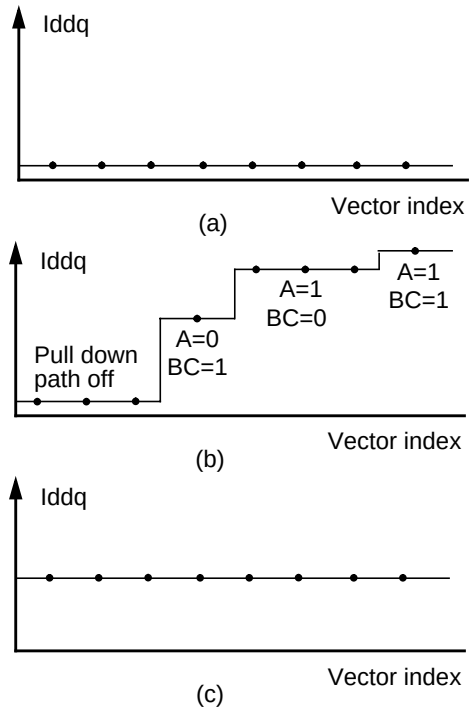

Figure 2. Current signatures for circuits in Figure 1.

circuit and, as such, are unlikely to cause a fault. On the other hand, "active" defects do affect switching nodes and therefore may cause performance failure. Our goal in die selection, then, will be to reject dies that have active defects, without rejecting those that have only passive defects or no defects at all (i.e., only pn junction and subthreshold background leakage current).

Figure 3 explains our die selection goals. Assume that there is some low level of current, lower than any active defect-related current (line a). Assume also that there is some other level of current that always indicates the existence of an unacceptable defect (line b). This limit could be set, for example, to handle concern for static power dissipation or reliability.

Region B, which lies in between these two limits, is the region of interest for current signatures. This is the region where the currents are lower than the highest acceptable background leakage or passive defect current, but high enough to indicate the possible existence of an unaccept-

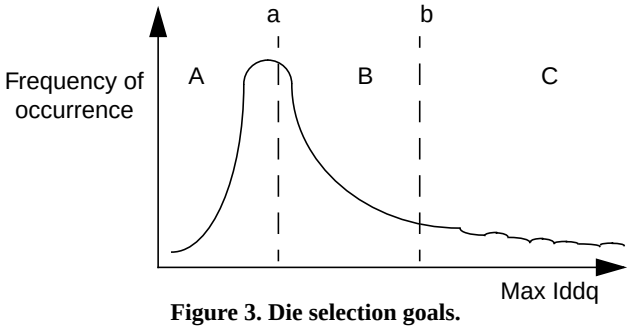

Figure 3. Die selection goals.

able defect. In this region, we need to distinguish dies containing active defects from those not containing active defects. Note that these are defects that would be missed by traditional Iddq testing, unless the Iddq limit is set at line a, in which case a substantial quantity of good dies would be rejected.

We say that a defect is "activated" when the required transitor(s) is turned on so that abnormal current flows due to the presence of the defect. We call the path through which the static current flows the "activation path." The active defect in Figure 1b has three different activation paths. Note that a passive defect is always activated and provides its own activation path. We use the term "leakage path" to cover both the background leakage current that flows when there is no defect on a circuit or when no defect is activated and the activation paths associated with active and passive defects.

Note that there are exceptional cases where an active defect is always activated, such as a short between an inverter input and output. Nevertheless, such shorts will still nearly always have multiple activation paths, because the driver and/or following gates will provide different activation paths.

Given the above terms, we can say that a circuit with an active defect is characterized by having more than one leakage path. Observe that the presence of more than one leakage path is reflected as a "step" in a current signature. As a result, one can detect the vast majority of active defects by detecting a step in the current signature.

3.2 Defect diagnosis

Current signatures are useful for defect diagnosis purposes because they provide a mechanism for reading key information about the leakage paths that exist on a die from the results of Iddq testing. This information can be used to increase the resolution of Iddq defect-location algorithms, such as those described in [9-17]. To illustrate this application, we refer to Figure 4a and Table 1. The circuit in Figure 4a is assumed to be built with minimum-sized transistors. The goal is to distinguish between two different defects: D1, a zero resistance bridge between node x and Vdd, and D2, a zero resistance bridge between node y and GND. The test set assumed to be applied is shown in the first column of Table 1. Column 2 gives the result of single-threshold Iddq testing on each vector in the presence of D1. Column 3 provides the same information in the presence of D2. The fact that the results are identical for the two defects demonstrates that they cannot be distinguished based on single-threshold Iddq results under the given test set (which happens to be exhaustive).

(Note that the two defects cannot be distinguished via voltage test diagnosis either, where D1 is modeled as a stuck-at-1 and D2 is modeled as a stuck-at-0. Both defects result in the output of the circuit being stuck-at-1 for any input vector.)

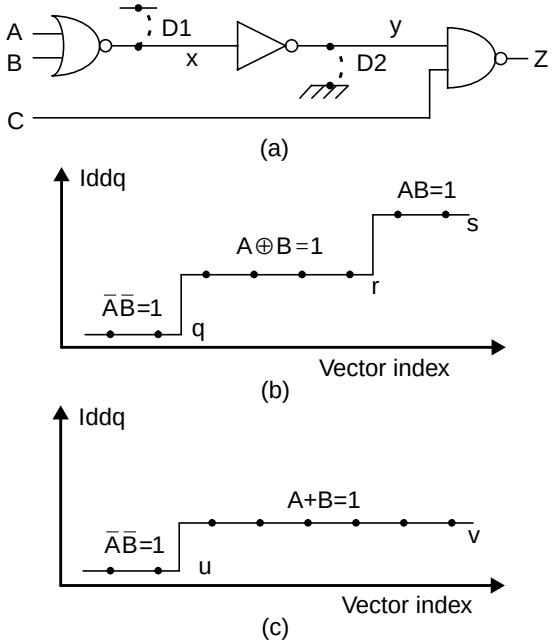

Figure 4. Example faulty circuit that contains either one of two possible zero resistance bridge defects (a); current signatures for example circuit in presence of D1 (b) or D2 (c).

Figure 4b and Figure 4c show the current signatures that result under the given test set. With D1 present, all defect current will flow through the defect and some subset of the pull-down network of the NOR. Because D1 is shorted to Vdd, no Iddq will flow in the inverter. D1 creates three unique leakage paths, which are labelled on the figure q, r and s. For D2, all defect current will flow through the inverter PMOS device and the defect. Because D2 is shorted to GND, no Iddq will flow in the NAND. D2 creates two unique leakage paths, labelled u and v. Columns 4 and 5 of Table 1 give the current signature results for the circuit in the presence of D1 and D2, respectively. In the presence of D2, input vectors 3-8 give the same result, while in the presence of D1, input vectors 7 and 8 give a different result from that of vectors 3-6. This difference in

Table 1. Test results for example circuit

Inputs			Single threshold Iddq test results		Current signature results (level labels)	
A	B	C	D1	D2	D1	D2
0	0	0	pass	pass	q	u
0	0	1	pass	pass	q	u
0	1	0	fail	fail	r	v
0	1	1	fail	fail	r	v
1	0	0	fail	fail	r	v
1	0	1	fail	fail	r	v
1	1	0	fail	fail	s	v
1	1	1	fail	fail	s	v

the results indicates that the two defects are distinguishable using current signatures. (Note that we do not need to pay attention to the absolute magnitudes of the current, only to the existence of "steps" and which vectors correspond to each step.)

4 Practical application

From the above discussion, we can conclude that the key to both die selection and defect diagnosis is step detection. For die selection, a step indicates the existence of at least two distinct leakage paths and that, in turn, indicates the presence of an active defect. For defect diagnosis, a step indicates a change between groups of measurements taken from one leakage path and those taken from another. Finding and characterizing all the steps means finding and characterizing all the leakage paths.

As discussed in Section 2, a step in a current signature is a difference between two consecutive measurements when all measurements are sorted according to magnitude. However, it is possible for two measurements to be different even if they are from the same leakage path. The first reason for the existence of such a difference is measurement noise. The second is that background current is not constant; instead it depends on circuit structure. This section discusses methods for finding and characterizing steps in the presence of these two obstacles.

To support our discussion we use both artificially synthesized and real die Iddq measurements. The real die examples are taken from an extensive CMOS circuit test experiment [19,20]. In this experiment, a large static CMOS circuit was tested with a number of testing methods, including Iddq measurements executed on almost 200 vectors. The Iddq measurements were repeated at three different test levels: at the wafer level, after the dies were packaged, and after the dies underwent burn-in. Voltage tests were also applied.

4.1 Noise

In reality, the same leakage path can produce different measured current each time it is sampled due to noise in the measurement system. We assume the noise follows a normal distribution. Iddq measurements made on a real product support this assumption. Figure 5 shows an example.

To depict a typical current signature obtained from a noisy test environment, Figure 6 shows an artificially synthesized illustration of measurements made on a circuit that has a gate affected by a defect similar to the one shown in Figure 1b. The measurements are shown in execution order in Figure 6a. We assume there are four leakage paths in the defective circuit, where the measurements taken on each of the four paths are represented with different plotting symbols. Figure 6b shows the same measurements sorted by magnitude. Here we assumed the range of currents in each path to be due to noise.

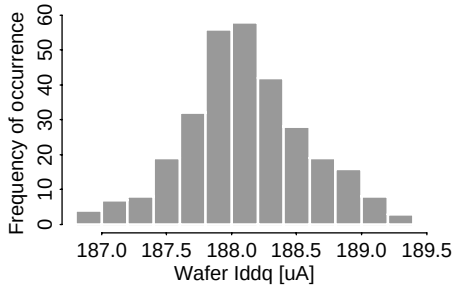

Figure 5. 300 measurements on a single vector on a single die.

In reality, the pattern from Figure 6 can be seen on a large number of defective dies. One of them is shown in Figure 7, where essentially all Iddq signature steps can be distinguished fairly easily (because the defect-generated step in the signature is much above the noise level).

Figure 8, on the other hand, shows an example of a die with a passive (i.e. no-step) current signature. Here, we

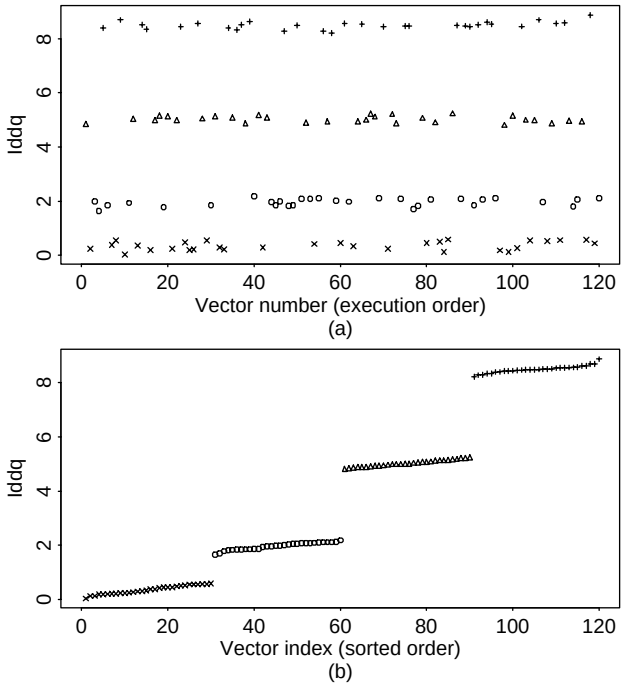

Figure 6. Synthetic illustration 1: measurements in execution order (a); current signature (b).

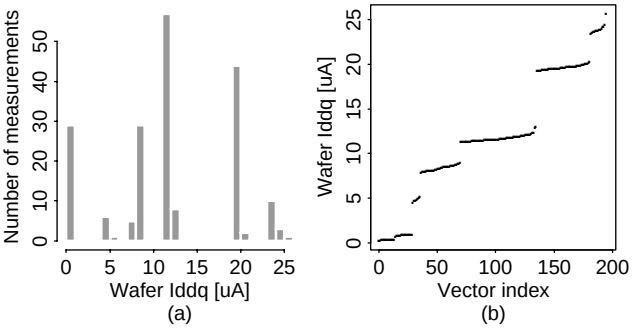

Figure 7. Die A: histogram of wafer Iddq measurements (a); current signature (b).

contend any differences among measurements are due to measurement noise. This die was confirmed by physical failure analysis to contain a defect in an inactive (non-switching) gate.

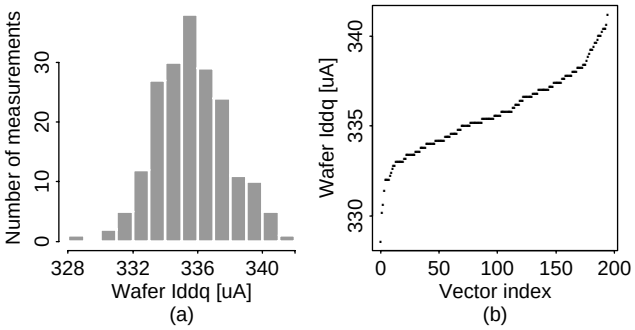

Figure 8. Die B: histogram of wafer Iddq measurements (a); current signature (b).

4.1.1 Die selection in the presence of noise

Our goal in die selection is to establish whether or not more than one leakage path exists on the die. To be practical for production testing, the die selection methodology should not require storing measurements for post-processing and should require applying as few vectors as possible.

Ideally, die selection would proceed by taking Iddq samples, one by one, and each time testing the hypothesis that the samples are from a single normally distributed random variable. Test execution would stop when the hypothesis can be rejected with sufficient confidence. In practice, however, the tester cannot reasonably do such a computation on the fly. Instead, that method can be approximated by examining each measurement and determining if it is sufficiently different from those that precede it to allow the conclusion that it is very likely to have been taken from a different leakage path.

In general, the amount of noise generated by the measurement system should be predictable. We define H_{noise} as the maximum Iddq minus the minimum Iddq from any single leakage path and M as the difference between the maximum and minimum measurements taken on the die. If $M > H_{noise}$, we reject the die.

Note that H_{noise} is likely to be a function of the magnitude of the measurement because most measurement devices have different measurement resolutions in different current ranges. This effect can be easily accounted for by defining H_{noise} relative to the measurements on which the comparison is being made.

Note also that we defined M based on all the measurements taken on the circuit. However, during actual die selection, a running maximum and minimum of the measurements can be kept and the test terminated as soon as two measurements are encountered that are sufficiently different. A more detailed description of the application of current signatures for production testing is given in [18].

4.1.2 Defect diagnosis in the presence of noise

Our goal in defect diagnosis is to determine the number of leakage paths, the magnitude of the current corresponding to each leakage path and the set of vectors that correspond to each path. In the presence of noise, the current corresponding to each leakage path can be seen as an independent and typically normally distributed variable. In essence, therefore, the defect-diagnosis task is identification of all independent random variables in a given set of Iddq measurements. Standard statistical methods, such as clustering techniques [21,22], can be applied to solve this problem. In most cases, we expect the leakage path currents to be spaced far enough apart relative to the measurement noise that measurements corresponding to different leakage paths can be distinguished as easily, as in the case of Die A of Figure 7 and Die C shown in Figure 9 (Note that two distinct leakage paths are visible on Die C, even though the maximum Iddq is only about 1μA.)

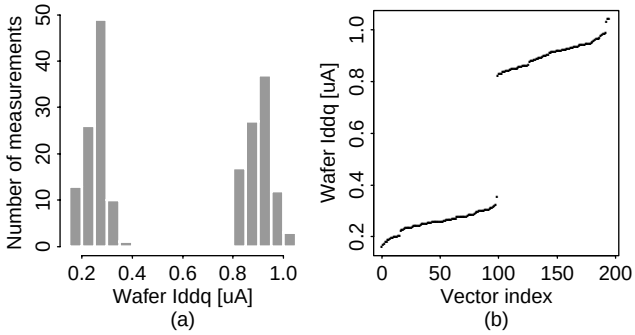

Figure 9. Die C: histogram of wafer Iddq measurements (a); current signature (b).

However, one must also consider cases in which the measurements taken on two different leakage paths overlap. Figure 10 shows a synthesized illustration of two distributions that overlap. In such a case there exist a number of possible solutions. The first is based on the possibility that the Iddq measurements histogram is bi-modal (or multi-modal). In that case, if we would test the hypothesis that all measurements are from a single normal distribution, we would be able to reject this hypothesis with a high level of confidence and a one-dimensional clustering algorithm could be applied to separate the measurements.

Another option is to perform multiple measurements on the same device, which should vastly enhance our ability to recognize independent Iddq paths. The potential of such an approach is illustrated via the synthesized example shown in Figure 10c, which describes results of double-socketing Iddq testing. (We use the term “socketing” to refer to an application of the test set.) Observe that the measurements from a hypothetical second socketing are plotted against the measurements on the same vectors from the first socketing. As in Figure 6, measurements taken on different leak-

age paths are represented with different plotting symbols. Given that the differences among currents within a distribution are due to random noise, vectors that originally fell in the range of one distribution should fall again within the range of the same distribution. The two measurements taken on the same vector during the two different socketings are independent, so within a single distribution, the measurements on the same vectors taken at the two socketings are uncorrelated.

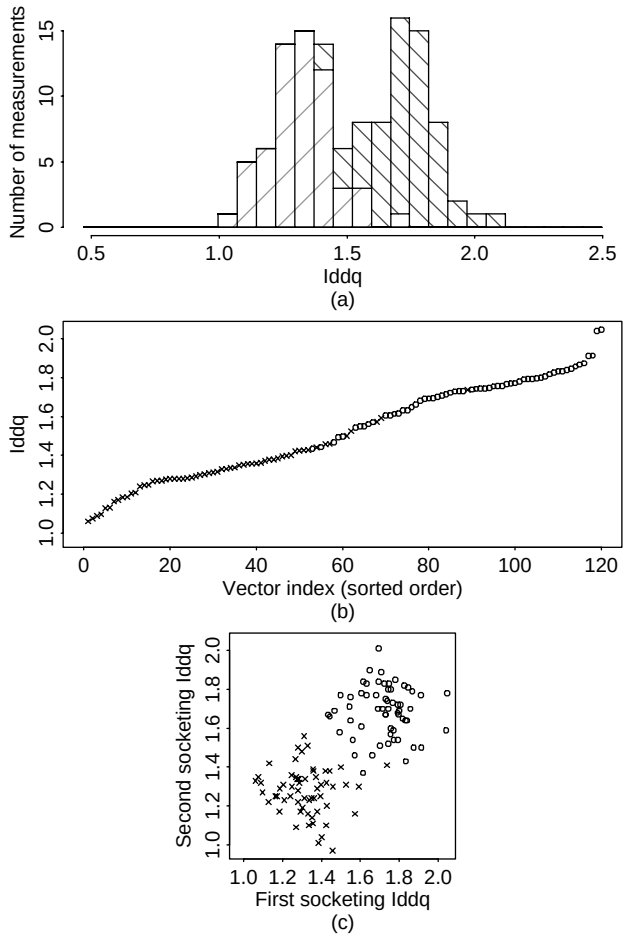

Figure 10. Synthetic illustration 2: histogram (a); current signature (b); second socketing measurement vs. first socketing measurement on each vector (c).

Note that it becomes easier to separate the measurements when we add the information of a second measurement on each vector. If we added a third measurement on each vector, separation would become even easier. Theoretically, it should be possible to keep adding new information from re-applications of the test set, each time adding a dimension to the clustering problem and making the separation easier. Practical limits may preclude applying the test more than a few times, but using the measurements on repeated test applications has the potential to be a very valuable way to improve the ability to separate samples from closely-spaced leakage paths.

Figure 11 and Figure 12 show the real die Iddq measurement results for two dies, Die D and Die E for which

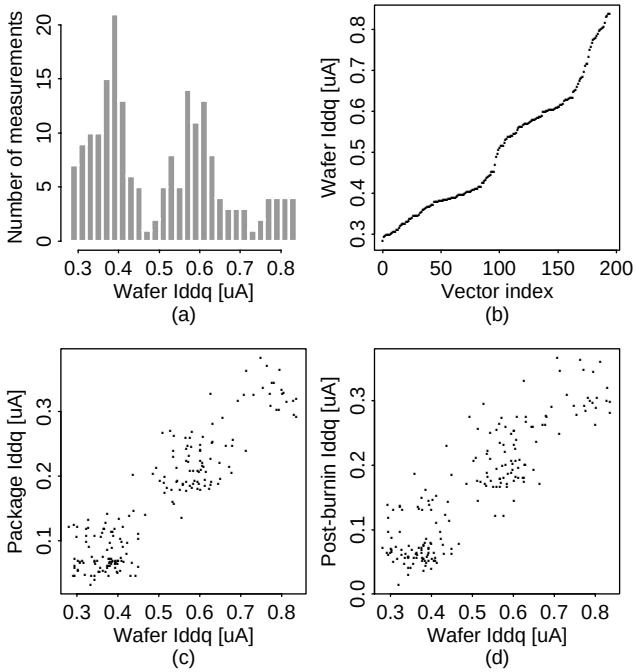

Figure 11. Die D: frequency of occurrence of wafer Iddq measurements (a); current signature (b); package vs. wafer test measurement on each vector (c); post-burnin vs. wafer test measurement on each vector (d).

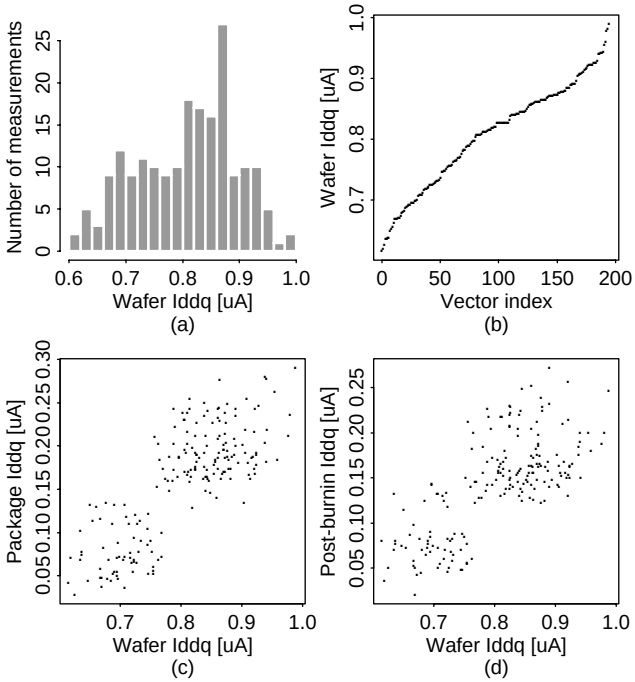

Figure 12. Die E: frequency of occurrence of wafer Iddq measurements (a); current signature (b); package vs. wafer test measurement on each vector (c); post-burnin vs. wafer test measurement on each vector (d).

double socketing measurements are plotted. (Note that for the real dies, the "second socketing" results were done after the dies underwent packaging. Note also that the packaged die measurements were done at a different temperature, 25˚C instead of 50˚C). Results from a third socketing, taken after the die underwent burnin are also given. Observe that all the plots characterizing Die D indicate the existence of three independent current paths; however the best evidence is provided by the scatter plots in Figure 11c and Figure 11d.

The potential of "double socketing" is even more evident in Figure 12. Observe that neither the Iddq histogram (Figure 12a) nor the one-dimensional current signature (Figure 12b) can be used easily to detect the number of current paths in Die E. However, it is quite evident from the scatter plots (Figure 12c and Figure 12d) that there must be two independent Iddq paths, which of course implies the existence of an active defect. Observe that in this case the ratio of noise to the size of the step is close to one and that detection of the active defect was accomplished on a very low current level.

Figure 13 shows a real die example where the separation between leakage paths is not easily visible, even with measurements from two socketings. This situation can occur when the measurements from several leakage paths overlap. Figure 14 shows results obtained from ten additional applications of the test set. To show the results in two dimensions, the average measurement on each vector of the

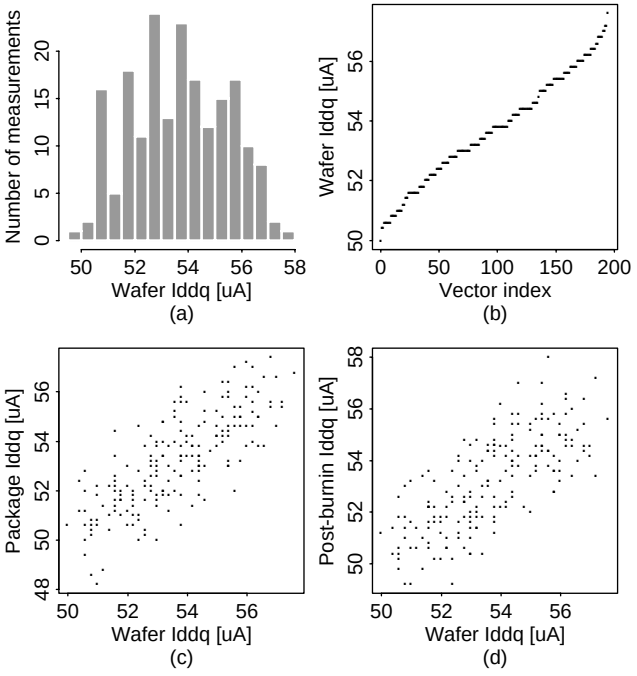

Figure 13. Die F: frequency of occurrence of wafer Iddq measurements (a); current signature (b); package vs. wafer test measurement on each vector (c); post-burnin vs. wafer test measurement on each vector (d).

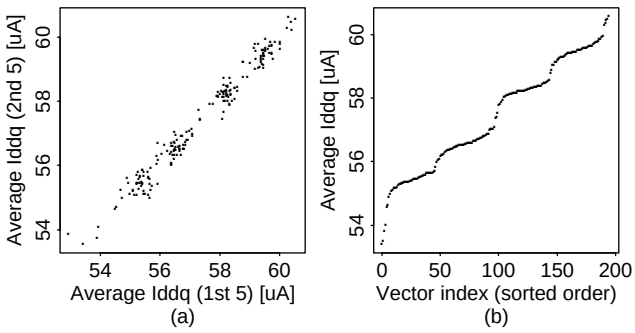

Figure 14. Die F: results of 10 repeated applications of the test set. Average measurements on each vector for second 5 applications vs. first 5 (a); average of 10 measurements on each vector in sorted order (b).

second five applications of the test set is plotted against the average on the same vector of the first five applications of the test. Here, the measurements separate into clusters, indicating several distinguishable leakage paths. The improved separation in Figure 14 compared to Figure 13 results from the fact that the averages plotted in Figure 14 give improved approximations of the true means of the distributions they sample compared to individual measurements, as plotted in Figure 13. Figure 14b shows in sorted order the average of all ten measurements taken on each vector.

Figure 15 shows the results for another die, Die G, where again it is difficult to distinguish measurements com-

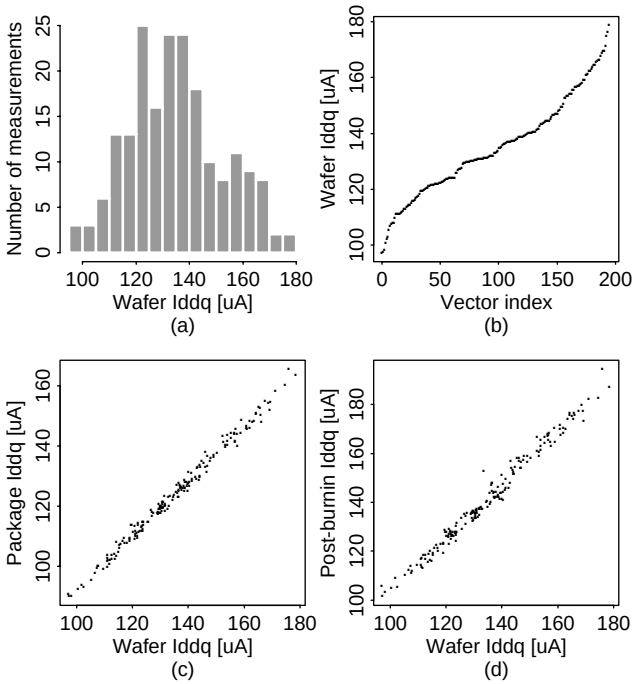

Figure 15. Die G: frequency of occurrence of wafer Iddq measurements (a); current signature (b); package vs. wafer test measurement on each vector (c); post-burnin vs. wafer test measurement on each vector (d).

ing from independent distributions. Figure 16a shows the results of the averages of the second five measurements on each vector versus the first five. Here a few clusters of points are visible, but a large number of points do not appear to fall into a cluster. The clusters are easier to see as flat segments between steps in Figure 16b, which plots in sorted order the average of the ten measurements taken on each vector. The fact that the points fall nearly on a straight line in Figure 16a indicates that the averages shown closely approximate the true mean of the distributions they sample. The points that do not fall into clusters, then, appear to represent leakage paths causing current of unique magnitudes. In this case, then, there are nearly as many (and very possibly more) unique ways for current to flow on the die as there are vectors. Our experience suggests that the vast majority of dies do not have such a very large number of leakage paths, but the example shows how the multiple socketing technique can be used to identify such cases.

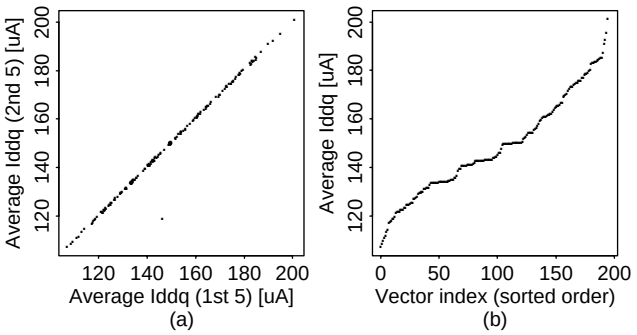

Figure 16. Die G: results of 10 repeated applications of the test set. Average measurements on each vector for second 5 application vs. first 5 (a); average of 10 measurements on each vector in sorted order (b).

Figure 14 and Figure 16 show repeated test application results for dies that show clear evidence of active defects. For comparison, Figure 17 shows similar results for a die that appears to have only a passive defect. The plots seem to confirm that the die contains only a single leakage path. (The discretization visible in the graph is a result of finite tester resolution.) Note that multiple-leakage path cases can be easily distinguished from single-leakage path cases without distinguishing all leakage paths simply by looking for correlation between the measurements at the different socketings. (First and second socketing measurements should not be correlated when they are from a single leakage path.)

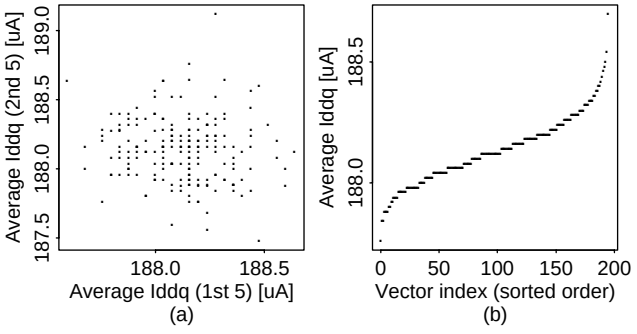

Figure 17. Figure H: results of 10 repeated applications of the test set. Average measurements on each vector for second 5 application vs. first 5 (a); average of 10 measurements on each vector in sorted order (b).

Note also that in practice it is often the case that testing results from more than one application of the test are available, as they were for our example dies, so that the multiple-socketing technique may not require any specially-dedicated applications of the test. Of course, in that case, the fact that the die may have undergone changes between the socketings must be taken into account. Cases where the number of leakage paths changes (e.g. due to a change in the nature of a defect) can be identified by careful analysis of the scatter plots. However, we expect it to be the case for most dies that, while the magnitude of the current of a given leakage path may change, the same paths will be visible at various test levels, as they were for the example dies. In such cases, the above techniques can be applied successfully without requiring any extra test effort.

4.1.3 Sample size

In general our ability to draw conclusions about the random variables from which the sample comes increases with the sample size. In addition, it is useful for the sample sizes from each of the leakage paths to be balanced, since balanced sample sizes are more amenable to successful application of separation techniques, such as clustering [21]. Fortunately, however, additional samples can be taken on existing test vectors. As a result, getting additional samples requires only extra test execution, not extra test generation. In particular, vectors that activate leakage paths that are difficult to activate (e.g. because they involve a difficult-to-control node) can be repeated to get additional samples. Note also that the more widely-spaced the current levels corresponding to different leakage paths are, the fewer are the samples needed to distinguish them.

Naturally, there has to be at least a single sample from a leakage path for its existence to be known. The fault coverage metric for defect diagnosis and die selection tests can be modified accordingly. For tests that will be used for die selection, the requirement is only that at least two leakage paths are sampled. For defect diagnosis tests, the more unique leakage paths that are activated, the better. The extra test generation effort for defect diagnosis-targeted tests is likely to be well-justified. The gains can be great in terms of defect diagnosibility and the cost very low relative to physical failure analysis.

4.2 Circuit personality

One of the key benefits of the differentially-based methodology for die selection suggested by the current signature

idea is that it is naturally well-suited to factoring out die-to-die variations in background leakage current. In general, variations in background current are caused by global processing variations, which act in such a way that if the background leakage is high on one vector, it is likely to be similarly high on all vectors. Since the current signature methodology focuses on steps between groups of similar measurements, it will be naturally immune to these variations.

Figure 18 shows plots of the measurements on one vector versus another for a few pairs of vectors. Each point on the graph represents the measurements taken on a pair of vectors for a single die. Data are shown for approximately 850 dies that passed all voltage testing applied and had a maximum Iddq at all testing levels of less than 1μA. The high degree of correlation seems to confirm our assumption that background current is likely to be similarly high on all vectors.

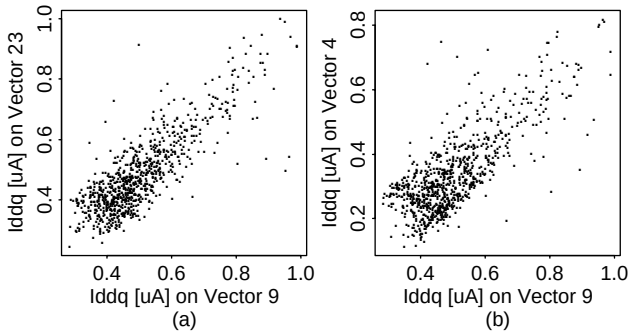

Figure 18. Background current on different vectors.

Despite the fact that background current on different vectors will tend to vary in a like fashion, there may still be vector-to-vector differences, as a result of circuit structure [23]. Some vectors may cause unusually high subthreshold leakage current, for example, if they put the circuit in a state where many large transistors are in an off state. The fact that such vector-to-vector differences result from the circuit structure, however, means that they should be consistent from one die to the next. As a result, it should be possible to define a "circuit personality" current signature, which can always be subtracted from the measurements on a given circuit. Any remaining steps should be due to a defect rather than the circuit structure. In practice, for die selection, that may mean masking the measurements made on certain vectors that are known to give elevated background current. For defect diagnosis, it should be possible to fully characterize the circuit personality signature for subtraction.

Figure 19 shows an example of a "circuit personality" signature for a real product. The graph represents the average measurement taken on each vector over the approximately 850 dies described above. The lines associated with each point represent the 95% confidence intervals on the means. Note that a few vectors stand out.

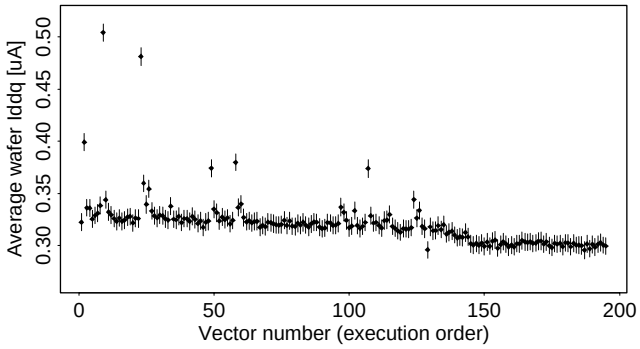

Figure 19. "Circuit personality" signature for real product.

For this product, the same vectors consistently produce the highest current on these approximately 850 very-low-current dies. Given that fact, a reasonable way to ensure that steps due to normal background current variation are not confused with those due to active defects is to perform masking on those few vectors. Figure 20a shows that the vast majority of "steps" in the current signatures of these dies are less than 20nA. Higher steps do exist; however, if the measurements on just the top two vectors from Figure 19 are masked, the number of steps exceeding 100nA reduces from almost 150 to under 20.

Note that the "circuit personality" subtraction is necessary only when the resulting "step" is large enough to be confounded with a step that could otherwise be due to a harmful active defect. Otherwise the natural immunity of the current signature technique to processing-condition-related variations in the background current should alone suffice to allow for Iddq-based testing that is effective in the face of high background current.

Note also that the natural immunity of current signatures to processing variations does rely on test vectors being similarly affected by different processing conditions. The authors can imagine cases where this rule may be violated. One such case could occur as a result of processing variations affecting various circuit structures in different ways. For example, abnormally low p-well doping causes

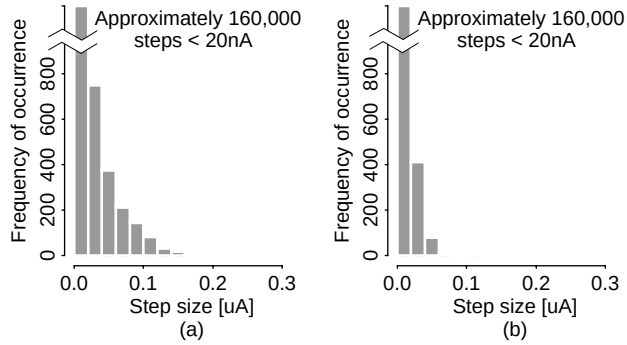

Figure 20. Histogram of all current signature steps for approximately 850 dies (a); same as Figure 20a, but with steps occurring on two vectors removed (b).

unusually low NMOS threshold voltages, but does not have the same effect on PMOS threshold voltages. If some vector turns off an unusually large number of NMOS devices, then, the rule could be violated. It is also necessary to mention that the decrease of minimum feature size is likely to aggravate ambiguity in the definition of the circuit personality signature. The reason is the expected increase in the variance of transistor off-currents.

4.3 Discussion

The above examples illustrate the potential of current signatures to be extremely sensitive defect indicators. In order to assess the die selection potential of current signatures for any particular test effort, the specific process/ design combination under test should be characterized to determine the frequency of occurrence of low current-causing active defects. The larger is region B (see Figure 3 in Section 3.1), the more effect the application of current signatures will have on the escape rate. In addition, the position of the test strategy in the trade-off between quality required of outgoing dies and test effort should be determined. As the quality requirements move toward a need to reject dies closer to region A, current signatures become more and more important. For applications where extremely high quality is required, they may prove to be indispensable.

5 Conclusions

From our study, we conclude that current signatures give a uniquely detailed picture of the static current behavior of defective and defect-free dies. This detailed picture can be very useful as a sensitive indicator of defects, even if they cause only a low level of Iddq. It can also be useful as tool for defect diagnosis. In particular, it can be used to distinguish between defects that cannot be distinguished using the results of traditional Iddq testing. Here we have presented strategies for applying current signatures in a realistic application environment, so that the potential of current signatures can be exploited as a powerful, high-resolution testing tool.

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References

[1] T. Williams, R. Dennard, R. Kapur, M. Mercer and W. Maly, “Iddq Test: Sensitivity Analysis of Scaling,” ITC, Oct. 1996, pp. 786-92.

[2] C. Hawkins and J. Soden, “Electrical Characteristics and Testing Considerations for Gate Oxide Shorts in CMOS ICs,” ITC, Nov. 1985, pp. 544-55.

[3] L. Horning, J. Soden, R. Fritzemeier and C. Hawkins, “Measurements of Quiescent Power Supply Current for CMOS ICs in Production Testing,” ITC, Sept. 1987, pp. 300-9.

[4] R. Rodriguez-Montanes, J. Segura, V. Champac, J. Figueras and J. Rubio, “Current vs. logic Testing of Gate Oxide Short, Floating Gate and Bridging Failures in CMOS,” ITC, Oct. 1991, pp. 510-18.

[5] Semiconductor Industry Association (SIA), The National Technology Roadmap for Semiconductors, 1994.

[6] W. Maly, “Testing-Based Failure Analysis: A Critical Component of the SIA Roadmap Vision” to appear in Proc. Int’l Symp. on Testing and Failure Analysis, 1997.

[7] W. Maly, H. Heineken, J. Khare, and P.K. Nag, “Design for Manufacturability in Submicron Domain,” Proc. of ICCAD, Nov. 1996, pp. 690-697.

[8] A. Gattiker and W. Maly, “Current Signatures,” IEEE VLSI Test Symposium, April 1996, pp. 112-117.

[9] D. Burns, “Locating High Resistance Shorts in CMOS Circuits by Analyzing Supply Current Measurement Vectors,” Int’l Symp. for Testing and Failure Analysis, November 1989, pp. 231-237.

[10] S. Chakravarty and M. Liu, “Algorithms for Current Monitor Based Diagnosis of Bridging and Leakage Faults,” Design Automation Conference, 1992, pp. 353-356.

[11] S. Naik and W. Maly, “Computer-Aided Failure Analysis of VLSI Circuits Using I_{DDQ} Testing”, IEEE VLSI Test Symp., April 1993, pp. 106-108.

[12] S. Millman and J. Acken, “Diagnosing CMOS bridging faults with stuck-at, Iddq and Voting Model Fault Dictionaries,” IEEE Custom Integrated Circuits Conf., 1994, pp. 17.2.1-4.

[13] R. Aitken, “A Comparison of Defect Models for Fault Location with Iddq Measurements,” ITC, Oct. 1993, pp. 1051-60.

[14] Y. Kwon and D. Walker, “Yield Learning via functional Test Data,” ITC, Oct. 1995, pp. 626-635.

[15] R. Aitken, “Modelling the Unmodellable: Algorithmic Fault diagnosis,” ITC Lecture Series II, October 1996, Lecture 2.2.

[16] D. Vallett, “An overview of CMOS VLSI Failure Analysis and the Importance of Test and Diagnostics,” ITC Lecture Series II, October 1996, Lecture 2.1.

[17] P. Nigh, D. Forlenza and F. Motika, “Application and Analysis of Iddq Diagnostic Software,” ITC 1997.

[18] A. Gattiker, P. Nigh, D. Grosch and W. Maly, “Current Signatures for Production Testing,” IEEE International Workshop on Iddq Testing, October 1996, pp. 25-28.

[19] P. Nigh, W. Needham, K. Butler, P. Maxwell and R. Aitken, “An Experimental Study Comparing the Relative Effectiveness of Functional, Scan, Iddq, and Delay-Fault Testing,” VLSI Test Symposium, April-May 1997, pp. 459-463.

[20] P. Nigh, W. Needham, K. Butler, P. Maxwell, R. Aitken and W. Maly, “So what is the optimal test mix? A discussion of the SEMATECH Methods Experiment,” ITC, Nov. 1997.

[21] R. Duda and P. Hart, Pattern Classification and Scene Analysis, John Wiley & Sons, New York, NY, 1973.

[22] R. Johnson and D. Wichern, Applied Multivariate Statistical Analysis, Prentice-Hall, Englewood Cliffs, NJ, 1982.

[23] A. Ferre and J. Figueras, “On Estimating Bounds of the Quiescent Current for Iddq Testing,” VLSI Test Symposium, April-May 1996, pp. 106-111.