Calibration and Characterization of Self-powered Floating-gate Usage Monitor with Single Electron per Second Operational Limit

Chenling Huang, *Student Member, IEEE,* Nizar Lajnef, *Member, IEEE,* and Shantanu Chakrabartty, *Member, IEEE*

***Abstract*—Self-powered monitoring refers to a signal processing technique where the computational power is harvested directly from the signal being monitored. In this paper, we present the design and calibration of a CMOS event counter for long-term, self-powered mechanical usage monitoring. The counter exploits a log-linear response of the hot-electron injection process on a floating-gate transistor when biased in weak-inversion. By configuring an array of floating-gate injectors to respond to different amplitude levels of the input signal, a complete analog processor has been designed that implements a level counting algorithm which is widely used in mechanical usage monitoring. Measured results from a fabricated prototype in a 0.5-μm CMOS process demonstrate that the processor can sense, store and compute over 10^5 usage cycles with an injection limit approaching one single electron per second and with a counting resolution of 5 bits. This paper also presents a calibration algorithm that is used for compensating the variations which arise due to device mismatch, power supply and temperature fluctuations. The maximum current rating of the fabricated analog processor has been measured to be less than 160 nA making it ideal for practical self-powered sensing applications.**

***Index Terms*—Sub-threshold analog circuits, event monitoring, floating-gate transistors, self-powering, impact-ionized hot-electron injection, level-crossing algorithms, structural health monitoring, ultra-low power sensors.**

I. Introduction

SELF-POWERED integrated circuits and systems are attractive for long-term, autonomous monitoring applications where the use of batteries or remote powering is considered to be impractical. Examples of such applications include long-term in-vivo monitoring of mechanical strain inside a biomechanical implant (knee-implant or a hip-implant) [1]-[3] or structural health monitoring (SHM) of civil engineering structures [4],[5]. Typically, self-powering can be achieved by harvesting electrical energy from two possible sources: (a) from auxiliary environmental signals that are different from the signal being monitored or (b) from the signal being monitored which is referred to as "self-powered monitoring" in this paper. Most energy harvesting processors reported in literature are based on the first approach [6]-[8] and operate using different auxiliary energy sources (e.g. solar, thermal and vibrational). These sources have been shown to be capable of generating $\sim$100 μW of continuous power that is widely believed to be the minimum requirement to operate a single sensor [9]-[11]. However, in many long-term monitoring applications the auxiliary source of ambient energy is unavailable, in which case "self-powered monitoring" is the only viable option. However, designing signal processors for self-powered monitoring poses significant challenges which include:

1. Non-volatile computation: All the internal state variables (intermediate and final) have to be stored on a non-volatile media to account for infrequent availability of power (i.e. blackouts). Also, unlike conventional processors the computation and non-volatile storage capabilities are required to be co-located to eliminate power dissipation due to data transfer.

2. Low-frequency of operation: The signals of interest in self-powered monitoring are typically low-frequency burst mode signals (for example mechanical loading with frequency 1-10 Hz), and therefore conventional methods of voltage/current multiplication [12] and voltage/power regulation can not be directly applied.

3. Sub-microwatt power consumption: Due to limited driving capability of the sensors, all computation, regulation and storage functions are required to be performed at a power budget level less than 1 μW. This is consistent with harvestable energy levels available in biomechanical implants [3] or civil structures [13].

These challenges obviate the use of conventional information processing techniques which is based on digital signal processing. Table I summarizes the power budgets corresponding to some of the state-of-the-art DSP sub-systems which demonstrates that existing DSP based solution is not

TABLE I
Power and Energy Budgets Reported in Literature for Different Operational Modes of a Sensor.

Operation	Commercial	Research
1-bit analog-digital (A/D) conversion	193 fJ[14]	50 fJ[15]
Digital signal processing*	40 mW[16]	100 μW[17]
Write 1 bit to non-volatile memory	200 nJ[18]	25 pJ[19]
Sleep mode	6 μW[20]	1 μW[21]
Pin leakage	110 nW[20]	2.2 nW[22]

* Operation is scaled to a processor speed of 100 MHz.

This work was supported in part by a research grant from the National Science Foundation (NSF), CMMI: 0700632 and by a contract from the federal highway administration (FHWA) contract no: DTFH61-08-C-00015.
Chenling Huang and Shantanu Chakrabartty is with the Department of Electrical and Computer Engineering, Michigan State University. Nizar Lajnef is with the Department of Civil and Environmental Engineering, Michigan State University.

suitable for self-powered monitoring (even when excluding power budgets required for regulation and biasing). As an alternative, analog signal processors with sub-microwatt power budgets have been reported in literature [23],[24] but they are not suitable for self-powering due to restrictions imposed by biasing, regulation and dynamic storage.

In [3] we had proposed a self-powering device that integrated sensing, data storage and computation functions by exploiting the computational primitives inherent in a piezoelectricity driven impact-ionized hot-electron injection (IHEI) process in floating-gate transistors [27],[28],[29]. However, the approach presented in [3] was susceptible to artifacts due to transistor mismatch and biasing conditions. In this paper we extend the work presented in [32] to provide a complete characterization of the floating-gate injection device, and we also describe a calibration algorithm that can be used for designing self-powered analog processors. One particular analog processing algorithm that is amenable to floating-gate injection is the level crossing algorithm (also known as the rain-flow algorithm in SHM) which has numerous applications in long-term SHM [33],[34].

A simplified version of the level crossing algorithm is shown in Fig. 1 where the signal to be monitored is plotted with respect to time. The signal amplitude is first quantized into several different threshold levels (S_1-S_6). The level-crossing algorithm then counts the cumulative duration for which the signal amplitude exceeds the threshold levels (crossover events are indicated by circles in Fig. 1). These level-crossing counts serve as important statistics which can be then used for prognosticating fatigue in mechanical structures [34]. In the rest of the paper we will describe, characterize and calibrate an array of floating-gate injectors to implement the level crossing algorithm.

The paper is organized as follows. Section II describes the hot-electron injection mechanism in floating gate transistors and proposes a mathematical model for a current starved floating-gate injector which is used for designing the analog processor. The injector is then experimentally shown to be robust to mismatch and variations in biasing conditions. Section III presents a circuit level implementation of the level-counting processor using an array of floating-gate injectors. The section also describes a calibration procedure for compensating artifacts introduced by initialization errors.

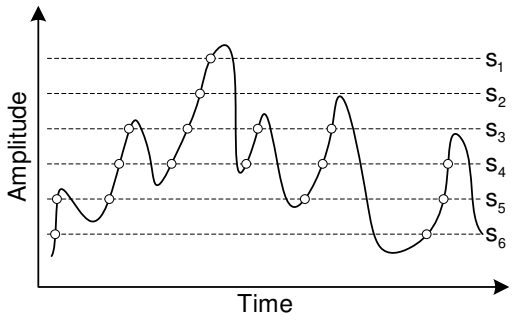


Fig. 1. Illustration of a level crossing algorithm: the transducer signal is plotted with respect to time and the events (level-crossings) are marked by circles.

Section IV describes a design example where the prototype fabricated in a 0.5-μm CMOS process has been interfaced with a polyvinylidene fluoride (PVDF) transducer. The integrated system is then demonstrated for real-time usage monitoring. Section V presents discussions, extensions and limitations of the proposed technique and section VI concludes the paper with some final remarks.

II. Principle of Operation and Mathematical Model

A. Impact-ionized Hot Electron Injection in Floating-gate Transistors

A floating-gate transistor is a metal-oxide-semiconductor field effect transistor (MOSFET) whose poly-silicon gate is completely surrounded by an insulator, which in a standard CMOS fabrication process is the silicon-dioxide (SiO_2) [27]. Because the gate is surrounded by high quality insulator, any electrical charges injected onto this gate is retained for a long interval of time ($>$ 8 years) [27],[29],[30]. This makes floating-gate transistors attractive for designing non-volatile memories. In this work we will use a p-channel floating-gate MOSFET instead of its n-channel counterpart due to limitation imposed by the 0.5-μm CMOS process which has been chosen for fabrication. Figure 2(a) shows the cross-section of a p-channel floating gate MOS transistor which is used to illustrate the mechanism of impact-ionized hot electron injection. IHEI in the pMOS transistor occurs when a high electric field is formed at the drain-to-channel depletion region. Due to this high-electric field, the holes, which are the primary carriers in pMOS transistors, gain significant energy to dislodge electrons by impact ionization (see Fig. 2(a)). The released hot-electrons accelerate towards the channel region and gain kinetic energy in such process. When the kinetic energy exceeds the silicon and silicon-dioxide ($>$ 3.2 eV) barrier, and if the momentum vector is correctly oriented towards the Si-SiO_2 barrier, the electrons are successfully injected into the oxide. The injection process is also shown using an energy band diagram in Fig. 2(b). As electrons are injected into the oxide and onto the floating-gate, its floating-gate potential decreases.

One of the disadvantages of using IHEI as a computational medium is that it requires a large voltage for operation. For example in a 0.5-μm CMOS process, a drain-to-source voltage greater than 4.1 V is required to start IHEI in a pMOS transistor. Fortunately, commonly available piezoelectric materials are capable of generating large voltages ($>$ 10 V), though with limited current driving capability ($<$ 1 μA). The limited current driving capability is not a problem for IHEI since it has been shown that when the pMOS transistor is biased in weak-inversion, the injection efficiency (ratio of injection current and source/drain current) is practically constant for different values of source current [25]. This implies that electron injection can operate at ultra-low current level which is ideal for self-powered sensing applications. Thus, piezoelectric transducers when coupled with pMOS floating-gate transistors could be used for self-powered monitoring of mechanical events. The principle of operation of the piezo-driven usage monitor used in this paper is shown in Fig. 2(c), where a piezoelectric sensor

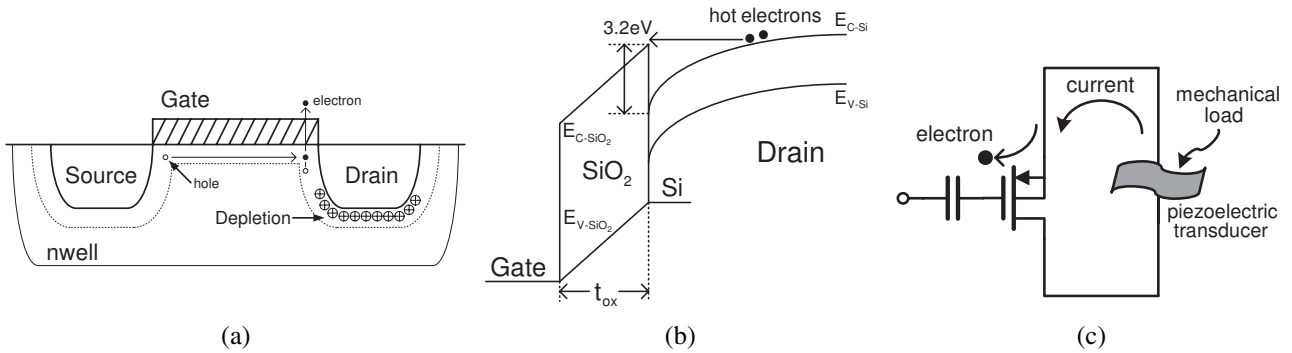


Fig. 2. (a): Illustration of IHEI process in a pMOS floating-gate transistor; (b): illustration of IHEI using an energy band-diagram; (c): illustration of the concept of piezoelectricity driven IHEI.

converts mechanical energy into electrical energy which is then used to inject electrons onto the floating-gate. The total electrons on the floating-gate is therefore indicative of the count of mechanical events.

However, IHEI is a positive feedback process. As more electrons are injected into the floating-gate, its potential decreases which in turn increases the drain current through the pMOS transistor. Increase in the drain current increases the probability of impact ionization, thus increases the hot-electron injection current. If left uncontrolled, IHEI will lead to the breakdown of the transistor. Therefore the current through the transistor is required to be carefully controlled in order to perform any useful and long-term computation. Next we derive a mathematical model of a floating-gate injector which is driven by a constant current source and is powered by a piezoelectric transducer.

B. Model of a Constant Current Floating-gate Injector

A circuit model of a constant current floating-gate injector is shown in Fig. 3. It consists of a pMOS floating-gate transistor whose source terminal V_s is driven by a constant current I_s through a triggering switch $SW1$.

The current source in Fig. 3 is powered by the signal being monitored, which for this example is the voltage generated by a piezoelectric transducer. The floating-gate voltage, denoted by V_{fg}, is controlled by the control gate voltage V_{cg} and tunneling voltage V_{tun} through capacitive coupling. The respective coupling capacitors are denoted by C_{fg} and C_{tun}. For the control gate capacitance C_{fg}, the respective plates of the capacitor are formed by poly-silicon layers whereas the tunneling capacitor is implemented using a moscap. The tunneling node V_{tun} is used for removing electrons from the floating-gate and in this work has been used for equalizing any residual charges found on the floating-gate post-fabrication. The schematic in Fig. 3 also consists of a triggering switch $SW1$ which is used to selectively turn ON and OFF the current flow through the floating-gate transistor. For the analysis presented in this section, both V_{cg} and V_{tun} are assumed to be constant and the source voltage V_s has been assumed to be properly initialized to a pre-determined value V_{s0}. Also, the trigger switch will be considered to be always ON. Under these conditions, the current source drives the source node such that it creates a high enough electric field at the drain-to-channel region to trigger the onset of the injection process. As hot-electrons are injected onto the floating-gate node, the potential V_{fg} decreases resulting in the decrease of potential V_s. To understand the dynamics of this simplified circuit, an empirical model for the injection is combined with an empirical model of the pMOS transistor. An equivalent circuit of this model is shown in Fig. 3(b) where I_s denotes the source current, I_d is the drain current, I_{inj} is the injection current, r_o is the drain-to-source impedance, $V_{s,d}$ is the source and drain voltages, C_{fg} is the floating-gate capacitance, C_{tun} is the tunneling capacitance and C_{gs} is the gate-to-source (bulk) capacitance. It is important to note that the values of the currents, r_o and C_{gs} are dependent on the voltages and currents and should not be confused with a small signal model. We will use a simple injection current model [25] for this analysis which is given by,

$$I_{inj} = \beta I_s \exp\left((V_s - V_d)/V_{inj}\right), \tag{1}$$

where β and V_{inj} are injection parameters which are a function of the transistor size and the process parameters. The current source I_s in Fig. 3(b) also ensures that the floating-gate transistor is biased in weak-inversion. For the source-to-drain voltage $V_{ds} > 200$ mV, the current I_s can be expressed as [35],

$$I_s = I_0 \exp\left(\frac{-V_{fg}}{nU_T}\right) \exp\left(\frac{V_s}{U_T}\right), \tag{2}$$

where I_0 is the characteristic current, V_{fg} and V_s are the floating-gate voltage and source voltage respectively, n is the slope factor [35] and U_T is the thermal voltage (26 mV at 300 K). Integrating the models described by equations (1) and (2) into the equivalent circuit model in 3(b) and solving the resulting differential equation, the following expression of V_s is obtained:

$$V_s(t) = -\frac{1}{K_2} \ln\left(K_1 K_2 t + \exp\left(-K_2 V_{s0}\right)\right), \tag{3}$$

with the values of K_1 and K_2 given by

$$K_1 = \frac{\beta I_s}{nC_t - C_{gs}}, K_2 = \frac{1}{V_{inj}},$$

where $C_t = C_{fg} + C_{tun} + C_{gs}$ denotes the total capacitance at the floating node. Derivation of the expression and any underlying assumptions are described in detail in Appendix I.

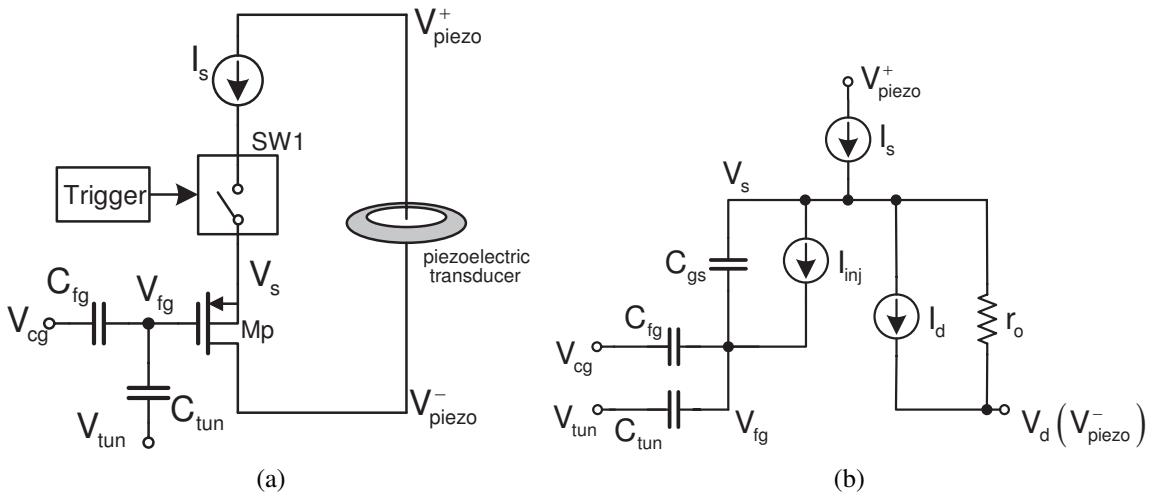


Fig. 3. (a): Schematic of a floating-gate injector; and (b): its equivalent circuit model.

V_{s0} in equation (3) is the initial source voltage and t represents the total duration for which the triggering switch (injection) is enabled. The plot of $V_s(t)$ as predicted by equation (3) is shown in Fig. 4 which also shows the measured results obtained from a prototype fabricated in a 0.5-μm CMOS process. The results show that the mathematical model is in close agreement with the measured results. In particular, it can be seen in Fig. 4 that the response of the injector consists of two distinct regions of operation. The first region is the linear region (see inset in Fig. 4) occurs under the condition $t \ll \left(\exp\left(-K_2 V_{s0}\right)/K_1 K_2\right.$ for which the equation (3) can be simplified as,

$$V_s(t) = V_{s0} - K_1 \exp\left(K_2 V_{s0}\right) t. \tag{4}$$

In deriving (4) we have used the approximation $\ln(1+x) \approx x$. Since the output of the injector $V_s(t)$ is a linear function of the injection duration t, the linear region is useful for monitoring short-term events (with a cumulative monitoring period less than 100 s). However, for long-term monitoring, which is the focus of this paper, the second region of operation called "log-linear" region is of importance.

Under the condition $t \gg \exp\left(-K_2 V_{s0}\right)/K_1 K_2$, equation (3) can be simplified to,

$$V_s(t) = -\frac{1}{K_2} \ln(K_1 K_2 t), \tag{5}$$

which shows that the voltage is a logarithmic function of the injection duration. The response is illustrated in Fig. 4 using both measured and empirical models, where it is shown to be valid for large durations (t $> 10^3$ s). In fact, the log-linear model is valid even beyond 10^5 seconds, where the injection currents are as low as one single electron per second. This can be readily verified from the measured response in Fig. 4, where the change in voltage observed on the floating gate node (with capacitance of 100 fF) over a duration of 10^4 second is 20 mV. Another interesting result that can be seen from equation (5) is that the effect of V_{s0} can be neglected when t is sufficiently large, and V_s is only dependent on the two constants, K_1 and K_2. The slope of the log-linear response is therefore completely determined by the $1/K_2$, while K_1 only introduces an offset. This offset captures all the artifacts arising due to biasing conditions, ambient temperature and fabrication parameters. Thus, equation (5) also provides a model for compensating these artifacts using a simple differential offset cancellation technique. Equation (5) can be written in its differential form as,

$$\Delta V_s(\Delta t) = \frac{1}{K_2} \ln\left(\frac{t_0}{t_0 + \Delta t}\right), \tag{6}$$

where t_0 denotes a reference injection time with respect to which the differential time interval Δt is measured. It can be readily seen from equation (6) that the differential operation is independent of the parameter K_1. However, for equation (6) to be useful, the robustness of the parameter K_2 still needs to be addressed.

We have conducted several experiments to quantify the robustness of the parameter K_2 to different biasing and mismatch conditions. Figure 5 shows the responses obtained from multiple injectors on the same chip that were biased with different current sources (I_s). The mismatch in the parameter

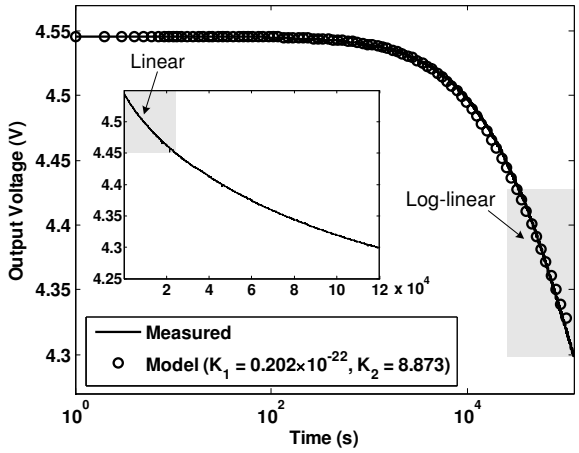


Fig. 4. Theoretical and measured response of the floating-gate injector plotted on a logarithmic scale and on a linear scale (inset).

(K_2) was calculated to be less than 10% for a bias current variation greater than 100%. The result is encouraging since it implies that the precision of the current source is not critical for the operation of the floating-gate injector.

Figure 6 shows the responses obtained from 8 injectors, 3 of which were measured from different prototypes fabricated in the same run where 5 of which were measured using prototypes fabricated in different runs. For these measurements, the mismatch in the parameter K_2 was calculated to be 4.3%. The results demonstrate that the response of the injector is robust to fabricated related mismatch. Figure 7 shows the response of the injector measured over a temperature range of -10^0C to 40^0C. Measured results show that the parameter K_2 linearly varies with temperature with the temperature coefficient measured to be $0.01V^{-1}T^{-1}$. The parameter K_2 therefore varies by $1V^{-1}$ for a temperature range of 100^0C, showing that injector response is robust with respect to temperature variations. Thus, the measured results summarized in Fig. 5-7 thus demonstrate that the parameter K_2 is robust to variations in biasing and ambient conditions.

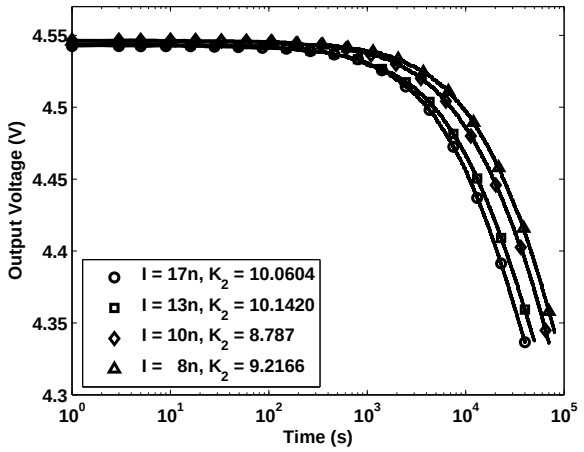


Fig. 5. Injector response measured at various source currents.

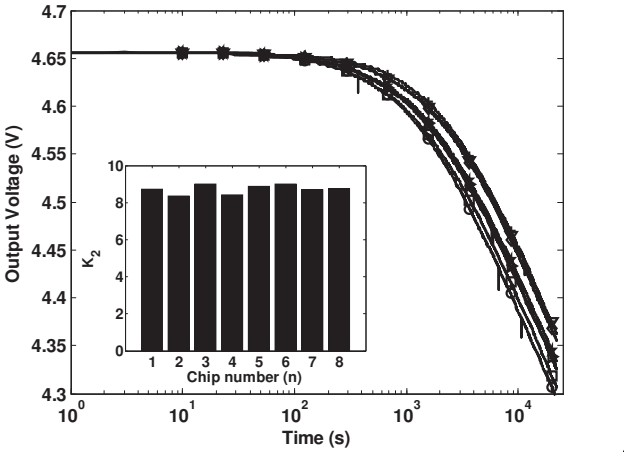


Fig. 6. Injector responses measured for using 8 prototypes fabricated in the same and different runs.

III. Implementation of the Usage Counter

This section describes CMOS implementation of the level-counting algorithm using an array of floating-gate injectors. The complete schematic of the event counter is shown in Fig. 8. It consists of a cascoded current reference, a startup circuit and an array of seven injector channels. Each channel consists of a floating gate injector (F1-F7) whose source is connected to the current reference through a series of diode-connected pMOS transistors (substrates are connected to source nodes respectively). To avoid clutter, only the control gates of the transistors have been shown in Fig. 8 and the tunneling nodes have been omitted. However, each floating-gate transistor has independent tunneling node which is used for its initialization. Table II summarizes the relative sizes of all the circuit elements used in the design. Transistors M1-M8 and resistor R form a standard current reference circuit biased in weak-inversion region, which produces a constant current reference according to,

$$I_{ref} = \frac{U_T \ln K}{R}, \tag{7}$$

where K is the ratio of width-to-length factors for transistors M1 and M5, and U_T is the thermal voltage. The reference current is copied by the mirrors P1-P14 which serve as source currents for the seven injector channels. As has been shown in measured results in Fig. 5-7 and using equation (6), temperature sensitivity of the current reference, power supply rejection and precision of the current mirror does not severely affect the differential response of the injector. Therefore, the current reference in Fig. 8 is sufficient to ensure proper functionality of the floating-gate injectors. The triggering circuit and switch (see Fig. 8 right) is implemented using a series of pMOS diodes (D1-D6). The diodes when biased by the reference current I_{ref} introduce voltage drop at the source of each injector. This ensures that the injection in each floating-gate transistor is triggered at different amplitude levels (V^+-V^-) of the input signal. As we will show in our measured results that this circuit architecture implements the level counting algorithm which was described in Fig. 1. The control gates of all the floating-gate transistors are connected to the voltage

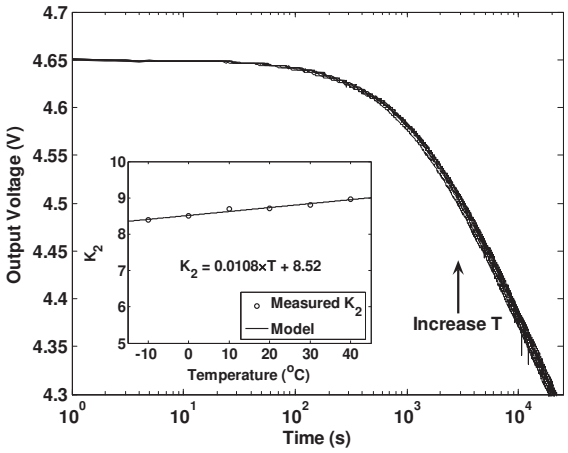


Fig. 7. Injector responses measured under different temperature conditions.

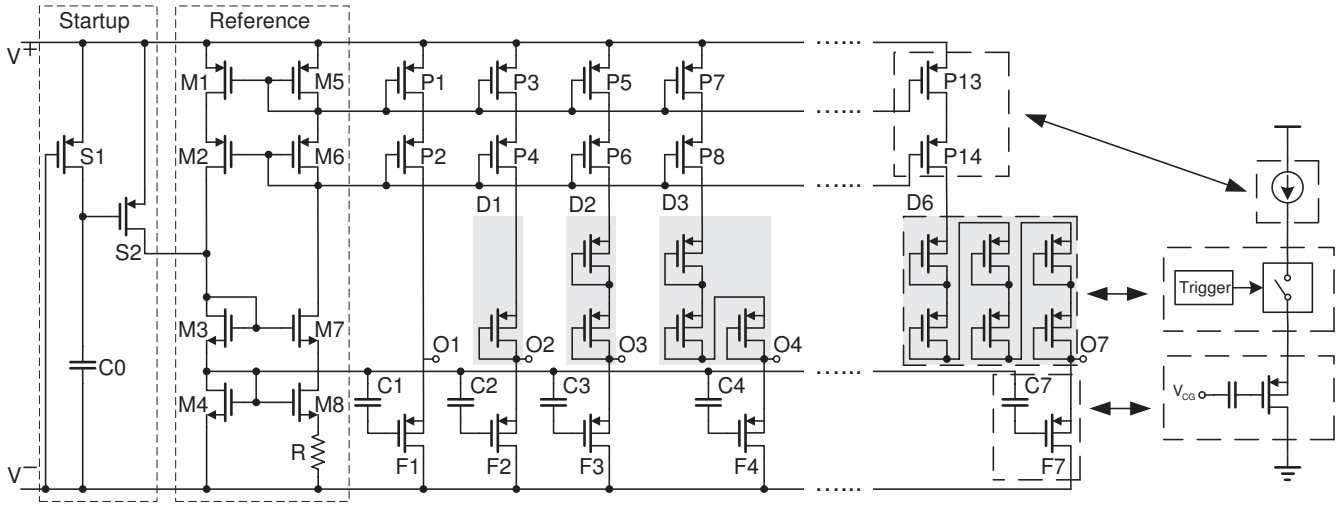


Fig. 8. Complete schematic of self-powered level-crossing processor.

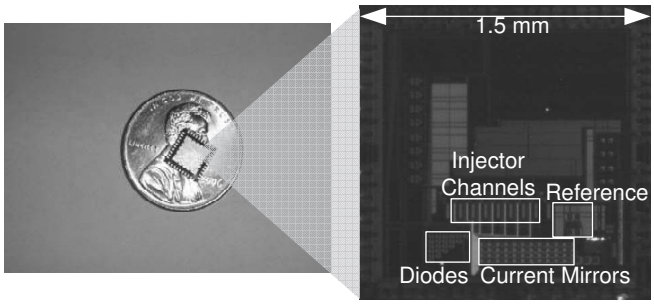


Fig. 9. The packaged prototype of the level-crossing processing and its photomicrograph.

TABLE II
COMPONENT SIZES USED IN FIG. 8.

Component	Parameter
M1	60 μm/10 μm
M2, M5-M6, P1-P16	30 μm/10 μm
M3-M4, M7-M8	60 μm/10 μm
D1-D7	10 μm/10 μm
F1-F8	60 μm/6 μm
C1-C8	100 fF
R	1.5 MΩ

TABLE III
SUMMARY OF MEASURED SPECIFICATIONS

Parameter	Value
Technology	0.5-μm CMOS
Die size	1.5 mm$\times$1.5 mm
Number of channels	7
Injection range	4.2 V - 8 V
Maximum current	160 nA
Power dissipation	800 nW @ 5 V
Setup time	$<$ 30 ms

reference which in turn is generated by the current reference circuit.

The output of each channel (O1-O7) is tapped at the source of the injectors with a unity-gain buffer. To ensure fully autonomous operation, each biasing terminal (tunneling node and buffer bias pins) is connected to pull-up or pull-down resistors (not shown in Fig. 8). Thus, in monitoring mode, the circuit is internally biased with only two input terminals (V^+ and V^-) which are connected directly to the output of the piezoelectric transducer. The pad diodes have been used as a full-wave rectifier as required by level counting algorithm.

Figure 9 shows the first version of the packaged prototype and its photomicrograph. Table III summarizes the measured specifications. In the current version, all the output signals (O1-O7) are physically accessible through the peripheral pads. The future versions of the prototypes will provide remote interrogation of the stored values on the injectors, which will in turn facilitate the embedded operation of the sensor.

A. Initialization of the usage counter

Before the prototype can be used for measurements, all the floating-gate injector channels have to be properly initialized. The initialization procedure equalizes any post-fabrication residual charges on the floating-gate. One such method reported in [31] exploits the metallization step in the CMOS process to equalize the charge across all the floating-gates. In this work, we use quantum mechanical tunneling of electrons to individually initialize the floating-gate injectors. First, the injector to be initialized is selected by connecting the sources of all other channels to the terminal V^-. This ensures that these channels are unaffected when the selected channel is being initialized. For the sake of clarity, the programming transistors have not been shown in Fig. 8. The injection is then initiated on the selected channel by applying a large potential difference across the terminals V^+ and V^-. As a result, the potential of the selected output node starts to decrease. FN tunneling is then employed by applying a large potential

($>$ 16 V) on the tunneling node (not shown in Fig. 8), which results in an increase in the output voltage. Both the procedures are repeated till the output node potential is programmed to V_{s0}=4.8 V. The choice of this voltage level was to ensure that a sufficient drain-to-channel potential exists to initiate the injection process when input voltage exceeds a prescribed threshold.

B. Level-crossing threshold adjustment

After the source voltage of each injector channel has been initialized to V_{s0}, the minimum voltage required to trigger the injector can be computed according to,

$$V^+ - V^- = V_{sat} + V_{s0} + M\frac{U_T}{\kappa}\ln\left(\frac{I_s}{I_0}\right), \qquad (8)$$

where V_{sat} is the minimum voltage drop for the cascoded current sources to function and M is the number of series pMOS diode-connected transistors for each channel. From equation (8), it can be seen that the resolution of thresholds in Fig. 1 can be controlled either by changing M or by changing the reference current I_s (using a different value of resistance R for the current reference). Figure 10 shows the measured results obtained after the output voltage of the first four injectors in Fig. 8 were initialized to 4.8 V and the input voltage (V^+-V^-) was varied from 4 V to 8 V. It can be seen from Fig. 10 that the responses of the injectors are offset by potential difference proportional to the number of series diodes. The offsets are not precisely equal among the channels due to the channel-length modulation effect of the current mirrors and the mismatch between the diodes. The result implies that different channels will start the injection at different levels of the input voltages. Figure 10 also illustrates the heuristic threshold level (drain-to-channel voltage) required to trigger the injector. For the 0.5-μm CMOS process, the injection threshold is approximately 4.2 V which also justifies the choice of the initialization voltage V_{s0}=4.8 V. However, it should be noted that the injector channels cannot be completely switched off when the amplitude is below the threshold. This is because the series combination of diodes implement an imperfect switching response.

C. Calibration of the processor

Unfortunately, the initialization procedure as described in Section III-A requires repeated injection and tunneling procedures and hence is prone to programming errors [27]. Even though the initialization procedure in Section III-A can equalize the post-fabrication charge on the floating-gates, the response of the injector is varies due to fabrication mismatch, parasitic capacitances and temperature variations. In this section, we present a calibration scheme that exploits the log-linear response of the floating-gate injector as described by equation (5). When the injector operates for a prescribed duration $t_0 \gg \exp(K_2 V_{s0})/K_1 K_2$, the response of the injector can be approximated from equation (5) by $V_s(t) \approx -\ln(t/t_0)/K_2$, where the effect of the initialization condition can be neglected. Therefore, all the initialization errors can be seen as the offset in the source voltage measured for each of the channel at t=0 s. The calibration procedure then employs pulse signal to trigger the injection to cancel out the errors. For initialization and mismatch errors which are less than 10%, the minimum number of calibration pulses required is approximately 10^3. This is verified using measured responses as shown in Fig. 11, where three injectors (corresponding to channels 1-3) are initialized using the procedure in Section III-A. It can be seen from the measured response that all the three injectors self-calibrate themselves (converge to the same output voltage) at the end of the calibration period. The duration of the calibration can be reduced if the initialization/mismatch error is smaller or the pulse with larger duty-cycle is used. Note that the calibration procedure would be typically performed prior to the deployment of the processor. Therefore the speed of this procedure can be significantly improved by continuous injection with higher frequency calibration pulses.

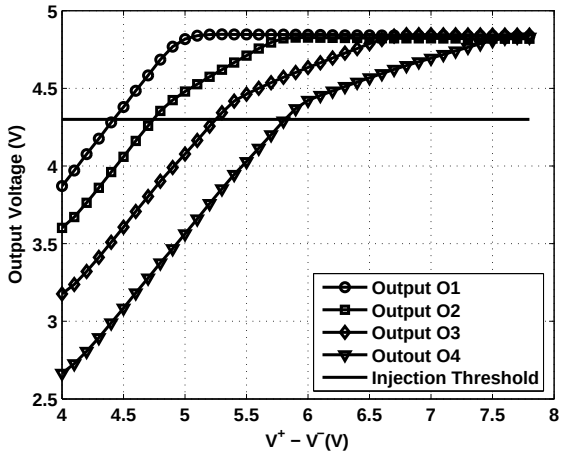


Fig. 10. Measured results showing that each injector channel can be programmed to different threshold levels.

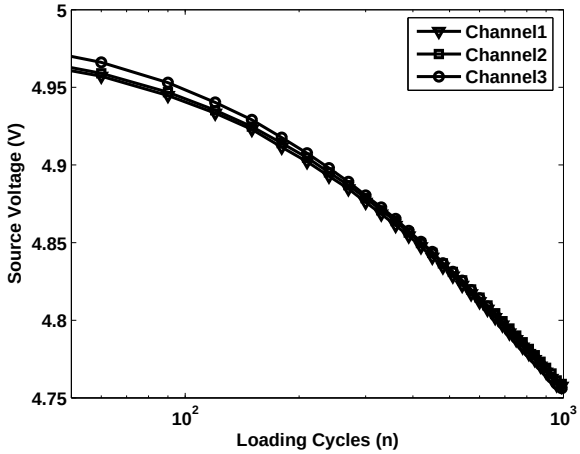


Fig. 11. Measured results verifying the calibration procedure of the injectors.

D. Counting resolution

The next set of experiments was used to determine the resolution of a single floating-gate injector to count the number of level-crossing events (when the amplitude exceeds a given threshold). For this experiment, the first injector channel was chosen and was subjected to voltage pulses with a duration of 1 second and amplitude of 5.5 V (generated using a programmable signal generator).The injector was first calibrated by applying 1,000 calibration pulses to eliminate any initialization/mismatch errors. The voltage pulses were then programmed according to the following conditions: for the first experiment, 256 voltage pulses were directly applied to the injector (referred to as relative count $\alpha = 256/256$ in the measured results); for the second experiment, only 248 out of 256 pulses were applied to the injector; the process was repeated using 240 out of 256 pulses till none of the pulses out of 256 was applied to the injector. The measured results for all the experiments are shown in Fig. 12(a). It can be seen that for different relative counts ($\alpha = [256/256 - 0/256]$), the injector response (in the log-linear region) is monotonically separated from each other. Mathematically, the relationship between the change in injector output voltage and the relative counts α can be expressed as,

$$\Delta V_s(t) = -\frac{1}{K_2} \ln\left(\frac{t_0 + \alpha\Delta t}{t_0}\right), \tag{9}$$

where t_0 is the calibration interval and Δt is the total monitoring period. If the response corresponding to $\alpha = 1$ is chosen as the reference, then the relative counts α corresponding to any arbitrary response can be inferred using equation (9) as,

$$\alpha = \frac{\exp\left[-K_2\Delta V_s(t)\right] - 1}{\exp\left[-K_2\Delta V_{sref}(t)\right] - 1}, \tag{10}$$

where ΔV_{sref} is the output voltage measured for the reference injector. Figure 12(b) shows the measured relative counts for two injectors as a function of the loading cycles. Also shown are the true counts for the injector response which is $240/256$ and $248/256$. We have verified that deviation of the measured count from the true is less than $\pm 8/256$, which implies that the resolution of the injector is 5 bits. However, we should also point out that the resolution of the injector can be improved by reducing any experiment artifacts that introduces error in measuring the output voltage of the injector.

E. Level-crossing counter

The next set of experiments was designed to evaluate the performance of the injector array for implementing the level-crossing algorithm. The floating-gate injectors were first initialized using the algorithm described in Fig. 11. The programmable voltage source was then used to generate an arbitrary periodic waveform consisting of three voltage levels (5.3 V, 6.1 V and 6.9 V). A sample voltage waveform used for one of the experiments is shown in Fig. 13, where the durations of the three levels were in the proportion of 3:2:1. The measured response from the injector array is also shown in Fig. 13. According to equation (9), the difference in the event counts translates into an offset in the log-linear response

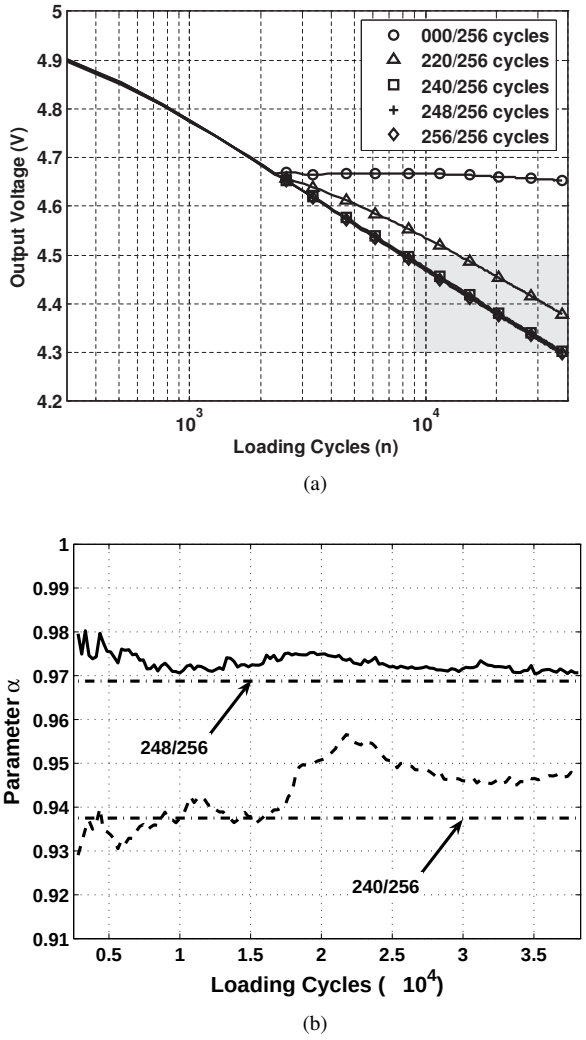


Fig. 12. Measured result to calculate the resolution for event counting: (a) change in source voltage measured for different relative counts of voltage pulses for over 100,000 events; (b) differential response measured for $\alpha = 240/256$ and $\alpha = 248/256$ with the reference being the response corresponding to $\alpha = 256/256$.

and is evident from the measured results (see Fig. 13 inset). Figure 14 shows measured injector responses (for the three channels) when different durations of events were applied (3:2.5:1). Comparing the Fig. 14 (inset) with Fig. 13 (inset), the relative shift in the offset for the second injector channel can be observed. For this experiment, the relative counts were estimated using equation (9). For the measured results shown in Fig. 13, the parameter α is computed to be equal to 0.30 for cell F3 and 0.71 for cell F2, which is close to the ratio 1/3 and 2/3. The sources of error arise from imperfect startup [36] and shutdown of the injector channels. The relative counts computed using measured results in Fig. 14 were also found to be in close agreement to the duty cycle of the applied periodic signal.

IV. Example for Usage Monitoring

In this section, we present an example where the fabricated prototype has been demonstrated as a mechanical usage monitor. The prototype was connected to a piezoelectric transducer

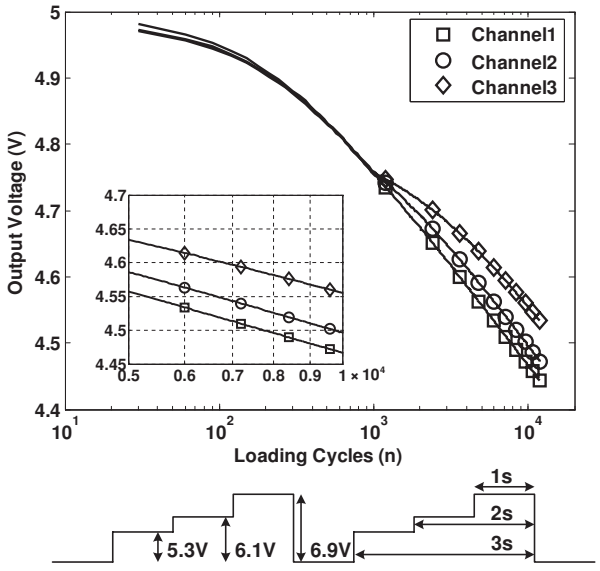


Fig. 13. Measured results obtained from the first 3 channels when a periodic signal (shown above) with a duty cycle in the ratio 3:2:1 is applied.

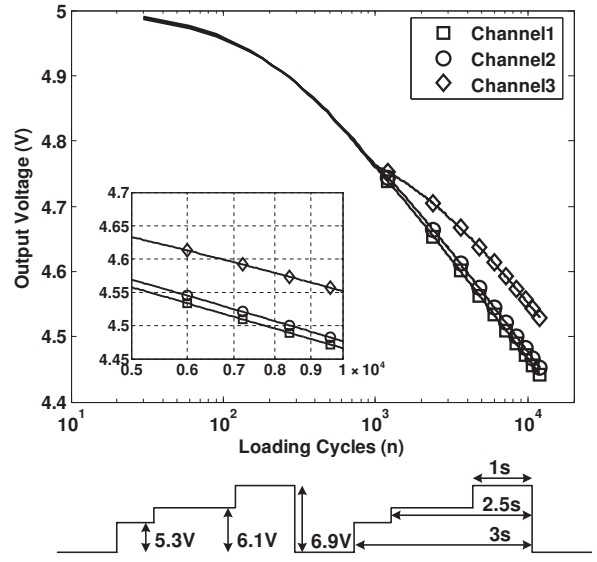


Fig. 14. Measured results obtained from the first 3 channels when a periodic signal (shown above) with a duty cycle in the ratio 3:2.5:1 is applied.

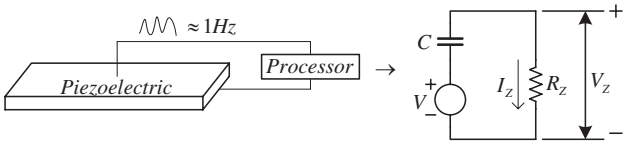


Fig. 15. Equivalent circuit model for piezoelectric transducer and the processor.

which was not only used for sensing variations in strain inside a mechanical structure, but also used for self-powering of the processor [5],[37],[38]. As described earlier, piezoelectric materials can generate large voltage signals (> 10 V), but exhibit limited current driving capability (< 1 μA). This attribute makes the transducer ideal for operating floating-gate injectors because the injection efficiency (injection current/source current) is invariant of the transistor bias current (could operate at pico-ampere current levels). However, a piezoelectric transducer also acts as an AC coupled voltage source and the frequency of loading for representative structures (e.g. bridges or biomechanical implants) is relatively low (< 1 Hz). This frequency is typically an order of magnitude lower than the resonant frequency of the transducer implying limited power harvesting capability. To understand the limitations imposed by the low-frequency operation, consider a simplified equivalent model of the prototype processor interfacing with the piezoelectric transducer as shown in Fig. 15 [39],[40]. The transducer has been modeled using an AC voltage source connected to a decoupling capacitor, C. The processor has been modeled as a simple resistive load R_Z.

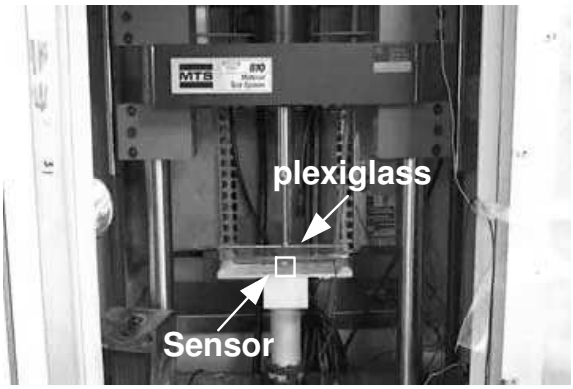


Fig. 16. MTS setup used for real-time evaluation of the analog processor interfacing with a PVDF transducer.

For a harmonic mechanical loading of the piezoelectric transducer at a frequency of f Hz, the magnitude of the voltage across the load is found to be,

$$V_Z(f) = \frac{2\pi f R_Z C V}{\left(1 + 4\pi^2 f^2 R_Z^2 C^2\right)^{1/2}}. \tag{11}$$

The power delivered to the load (processor) is given by $P_Z = V_Z^2(f)/R_Z$ and can be optimized with respect to R_Z. The optimal value of R_Z is given by,

$$R_Z = \frac{1}{2\pi f C}. \tag{12}$$

For a loading frequency of 1 Hz and for a typical capacitance (10 nF) of a polyvinylidene fluoride (PVDF) type piezoelectric material the optimal impedance of the processor is determined to be 15 MΩ. Thus, for a 5 V input voltage, this loading condition is equivalent to a maximum current of 300 nA. Meanwhile, the total current drawn by the fabricated prototype has been measured to be 160 nA at 6.7 V which is clearly less than the optimal loading condition. Thus, the proposed level-crossing processor is ideal for self-powered sensing using piezoelectric transducers.

For our experiment, the integrated sensor (piezoelectric transducer and analog processor) was attached to a plexiglass beam and the setup was mounted on a mechanical testing system (MTS) as shown in Fig. 16. The MTS machine was then programmed to generate two distinct strain levels of

2100 $\mu\varepsilon$ and 2500 $\mu\varepsilon$ respectively[1]. The mechanical loading was cyclically applied to the plexiglass beam. Figure 17(a) shows the measured results when 2100 $\mu\varepsilon$ strain was applied and only the first channel was shown to record a change in output voltage. When loading cycles corresponding to 2500 $\mu\varepsilon$ strain was applied, both channels 1 and 2 recorded the changes in voltage while the channel 3 voltage remained unchanged (shown in Fig. 17(b)). Although no calibration was performed in advance, the offset in measured output voltage could be used to determine the count of loading cycles with different strain levels.

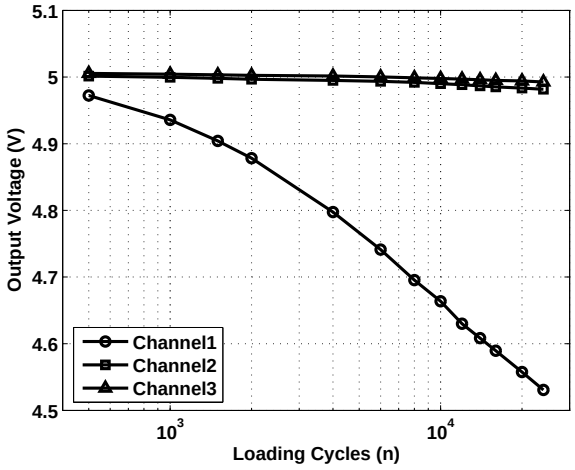
V. Discussions

Even though the measured results shown in the previous sections have demonstrated the operation of the floating-gate injectors for up to 10^5 loading cycles, we have observed deviations from the log-linear response beyond 10^5 loading cycles. Figure 18 shows a sample response obtained using three injectors (channels 1-3) operating up to 10^6 loading cycles. It can be seen from Fig. 18, that the response follows a superposition of two log-linear responses. We believe that the appearance of the superposition term occurs due to contribution from interstitial traps which releases electrons back in to the transistor channel [41]. At high injection rates (greater than 100 electrons per second) the de-trapping behavior is masked but becomes dominant when the injection rate reaches as low as 1 electron per second. We anticipate the deviation from the log-linear response is not problematic for long-term usage monitoring as the response is still monotonic with respect the number of loading cycles. However, the calibration procedure to determine the relative counts would have be modified to reflect the observed deviation.

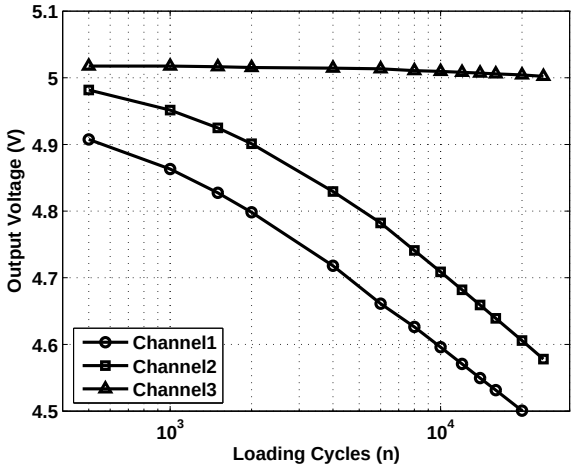
Even though the power dissipation of the fabricated prototype is less than 800 nW which makes it suitable for self-powered usage monitoring at a harmonic loading of 1 Hz (which is typical of most mechanical loading), there are applications which require monitoring at frequencies than 0.1 Hz. These applications include earthquake monitoring or monitoring strain cycles due to daily temperature variations. In such cases, the required power dissipation is less than 30 nW [13]. We believe that the current design can achieve this requirement by starving the injection currents using a higher value of current reference resistance R.

Another important consideration in IHEI based processor design is its long-term reliability. Most high-voltage failure mechanisms in a CMOS process are attributed to :(a) avalanche breakdown and (b) oxide breakdown. In avalanche breakdown, the impact ionization leads to a positive feedback process that culminates with the failure of the transistor. In this work, the avalanche process is carefully controlled by starving the source current of the transistor. As a result, the injector is a negative feedback circuit where the number of electrons injected into the oxide is significantly limited. In fact we have operated the injector continuously for more than 12 months without observing any failure. The second failure

[1] $1\mu\varepsilon$ (called micro-strain) refers to a deformation of 10^{-6} m for the dimension of the structure being 1 m.



(a)



(b)

Fig. 17. Voltage responses measured when the prototype is interfaced with a PVDF transducer and subjected to controlled cyclic strain levels with magnitude (a) 2100 $\mu\varepsilon$ and (b) 2500 $\mu\varepsilon$.

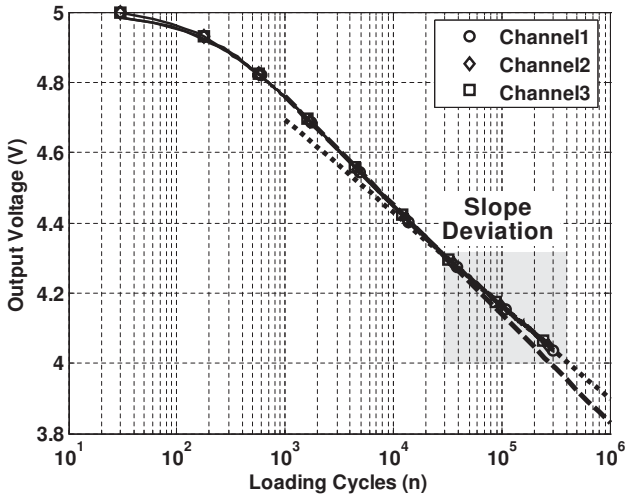


Fig. 18. Slope deviation observed for injection currents less than 1 electron per second.

mechanism is due to the oxide breakdown where repeated application of high electric field creates traps finally lead to its breakdown. For the 0.5-μm CMOS process voltages greater than $15\ V$ are required for quantum mechanical tunneling and for creating stress related artifacts. The voltage range is beyond the operating range of the processor.

For this paper, the minimum voltage required to initiate the injection process is approximately 4.2 V. Even though piezoelectric transducers can easily generate the operational voltage, other transducers only generate sub-volt signals and hence can not be interfaced with the prototype. We anticipate that this limitation could be overcome by using a sub-100 nm processes where the quantum mechanical tunneling could be used instead of the hot-electron injection process. However, it remains to be verified how the physics of tunneling could be exploited to obtain the desired "log-linear" response. Also, gate-leakage could also pose a significant problem for the process with smaller feature size [42]. Thus, the transistors with thick gate are necessary to retain the charges on the floating-gate node.

VI. Conclusion

In this paper, we presented a design of a CMOS analog processor that can be used for long-term, self-powered mechanical usage monitoring. The processor exploits computational primitives inherent in an impact-ionized hot-electron injection on a floating-gate transistor that is biased in weak-inversion region. We have demonstrated that the responses of the current starved injection to be robust to device mismatch and temperature variations. Also, we presented a level counting processor that can sense, store and compute over 10^5 event cycles with injection currents less than 1 electron per second. The power dissipation of the prototype was measured to be less than 800 nW at 5 V which facilitates its powering by harvesting vibration energy using a piezoelectric transducer. In this modality, the proposed integrated circuit has numerous applications in long-term structural health monitoring, where a large number of the sensors could be embedded directly inside a material (implants or rudders) and can autonomously record statistics of its mechanical loading (usage) [38].

Acknowledgment

This research was supported in part by a research grant from the National Science Foundation (NSF), CMMI: 0700632 and by a contract from the federal highway administration (FHWA) contract no: DTFH61-08-C-00015.

Appendix I

To derive equation (3), we will first present all the Nodal equations for the equivalent circuit in Fig. 3(b). If the floating-gate is properly initialized, the charge on the floating node Q_g is given by,

$$Q_g = C_{fg}(V_g - V_c) + C_{tun}(V_g - V_{tun}) + C_{gs}(V_g - V_s). \quad (13)$$

The injection current I_{inj} modifies the floating gate charge according to,

$$\frac{\partial Q_g}{\partial t} = I_{inj} = I_s \exp\left(\frac{V_s}{V_{inj}}\right) \quad (14)$$

which is connected to equation (13) by,

$$\frac{\partial Q_g}{\partial t} = C_t \frac{\partial V_g}{\partial t} - C_{gs}\frac{\partial V_s}{\partial t} \quad (15)$$

where $C_t = C_{fg} + C_{tun} + C_{gs}$. Also applying current conservation at the node V_s leads to,

$$I_s = I_{inj} + I_d + \frac{V_s}{r_o} + C_{gs}\frac{\partial V_s}{\partial t} - C_{gs}\frac{\partial V_{fg}}{\partial t}, \quad (16)$$

where the drain current I_d of the transistor M_P in weak-inversion is given by,

$$I_d = I_0 \exp\left(\frac{-V_{fg}}{nU_T}\right)\exp\left(\frac{V_s}{U_T}\right). \quad (17)$$

Equations (13)- (17) form a set of coupled differential equations whose closed form solution is difficult to obtain. We will therefore assume that $I_s \approx I_d$ for the following derivation which is reasonable since the I_{inj} and the current charging the bulk/source capacitance C_{gs} is small compared to the source current I_s. Since the source current I_s is constant, the expression of the floating-gate voltage with the other parameters can be obtained from (2) as,

$$V_{fg} = nV_s - nU_T \ln\left(\frac{I_s}{I_0}\right). \quad (18)$$

Equation (18) when combined with the differential equation (15) and (14) leads to

$$I_{inj} = -(nC_t - C_{gs})\frac{\partial V_{fg}}{\partial t}. \quad (19)$$

Equating (19) with (1), the following equation is obtained,

$$\beta I_s e^{V_s/V_{inj}} = -C_t\frac{\partial V_{fg}}{\partial t} = -C_t\frac{\partial V_s}{\partial t}, \quad (20)$$

using equation (18). The above equation can be simplified as,

$$\frac{\partial V_s}{\partial t} = -K_1 \exp\left(K_2 V_s\right),$$

with,

$$K_1 = \frac{\kappa\beta I_s}{C_t}, K_2 = \frac{1}{V_{inj}}.$$

Solving this first-order differential equation leads to the desired relationship,

$$V_s(t) = -\frac{1}{K_2}\ln\left(K_1K_2t + \exp\left(-K_2V_{s0}\right)\right). \quad (21)$$

References

[1] S. R. Platt, S. Farritor, K. Garvin, and H. Haider, "The use of piezoelectric ceramics for electric power generation within orthopedic implants," *IEEE/ASME Transactions on Mechatronics*, vol. 10, no. 4, pp. 455–461, 2005.

[2] N. Mukherjee, R. D. Roseman, and J. P. Willging, "The piezoelectric cochlear implant: Concept, feasibility, challenges, and issues," *Journal of Biomedical Materials Research*, vol. 53, no. 2, pp. 181–187, 2000.

[3] N. Lajnef, N. Elvin and S. Chakrabartty, "A piezo-powered floating-gate sensor array for long-term fatigue monitoring in biomechanical implants," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 2, no. 3, pp. 164–172, 2008.

[4] Y. S. Lee, "Health monitoring of bridge structures and components using smart-structure technology," *Project Report from Bridge Engineering Center of Iowa State University*, 2005.

[5] H. A. Sodano, D. J. Inman, and G. Park, "A review of power harvesting from vibration using piezoelectric materials," *The Shock and Vibration Digest*, vol. 36, no. 3, pp. 197–205, 2004.

[6] C. Alippi, and C. Galperti, "An adaptive system for optimal solar energy harvesting in wireless sensor network nodes," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 6, pp. 1742–1750, 2008.

[7] B. C. Yen, and J. H. Lang, "A variable-capacitance vibration-to-electric energy harvester," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 2, pp. 228–295, 2006.

[8] R. Amirtharajah, and A. Chandrakasan, "A micropower programmable DSP using approximate signal processing based on distributed arithmetic," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 337–347, 2004.

[9] S. Roundy, P. K. Wright, and J. M. Rabaey, "Energy scavenging for wireless sensor networks with special focus on vibrations," *Boston: Kluwer*, ISBN-10: 1402076630, 2004.

[10] S. Roundy, P. K. Wright, and J. Rabaey, "A study of low level vibrations as a power source for wireless sensor nodes," *Computer Communications*, vol. 26, no. 11, pp. 1131–1144, 2003.

[11] B. A. Warneke, and K. S. J. Pister, "Exploring the limits of system integration with Smart Dust," *2002 Proceedings of the ASME International Mechanical Engineering Congress and Exposition (IMECE'02)*, IMECE2002-39360, New Orleans, Louisiana, 2002.

[12] J. Yi, W. H. Ki, and C. Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 1, pp. 153–166, 2007.

[13] N. Elvin, N. Lajnef, and A. Elvin, "Feasibility of structural monitoring with vibration powered sensors", *Smart Materials and Structures*, vol. 15, no. 4, pp. 977–986, 2006.

[14] Texas Instrument: ADS61B29 12-bit 250 MSPS ADC Data Sheet.

[15] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, and G. Van der Plas, "A 2.2 mW 5b 1.75GS/s folding flash ADC in 90nm digital CMOS," *IEEE International Solid-State Circuits Conference (ISSCC'2008) Digest of Technical Papers*, pp. 252–253, 611.

[16] Texas Instrument: C54x 16-bit fixed-point DSP Data Sheet.

[17] H. Suzuki, H. Takata, H. Shinohara, E. Teraoka, M. Matsuo, T. Yoshida, H. Sato, N. Honda, N. Masui, and T. Shimizu, "1.047GHz, 1.2V, 90nm CMOS, 2-way VLIW DSP core using saturation anticipator circuit," *2006 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 152–153, 2006.

[18] Micron Technology: NAND Flash Memory Data Sheet.

[19] Cavendish: Cavendish Kinetics Corp, MEMS memory Data Sheet.

[20] Texas Instrument: MSP430F5438 16-Bit Microcontroller Data Sheet.

[21] J. Kwong, Y. K. Ramadass, N. Verma, and A. P. Chandrakasan, "A 65 nm sub-V_t microcontroller with integrated SRAM and switched capacitor DC-DC converter," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 115–126, 2009.

[22] J. Kao, "Subthreshold leakage control techniques for low power digital circuits," *Ph.D. Thesis*, Massachusetts Institute of Technology, 2001.

[23] P. Leong, and M. Jabri, "A low-power VLSI arrhythmia classifier," *IEEE Transactions on Neural Networks*, vol. 6, no. 9, pp. 1435–1445, 1995.

[24] S. Chakrabartty, and G. Cauwenberghs, "Sub-microwatt analog VLSI trainable pattern classifier," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1169–1179, 2007.

[25] P. Hasler, "Foundations of learning in analog VLSI," *Ph.D. dissertation*, Dept. Comput. Neural Syst., California Inst. Technol., Pasadena, CA, 1997.

[26] C. Dorio,P. Hasler,B. Minch and C.A. Mead, "A single-transistor silicon synapse," *IEEE Trans. Electron Devices*, vol. 43, no. 11, pp. 1972–1980, 1996.

[27] A. Bandyopadhyay, G. J. Serrano, and P. Hasler, "Adaptive algorithm using hot-electron injection for programming analog computational memory elements within 0.2% of accuracy over 3.5 decades," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 9, pp. 2107–2114, 2006.

[28] Y. L. Wong, M. H. Cohen, and P. A. Abshire, "A 1.2-GHz comparator with adaptable offset in 0.35-μm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 9, pp. 2584–2594, 2008.

[29] E. Ozalevli, H. J. Lo, P. E. Hasler, "Binary-weighted digital-to-analog converter design using floating-gate voltage references," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 4, pp. 990–998, 2008.

[30] E. Ozalevli, and P. E. Hasler, "Tunable highly linear floating-gate CMOS resistor using common-mode linearization technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 4, pp. 999-1010, 2008.

[31] E. Rodriguez-Villegas, M. Jimenez, and R. G. Carvajal, "On dealing with the charge trapped in floating-gate MOS (FGMOS) transistors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 2, pp. 156–160, 2007.

[32] N. Lajnef, S. Chakrabartty, and N. Elvin, "Calibration and characterization of self-powered floating-gate sensor arrays for long-term fatigue monitoring", *IEEE International Symposium on Circuits and Systems (ISCAS'2008)*, pp. 1096–1099, Seattle, 2008.

[33] Y. L. Lee, J. Pan, R. Hathaway, and M. Barkey, "Fatigue testing and analysis: theory and practice," ISBN-10: 0750677198, 2004.

[34] S. Suresh, "Fatigue of materials," 2nd edition, Cambridge University Press, ISBN-10: 0521578477, 1998.

[35] E. Vittoz, and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE Journal of Solid State Circuits*, vol. 12, no. 3, pp. 224–231, 1977.

[36] S. Mandal, S. Arfin, and R. Sarpeshkar, "Fast startup CMOS current references," *2006 IEEE International Symposium on Circuits and Systems (ISCAS'2006)*, pp. 2845–2848, 2006.

[37] L. Chao, C. Y. Tsui, and W. H. Ki, "A batteryless vibration-based energy harvesting system for ultra low power ubiquitous applications," *2007 IEEE International Symposium on Circuits and Systems (ISCAS'2007)*, pp. 1349–1352, 2007.

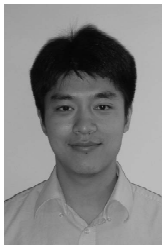
[38] N. Elvin, A. Elvin, and D. H. Choi, "A self-powered damage detection sensor," *The Journal of Strain Analysis for Engineering Design*, vol. 38, no. 2, pp. 115–125, 2003.

[39] M. Ferrari, V. Ferrari, D. Marioli, and A. Taroni, "Modeling, fabrication and performance measurements of a piezoelectric energy converter for power harvesting in autonomous microsystems," *Instrumentation and Measurement*, vol. 55, pp. 2096–2101, 2006.

[40] L. Mateu, and F. Moll, "System-level simulation of a self-powered sensor with piezoelectric energy harvesting," *Sensor Technologies and Applications*, pp. 399–404, 2007.

[41] R. Bellens, E. de Schrijver, G. Van den bosch, G. Groeseneken, P. Heremans, and H. E. Maes, "On the hot-carrier-induced post-stress interface trap generation in n-channel MOS transistors," *IEEE Trans. Electron Devices*, vol. 41, no. 3, pp. 413–419, 1994.

[42] H. K. O. Berge, and P. Hafliger, "A gate leakage feedback element in an adaptive amplifier application," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 2, pp. 101–105, 2008.



Chenling Huang received the B.Sc. and the M.Sc. degrees in Microelectronics from Fudan University, Shanghai, China in 2004 and 2007. Currently, he is pursuing the Ph.D. degree at Department of Electrical and Computer Engineering from Michigan State University. His research interests include the system and circuit design of integrated self-powered sensors, hybrid energy harvesting system, and low power mixed-signal CMOS circuit design.

Nizar Lajnef received his B.S degree in Mechanical Engineering from Tunisia Polytechnic School (TPS), Tunis, Tunisia, in 2004. He received two M.S degrees, in Computational Mechanics from TPS in 2005 and in Civil Engineering from Michigan State University (MSU) in 2008, and a Ph.D degree in Civil Engineering from MSU in 2008. He is currently an assistant professor in the department of Civil and Environmental Engineering at Michigan State University. His current research interests include sensors design for structural health and usage monitoring, damage detection algorithms with application to civil, mechanical and biomechanical structures. He submitted two patents on the area of sensor design and testing. Dr. Lajnef was a recipient of the Nothstine fellowship and the most outstanding Ph.D student award in 2007.

Shantanu Chakrabartty (M'96) received his B.Tech degree from Indian Institute of Technology, Delhi in 1996, M.S and Ph.D in Electrical Engineering from Johns Hopkins University, Baltimore, MD in 2001 and 2004 respectively. He is currently an assistant professor in the department of electrical and computer engineering at Michigan State University. From 1996-1999 he was with Qualcomm Incorporated, San Diego and during 2002 he was a visiting researcher at University of Tokyo. His current research interests include low-power analog and digital VLSI systems, hardware implementation of machine learning algorithms with application to biosensors and biomedical instrumentation. Dr. Chakrabartty was a recipient of The Catalyst foundation fellowship from 1999-2004 and received the best undergraduate thesis award in 1996. He is currently a member for IEEE BioCAS technical committee, IEEE Circuits and Systems Sensors technical committee and serves as an associate editor for Advances in Artificial Neural Systems from Hindawi publications.