High-Speed Mechanically Flexible Single-Crystal Silicon Thin-Film Transistors on Plastic Substrates

Jong-Hyun Ahn, Hoon-Sik Kim, Keon Jae Lee, Zhengtao Zhu, Etienne Menard, Ralph G. Nuzzo, and John A. Rogers

***Abstract*—This letter describes the fabrication and properties of bendable single-crystal-silicon thin film transistors formed on plastic substrates. These devices use ultrathin single-crystal silicon ribbons for the semiconductor, with optimized device layouts and low-temperature gate dielectrics. The level of performance that can be achieved approaches that of traditional silicon transistors on rigid bulk wafers: effective mobilities $> 500\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, ON/OFF ratios $> 10^5$, and response frequencies > 500 MHz at channel lengths of 2 μm. This type of device might provide a promising route to flexible digital circuits for classes of applications whose performance requirements cannot be satisfied with organic semiconductors, amorphous silicon, or other related approaches.**

***Index Terms*—Flexible circuits, printed transistors, silicon-on-insulator (SOI) wafer, thin film transistor (TFT).**

I. Introduction

SEMICONDUCTORS based on organic small molecules and polymers provide a route to printed electronics on low-temperature plastic substrates [1]. Although useful systems in areas such as displays can be achieved with these materials, the modest performance (i.e., device mobilities typically less than 1–2 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$), which is currently possible may limit the range of applications. Some recent research that is designed to address this issue, while retaining the attractive processing attributes of the organics, explores the use of unusual structural forms—micro/nanowires, platelets, ribbons, etc.—of high quality single-crystal inorganic semiconductors [2]–[6]. There are two general techniques for generating the printable elements: one that uses direct guided growth [6] and another that applies lithographic and etching methods to wafer scale sources of a material [2]–[4]. The latter approach is attractive because the quality of the material, its doping levels, etc., are all controlled by the well-known processes used to create the wafers.

Manuscript received February 9, 2006; revised March 13, 2006. This work was supported in part by the Defense Advanced Projects Agency under Contract F8650-04-C-710 and by the U.S. Department of Energy under Grant DEFG02-91-ER45439. Devices were fabricated using the Frederick Seitz Materials Research Laboratory facilities and were characterized in the Center for Microanalysis of Materials, both of which are supported in part by the U.S. Department of Energy under Grant DEFG02-91-ER45439. The review of this letter was arranged by Editor J. Sin.

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Digital Object Identifier 10.1109/LED.2006.874764

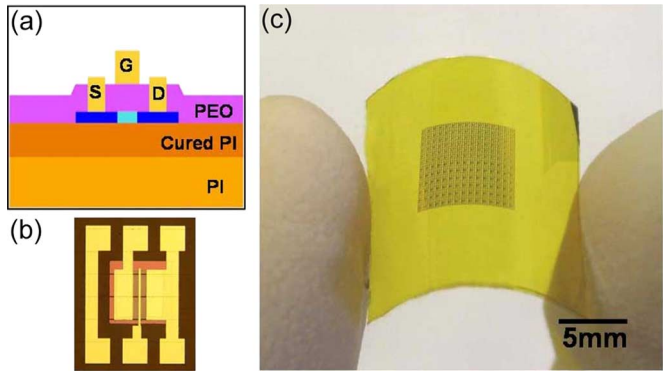

Fig. 1. (a) Schematic cross-sectional view of a single-crystal silicon TFT on PI (PI; 25-μm thick) with a SiO_2 layer deposited by low-temperature PECVD as a gate dielectric (PEO; 100-nm thick). (b) Optical-micrograph top view of a typical device. (c) Optical images of an array of devices on a plastic substrate.

This letter describes transistors that use single-crystal silicon ribbons on thin polyimide (PI) substrates with low-temperature dielectrics and optimized device layouts on flexible PI substrates, and which achieve much better characteristics than those of the devices reported previously [2], [3]. Measurements of both the DC and high-frequency responses for a range of channel lengths and bending configurations reveal excellent electrical properties: mobilities $> 500\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$; subthreshold slopes < 230 mV/dec; ON/OFF ratios $> 10^5$; threshold voltages < 1 V; stable operation to bending radii < 3 mm. Devices of this type have the potential to be useful for a range of large area electronic systems that demand high performance, such as sensor arrays, emissive displays, structural health monitors, and steerable antennas [7].

II. Device Fabrication

Fig. 1(a) presents a schematic cross-sectional view of a device. The fabrication begins with the definition of contact doped thin ribbons of single-crystal silicon, which we refer to as microstructured silicon (μs$-$Si), by processing a silicon-on-insulator wafer (SOI) (Soitec unibond with a 290-nm top Si layer with doping level of $6.0-9.4\times10^{14}/\mathrm{cm}^3$). The first step involved phosphorus-diffusion process, using a solid source, through a photolithographically defined layer of plasma-enhanced chemical vapor deposited SiO_2 (PEO) as a mask to control where the dopant diffuses into the silicon. We used techniques described previously to generate the μs$-$Si [2] and to print it onto a PI sheet spin coated with a thin layer ($\sim 1.0\ \mu$m) of liquid PI precursor (polyamic acid, Sigma_Aldrich Inc.). The gate dielectric layer consisted of a layer of SiO_2 (thickness

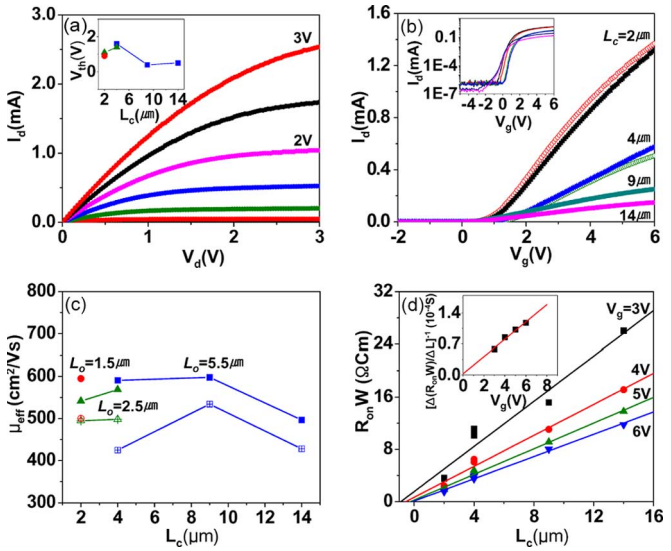

Fig. 2. (a) Typical current–voltage characteristics of a TFT on a PI substrate, with $L_c = 9$ μm, $L_o = 5.5$ μm, and $W = 200$ μm. Inset shows the threshold voltage as a function of channel length for the devices. (b) Transfer curves ($V_d = 0.1$ V) of devices with channel lengths and channel overlap distances, from top to bottom, of ($L_c = 2$ μm, $L_o = 1.5$ μm), ($L_c = 2$ μm, $L_o = 2.5$ μm), ($L_c = 4$ μm, $L_o = 2.5$ μm), ($L_c = 4$ μm, $L_o = 5.5$ μm), ($L_c = 9$ μm, $L_o = 5.5$ μm), and ($L_c = 14$ μm, $L_o = 5.5$ μm). The channel width in each case is 200 μm; inset shows a logarithm plot of (b) transfer curves. (c) Effective mobility in the linear (filled) and saturation (open) regimes as a function of channel length. (d) Width-normalized ON resistance as a function of channel length at different gate voltages. The solid lines represent the linear least square fit of the data. The inset shows the sheet conductance, determined from the reciprocal of the slopes of the linear fitting in (d), as a function of gate voltage.

~ 100 nm) deposited by plasma-enhanced chemical vapor deposition (PECVD) using SiH_4 and N_2O at 250 °C. Source, drain, and gate electrodes of Cr/Au (5/100 nm by electron-beam evaporation) were defined in a single step by photolithography and wet etching. The resulting arrays of single-crystal-silicon thin film transistors (TFTs) were mechanically flexible due to the bendability of the PI sheet (thickness of 25 μm) and the small device thickness (< 0.5 μm). Fig. 1(b) shows an optical micrograph of a typical device, with probing pads configured for microwave testing. Fig. 1(c) shows a large array of such devices.

III. Result and Discussion

Fig. 2 presents DC measurements of a representative device with a channel length (L_c) of 9 μm, channel overlap distance (L_o; defined by the distance that the gate electrode extends over the doped source/drain regions) of 5.5 μm, and channel width (W) of 200 μm [see Fig. 2(a)]. Effective device mobilities calculated by standard field-effect transistor models [8] for this device were 600 $\text{cm}^2/\text{V}\cdot\text{s}$ in the linear regime and 530 $\text{cm}^2/\text{V}\cdot\text{s}$ in the saturation regime. These mobilities exceed even those typically observed for laser annealed polycrystalline silicon transistors on plastic substrates [9]. The inset of Fig. 2(a) shows that the threshold voltages (V_{th}) for devices with different channel lengths have a narrow distribution near 0 V. Fig. 2(b) presents transfer curves for devices with different channel lengths between 2 μm and 14 μm, channel overlap distance between 1.5 and 5.5 μm, and channel width of 200 μm. The ON/OFF ratios are $> 10^5$.

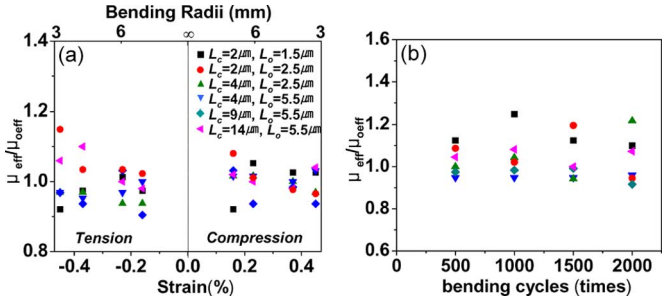

Fig. 3. (a) Normalized effective mobility ($\mu_{\text{eff}}/\mu_{0\text{eff}}$) as a function of bending-induced strain and bending radius. (b) Normalized effective mobility after bending (to 3-mm radius; 0.44% strain) and unbending the devices several thousand times.

Fig. 2(c) presents the effective mobilities of devices in the linear and the saturation regimes as a function of the channel length. The channel-length invariance of these mobilities suggests that contact resistance has a negligible effect on these devices. To quantify the contact resistances, we performed scaling analysis [10]. Fig. 2(d) presents width-normalized resistance in ON-state (R_{on}) as a function of the channel length at different gate voltages. The contact resistance, as determined from the intercept of linear fit of the $R_{\text{on}}W$ versus L_c in Fig. 2(d), is negligible compared with the channel resistance for the range of channel lengths investigated here. The inset shows the variation of sheet conductance as gate voltage. The linear least square curve fit provides the intrinsic device threshold voltage of -0.14 V and intrinsic mobility of 510 $\text{cm}^2/\text{V}\cdot\text{s}$.

Good mechanical bendability is critically important for applications in flexible electronics. We evaluated flexibility by performing frontward and backward bending tests. Fig. 3(a) shows the effective device mobility in the linear regime, normalized by the value in the unbent state $\mu_{0\text{eff}}$ as a function of strain and bending radius. For this range of strains, we observed only small changes in $\mu_{\text{eff}}/\mu_{0\text{eff}}$, threshold voltage, and ON/OFF ratio. Fig. 3(b) shows variation of $\mu_{\text{eff}}/\mu_{0\text{eff}}$ after several thousand bending cycles of tensile strain between 0% and 0.44%. After 2000 cycles, the $\mu_{\text{eff}}/\mu_{0\text{eff}}$, the threshold voltage, and the ON/OFF ratio change less than 20%. These results suggest that the single-crystal μs$-$Si transistors may have good fatigue properties, even at the extreme bending radii of 3 mm examined here.

High-frequency characteristics were measured in the common-source configuration using an Agilent E5062A network analyzer and Cascade Microtech RF-1 probe station. Fig. 4(a) shows the current gain (H_{21}) versus transition frequency (f_T) for a drain bias (V_d) of 2 V and a gate bias (V_g) of 2 V. This value was $f_T = 515$ MHz for a typical device with $L_c = 2$ μm and $L_o = 1.5$ μm. This high-frequency operation approaches the radio frequency (RF) levels of performance needed to support the systems such as large active antennas operating in the UHF regime [7]. Fig. 4(b) shows a reasonable agreement between the measured (filled) and calculated (open) f_T values for devices with different channel lengths and overlap distances. The calculations use a simple model[1] that

[1]Theoretical f_T value was calculated using a simple equation, $f_T = g_m/[2\pi(C_{\text{gs}} + C_{\text{gd}})]$, where g_m, C_{gs} and C_{gd} are transconductance, gate–source capacitance and gate–drain capacitance, respectively.

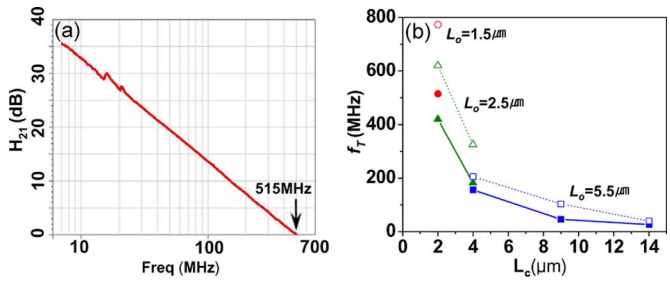

Fig. 4. (a) Experimental plots of H_{21} obtained from TFT of $L_c = 2$ μm and $L_o = 1.5$ μm with $V_g = 2$ V and $V_d = 2$ V. (b) Dependence of f_T on the gate length of TFTs: Measured (filled) and calculated values (open).

overestimates the frequencies since it does not include parasitic or fringing capacitances. The data suggest that f_T could be increased significantly further by reducing the channel length and overlap distance.

IV. Conclusion

This letter presents materials and processing approaches to achieve high-performance bendable silicon transistors on plastic substrates with high-frequency capabilities. The levels of DC and high-speed operating characteristics exceed other reported approaches and may, as a result, expand the range of application possibilities for flexible electronics.

Acknowledgment

J.-H. Ahn would like to thank Prof. J.-C. Jung and Prof. W.-C. Zin at POSTECH, Korea, for the valuable discussions on polyimide and the Korea Research Foundation (KRF) for the postdoctoral fellowship support (M01-2004-000-20108-0). H.-S. Kim would like to thank Prof. E. Rosenbaum at University of Illinois at Urbana-Champaign (UIUC) for the valuable discussions on device physics.

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