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Education

Ph.D.	Computer Science, U.C. San Diego	September, 2000
M.S.	Computer Science, U.C. San Diego	May, 1994
B.S.	Computer Engineering, U.C. San Diego	May, 1993

Professional Experience

May, 2003 – present	Adjunct Assistant Professor	CSE Dept. U.C. San Diego
May, 2003 – present	Assistant Research Scientist	San Diego Supercomputer Center
May, 2001 – May, 2002	Lecturer	CSE Dept. U. C. San Diego
Feb, 2000 – April 2003	Mgr. PMaC Group	San Diego Supercomputer Center
Aug, 1997 – Feb. 2000	Staff/Grad Student	San Diego Supercomputer Center
Mar, 1995 – July 1997	Mgr. Vis. Group	San Diego Supercomputer Center
May, 1994 – Feb., 1995	Programming Staff	San Diego Supercomputer Center

Awards

- 2005 UCSD Mentor Recognition Award for preparing undergraduate students for graduate studies
- 2nd highest score overall, UCSD Computer Science Comprehensive Exams 1998

Published Works

1. Oliker, L., R. Biswas, R. Van der Wijngaart, D. Bailey, and A. Snavely: Performance Evaluation and Modeling of Ultra-Scale Systems, Frontiers of Scientific Computing, M. A. Heroux, P. Raghavan and H. D. Simon editors, book to be published by SIAM 2007
2. Lee, C. B. and A. Snavely: On the User-Scheduler Dialogue: Studies of User-Provided Runtime Estimates and Utility Functions, International Journal of High Performance Computing Applications, in press, to appear 2007
3. Chen Y. and A. Snavely: Metrics for Ranking the Performance of Supercomputers, Cyberinfrastructure Technology Watch Journal: Special Issue on High Productivity Computer Systems, J. Dongarra Editor, Volume 2 Number 4, in press, to appear February 2007
4. Wolter, N., M. O. McCracken, A. Snavely, V. Basili, L. Hochstein, T. Nakamura: What's working in HPC?, Cyberinfrastructure Technology Watch Journal: Special Issue on High Productivity Computer Systems, J. Dongarra Editor, Volume 2 Number 4, in press, to appear, February 2007

5. Laurenzano, M., M. Tikir, L. Carrington, and A. Snavely: The PMaC Binary Instrumentation Library for PowerPC, Workshop on Instrumentation and Applications, to be held in conjunction with ASPLOS XII, October, 2006, San Jose
6. Hoisie, A., D. J. Kerbyson, C. L. Mendes, D. A. Reed, A. Snavely: Special section: Large-scale system performance modeling and analysis. Future Generation Computer Systems 22(3): 291-292 (2006)
7. Carrington, L., A. Snavely, N. Wolter: A performance prediction framework for scientific applications, Future Generation Computer Systems, 22(3): 336-346 (2006)
8. Khalili, O., J. He, C. Olschanowsky, A. Snavely, H, Casanova: Measuring the Performance and Reliability of Production Computational Grids, The 7th IEEE/ACM International Conference on Grid Computing, September 2006, Barcelona, Spain (Acceptance rate 18%)
9. Weinberg, J. and A. Snavely: User-guided symbiotic spacesharing of real workloads, ICS06 (The 20th ACM International Conference on Supercomputing), June 2006, Cairns, Australia (Acceptance rate 26%)
10. Gao, X., A. Snavely, L. Carter: Path Grammar Guided Trace Compression and Trace Approximation, HPDC-15 (The 15th IEEE International Symposium on High Performance Distributed Computing), June 2006, Paris (Acceptance rate 13%)
11. Weinberg, J. and A. Snavely: Symbiotic Space-Sharing on SDSC's DataStar System, 12th Workshop on Job Scheduling Strategies for Parallel Processing held in Conjunction with SIGMETRICS 2006, Saint-Malo, France
12. Tamjidi, D., S. Gidwani, A. Snavely: A Case Study on Reconfigurable Computing Using HMMER on the Starbridge HC-62 Platform, 2006 IEEE Computer Annual Symposium on VLSI (ISVLSI 2006), March 2006, Karlsruhe, Germany
13. Weinberg, J., M. O. McCracken, A. Snavely, E. Strohmaier: Quantifying Locality in the Memory Access Patterns of HPC Applications, Proceedings of the ACM/IEEE SC2005 Conference on High Performance Networking and Computing, 50, November 2005, Seattle (Acceptance rate 22%)
14. Carrington, L., M. Laurenzano, A. Snavely, R. Campbell, L. Davis: How well can simple metrics represent the performance of HPC applications?, Proceedings of the ACM/IEEE SC2005 Conference on High Performance Networking and Computing, 48, November 2005, Seattle (Acceptance rate 22%)
15. Bailey, D. H. and A. Snavely: Performance Modeling: Understanding the Present and Predicting the Future, Euro-Par 2005: 93-101, September 2005, Lisbon (Acceptance Rate 31%)
16. Malony, A. D., T. Fahringer, A. Snavely, L. Silva: Topic 2 - Performance Prediction and Evaluation. Euro-Par 2005: 93
17. Gao, X., B. Simon, A. Snavely: ALITER: An Asynchronous Lightweight Instrumentation Tool for Event Recording, Workshop on Binary Instrumentation and Applications held in conjunction with PACT2005, ACM SIGARCH Computer Architecture News, Volume 33 Issue 5, 33:38, September 2005, St. Louis
18. Gao, X., M. Laurenzano, B. Simon, A. Snavely: Reducing Overheads for Acquiring Dynamic Traces, International Symposium on Workload Characterization (ISWC05), September 2005, Austin
19. Laurenzano, M., B. Simon, A. Snavely, M. Gunn: Low Cost Trace-driven Memory Simulation Using SimPoint, Workshop on Binary Instrumentation and Applications

(held in conjunction with PACT2005), ACM SIGARCH Computer Architecture News, Volume 33 Issue 5, 81:86, September 2005, St. Louis.
20. Carrington, L., X. Gao, N. Wolter, A. Snavely, and R. Campbell: Performance Sensitivity Studies for Strategic Applications, Department of Defense Users Group Conference 2005 , June 2005, Nashville
21. Carrington, L., X. Gao, A. Snavely, R. Campbell: Profile of AVUS Based on Sampled Memory Tracing of Basic Blocks, Department of Defense Users Group Conference 2005 , June 2005, Nashville
22. Hollingsworth, J. K., A. Snavely S. Sbaraglia, K. Ekanadham: EMPS: An Environment for Memory Performance Studies, NSF Next Generation Software Program Workshop (held in conjunction with IPDPS), April 2005, Denver, CO
23. Carrington, L., N. Wolter, A. Snavely, and C. B. Lee: Applying an Automated Framework to Produce Accurate Blind Performance Predictions of Full-Scale HPC Applications, Department of Defense Users Group Conference 2004, Williamsburgh, June 2004
24. Lee, C. B., Y. Schwartzman, J. Hardy, A. Snavely: Are user runtime estimates inherently inaccurate?, Workshop on Job Scheduling Strategies for Parallel Processing (JSSPP 2004:253-256), held in conjunction with SIGMETRICS, New York, June 2004
25. Chun, G., H. Dail, H. Casanova, A. Snavely: Benchmark Probes for Grid Assessment, High-Performance Grid Computing Workshop, IPDPS, Santa Fe, NM, April 2004
26. Snavely, A., G. Chun, H. Casanova, R. Van der Wijngaart, M. Frumkin: Benchmarks for Grid computing: A Review of Ongoing Efforts and Future Directions, SIGMETRICS Performance Evaluation Review (PER), 30(4):27-32, March 2003
27. McCracken, M. O., A. Snavely, A.D. Maloney: Performance Modeling for Dynamic Algorithm Selection, International Conference on Computational Science 2003:926-935, June 2003, Melbourne
28. Gao X. and A. Snavely: Exploiting Stability to Reduce Time-Space Cost for Memory Tracing, International Conference on Computational Science 2003:966-975, June 2003, Melbourne
29. Carrington, L., A. Snavely, X. Gao, and N. Wolter: A Performance Prediction Framework for Scientific Applications, International Conference on Computational Science 2003:926-935, June 2003, Melbourne
30. Snavely, A., X. Gao, C. B. Lee, N. Wolter, J. Labarta, J. Gimenez, P. Jones: Performance Modeling of HPC Applications, ParCo, October, 2003, Dresden
31. Snavely, A., L. Carrington, N. Wolter, J. Labarta, R. Badia, A. Purkayastha: A Framework for Application Performance Modeling and Prediction, Proceedings of the ACM/IEEE SC2002 Conference on High Performance Networking and Computing, Baltimore (Acceptance rate 29%)
32. Snavely, A., D. Tullsen, and G. Voelker: Symbiotic Jobscheduling with Priorities for a Simultaneous Multithreading Processor, Proceedings of the International Conference on Measurements and Modeling of Computer Systems, SIGMETRICS 2002, 66:76, Marina Del Rey, (Acceptance rate 14%)
33. Snavely, A., L. Carrington, and N. Wolter: Modeling Application Performance by Convolving Machine Signatures with Application Profiles, IEEE Workshop on Workload Characterization, December 2001, Austin

34. Snavely, A. and D. Tullsen: Symbiotic Jobscheduling for a Simultaneous Multithreading Machine, ASPLOS-IX Proceedings of the 9th International Conference on Architectural Support for Programming Languages and Operating Systems, 234:244, 2000, Boston
35. Carrington, L., N. Wolter, and A. Snavely: A Framework for Application Performance Prediction to Enable Scalability Understanding, Scaling to New Heights Workshop, May 2002, Pittsburgh
36. Snavely, A., and L. Carter: Symbiotic Jobscheduling on the MTA, Workshop on Multi-Threaded Execution, Architecture, and Compilers, January 2000, Toulouse.
37. Pfeiffer, W., L. Carter, A. Snavely: Evaluation of a Multithreaded Architecture for Defense Applications, SDSC Technical Report #43, January 2000
38. Snavely, A., G. Johnson and J. Genetti: Data Intensive Volume Visualization on the Tera MTA and Cray T3E, Advanced Simulation Technologies Conference, April 1999, San Diego
39. Carter, L., J. Feo (Tera) and A. Snavely: Performance and Programming Experience on the Tera MTA, Proceedings of the Ninth SIAM Conference on Parallel Processing for Scientific Computing, 1999, San Antonio
40. Snavely, A., N. Mitchell, L. Carter, J. Ferrante, D. Tullsen: Explorations in Symbiosis on two Multithreaded Architectures, M-TEAC, January 1999, Orland.
41. Boisseau, J., L. Carter, A. Snavely, D. Callahan, J. Feo, S. Kahan, Z. Wu: CRAY T90 vs. Tera MTA: The Old Champ Faces a New Challenger, Cray User's Group Conference, June 1998, Stuttgart
42. Snavely, A., L. Carter, J. Boisseau, A. Majumdar, K. S.Gatlin, N. Mitchell, J. Feo, B. Koblenz: Multi-processor Performance on the Tera MTA, SC 98, November 1998, Orlando

Invited Professional Talks and Community Building Activities

- Co-organizer and speaker at upcoming SC2006 Birds of a Feather Sessions “Is 99% Utilization of a Supercomputer a Good thing?” and also “Evaluating Petascale Infrastructure Systems: Benchmarks, Models, and Applications”, November 2006, Orlando
- Invited co-organizer, chair, and speaker, “NSF Workshop on PetaScale Computing for Biologists”, an interdisciplinary workshop bringing together distinguished biologists and computer scientists at NSF headquarters, August 2006
- Invited speaker: NSF Office of Cyberinfrastructure Distinguished Speaker Series, “Getting the Most out of Supercomputers”, at NSF headquarters Arlington, May 2006
- Invited co-organizer, chair, and speaker, “NSF Workshop on PetaScale Computing for the Geosciences”, an interdisciplinary workshop bringing together distinguished geophysicists and computer scientists at SDSC. San Diego, April 2006
- Invited presentation to Congressional Staff: “Who needs a supercomputer?”, at Rayburn Building, Congress of the United States, November 2005
- Session co-chair and speaker “NSF SBE-CISE Workshop on Cyberinfrastructure and the Social Sciences”, Warrington, Virginia. March 2005
- Co-organizer, chair, and speaker “Tour de HPC Cycles”, Seattle, Washington. Panel at SC|05

- Co-organizer and speaker “High-Performance Grid Computing Workshop”, Santa Fe, New Mexico. In conjunction with IPDPS 2004
- Co-organizer and speaker, “Methods for Performance Engineering of Scientific Applications”, SC'04 2004
- Co-organizer and speaker, “PERC Tools for HPC Performance Modeling”, Sigmetrics/Performance 2004
- Invited speaker, “Reconfigurable Supercomputing”, MAPLD 2003
- Co-organizer and speaker, “PERC Tools”, SciComp 2003
- Co-organizer and speaker, “Tools for Performance Analysis and Prediction”, SC2002
- Co-organizer and speaker, “Reconfigurable Supercomputing”, SC2002
- Co-organizer and speaker, “A Framework for Performance Analysis and Prediction”, PTOOLS 2002

Grants

The Performance Evaluation Research Center (PERC) a DOE SciDAC Integrated Software Infrastructure Center (DE-FC02-01ER25491). Robert Lucas PI, Allan Snavely Co-PI (and others see perc.nersc.gov) FY02-FY04 ($600K UCSD budget), then continuing in same role for PERC-II (DE-FC02-01ER2541) FY05-FY07 ($541K UCSD budget), and then continuing in same role for Performance Evaluation Research Institute (PERI), (DE-FC02-06ER25760), FY07-FY11 ($1,425K UCSD budget only).

The Cyberinfrastructure Evaluation Center, (NSF-OCI-0516162) Allan Snavely PI, Dan Reed is equal collaborative PI, FY05-FY08, ($600K UCSD budget).

Workshop on Petascale Computing and the Geosciences, (NSF-GEO-0621611), Allan Snavely PI, FY06-FY07, ($80K).

Workshop on Petascale Computing and the Biosciences, (NSF-BIO-0632517), Allan Snavely, PI, David Bader and Gwen Jacobs, Co-PIs, FY06-FY07, ($54,488).

Feasibility of taking MAS (Megnetohydrodynamic Algorithm outside a Sphere) to petascale, (NSF-ATM-0637994), Allan Snavely, PI, FY06-FY07 ($40K).

Feasibility of taking the WRF (Weather Research and Forecasting) model to petascale, (NSF-ATM- 0637239) Allan Snavely, PI, FY06-FY07 ($39,553).

Performance Measurement & Modeling of Deep Hierarchy Systems, (NSF-NGS-0406312), Allan Snavely PI, Jeff Hollingsworth is equal collaborative PI, FY04-FY07, ($262K UCSD budget)

High Performance Computing Benchmarks Initiative, a Department of Defense funded effort (via interagency funds transfer to NSF) to develop relevant performance models for applications of interest to DOD and the wider community. Allan Snavely, PI, FY02-FY08, ($1,305K).

PetaScale Execution Time Evaluation (DE-FG02-04ER25598) a DOE funded investigation into how to best evolve HPC architectures over the next 10 years. Allan Snavely PI, Robert Lucas and Jeff Vetter are equal collaborative PIs, FY04-FY07 ($900K UCSD budget).

PetaScale Development Time Evaluation (DE-FG02-04ER25634) a DOE funded investigation into how to best program evolving HPC architectures over the next 10 years, Allan Snavely, PI, Jeremy Kepner and others are equal collaborative PIs, FY04-FY07 ($150K UCSD budget).

Data-intensive Grid Benchmark (CNS- 0230925), Chaitan Baru, PI, Allan Snavely and Henri Casanova, Co-PIs. FY02-FY05 ($750K).

Course Taught at UCSD

Undergraduate Computer Architecture, 2001-2003
Advanced Graduate Compilers, 2003
Graduate Scientific and Parallel Computing, 2004
Graduate Seminar: Largescale Systems, 2005-2006

Professional Activities

Co-author on the NSF report Petascale Computing in the Biological Sciences, 2006

Co-author on the NSF report Establishing a Petascale Collaboratory for the Geosciences, 2005

Co-founder of the Grid Benchmarking Research Group in the Global Grid Forum, 2002

Technical Papers Co-Chair SC2005

U.S. Vice-Chair for Performance Euro-Par 2005 (Lisbon), Euro-Par 2006 (Dresden)

Program Committee, Fourth Workshop on High Performance Grid Computing (HPGC '07) in conjunction with the 21st International Parallel and Distributed Processing Symposium (IPDPS '2007)

Deputy Panels Chair and Technical Papers Committee, SC2003. Panels Chair, SC2004. Technical Papers Committee, SC 2007

Program Committee ICS05, 2005

Reviewer for the Federal Plan for High-End Computing: Report of the High-End Computing Revitalization Task Force (HECRTF), May 2004

Vice-Chair for Performance and Metrics: Workshop on the Road Map for the Revitalization of High End Computing, May 2003

Reviewer for NWO Computer Science Open Competition Netherlands (on going)

Reviewer for NERSC ERCAP computational reviews (on going)

Reviewer for DoD Grand Challenge Compute projects (on going)

Steering committee, HPC Users Forum (on going)

Advisory panel Star Bridge Systems (see www.starbridgesystems.com) (on going)

Co-Chair, Workshop on Performance Modeling and Prediction, ICCS, Melbourne, 2003

Co-Organizer, Workshop on Grid Benchmarking, IPDPS04, Santa Fe, 2004

Technical Referee

ACM Transactions on Architecture and Code Optimization (TACO)

IEEE Transactions on Computing (TOCS)

Advising and Mentoring

- Xiaofeng Gao (co-advised with Larry Carter), Ph.D. granted 2006, Thesis entitled "Reducing Time and Space Cost for Memory Tracing," (now at Microsoft)
- Gregory Lee, M.S. granted 2006, Thesis entitled "Scalable Dynamic Instrumentation for Large Scale Machines," (now at Lawrence Livermore National Laboratory)
- Siddharth Gidwani, M.S. granted 2005, Thesis entitled "Implementation of HMMer on a Reconfigurable Processor," (now at Microsoft)
- Jon Weinberg, M.S. granted 2005, Thesis entitled "Quantifying Locality In The Memory Access Patterns of HPC Applications," (now still my Ph.D. student)
- David Tamjidi, M.S. granted 2005, Thesis entitled "An Overview and Benchmark Study of the Starbridge Reconfigurable Computing Platform," (now consulting in Italy)

Current Ph.D. students: Michael O. McCracken (co-advised with Jeanne Ferrante), Cynthia Bailey Lee, Michael Laurenzano, Jiahua He (supported by Intel), Jon Weinberg

Current Masters students: Omid Khalili (hired already by Apple), Geoffrey Romer (hired already by Google)

References

Larry Carter (advisor)
Professor Emeritus
Computer Science and Engineering Dept.
University of California, San Diego
9500 Gilman Drive, Mail Code 0404
La Jolla, CA 92093-0404
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Jack Dongarra
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University of Tennessee
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1122 Volunteer Blvd
University of Tennessee
Knoxville, TN 37996-3450
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Fran Berman
High-Performance Computing Endowed Chair
Director, San Diego Supercomputer Center
9500 Gilman Drive, Mail Code 0505
La Jolla, CA 92093-0505
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Dan Reed
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