A 0.25-μm, 600-MHz, 1.5-V, Fully Depleted SOI CMOS 64-Bit Microprocessor

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***Abstract*—A 0.25-μm, four-layer-metal, 1.5-V, 600-MHz, fully depleted (FD) silicon-on-insulator (SOI) CMOS 64-bit ALPHA1 microprocessor integrating 9.66 million transistors on a 209-mm^2 silicon die has been developed leveraging the existing bulk design. FD-SOI technology is used because it has better immunity for dynamic leakage current than partially depleted SOI in high-speed dynamic circuits without body contact. C–V characteristics of metal-oxide-silicon-oxide-silicon with and without source-drain junctions are described to explain the behavior of FD-SOI transistor. Race, speed, and dynamic stability have been simulated to reassure the circuit operation. Key process features are shallow trench isolation, 4-nm gate oxide, 30-nm co-silicide, 46-nm silicon film, and 200-nm buried oxide. The FD-SOI microprocessor runs 30% faster than that of bulk, and it passes the reliability and system test.**

***Index Terms*—Cascode voltage switch logic (CVSL), chemical mechanical polishing (CMP), circuits, CMOS, critical path, C–V, dynamic CMOS circuit design, floating body effect (FBE), fully depleted, microprocessor, partially depleted, race, short channel effect (SCE), silicon on insulator (SOI), threshold voltage.**

I. Introduction

ALPHA microprocessor speed has been improved 31% per year since 1992, and it will reach up to 3.5 GHz by 2004 at this rate. But when a CMOS technology advances beyond 0.25 μm, the speed benefits from scaling down begin to taper off. There are more severe problems such as short channel effects (SCE's), thin gate oxide, poor subthreshold slope, large parasitics, low operating voltage, and large interconnect delay. These problems limit the improvement of each new process generation. Many boosting technologies such as SOI, Cu, and flip-chip package have been developed to compensate for these problems. The speed impact of these technologies is shown in Fig. 1 as a dashed line based on assumptions in Table I.

A 0.25-μm, four-layer-metal, 1.5-V, 600-MHz, fully depleted silicon-on-insulator (FD-SOI) CMOS 64-bit microprocessor [1] integrating 9.66 million transistors on a 209-mm^2 silicon die has been developed leveraging the existing bulk design [2]–[9]. The implementation and the technology features are in Tables II and III, respectively.

II. Microarchitecture

This microprocessor uses outstanding CMOS circuit design technique and methodology [10] to achieve the highest speed in a given microarchitecture and technology. This work demonstrates that a microprocessor that integrates the high-performance microarchitecture as shown in Fig. 2 can be successfully implemented using FD-SOI CMOS technology.

TABLE I
Speed Tradeoffs

Start with Alpha 21264A 1GHz @2.0V, 0.25µm 6-metal bulk CMOS wire bonding		
• SOI (C_j reduction):	Speed Increase = 1.2X	=> 1.2GHz
• Flip-chip (IR drop reduction):	Speed Increase = 1.1X	=> 1.3GHz
• Cu (R_{int} reduction):	Speed Increase = 1.1X	=> 1.4GHz
• Low-k (C_{int} reduction):	Speed Increase = 1.05X	=> 1.5GHz
• Design (critical path improvement):	Speed Increase = 1.1X	=> 1.6GHz
• Low Vdd (voltage reduction):	Speed Increase = 1.3X	=> 2.1GHz
• Scaling (0.25µm ->0.18µm):	Speed Increase = 1.5X	=> 3.2GHz
• Scaling (0.18µm ->0.13µm):	Speed Increase = 1.5X	=> 4.8GHz

TABLE II
Implementation Features

- Nominal Vddi: 1.5V ± 100mV / Vdd: 2.0V ± 100mV
- 600MHz 14W @Vddi = 1.5V, Vdd = 2.0V and 85ºC
- 9.66 Million Transistors @14.4mm x 14.5mm (209mm^2)
- 8K ICache and 8K Dual Read DCache
- 96K 3-Way Set Associative SCache
- 4-Way Superscalar: 2 Integer Pipe, 2 Floating Point Pipe
- 499 Pin IPGA (296 Signal Pins, 200 Vddi/Vdd/Vss, 3 Unused)
- 0.25µm Gate Length @0.35µm Drawn Database

TABLE III
Technology Features

- 0.25µm 4-Metal FD-SOI CMOS
- SOI Thickness: 46nm
- BOX Thickness: 200nm
- Isolation: Shallow Trench Isolation
- Gate Oxide: 4nm GNOX
- Transistor: Dual Gate Co-Silicide
- V_{TN}/V_{TP}: 0.36V/-0.36V
- Subthreshold Swing: 74mV/dec for nMOSFET

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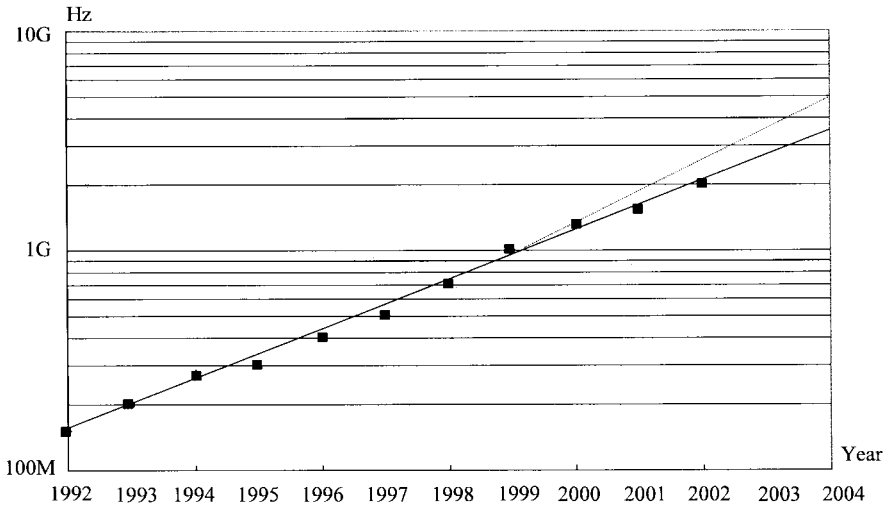


Fig. 1. Alpha CPU speed versus time. Dashed line shows the speed boost thanks to emerging technologies such as SOI, Cu, and flip-chip package.

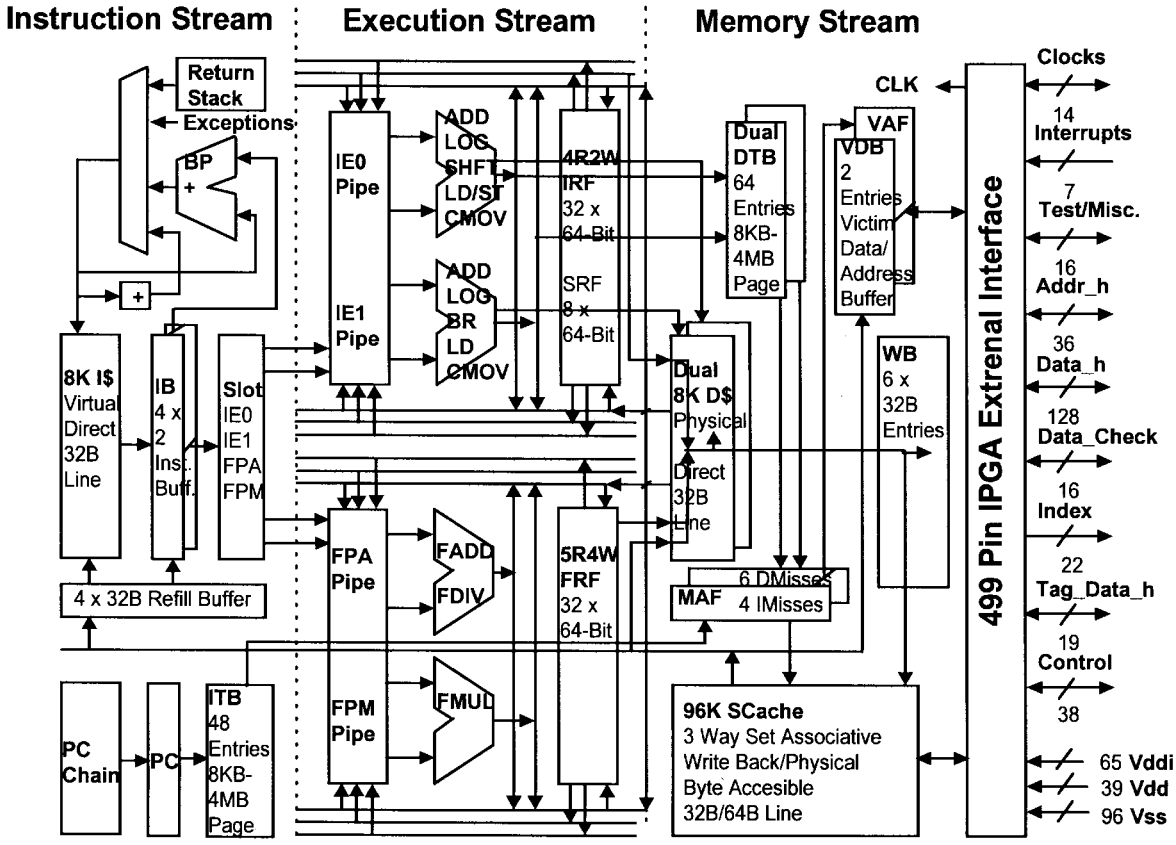


Fig. 2. Microarchitecture overview. Note the three major streams: instruction, execution, and memory.

III. SOI CMOS Technology

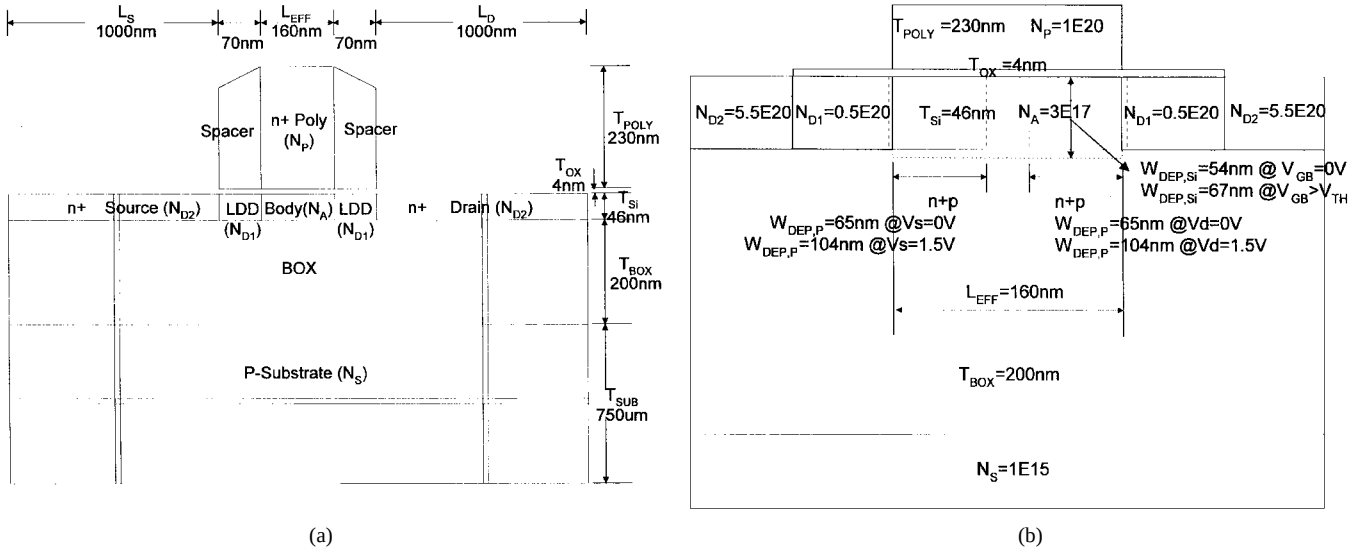
A. Technology Tradeoffs

There are many advantages in SOI such as reduction in junction capacitance, reduction of dynamic power, high immunity to soft errors, improvement in packing density and latchup, low operating voltage, more stacked transistors, candidate for double gate transistor [11], excellent microwave characteristics [12], candidate for high-temperature applications [13] and perfect isolation by simple fabrication process.

Despite of all these advantages, SOI has not been commercially successful due to inherent problems in material, process, device, and design. SOI is a less mature technology for mass production of low-cost, low-defect density wafer and process, and it needs critical control of the silicon thickness and surface microroughness. A 50-nm film with 5-nm nonuniformity across the wafer can result in V_t instability of $\sim$0.1 V [14], and microroughness below 0.5-nm rms is critical for wafer bonding [15]. High series resistance associated with source-drain in SOI dramatically reduces the output currents in thin silicon film. The body is floating in SOI and results in floating

TABLE IV
PD-SOI VERSUS FD-SOI

	PD-SOI	FD-SOI		PD-SOI	FD-SOI
Performance	Good	Good	Manufacturability	Good	Poor
Design Compatibility	Poor	Good	Breakdown Voltage	Good	Poor
CAD Environments	Poor	Poor	Leakage Current	Good	Poor
Stability w/ contact	Good	Fair	Transconductance	Good	Poor
Stability w/o contact	Poor	Good	Short Channel Effect	Poor	Good
Operation Voltage	High	Low	Body Contact	Good	Poor
History Dependence	Poor	Good	Body Effect	Good	Good
Parasitic Bipolar Effect	Poor	Good	Self-Heating	Poor	Poor



(a) (b)

Fig. 3. (a) Schematic cross section of the FD-SOI NMOS transistor. (b) Depletion width at $Q_{\rm ssf} = 0.1$ fC/μm^2.

body effects (FBE's) such as kink current, low breakdown voltage, hysteresis, and self-heating, though the self-heating can be neglected in most digital circuits due to high-speed switching [16].

It is common to provide the body contact to minimize the FBE [17]. Source engineering to lower the diffusion potential is also used to mitigate the FBE by recombination of the impact ionized carriers [18]. FD-SOI assumes no neutral region in the body so that the impact ionized carriers can be injected into the source by gradual diffusion or recombination. FD-SOI technology has been more promising than partially depleted (PD)-SOI in that it has less FBE without body contact. It also provides inherent immunity to SCE due to thin film thickness, which removes the shared depletion charge section. FD-SOI provides excellent scaling properties [19], steep subthreshold slope, stable dynamic operations, and reduced hot-electron effects due to less steep potential drop near the drain induced by back gate. FD-SOI allows a lighter substrate doping for SCE, and it improves transconductance for less velocity saturation due to reduction of lateral field.

However, FD-SOI has many shortcomings. It is difficult to control the V_t, which is coupled by back gate bias in FD-SOI, and also it is dependent on the uniformity of film thickness. PD-SOI may have better short channel effects if it scales down to the 100-nm regime. Also, PD-SOI has higher breakdown voltage, higher driving current, and better series resistance in source-drain. FD-SOI is more sensitive to total dose effects, which control the state densities of oxide interfaces. The pros and cons for FD-SOI and PD-SOI are listed in Table IV.

B. FD-SOI Transistor

FD-SOI has excellent features compared to bulk and PD-SOI not only for the digital but also for the analog circuits [20], [21]. The cross section of the FD-SOI NMOS transistor used in this work is shown in Fig. 3(a). The 46-nm silicon thickness makes the body deplete in all operation ranges. Vertical depletion width at 0-V gate bias is reached up to 65 nm, as shown in Fig. 3(b), when the $Q_{\rm ssf}$ (oxide surface state charge for front gate) is assumed to be 0.1 fC/μm^2. Lateral

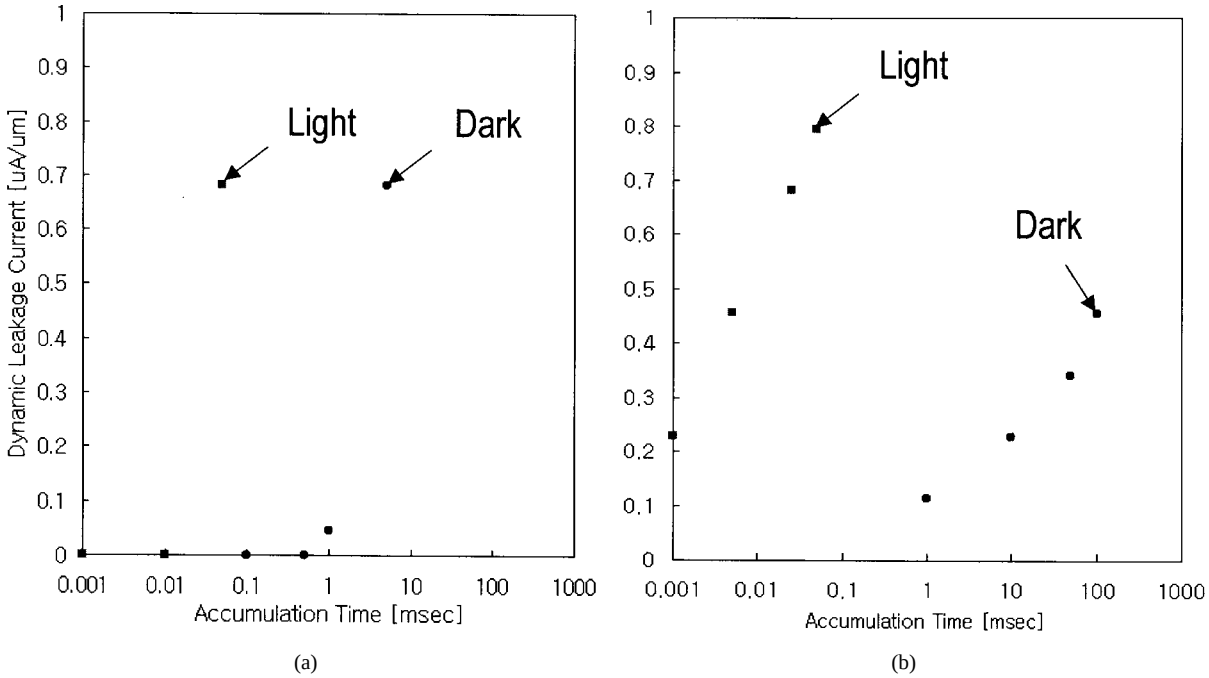


Fig. 4. Dynamic leakage current: (a) FD-SOI and (b) PD-SOI.

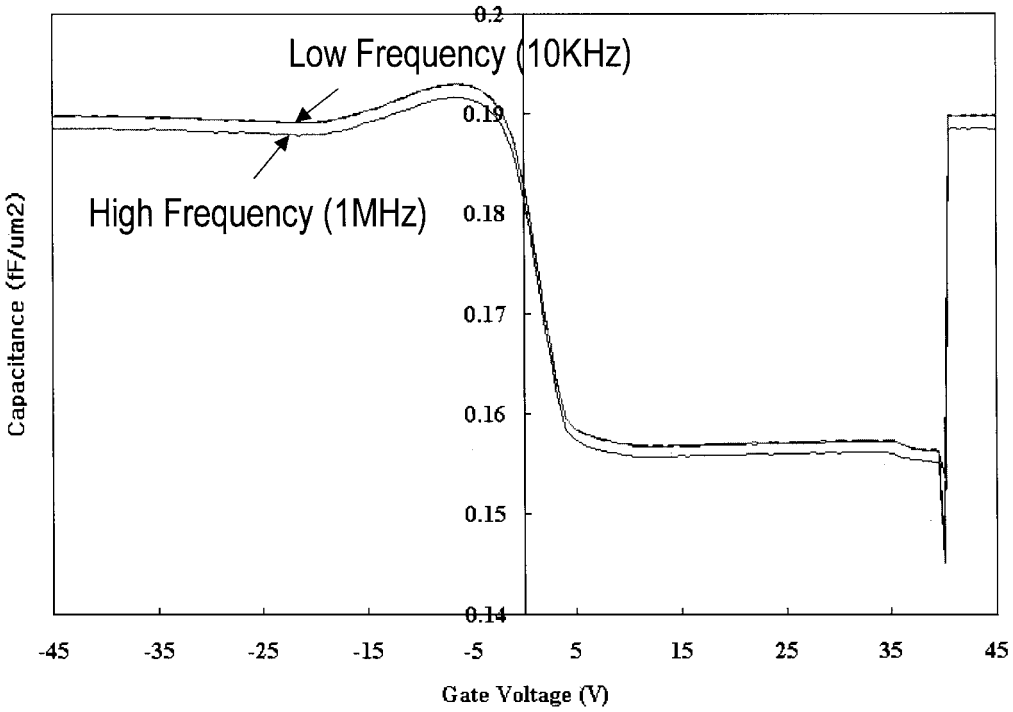


Fig. 5. Low- and high-frequency C–V curve for MOSOS structure.

depletion widths are also shown for each bias condition. The level of depletion provides the explanation for kinks and dynamic instabilities for FD-SOI where the mechanism is different since there is no neutral body region [22]. Hole distribution and electric field in the body defines the level of depletion as deep or mild.

Dynamic leakage currents for FD-SOI and PD-SOI have been measured following the known method [23]. The results shown in Fig. 4 imply that FD-SOI has dynamic leakage current as low as 0.045 μA/μm when the charging time is 1 ms. But it increases exponentially to 0.7 μA/μm at 7 ms in FD-SOI. While the PD-SOI has 0.11 μA/μm at 1 ms, it increases linearly to 0.2 μA/μm at 10 ms. It can be explained as the high field driven holes are accumulated under gate, and they are multiplied exponentially in FD-SOI after it reaches critical density that is similar as breakdown. PD-SOI has the neutral region for gradual carrier multiplication so that the increase rate of dynamic leakage current is slower than that

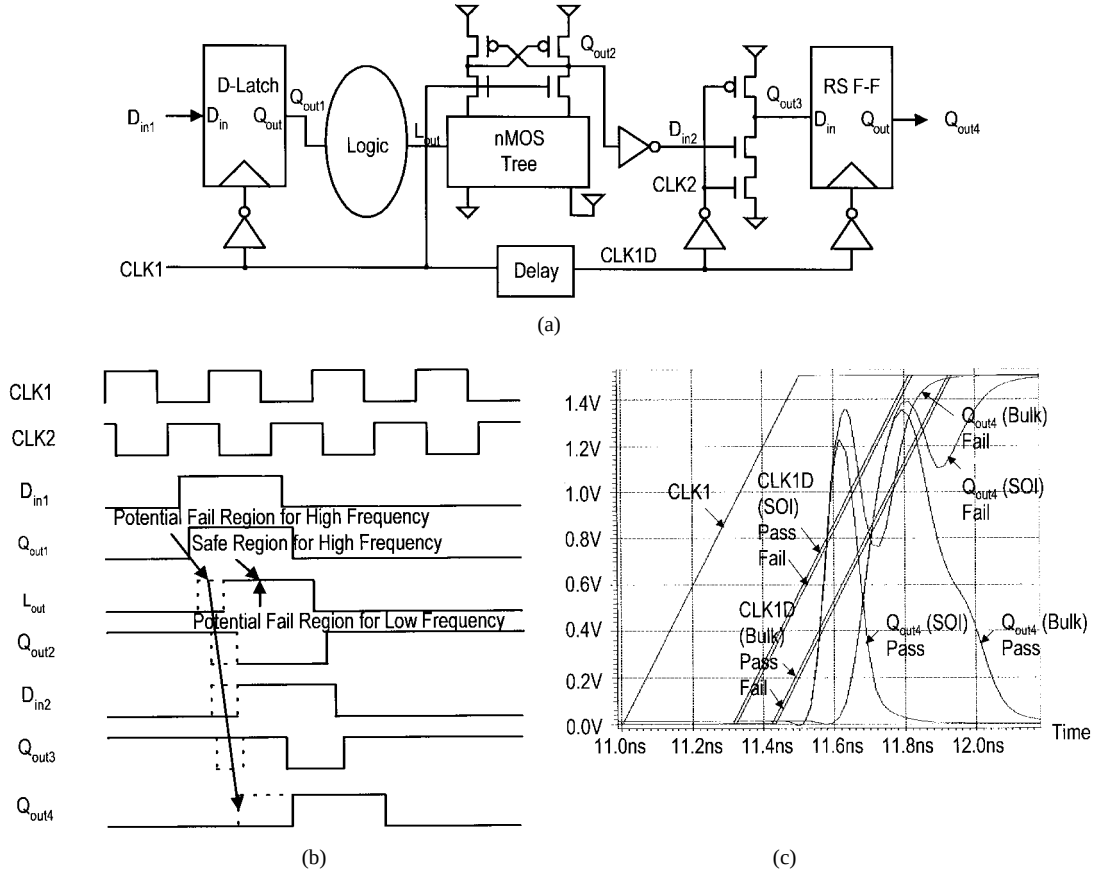


Fig. 6. (a) Schematics for frequency-dependent race case study, (b) timing diagram, and (c) simulation results.

of FD-SOI. As a result, FD-SOI is good for dynamic circuits that are refreshed per several milliseconds at maximum. This microprocessor uses intensive dynamic circuits, and FD-SOI is preferred.

Two types of metal-oxide-silicon-oxide-silicon (MOSOS) C–V curves have been studied. One is for the MOSOS capacitor, which is completely enclosed by the oxides as top for front gate, bottom for back gate, and two sides for shallow trench isolation (STI). Because there is no carrier in and out for this enclosed capacitor, the field driven holes are gathered in some region inside the body, and it becomes the accumulation layer. The existence of this accumulation layer is shown in the C–V curve in Fig. 5 as up and down of the capacitance depending on gate potential [19], [24], [25]. When the body is split with two capacitors in between the accumulation layers, the capacitance decreases. The capacitance increases if there is no accumulation layer inside the body. The other type is for the MOSOS capacitor with source-drain junctions, and it results in a similar C–V curve as that of bulk. It shows that there are no accumulation region for this structure because the gathered holes are diffused to source-drain junctions.

IV. Circuit Design

This microprocessor uses intensive dynamic circuits such as dynamic-level sensitive latch, multistage domino in a single phase, multistage cascode voltage switch logic (CVSL) circuits with huge clock drivers, and precise clock skew control network [2]–[6]. FD-SOI is used to provide the dynamic stability without body contact. There are three major types of design work for FD-SOI. First, the race has been verified in FD-SOI because the significant reduction in junction capacitance causes speed kinks in dynamic NMOS trees. Second, the circuit speed has been evaluated. Last, the dynamic stability also has been simulated.

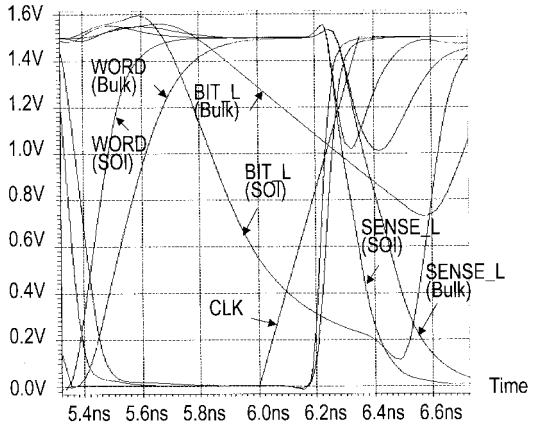


Fig. 7. Critical path circuit simulations of the Dcache read for the FD-SOI versus bulk.

A. Race

It is well known that race can occur at any frequency. But it is interesting that the frequency-dependent race can occur in

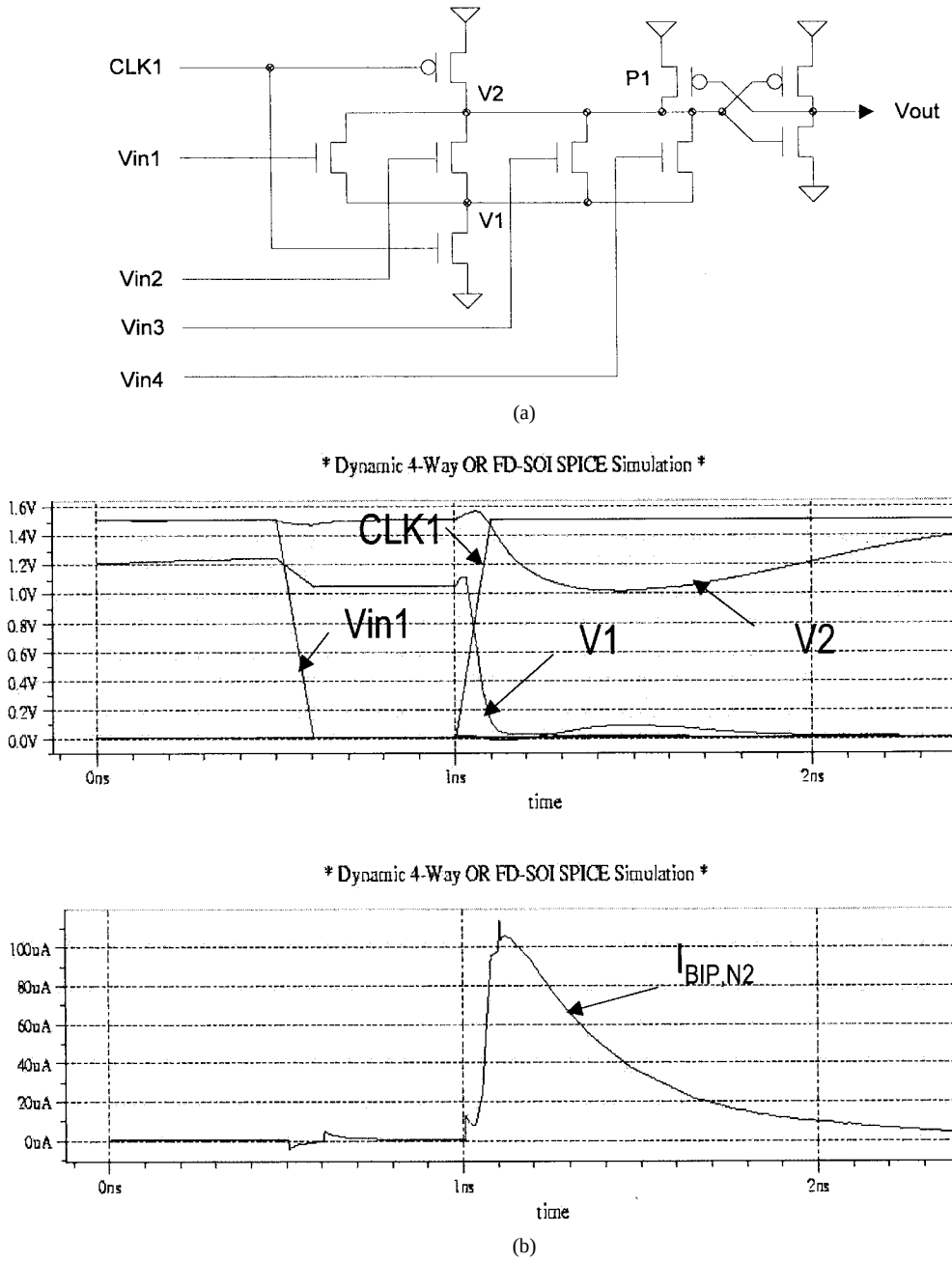


Fig. 8. (a) Dynamic four-way OR circuit and (b) SPICE simulation results for the circuit.

a certain circuit style, as shown in Fig. 6(a). This circuit may work at high frequency but may not work at low frequency. It is composed of a CLK2 latch, some logic function, and a CVSL CLK1 latch. The output of the CVSL latch is driven into CLK2 multistage domino logic, and CLK2 RS flip-flop samples the domino output. If NMOS trees in CVSL and domino are too fast because of significant reduction in junction capacitance, $L_{\rm out}$ may possibly race through to $Q_{\rm out4}$ during the overlapping period between CLK1 and CLK2, as shown in Fig. 6(b). If $L_{\rm out}$ comes out in CLK1-high as designed, there is no race issue for this circuit. If $L_{\rm out}$ comes out before CLK1-high because of faster SOI NMOS tree in CVSL and domino or because of low frequency, it may possibly race through the circuits. It shows the frequency-dependent characteristics. The pass–fail margin in clock skew to tolerate this race is simulated as 400 ps in the bulk case, as shown in Fig. 6(c). It is reduced to 300 ps in FD-SOI.

B. Speed

A data cache read path is simulated to evaluate the speed improvement as shown in Fig. 7. FD-SOI runs 20–30% faster than bulk in normal circuits such as wordline access, though FD-SOI records 50% faster in bitline evaluation where the junction capacitances are dominant. As a result, SOI is expected to record 20–30% faster than bulk, and it is correlated well with real speed in silicon.

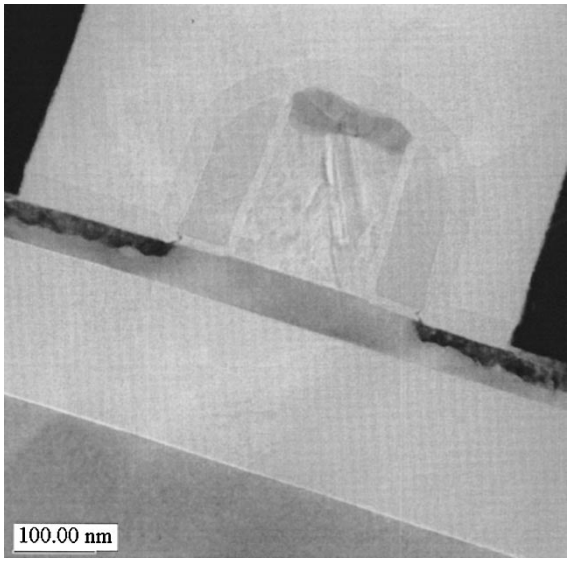


Fig. 9. Fabricated FD-SOI transistor.

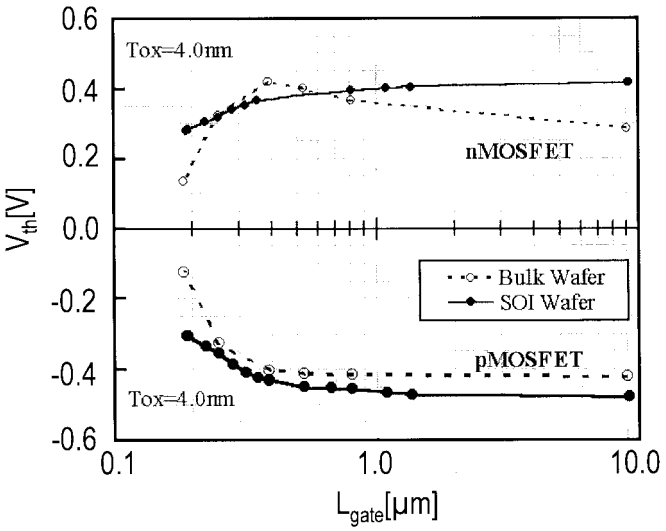


Fig. 10. Reducing short channel effect in FD-SOI compared to bulk.

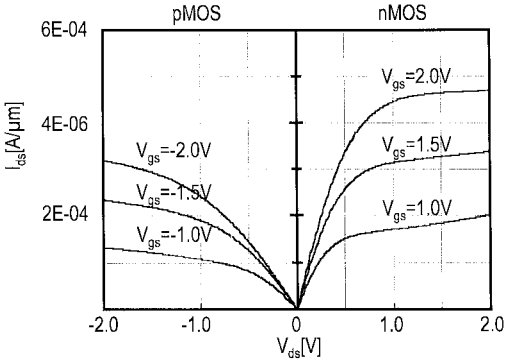


Fig. 11. $I_{\rm ds}$–$V_{\rm ds}$ curves show no appreciable kink effect in FD-SOI CMOS transistors.

C. Dynamic Stability

Dynamic stability has been simulated for four-way dynamic OR circuits, as shown in Fig. 8(a). This circuit does not fail even though the P1 feedback PMOS transistor width is reduced to 2 μm in this work, as shown in Fig. 8(b). The amount of bipolar current is also shown in Fig. 8(c). Previous work on PD-SOI reported failure at this condition [26], [27]. This microprocessor uses intensive dynamic circuits, which are mostly refreshed every cycle. In the actual circuits, the dynamic leakage is less than this simulation and is not sufficient to cause a failure before the next refresh occurs.

V. Process

A 0.25-μm FD-SOI dual-gate CMOS—n^+ poly gate for NMOS and p^+ poly gate for PMOS—technology has been developed. Both SIMOX and bonded wafers are used. The FD-SOI transistor is manufactured as shown in Fig. 9 with 4-nm gate oxide, 46-nm film thickness, and 200-nm buried oxide (BOX) thickness. A trench is etched in thin film for field definition and is refilled with insulator material to form the STI. The surface is planarized by a chemical mechanical polishing (CMP) process. The trench isolation process has been optimized to minimize the consumption of superficial silicon layer on BOX layer during fabrication and to minimize the residual stress of SOI devices. A krypton fluoride (KrF) laser is used to etch the gate pattern. The spacer of the transistor is deposited using CVD silicon dioxide and silicon nitride. An NMOS channel is implanted by BF2, and source-drain regions are implanted by As. A PMOS channel is implanted by P, and source-drain regions are implanted by BF_2. Because Co has no resistivity degradation in narrow gate line and source-drain regions, a super-thin cobalt silicide film process to lower the resistance of the transistor gate, source, and drain is used. It maximizes the transistor performance. CVD silicon oxide is deposited and CMP is carried out for premetal planarization. Four-layer metal interconnections are formed by W-plug and Al alloy deposition. The final step is nitride passivation.

There have been fewer short channel effects as shown in Fig. 10 in SOI. The threshold voltage shifts in short channel are not as serious as those in bulk because there is less charge sharing in FD-SOI, as discussed in Section III. A steep subthreshold current slope of 74 mv/dec is obtained. $I_{\rm ds}$ (saturation current) of NMOS and PMOS is 330 and 220 μA/μm at 1.5 V for $V_{\rm ds}$ and $V_{\rm gs}$, respectively, as shown in Fig. 11, which also shows that there is no appreciable kink current for both FD-SOI transistors. The junction capacitance decreases by an order of the magnitude in SOI compared to that of bulk, and the dependence of operating voltage for junction capacitance is minimum in FD-SOI compared to that of PD-SOI and bulk. The difference of junction capacitances between 2.0 and 0.0 V are 6.8 fF for bulk, 5.7 fF for PD-SOI, and 0.6 fF for FD-SOI in 14 μm $\times$ 0.91 μm p^+ gated diode. Because the FD-SOI body is depleted in all operation ranges, the difference between operating voltages can be minimized.

VI. Test

The shmoo shown in Fig. 12 demonstrates the fabricated chip operating beyond 600 MHz at 1.5 V and 85 °C, which

TABLE V
BULK VERSUS SOI

	Bulk microprocessor	SOI microprocessor	SOI / bulk
Technology	0.25um bulk CMOS	0.25um FD-SOI CMOS	
Speed @1.6V	476MHz	625MHz	1.3
Chip capacitance	12.3nF	9.2nF	0.75
Power dissipation	71mW/MHz	21mW/MHz	0.3

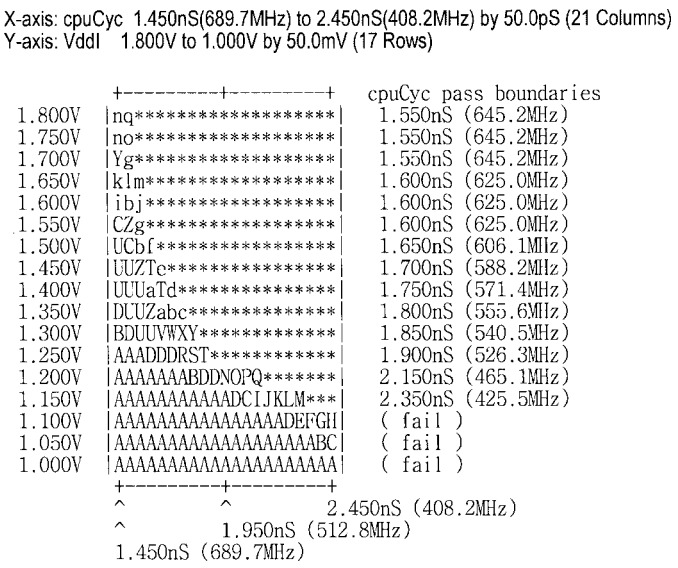


Fig. 12. Shmoo plot for 606.1 MHz at 1.5 V and 85 °C.

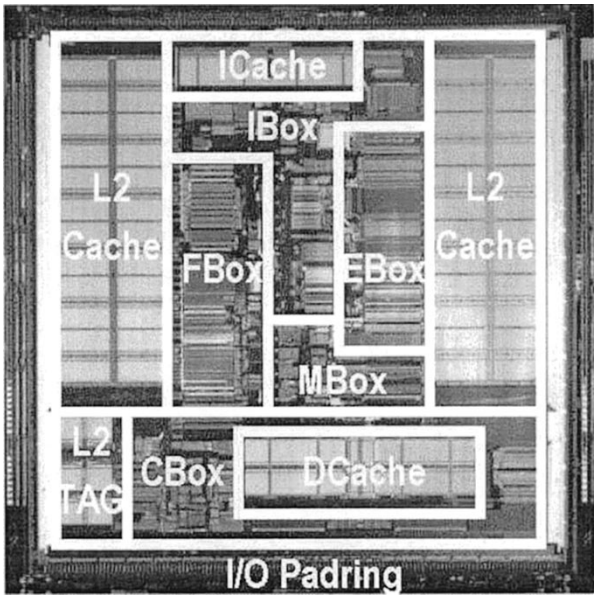


Fig. 13. Chip micrograph.

is 30% faster than that of the bulk chip. The apples-to-apples comparison between 21 164-SOI and 21 164-bulk is listed in Table V. It demonstrates a great power reduction along with low operating voltage in SOI. The chip has passed the high-temperature operating life test, as well as all the system validation tests under Windows NT 4.0 in a motherboard running at 600 MHz. The system runs DVD software for several days without any problem.

VII. CONCLUSIONS

A 0.25-μm, four-layer-metal, 1.5-V, 600-MHz, FD-SOI CMOS 64-bit microprocessor integrating 9.66 million transistors on a 209-mm^2 silicon die has been successfully manufactured, as shown in Fig. 13.

The microprocessor has been waiting for the technology that can provide more transistors with faster speed with less power and lower operating voltage, as well as more interconnections with faster speed with fewer electrical and physical shortcomings. SOI provides a step-function improvement of the microprocessor speed compared to bulk by 20–30% in the same geometry technology.

REFERENCES

[1] Y. W. Kim *et al.*, "A 0.25 μm 600 MHz 1.5 V SOI 64-bit ALPHA Microprocessor," in *ISSCC Dig. Tech. Papers*, Feb. 1999, pp. 432–433.
[2] W. Bowhill *et al.*, "A 300 MHz 64 b quad-issue CMOS microprocessor," in *ISSCC Dig. Tech. Papers*, Feb. 1995, pp. 182–183.
[3] B. Benschneider *et al.*, "A 300 MHz 64 b quad-issue CMOS RISC microprocessor," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1203–1214, Nov. 1995.
[4] W. Bowhill *et al.*, "Circuit implementation of a 300-MHz 64-bit second-generation CMOS Alpha CPU," *Digital Tech. J.*, vol. 7, no. 1, pp. 100–118, 1995.
[5] P. E. Gronowski *et al.*, "A 433 MHz 64 b quad-issue RISC microprocessor," in *ISSCC Dig. Tech. Papers*, Feb. 1996, pp. 222–223.
[6] P. E. Gronowski *et al.*, "A 433 MHz 64 b quad-issue RISC microprocessor," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1687–1696, Nov. 1996.
[7] J. H. Edmondson, P. Rubinfeld, R. Preston, and V. Rajagopalan, "Superscalar instruction execution in the 21164 Alpha microprocessor," *IEEE Micro Mag.*, pp. 33–43, Apr. 1995.
[8] J. Edmondson *et al.*, "Internal organization of the Alpha 21164, a 300-MHz 64-bit quad-issue CMOS RISC microprocessor," *Digital Tech. J.*, vol. 7, no. 1, pp. 119–135, 1995.
[9] D. P. Bhandarkar, *Alpha Implementations and Architecture*. Bedford, MA: Digital Press, 1996, pp. 168–215.
[10] W. J. Grundmann *et al.*, "Designing high performance CMOS microprocessors using full custom techniques," in *Proc. 34th DAC*, 1997, pp. 722–727.
[11] H.-S. Wong *et al.*, "Design and performance considerations for sub-0.1 μm double-gate SOI MOSFET's" in *IEDM Tech. Dig.*, Dec. 1994, pp. 747–750.
[12] J.-P. Raskin, R. Gillon, J. Chen, D. Vanhoenacker-Janvier, and J.-P Colinge, "Accurate SOI MOSFET characterization at microwave

frequencies for device performance optimization and analog modeling," *IEEE Trans. Electron Devices*, vol. 45, pp. 1017–1025, May 1998.
[13] F. Faccio, F. Anghinolfi, E. H. M. Heijne, P. Jarron, and S. Christoloveanu, "Noise contribution of the body resistance in partially-depleted SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 45, pp. 1033–1037, May 1998.
[14] T. C. Hsiao, P. Liu, and J. C. S. Woo, "Advanced technologies for optimized sub-quarter-micrometer SOI CMOS devices," *IEEE Trans. Electron Devices*, vol. 45, pp. 1092–1099, May 1998.
[15] M. Horiuchi, T. Teshima, K. Tokumasa, and K. Yamaguchi, "High-current small-parasitic-capacitance MOSFET on a Poly-Si interlayered (PSI: Ψ) SOI wafer," *IEEE Trans. Electron Devices*, vol. 45, pp. 1111–1115, May 1998.
[16] J. S. Brodsky, R. M. Fox, D. T. Zweidinger, and S. Veeraraghavan, "A physics-based, dynamic thermal impedance model for SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 44, pp. 957–964, June 1997.
[17] S. C. Kuehne, A. B. Y. Chan, C. T. Nguyen, and S. Hong, "SOI MOSFET with buried body strap by wafer bonding," *IEEE Trans. Electron Devices*, vol. 45, pp. 1084–1091, May 1998.
[18] T. Ohno, Y. Kado, and T. Tsuchiya, "Suppression of parasitic bipolar action in ultra-thin-film fully-depleted CMOS/SIMOX devices by Ar-Ion implantation into source/drain regions," *IEEE Trans. Electron Devices*, vol. 45, pp. 1071–1076, May 1998.
[19] F. A. Ikraiam, R. B. Beck, and A. Jakubowski, "Modeling of SOI-MOS capacitors C-V behavior: Partially- and fully-depleted cases," *IEEE Trans. Electron Devices*, vol. 45, pp. 1026–1032, May 1998.
[20] J.-P. Colinge, "Fully-depleted SOI CMOS for analog applications," *IEEE Trans. Electron Devices*, vol. 45, pp. 1010–1015, May 1998.
[21] D. Chang, J. G. Fossum, S. K. Reynolds, and M. M. Pelella, "Kink-free SOI analog circuit design with floating-body/NFD MOSFET's," *IEEE Electron Device Lett.*, vol. 18, no. 12, pp. 602–605, Dec. 1997.
[22] J. G. Fossum *et al.*, "Subthreshold kink in fully depleted SOI MOSFET's," *IEEE Electron Device Lett.*, vol. 16, pp. 542–544, Dec. 1995.
[23] F. Assaderaghi, G. G. Shahidi, L. Wagner, M. Hsieh, M. Palella, S. Chu, R. H. Dennard, and B. Davari, "Transient pass-transistor leakage current in SOI MOSFET's," *IEEE Electron Device Lett.*, vol. 18, pp. 241–243, June 1997.
[24] L. J. McDaid *et al.*, "Interpretation of capacitance-voltage characteristics on silicon-on-insulator (SOI) capacitor," *Solid-State Electron.*, vol. 32, no. 1, pp. 65–68, 1989.
[25] F. T. Brady *et al.*, "Determination of the fixed oxide charge and interface trap densities for buried oxide layers formed by oxygen implantation," *Appl. Phys. Lett.*, vol. 52, no. 11, pp. 886–888, Mar. 1988.
[26] P.-F. Lu, C.-T. Chuang, J. Ji, L. F. Wagner, C.-M. Hsieh, J. B. Kuang, L. L.-C. Hsu, M. M. Palella, S.-F. S. Chu, and C. J. Anderson, "Floating-body effects in partially depleted SOI CMOS circuits," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1241–1253, Aug. 1997.
[27] C.-T. Chuang, P.-F. Lu, and C. J. Anderson, "SOI for digital CMOS VLSI: Design considerations and advances," *Proc. IEEE*, vol. 86, pp. 689–720, Apr. 1998.

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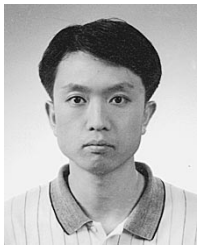

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