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Performance Analysis of Universal Filter Using CNTFET

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***Abstract*— In this paper the performance is analyzed of universal filter which is designed using DDCC based on CNTFET technology. This filter contains three output and four input terminals. DDCC circuit with CMOS suffers from the problem of leakage current and low frequency response. But DDCC designed using CNTFET gives better frequency response than CMOS based DDCC. This nanotechnology improves packaging density. Circuits designed using CNTFET has very high device density, higher temperature stability. Simulation results show that power consumption is very low in case of this proposed filter. The performance of the proposed circuit is confirmed from HSPICE simulation results.**

***Keywords*— CNTFET, DDCC, HSPICE**

I. INTRODUCTION

Filter can be designed by using current mode circuits such as operational amplifier and differential difference current conveyor or by using different active elements. Due to good bandwidth and low power consumption, DDCC and op-amps are famous now a day. Structures using the op-amp and the resistors are not suitable for IC fabrication. DDCC is the combination of CCII and DDA. In this paper, a single DDCC (using CNTFET technology) based filter employing two resistors and two capacitors is proposed. Current-mode circuits are a better choice for accuracy and high frequency performances. The DDCC implementation with carbon nanotube field effect transistor shows better high frequency performance [7]. This paper is organized as follows. The section-II consist the basic introduction of the carbon nanotube field effect transistor. In the section-III, the basics of differential difference current conveyor (DDCC) are shown. In the section-IV, the designs of universal filter using CNTFET is presented. Section V shows its performance, simulation result and comparison with CMOS based circuits.

II. CNTFET TECHNOLOGY

There has been enormous development in embed in number of transistors in the IC. The development is facing issues due to increase in cost, to fabricate devices with smallest features from 350nm to 100nm.

And also the device can not function properly in ultra-density integration due to short channel effects, generation hot electronics etc. In order to continue the miniaturization of circuit elements down to nanometre scale, researchers investigated the concepts of nanotechnology to build CMOS devices. CNTs are sheets of graphene rolled into tubes. The single-walled CNT can be either metallic or semiconducting depending on the chirality (i.e., the direction in which the graphene sheet is rolled). Semiconducting nanotubes have attracted the widespread attention of device/circuit designers as an alternative channel implementation for high performance transistors.

The nano scale devices like carbon nanotube field effect transistor, due to its property it can perform both as switches and amplifiers. In this paper we will discuss how these nano electronics devices can be used in the real time applications. I_{on}/I_{off} ratio for CNTFETs is greater than the conventional MOSFETs and mobility of charge carriers in the Carbon Nanotube Field Effect Transistor (CNTFET) is also high as compared to the conventional MOSFETs [6].

III. DDCC DEVICE

The electrical symbol of DDCC is shown in fig.2. It provides the advantages of CCII and differential difference amplifier (DDA) such as larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry, low power consumption and high-input impedance. It has three voltage input terminals: Y1, Y2 and Y3 which have high input impedance. There is a low impedance current input terminal X. Terminal Z is a high impedance current output terminal . Fig.3 shows the implementation of DDCC using CMOS [2]. In this paper we are using CNTFET at place of conventional CMOS for improving the performance of DDCC [7]. Using CMOS universal filter is already designed. In this paper supply voltage is applied 0.9v. Due to less supply voltage power consumption is low. But performance is not degraded. DDCC circuits are used for universal filter as explained in previous paper [1].

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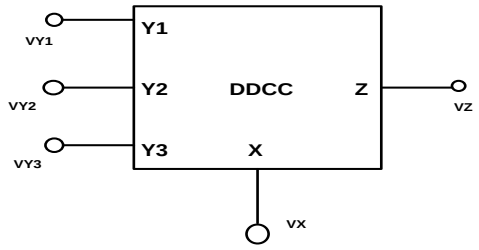

Fig 2. Electrical symbol of DDCC

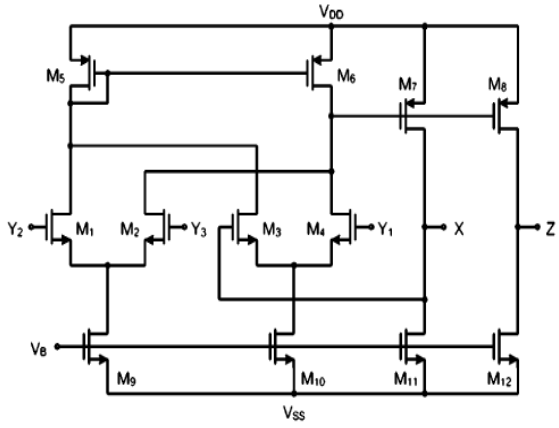

Fig 3. CMOS implementation of DDCC

The input-output characteristic of the DDCC is described by matrix equation as follows. This equation is for DDCC+.

$$\begin{pmatrix} V_x \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{pmatrix} = \begin{pmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_x \end{pmatrix}$$

IV. Universal Filter Using CNTFET

Using one DDCC, universal filter that contains two resistors and two capacitors is implemented. Circuit, which is implemented using CNFET, is shown in fig. 4. The circuit employs three DDCCs, two grounded capacitors and one grounded resistor. Note that the employment of grounded capacitors is more suitable for integrated circuit implementations [9].

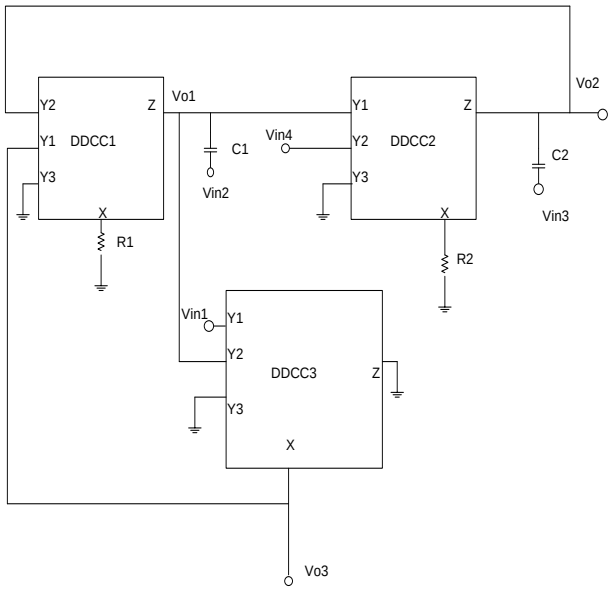

Fig 4. Universal Filter

Case 1: When input is applied at Vin1:

Vout1-Bandpass, Vout2-Lowpass, Vout3-Bandstop

Case 2: When input is applied at Vin2

Vout1 and Vout3-Highpass (Inverting and Non-inverting), Vout2-Bandpass.

Case 3: When input is applied at Vin3

Vout1 and Vout3-Bandpass (Inverting and Non-inverting)

Case 4: When input is applied at Vin4

Vout1 and Vout3-Lowpass (Inverting and Non-inverting)

V. Simulation Results

For simulation HSPICE VER-A 2008-03 tool is used. In this chapter simulation is done for second proposed filter. Filter is designed with fo =0.485MHz, C1 = 30pF, C2= 25pf and R1 = R2 =10kΩ. The biasing voltage V_b was taken as -0.70V. From fig. 5 to 8, represent the simulated amplitude-frequency responses for previously explained four cases respectively.

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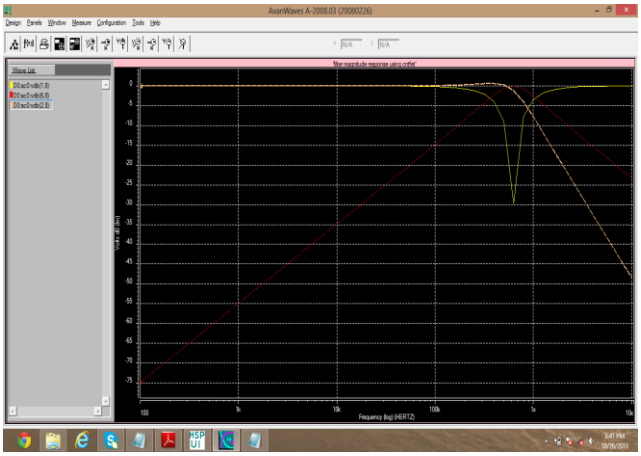

Fig 5. Magnitude response when input is applied at Vin1

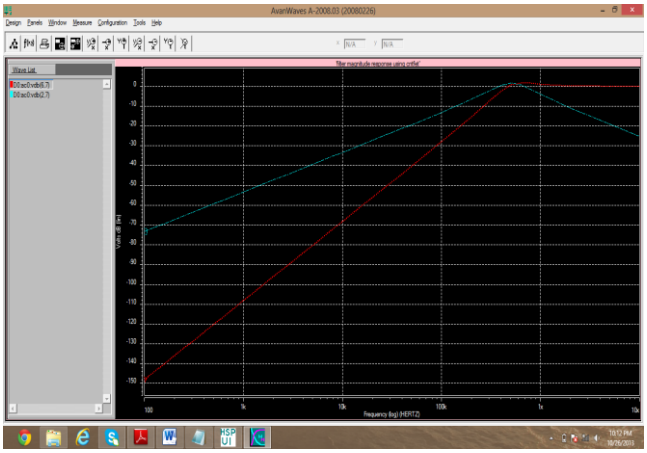

Fig 6. Magnitude response when input is applied at Vin2

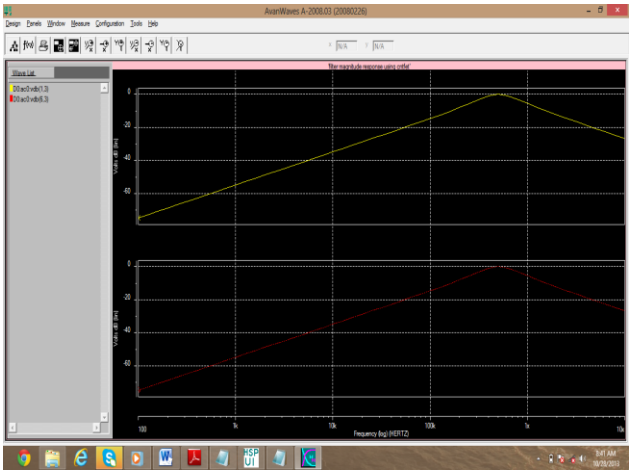

Fig 7. Magnitude response when input is applied at Vin3

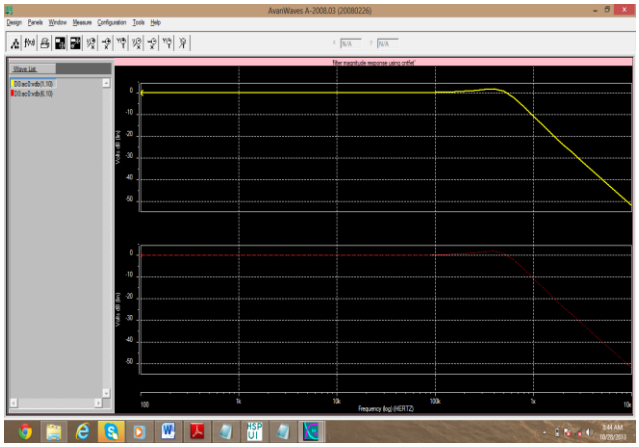

Fig 8. Magnitude response when input is applied at Vin4

For case 4 inverting and non-inverting lowpass filter is shown in fig. 9. CMOS based filter response is shown in fig. 10.

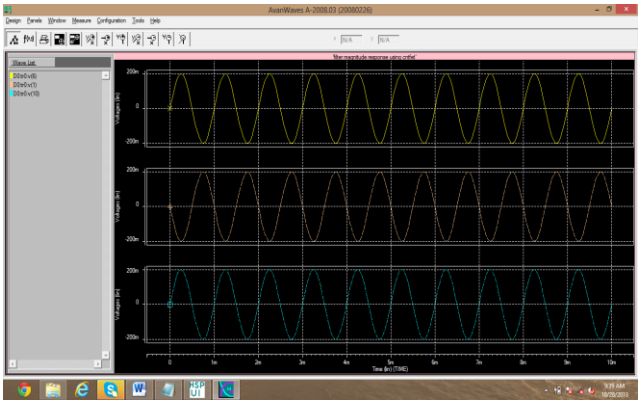

Fig 9. Transient response of inveriting and non-inverting lowpass filter

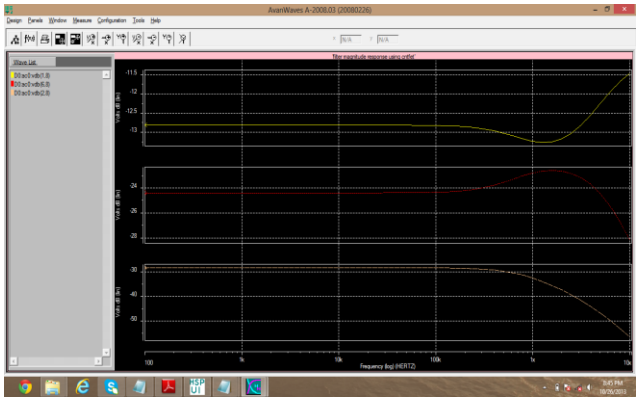

Fig 10. Magnitude response of BP, LP & BS filter using CMOS

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CNFET based circuit works upto 0.3v but CMOS based circuits do not work properly below 0.9v power supply. Below 0.3v power supply CNFET based circuits are failed. Power consumption is less for filter using CNFET.

Table:
Temperature and power consumption relation for BP, BS and LP filter using CNTFET

S.No	Temperature(^{0}C)	Power Consumption(Watt)
1.	25	$2.117x10^{-6}$
2.	50	$3.276x10^{-6}$
3.	100	$6.57x10^{-6}$

VI. CONCLUSION

The performance of the proposed circuit is confirmed from HSPICE simulation results. The CNTFET technology works on 0.9 V_{dc} drive voltage, the circuit is very power efficient. The obtained cutoff frequency is 0.75e+05 Hz. Power consumption is 56.6mw for CMOS based circuit. CNTFET based result are more close to theoretical value and more temperature stable.

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