Control Design for Electronic Power Converters

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Control Design for Electronic Power Converters

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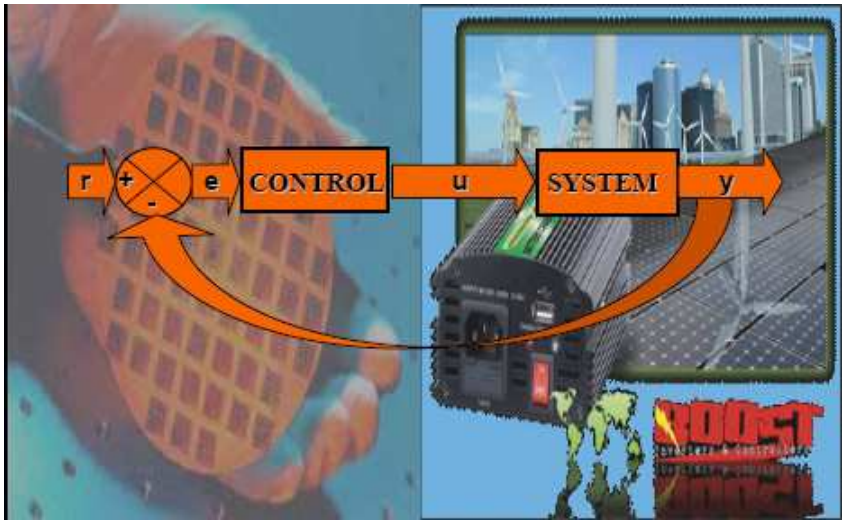
PhD Thesis



Control Design for Electronic Power Converters

By
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Supervised by
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A mi familia y a Alexandre

Contents

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Notation

The following symbols and conventions will be used consistently throughout the thesis.

$\equiv$	identically equal
$\not\equiv$	not identically equal
$\approx$	approximately equal
$\triangleq$	defined as
$<(>)$	less (greater) than
$\leq(\geq)$	less (greater) than or equal to
$\ll(\gg)$	much less (greater) than
$\pm$	plus and minus
$\forall$	for all
$\in$	belongs to
$\subset$	subset of
$\cap$	intersected with
:	such as
$\rightarrow$	tend to
x^T	the transpose of a vector x
∞	infinity
$\sum$	summation
$\|x\|$	the absolute value of x
$\|\|x\|\|$	the norm of a vector x
$\|\|x\|\|_p$	the p-norm of a vector x
$[a,b]$	closed interval from a to b
$\{1,2,...,N\}$	the set from 1 to N
x_k	discrete variable
q^{-1}	discrete-time delay or parameter, i.e., $x_{k-1} = q^{-1}x_k$
$\mathbb{R}^n$	the n-dimensional Euclidean space
$\mathbb{R}^+$	the semi-positive-dimensional Euclidean space
$\mathbb{N}$	the set of natural numbers
$\mathbb{Z}$	the set of integer numbers

$Re\ z$	the real part of a complex variable z
(x,y)	metric space
I_n	n-dimensional identity matrix
$\text{diag}[a_1,...,a_n]$	a diagonal matrix with diagonal elements a_1 to a_n
$O(\cdot)$	order of magnitude notation
$f: S_1 \to S_2$	a function f mapping a set S_1 into a set S_2
$\frac{\partial f}{\partial x}$	the Jacobian matrix
$\dot{y}$	the first derivative of y with respect to time
$\frac{d}{dt}$	the first derivative of y with respect to time
$\lambda_{min}(P)$	the minimum eigenvalue of symmetric matrix P
$P > 0$	a positive definite matrix
$P \geq$	a positive semidefinite matrix P
e	neperian number
s	the Laplace variable
sign	sign function
max	maximum
min	minimum
exp	exponential function
sin	sine
cos	cosine
$\text{dist}(p,M)$	the distance from a point p to a set M
$\lim_{x\to c} f(x)$	limit of $f(x)$ as x approaches c
$\text{sat}_m^M(x)$	is defined as $\begin{cases} M & \text{if} \quad x > M \\ x & \text{if} \quad m \leq x \leq M \\ m & \text{if} \quad x < m. \end{cases}$
$\mathscr{C}o$ is the convex hull of a set	
$\text{round}(x)$	is the nearest integer to x
ζ^+	denotes $\zeta(k+1)$
ζ^-	denotes $\zeta(k)$
$\Delta\zeta \triangleq \zeta^+ - \zeta^-$	the value of ζ in two consecutive sampling time
$\mathscr{L}_2$	is the space of $\{x\}$ with the norm: $\|x\|_2^2 \triangleq \sum_{k=0}^{\infty} x^T x < \infty$
H_∞	H-infinite method
$\square$	designation of the end of definition
$\blacksquare$	designation of the end of proof
$[xx]$	see reference number xx in the bibliography

Acronyms

AC	Alterning current
BVP	Boundary Value Problem
DC	Direct current
DVS	Dynamic Voltage Scaling
ENARC	ENergy Aware Controller
GALS	Globally-Asynchronous and Locally Synchronous Systems
HPF	High Pass Filter
IVP	Initial Value Problem
LDVS	Local Dynamic Voltage Scaling
LMI	Linear Matrix Inequalities
LPF	Low Pass Filter
PC	Personal Computer
PHC	PHase Controller
PI	Proportional-Integral
PLL	Phase-Lock Loop
PMOS	P-channel Metal-Oxide-Semiconductor field-effect transistor
PSS	Power Supply Selector
QoS	Quality of Service
SDP	Semidefinite Program
SMPC	Switched-Mode Power Converter
SoC	System on Chip
SOS	Sum Of Squares
THD	Total Harmonic Distortion
VLSI	Very Large Scaling Integration
VHDL-AMS	Verilog Hardware Description Language-Analog and Mixed-Signal

Chapter 1

Introduction

1.1 Introduction to power converters

Power converters are electronic circuits associated to the conversion, control, and conditioning of electric power. The power range can be from milliwatts, mobile phone, for example, to megawatts, in electric power transmission systems. Reliability of the power converters become a key industrial focus. Electronic devices and control circuit must be highly robust in order to achieve a high useful life. A special accent must be set on the total efficiency of the power electronic circuits. Firstly, because of the economic and environmental value of wasted power and, secondly, because of the cost of energy dissipated that it can generate. Even a small improvement in converter power efficiency translates to improved profitability of the investment in the electronic market [33, 100].

Among all electronic converters, the most common technology is switched-mode power converters (SMPC) [118]. They convert the voltage input to another voltage signal, by storing the input energy temporarily and then releasing that energy to the output at a different voltage. This switched-mode conversion has a particular interest due to the fact that it can switch at high frequency in a very efficient way. Power is controlled (even modified) by controlling the timing that the electronic switches are “on” and “off”.

A much greater emphasis is required on achieving high-power efficiency in low-power level electronic technology, since few low-power circuits can tolerate a power efficiency less than 85%. Converters are used in these circuits in order to change the supply voltage in the blocks of the System on Chips (SoCs) according to performance requirements, for power efficiency reasons. Research have been focused on developing electronic circuits that can be employed as switches. e.g. approximating ideal closed or open switches, as the Vdd-hopping converter [98].

1.1.1 Converters classification

Power converters control the flow of power between two systems by changing the character of electrical energy: from direct current to alternating current, from one voltage level to another voltage, or in some other way.

Here, some important way to classify the power converters are described. The aim of this section is not to make a rigorous converter classification, either to make a state of the art, because it is not the purpose of this thesis. It is only desired to understand some properties of these kind of circuits.

The most common classification of power conversion systems is based on the waveform of the input and output signals, in the case whether they are alternating current (AC) or direct current (DC) [33], thus:

- **DC to DC**.
- **DC to AC**. Inverter.
- **AC to DC**. Rectifier.
- **AC to AC**. Transformer.

At the same time, the devices within converters can be switched in different ways [72, 79, 100]. If the devices switch at the line frequency (normally, $50Hz$ or $60HZ$), they can be *line frequency converters* (naturally commutated converters) or *high-frequency switching* (forced-commutated converters).

Depending on the character of the input source, they may be *voltage-source converters* or *current-source converters*. Moreover, converters may be of low, medium or high voltage and/or current level. Another sort of classification may be performed according to the size of the output signal obtained from the input signal; if the converter accomplishes a lower output signal it is well known as *step-down*, and if it obtains a larger signal, it is known as *step-up* [2].

1.1.2 DC-DC converters

DC-DC converters are electronic circuits that change the DC operating voltage or current. They have recently aroused the interest in the current market due to its wide range of applicability. Normally, they are designed in order to transfer power from the input to the output

in one direction. However, in the case of switches topologies, the power moving may be also bidirectional, being very useful to develop new converter topologies for other applications, as can be an inverter topology [25].

They have a particular interest in low-power circuits, as cellular phone and personal computers (PCs). This sort of technology are composed of many sub-circuits that require an own voltage level from an external supply (higher, lower or even negative) or battery. DC-DC converters have a special role in these kind of systems, since they can be employed to change the voltage from a partial lowered battery voltage thereby. This is based on the Dynamic Voltage Scaling technic (DVS) [27, 89, 136]. The main idea of DVS is to vary the supply voltage in order to consume a minimal amount of energy. This fact improves the power efficiency and saves space in spite of using multiple batteries to accomplish the same voltage level [82].

1.1.3 DC-AC converter

DC-AC converters, or commonly named inverters, can obtain a certain amplitude and frequency of the AC voltage and/or current without using normally an intermediate DC stage. This electrical device is a power electronic oscillator [118]. An electronic oscillator is just an electric circuit that produces a repetitive signal, as a sine-wave output signal. Generally, they are SMPCs.

These kind of circuits require an efficient control for the switches devices that, in many occasions, can be quite complex due to system structure. Therefore, to design a suitable control law currently is a subject of much research [22, 107].

1.1.4 AC-DC converter

The process that converts AC to DC is known as rectification, hence, these converters are also called rectifier. Among others applications, they are used in power supplies and detector of radio signals.

The rectification can be half-wave or full-wave. In the first case (half-wave rectification), only one half of the input waveform can be employed to reach the desired output. Therefore, only this half AC wave (positive or negative) is converted. The efficiency will depend of the kind of application. It is clear, that it is not useful for power transfer. The full-wave rectification can convert the whole of the input waveform to achieve the constant output signal. It becomes more efficient [59, 137].

1.1.5 AC-AC converter

AC-AC converters are employed to transform an AC input signal to another AC output signal with an arbitrary amplitude. Likewise, depending on the converter complexity, the frequency can be changed as well. The efficiency of these kind of systems depends on the type of circuit employed. It is clear that a higher power density and reliability will be obtained with a conversion in one single stage [139].

1.2 Research motivation

A lot of research has recently been focused on converters due to the increasing deal of interest in power electronics. This is mainly caused by their broad applicability domain that includes battery-operating portable equipment, computers, appliances, vehicles, industrial electronic equipment, uninterruptible power supplies, telecommunication systems and much more. This current research is specially focused on finding highly-efficient converter topologies for every system application and, on designing control mechanisms that accomplishes the converter objectives. On this way, one or more electrical parameters can be regulated with a high reliability and efficiency, e.g., the supply voltage of an appliance, the temperature of an oven, the speed of a motor, the supply voltage within calcul node of a SoCs [41, 141].

Tackling the control problem in detail for every converter is out of the scope of a thesis. That is why, among all variety of converters, this thesis is focused on providing a control solution for two converters topologies, which have some interesting properties and applications. The converters that will be dealt with are: firstly, a switch inverter topology; and secondly, a DC-DC converter for low power application.

1.2.1 Boost inverter

As was said before, inverters are devices that obtain a current output signal capables from passing through zero. The inverters are generally SMPCs, and their topologies are derived from coupling one or more basic switch topologies. Among them, it can be found the boost-buck inverter [95], the buck-boost inverter [90], the buck inverter [127], the boost inverter [25].

The first part of this thesis is focused on a boost inverter. Its interest is due to its step-up property, which is achieved through a signal stage. In this case, two DC-DC boost converters are connected with a load between them, thus it has a bidirectional current [25].

In this system, four switches have to be controlled by two control signals, in order to control the two output voltages of each DC-DC boost converter. Not only the voltage amplitude must be controlled, but the phase of both signal must also be controlled to achieve the specified output voltage.

Several control laws have been designed for this converter from other authors [25, 126, 149], applying different control strategies. In this thesis, a novel control strategy based on energy shaping for generation of oscillations is employed [16,58], being the control objective a limit cycle. The novelty of this method is that it does not need to track any reference signal to achieve an oscillatory character in the output signal.

1.2.2 DC-DC Vdd-Hopping converter

The second part of the thesis is focused on a DC-DC converter employed in low-power applications. As mentioned, the demand for high efficiency DC-DC converters is increasing dramatically, especially in battery-operated devices such as cellular phones and personal computers.

In SoCs, to extend battery life has a particular role. By employing DC-DC converters based on power-saving, power efficiency in SoCs can be significantly increased, thereby extending battery life. The goal of these efficiency DC-DC converters is to adapt dynamically the supply voltage of the chip according to the required performance level. This is the DVS idea mentioned before. Numerous DC-DC converters employed for this aim have been proposed over the years to increase the power efficiency of an SoCs. The most commonly used topologies in DC-DC converters in low-power electronics are: continuous buck converters [119, 143, 153], boost converters [36], buck-boost [125, 142] converters and charge pump [125], among others. However, while converters may decrease conduction losses, additional losses can be added if switched devices are employed. In low-power applications where a high-efficiency is required, other different topologies far from switched-mode are employed.

In [98], a discrete DC-DC converter was proposed based on the 'Vdd-Hopping' technique. This method is expired in scaling the voltage supply V_{dd} in a discrete way, delivering two small voltage levels according to the optimum V_{dd} required for every performance [75, 106, 128]. Hence its name of 'DC-DC Vdd-Hopping converter'. Therefore, this technique replaces the continuous adjustable voltage, just to two set-points [83], so that it reaches a high-efficiency and reduced size. Likewise, it is a very simple system, becoming easily controllable [55].

This converter is employed in a French gouvernement project, with a very ambitious objective: 'to reduce the size of the SoCs to 32*nm*'. For this, a new technology must be

Converter	Power level	Conversion	Scales	Model order
Boost Inverter	More suitable for medium and high power	DC-AC	normal	4^{th}
Vdd-Hopping Converter	Low power	DC-DC	micro- or nano-scales	1^{st}

Table 1.1: Main differences between boost inverter and Vdd-Hopping converter

developed, since the currently technology applied to $45nm$ can not be employed for physical reasons. Here, the control may take a particular role since, a suitable control law can achieve the equilibrium and the demanded requirements, as well. For instance, it has to achieve the highest efficiency (among other goals) to achieve the global project objective.

1.3 Main objectives

The two selected converters have different natures and applications, and hence, they may have different control objectives. They covers a wide range of the power converter domain. The boost inverter normally is applied to medium and high power level for normal scales; and DC-DC Vdd-hopping converter is used in low-power technology for micro-scales or nano-scales. Likewise, conversions are DC-to-DC, and DC-to-AC. The DC-AC converter is based on the switched-mode classical topology, as is the boost inverter; and the DC-DC converter has a topology far from the common structures. The complexity of the systems are quite different, from a 1^{st}-order model in the DC-DC converter to a 4^{th}-order. Table 1.1 summarizes these differences.

That does not mean that these two applications completely cover all power converter domain. In fact, there are other features that have not been taken into account, as is the different natural- or forced-commuted characteristic, the input sources, the level of the output signal, among others.

These two converter applications, as for its work context as for its different characteristics, have some different control objectives.

1.3.1 Controlling a boost inverter

The first application is focused on controlling an SMPC boost inverter. This converter is particularly interesting because it does not only allow to generate an alternating current, but it can also obtain an output voltage larger than the input signal. It has a high efficiency due to its switching character. Nevertheless, it has a non-minimum phase, 4^{th}-order model. In addition, the desired behavior is not an equilibrium point but a limit cycle.

Due to all the mentioned boost inverter characteristics, the main objective is to design a control law that guarantees not only the convergence to the desired limit cycle, but also the stability of it, with the particularity that no external reference is applied to the system. Likewise, the system has to accomplish right performance not only for known loads, but also for unknown loads. Another important aim is to estimate a set of initial voltage and current values, for which the system variables tend to the desired limit cycles when the control law before is applied to the boost inverter.

If all these objectives are achieved, a control system guarantees a stable and robust behavior from an initial condition, which is within an estimated attraction region. And, in addition, the system is autonomous in the sense that no reference signals are needed.

1.3.2 Controlling a DC-DC Vdd-hopping converters

The second application deals with the control of a discrete DC-DC Vdd-Hooping converter. This is a low-power converter with a high-efficiency. Furthermore, it has nice properties, for instance, it has a 1^{st}-order and its control objective is an equilibrium. Nevertheless, in low-power technology, this level of efficiency may not become enough if certain requirements are demanded (e.g. high energy-efficiency, small current peaks and reduced space) to achieve a certain objective. For this, to design a control law focused on achieving an optimal energy-efficiency may be an attractive control problem in order to reach this objective. Indeed, the control problem of the Vdd-Hopping converter in this thesis comes directly demanded by the industry. Concretely, it is included in a French national project called ARAVIS, sponsored by the global competitive cluster Minalogic[1].

The main control objective of this converter is to guarantee that the system reaches the desired equilibrium point, achieving certain required features as: high-efficiency, stability, low computational cost, robustness with respect to parameter uncertainties and robustness with respect to delays due to synchronization and computation issues [45]. In this way, the control law must be designed taken these objectives into account.

[1] http://www.minalogic.com/

1.4 Thesis structure

This thesis, as is noted above, is composed of two parts. Part I covers Chapters 2 to 5 while Part II covers Chapter 6 to 10. Conclusions are drawn in Chapter 11.

The first part deals with controlling the boost inverter. In Chapter 2, the model of the double boost converter (boost inverter) is presented. Likewise, the objectives are specified in details, just as a particular solution is proposed in order to resolve the raised problem. Chapter 3 shows the general idea of producing oscillating behavior by means of the generation of a limit cycle through energy shaping. This idea yields a controller for the boost inverter, but it is shown that the behavior is not acceptable due to a lack of synchronization. Therefore, a phase controller is added to achieve the synchronization of an isolated boost inverter as well as the synchronization of the boost inverter with a pre-specified signal. Chapter 4 deals with the unknown-load case, which is solved by means of an adaptation mechanism design. A stability analysis for the full-system is also studied by using singular perturbation analysis. Chapter 5 is devoted to develop a method of estimating an attraction domain. This method deals with control and state constraints. It is employed to provide an estimated attraction domain for the boost inverter.

The second part of the thesis is focused on controlling the DC-DC Vdd-Hopping converter. In Chapter 6, a summary of the ARAVIS project work context, where this research is included, is performed. Likewise, the control objectives required for this DC-DC converter in the ARAVIS project are defined. In Chapter 7, a set of controllers are presented and discussed. From the control solution that offers the best performance, a controller is developed in order to achieve the control objectives. For this, optimal control theory as well as adaptation methods are applied. Nevertheless, it has an important drawback, its implementation is not simple, thus it is not suitable in the ARAVIS project. Next, another controller is developed in Chapter 8. This proposed control solution is developed from the simplest control implementation of the set of controllers presented in Chapter 7. This controller presents good properties for the project. In Chapter 9, a rigorous stability analysis is developed for the closed-loop system with this last controller. Chapter 10 presents an optimal tuning mechanism for the control constants in order to deal with delays and parameter uncertainties. This development copes with resolving a H_∞ problem, proposing some Linear Matrix Inequalities (LMIs) developed from Lyapunov Krasovskii method.

Part I

Controlling a DC-AC Boost Converter

Chapter 2

Introduction

DC-DC power converters have a very large presence in all kind of electronic circuits, from industrial applications (spacecraft power systems, DC motor drives, telecommunication equipment) to personal applications (PCs, office equipment, electrical appliance). These systems provide a regulated DC voltage level (V_o) from an unregulated DC voltage level (V_{in}).

High efficiency is the most important requirement for DC-DC converters in a wide range of load power, since it directly affects the battery lifetime [42]. It can be achieved using 'switched-mode'. A switched-mode power converter (SMPC) is characterized by rapidly switching on and off some devices, transferring a rate of energy from the input to the output. This rate of energy is controlled by a duty cycle[1] to minimize the dissipated energy. The switching effect is achieved by transistors, which dissipates little power when it is outside of its active region. In addition, SMPCs have an inductor, whose main function is to limit the current slew rate through the power switch. This action help to limit the otherwise high peak current. Moreover, the inductor stores the energy, which can be recovered in the discharge phase [43, 118]. This approach is also used in alternating current (AC) applications.

The basic components of the switching circuit can be rearranged to form a:

1. **Buck converter.** It is a step-down: the output voltage is lower than the input voltage.
2. **Boost converter.** It is a step-up: the output voltage is larger than the input voltage.
3. **Buck-boost converter.** It can be a step-down or a step-up. Its main characteristic is that it inverts the polarity of the voltage.
4. **Cuk converter.** It has the same features that a buck-boost converter, with other different configuration.

[1] Duty cycle is the fraction of time that a system is operated.

5. **SEPIC converter.** It can be a step-down or a step-up, but it does not invert the voltage polarity.

From these topologies other converters can be obtained [96, 100].

A buck or boost topology, by oneself, can not achieve alternating current. Physical reasons prevent the output current signal from passing through zero. Hence, some topologies have been proposed in order to obtain the alternating current condition.

Traditionally, DC-AC converters (or inverters) are based on the buck topology. Nevertheless, this kind of configurations obtain an AC output voltage lower in amplitude than the input voltage [90]. In applications that require a boosting output, this problem is solved by using two-stages. One-stage to change the signal from DC to AC, and the other stage, to raise the amplitude [121]. These topologies have the drawback of needing more space and dissipating more energy since they use more components.

In [25], a new inverter was proposed composed of two boost converter. It is known as boost inverter. This inverter has as main advantage that it generates an AC output voltage from a lower DC voltage in a single stage. As side effect, it has a higher efficiency and a better signal quality with respect to the traditional buck inverters [126, 147]. These nice properties are only achieved with a suitable controller. Hence, to design an appropriate control law has an important relevance for these kind of circuits.

The boost inverter may be used in diverse applications, as for example in photovoltaic system market. The solar cells can charge a battery up with a DC voltage of $48V$. When they are used in domestic installations, a standard domestic AC power is required as power supply [15, 29]. Therefore, a boost inverter provides in these kind of applications a better benefit. Its structure allows to isolate as well as to increase the voltage. Moreover, it ensures that the power conversion is done with reduced energy losses [3, 4]. Figure 2.1 represents a domestic photovoltaic installation.

2.1 Boost inverter

A boost circuit is usually employed as a DC-DC converter, being especially interesting because it generates an output voltage larger than its input voltage, i.e., it is a voltage elevator. In [46, 48], there is a proposition of using this boost circuit as a way to convert DC voltage into an oscillating voltage. However, alternating current cannot be generated with this converter, since the output current cannot change its sign. For this, an inverter is yielded by duplicating the boost circuit [25].

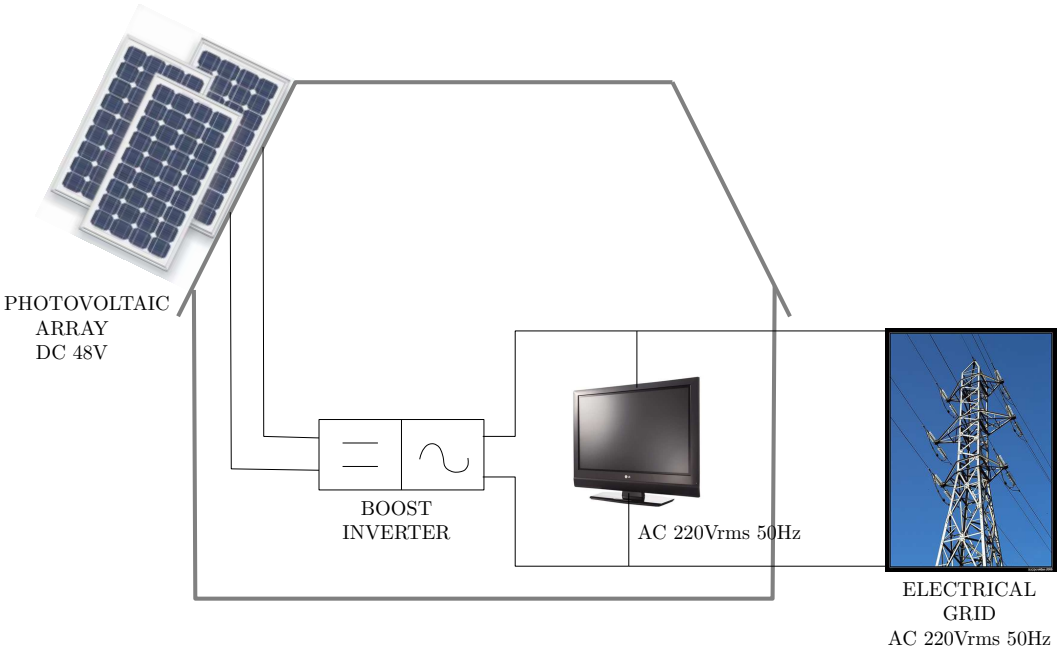


Figure 2.1: Domestic photovoltaic installation.

The boost inverter is made up of two DC-DC converters[2] and a load connected differentially across them, having a bidirectional current (see Fig. 2.2). Each converter produces a DC-biased sine wave output, v_1 and v_2, so that each source generates a unipolar voltage. Voltages v_1 and v_2 should present a phase shift equal to 180°, to maximize the voltage excursion across the load. In this way, to generate an oscillatory signal without bias is possible. The circuit implementation is shown in Fig. 2.3.

In order to simplify the analysis, a part of the boost inverter is replaced by a constant voltage source as is shown in Fig. 2.4. Once the desired results are obtained, they are extrapolated to the full inverter. Note that, this replacement shows more clearly the bidirectional current of each boost DC-DC converter.

2.1.1 System description

Now, some assumptions about the boost inverter are presented.

Assume that:

[2]Throughout this part of the thesis, each part of the boost inverter will be referred as 'boost DC-DC converter' since each part is a normal boost converter that is commonly used as a DC-DC converter. Nevertheless, it should be taken into account that, in the boost inverter, each part does not act as a DC-DC converter.

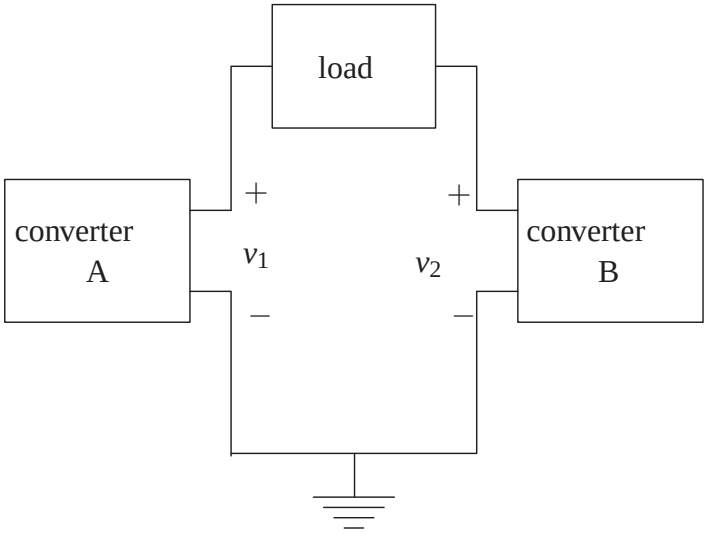


Figure 2.2: Basic representation of the boost inverter.

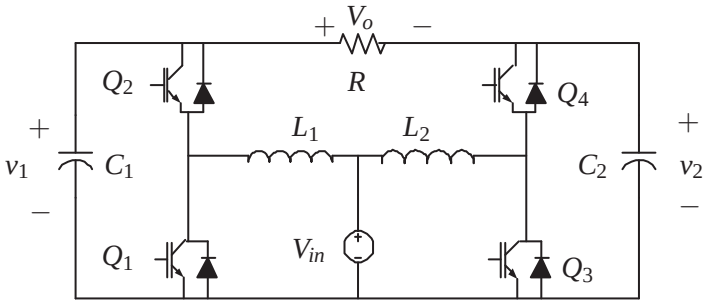


Figure 2.3: Boost inverter model.

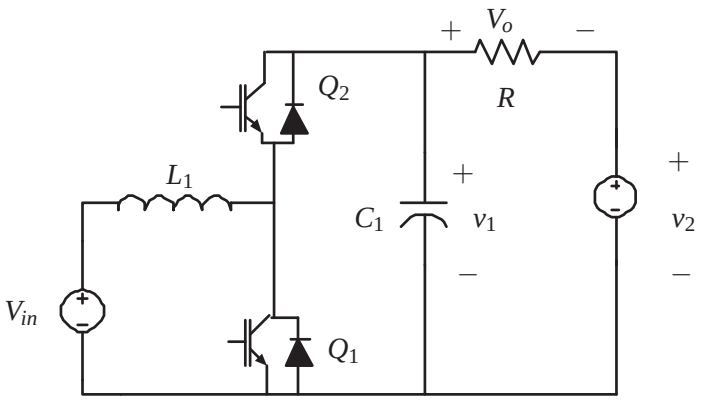


Figure 2.4: Boost inverter model with replacement of a voltage source.

- all the components are ideal and the currents of the converter are continuous,
- the power supply is constant and known,
- the converter operates at a high-switching frequency,
- the inductances $L_1 = L_2$, and the capacitances $C_1 = C_2$, are known and symmetric,
- v_1 and v_2 are positive and sinusoidal voltages.

The circuit shown in Fig. 2.4 is driven by the transistor ON/OFF inputs, Q_i. This yields two modes of operation illustrated in Fig. 2.5. Formally, this circuit generates a switched model. For control purposes, it is common to use an average model described in terms of the mean current and voltage levels [97]. This averaging process may reach an averaged, smooth, nonlinear, continuous-time ordinary differential equation (ODE), as will be seen below.

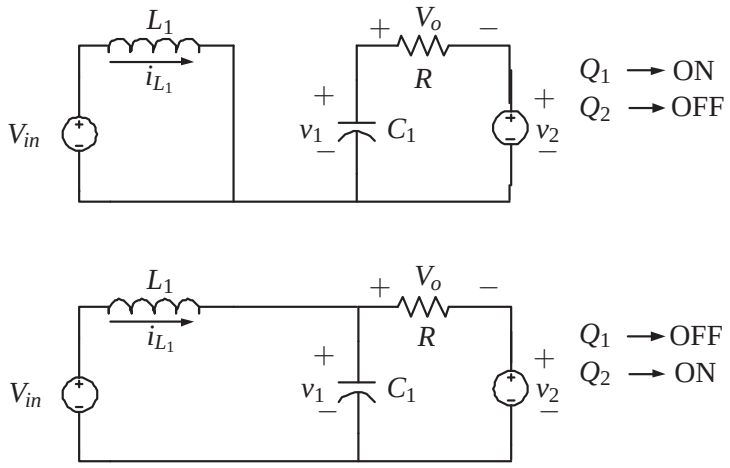


Figure 2.5: Operation modes.

If the control variable, q, is defined as $q = 0$ when $Q_1 = \text{OFF}$ and $Q_2 = \text{ON}$, and $q = 1$, when $Q_1 = \text{ON}$ and $Q_2 = \text{OFF}$, the converter dynamic equations are

$$L_1 \frac{di_{L_1}}{dt} = -v_1 + qv_1 + V_{in} \tag{2.1}$$

$$C_1 \frac{dv_1}{dt} = i_{L_1} - qi_{L_1} - \frac{v_1}{R} + \frac{v_2}{R}. \tag{2.2}$$

Now, $\underline{u}_1 = 1 - q$ is taken as the control action in equations (2.1)–(2.2); obtaining

$$L_1 \frac{di_{L_1}}{dt} = -\underline{u}_1 v_1 + V_{in} \tag{2.3}$$

$$C_1 \frac{dv_1}{dt} = \underline{u}_1 i_{L_1} - \frac{v_1}{R} + \frac{v_2}{R}, \tag{2.4}$$

where $\underline{u}_1$ is the control variable, which can only take two values $\underline{u}_1 \in \{0,1\}$. However, it is usual to consider its average value $u_1(t) = \frac{1}{T}\int_t^{T+t} \underline{u}_1(s)ds$ where T is the switching period [97]. Therefore, u_1 is a continuous variable defined as $u_1 \in [0,1]$.

The full inverter structure according to Fig. 2.3 is

$$L_1 \frac{di_{L_1}}{dt} = -u_1 v_1 + V_{in} \tag{2.5}$$

$$C_1 \frac{dv_1}{dt} = u_1 i_{L_1} - \frac{v_1}{R} + \frac{v_2}{R} \tag{2.6}$$

$$L_2 \frac{di_{L_2}}{dt} = -u_2 v_2 + V_{in} \tag{2.7}$$

$$C_2 \frac{dv_2}{dt} = u_2 i_{L_2} + \frac{v_1}{R} - \frac{v_2}{R}, \tag{2.8}$$

where u_2 controls the other part of the full system (remember that this part has been replaced by a constant voltage source).

The main difficulty of system (2.5)–(2.8) copes with its control, because of:

- system nonlinearities. The control signals multiply the state variables. This kind of system are more difficult to study [76].
- The linear part of system (2.5)–(2.8) is nonminimum phase because it has poles in the positive semiplane. Therefore, it is not stable in open-loop [131].
- It is 4^{th} order, which is a relatively high order.
- The current signal is indirectly controlled. An alternating current signal can be achieved by a suited control-law that controls the voltage output [48].
- A phase shift of 180° is not necessarily achieved. In order to reach a right performance with this inverter, both voltages signals must present this phase shift [25].
- Boost inverter is a double oscillator, thus it does not present two equilibrium points but two limit cycles.
- The control law variables are saturated because of duty-cycle signals [25].
- Loads in this kind of systems are unknown or/and slowly variable [63].

2.2 Control problem objectives

As mentioned before, the main objective for the boost inverter is to generate alternating current. Hence, it can produce an oscillating voltage centered around zero, and thus, it can

achieve negative voltages. Its main drawback, however, is its control due to the complexity of the system structure.

The general control objectives for the boost inverter, which are common in switching electronics converters, are:

1. to generate a stable output voltage with an amplitude equal to the desired voltage. Furthermore, in certain applications, it is required that the output voltage has a pre-specified phase;
2. to ensure the performance for unknown or/and slowly variable loads;
3. in the case that the control law does not guarantee global stability, to study an attraction domain composed of all initial conditions that ensure a convergency to the system right performance. This estimation of the region of attraction is important for the design of the starting phase.

In this thesis, these general objectives can be achieved for a particular solution made up of some proposed specific objectives:

1. to design a suitable control law for the duty cycle by using energy shaping, without introducing reference signals;
2. to achieve an anti-synchronization[3] between the voltage signals of each side of the circuit;
3. to propose an adaptive control to deal with unknown and/or slowly varying loads and,
4. to estimate an attraction domain for the resulting system.

Figure 2.6 shows a block diagram of the solution proposed in this thesis for the boost inverter control problem. Note that the user has to specify the desired amplitude and frequency of the output voltage, as well as that the initial conditions belong to an estimated attraction domain to ensure the system convergency.

2.2.1 Control law

The control of switched-mode inverter is usually accomplished by tracking a reference (sinusoidal) signal [20, 35, 126, 150]. The use of this external signal makes the closed-loop system

[3] In this thesis it is said that two sinusoidal signals of the same frequency are anti-synchronized, or in anti-phase, when the phase shift between them is equal to 180°.

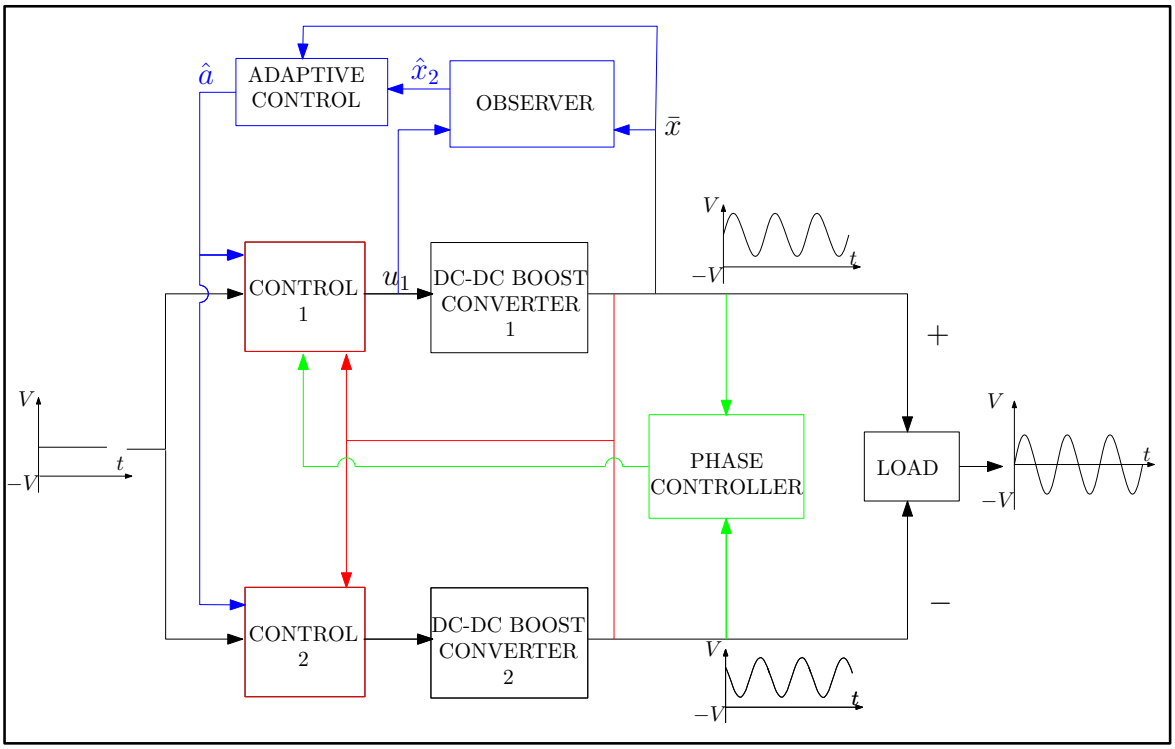


Figure 2.6: General control problem.

non-autonomous in such a way that its analysis is more involved than if it were autonomous. In these kind of systems, the control objective can be seen as the generation of a stable limit cycle defined by a given amplitude and frequency. Figure 2.7 shows the control objective, which corresponds to the valley of a certain surface with a 'Mexican-hat' shape [115]. If a control law is able to produce such a limit cycle, alternating current will be generated without the need to introduce a time-dependent reference signal. The generation of limit cycles to produce self-oscillations has been successfully applied to electro-mechanical systems [56, 57]. Applications to electronic devices are [16, 58], where a three-phase UPS and a boost converter are controlled using this method. The idea behind [19, 73] is similar but there a sliding mode controller is proposed.

In Chapter 3, this approach is applied to a nonlinear boost inverter [11]. Several approaches have been applied to control this topology of inverter. For instance, in [25, 126], sliding mode method is applied and, in [148], the control is based on passivity. Nevertheless, these methods need a reference signal.

Therefore, the main contribution in this part of the thesis is to control the boost inverter without using any reference signal, i.e., the system becomes autonomous [24, 150]. Figure 2.8 shows the autonomous structure that replaces the standard feedback control loop. This is a sub-control problem, since both current and voltage signals are controlled by the same control variable.

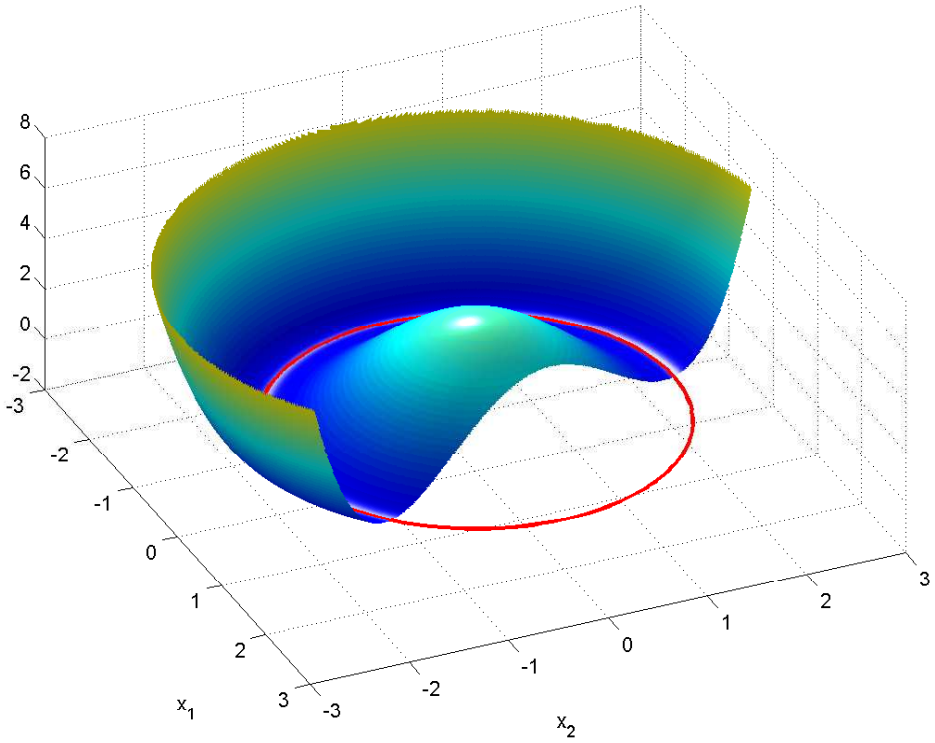


Figure 2.7: Desired energy function: Mexican-hat shape.

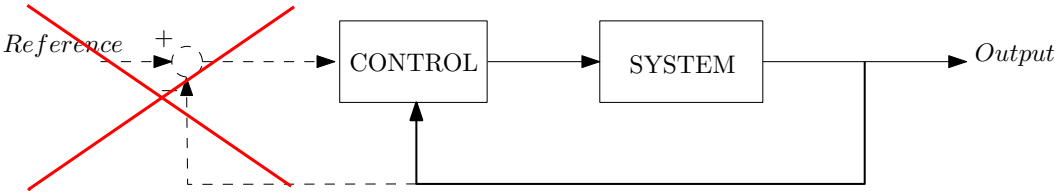


Figure 2.8: Autonomous feedback control loop.

It is shown that the direct application of the approach proposed in [16] and [58] does not fulfill the objective due to the lack of anti-synchronization between both parts of the circuit. In order to achieve anti-synchronization, a phase controller (PHC) in an external loop is added to the previous control law. This approach is also applied to synchronize[4] the output with a given signal. An example of such a configuration is the synchronization of the boost inverter with the electrical grid (as in the photovoltaic case) in order to achieve a satisfactory power factor, which is shown in Fig. 2.6.

The circuit performance is validated in the simulation of a practical case presented in this chapter.

Previous results were extended to the case that the load is not purely resistive but it is inductive, as is usually the case in industrial applications. In [10], the extension to the controller based on energy shaping method considering an inductive load was presented, taking also into account the PHC.

2.2.2 Adaptive control

Previously, a control law satisfying previous requirements was designed in Chapter 3. It has been supposed that the load is known and constant. However, it is well known in industrial applications that the load can be unknown or suffer perturbations. This problem in switched-mode converters is usually dealt with by using adaptation mechanisms along with other techniques such as feedback stabilization [63], input-output feedback linearization [64], backstepping [123, 135], grid-point modeled [102], sliding modes [28, 134, 145], predictive control [94] or fuzzy logic control [40]. In [108], an adaptive control is obtained for a part of the DC-DC boost converter, which is controlled using the oscillation generation approach mentioned before. This adaptive controller is computed using passivity arguments. This approach is not easily applicable to the boost inverter because its model is more involved than the converter of [108].

In Chapter 4, the goal is to design a load-adaptation mechanism for the boost inverter controlled by energy shaping methodology. In order to estimate the load, a state observer is designed for any system variable even when the state variables are measured (Fig. 2.6). This provides a fast, successful adaptation of the load parameter [7]. This approach is applied by simulation to a real industrial case.

The stability of the full system is analyzed by singular perturbation analysis, [76, 78]. For the sake of simplicity, the phase controller is not considered in this analysis. The resulting adaptive control is tested by simulations.

[4] In this thesis it is said that two sinusoidal signals of the same frequency are synchronized when the phase shift between them is equal to 0°.

The extension to case of unknown and non-purely resistive load using the adaptation mechanism before is published in [12]. In this application two parameters of the load are adapted at the same time.

2.2.3 Attraction domain

In Chapter 3, a control law for the boost inverter is designed satisfying its main objectives. Ideally, the designed control law guarantees global stability by means of a Lyapunov function. In practice, however, the control law does not achieve global stability due to two reasons: firstly, the ideal control signal cannot be implemented globally due to control signal saturation; and secondly, the circuit imposes physical constraints on certain state variables: the capacitor voltages, for example, cannot be negative. Consequently, it is necessary to estimate an attraction region for the boost inverter. This attraction region is composed of all initial conditions of the system that guarantee the convergency to the right behavior. There is a starting phase, which is very common in this kind of systems [13, 91, 156], that must bring the state of the system into a point inside this region. The attraction domain estimation problem presents several difficulties. The main drawback is the complexity of the control law, which is a rational function with a high degree polynomial numerator. Moreover, it is necessary to highlight that the desired behavior does not correspond to an equilibrium point but to a limit cycle. Therefore, to obtain an estimated attraction domain for the boost inverter can be quite involved.

There exist many published methods to estimate the region of attraction (see, for example [54, 76] and the references therein). One example of this kind of methods is based on Lyapunov theory, in which closed Lyapunov-function level surfaces are employed to determine approximate sort of 'conservative' estimations for the region of attraction [76] (see Fig. 2.9). These methods often employ polynomial systems [85, 124, 146].

Chapter 5 presents a method of estimating an attraction domain, considering state and control-signal constraints. This approach can be applied to a class of system, whose local system stability was previously guaranteed by a Lyapunov function, as is the problem proposed here. By means of employing this Lyapunov function to estimate a 'conservative' attraction domain, a simple computational approach can be generated, although the model and/or control law have a relative high degree and complexity. In order to apply the method, the closed-loop system must be in a polynomial form, in such a way that the problem is transformed in a sum of squares (SOS) optimization problem [117].

This method is applied to estimate an attraction domain for the boost inverter. It is remarked, that the computed attraction region obtained from this Lyapunov function considers physical system constraints, containing control law saturations. The application of this method is very simple and satisfactory results are obtained.

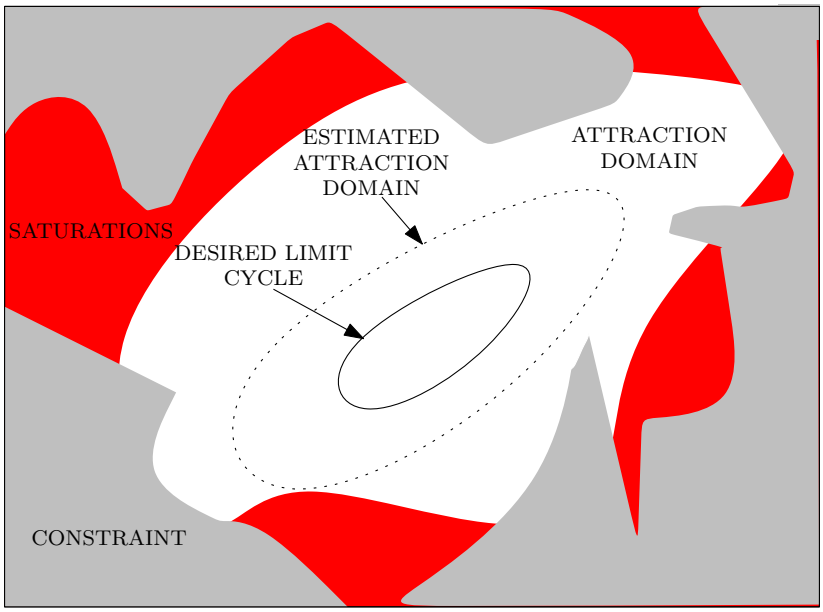


Figure 2.9: System attraction domain with constraints.

Chapter 3

Control of the DC-AC boost converter by energy shaping

This chapter exposes a novel control strategy for nonlinear boost inverter. Boost inverter is nonminimum phase 4^{th} order nonlinear system, which has not an equilibrium point but a limit cycle. The control objective is not only to obtain a right system performance, but also to guaranty the system stability. In addition, it is necessary to mention that it is a sub-control problem. The control law has to control voltage as well as current signal.

The idea behind is based on generating an autonomous stable oscillator. The interesting advantage of this method is that an external reference signal is not needed. This aim is achieved by using energy-shaping methodology with a suitable Hamiltonian function which defines the desired system behavior [44]. This approach guaranties the system stability.

The only missed thing in the developed controller is to synchronize the voltage signals with a phase shift of 180°. This is important in order to obtain the desired response. For this, a phase controller is added to the control law in order to achieve 180°-synchronization between both parts of the circuit, as is shown in Fig. 3.1. In addition, this idea is used to synchronize the voltage output with a pre-specified signal, e.g. synchronization with the electrical grid. The resulting control is tested by means of simulations.

3.1 Normalized average model

Assume system (2.3)–(2.4) is only subject to a resistive load. In order to simplify the control study, a known change of variable is employed [18, 133], in order to achieve a normalize

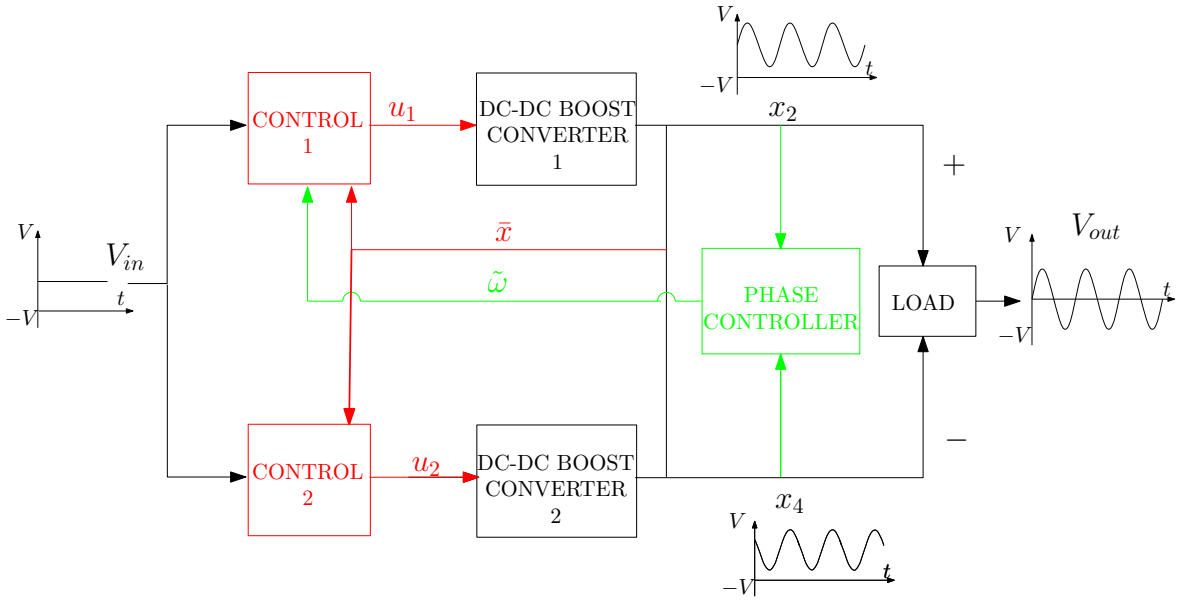


Figure 3.1: Controlled boost inverter with PHC.

model:

$$x_1 = \frac{1}{V_{in}}\sqrt{\frac{L_1}{C_1}}i_{L_1} \tag{3.1}$$

$$x_2 = \frac{v_1}{V_{in}} \tag{3.2}$$

$$x_3 = \frac{1}{V_{in}}\sqrt{\frac{L_1}{C_1}}i_{L_2} \tag{3.3}$$

$$x_4 = \frac{v_2}{V_{in}} \tag{3.4}$$

where x_1 and x_3 are the averaged currents and x_2 and x_4 are the averaged voltages. The normalized time scale is

$$\tilde{t} = \omega_n t \tag{3.5}$$

with

$$\omega_n = \frac{1}{\sqrt{L_1 C_1}}, \tag{3.6}$$

which yields

$$\dot{x}_1 = -u_1 x_2 + 1 \tag{3.7}$$

$$\dot{x}_2 = u_1 x_1 - a x_2 + a x_4, \tag{3.8}$$

$$\dot{x}_3 = -u_2 x_4 + 1 \tag{3.9}$$

$$\dot{x}_4 = u_2 x_3 + a x_2 - a x_4, \tag{3.10}$$

where $a = \frac{1}{R}\sqrt{\frac{L_1}{C_1}}$. Note that ω_n is the natural frequency and a is twice the damping.

Remark 3.1 *$\dot{x}_1$, $\dot{x}_2$, $\dot{x}_3$ and $\dot{x}_4$ are time derivatives of x_1, x_2, x_3 and x_4, respectively, with respect to $\tilde{t}$.*

As mentioned in the chapitre before, for simplicity, the simplified boost inverter (2.3)–(2.4) is dealt with and, later, the results are extrapolated to the full system.

Focussing on the simplified system. If u_1 is eliminated in (3.7)–(3.8), next equation is obtained

$$x_1(1-\dot{x}_1) = x_2(\dot{x}_2 + ax_2 - ax_4). \tag{3.11}$$

This equation is an implicit equation, which relates the state variables (x_2, x_4) and their time derivatives and does not depend on the control signal u. Note that x_4 can be considered an exogenous input in system (3.7)–(3.8). Equation (3.11) can be understood as the internal dynamic of the system. If $\dot{x}_1 = 0$ and $\dot{x}_2 = 0$ is performed, the equilibrium manifold is $x_1 = ax_2(x_2 - x_4)$. In this way, the internal dynamic of system (3.7)–(3.8) given by (3.11) acts as a constraint on the system states.

From Eq. (3.11), it is possible to see that given x_4, and only controlling x_1, variable x_2 can be indirectly controlled[1]. Moreover, the stability of the system is maintained [48].

3.2 Energy shaping control for generation of oscillations

3.2.1 Approach overview

The generation of alternating current in electronic converters can be achieved by generating a stable limit cycle without the need to introduce a reference signal. To do this, an oscillatory target system may be defined and by matching its equations and system equations (3.7)–(3.8) a control law can be obtained. In order to define the target system, consider the following energy-like function

$$H_0(\eta_1, \eta_2) = \frac{1}{4}\Gamma_1^2(\eta_1, \eta_2), \tag{3.12}$$

where η_1 and η_2 are state variables and $\Gamma_1(\eta_1, \eta_2) \triangleq \omega^2(\eta_1 - \eta_{10})^2 + (\eta_2 - \eta_{20})^2 - \mu$. Parameters ω, η_{10}, η_{20} and $\mu > 0$ should be chosen so that the closed curve $\Gamma_1 = 0$ defines the desired behavior. This curve is an ellipse centered at point (η_{10}, η_{20}). A dynamical system can be defined such that this closed curve is its limit set. This can be reached by

[1]For the full system, it is had: $x_1(1-\dot{x}_1) = x_2(\dot{x}_2 + a(x_2 - x_4))$ and $x_3(1-\dot{x}_3) = x_4(\dot{x}_4 + a(x_4 - x_2))$. Thus, controlling x_1 and x_3, the desired behaviors for x_2 and x_4 can be obtained.

adopting H_0 as a Hamiltonian function [16, 108], and defining the Hamiltonian dynamical system

$$\begin{bmatrix} \dot{\eta}_1 \\ \dot{\eta}_2 \end{bmatrix} = \begin{bmatrix} -k_{a_1} & \frac{1}{\Gamma_1} \\ -\frac{1}{\Gamma_1} & -k_{a_2} \end{bmatrix} \begin{bmatrix} \frac{\partial H_0}{\partial \eta_1} \\ \frac{\partial H_0}{\partial \eta_2} \end{bmatrix}, \tag{3.13}$$

which, after using (3.12), results in

$$\dot{\eta}_1 = (\eta_2 - \eta_{20}) - k_{a_1}\omega^2(\eta_1 - \eta_{10})\Gamma_1 \tag{3.14}$$
$$\dot{\eta}_2 = -\omega^2(\eta_1 - \eta_{10}) - k_{a_2}(\eta_2 - \eta_{20})\Gamma_1. \tag{3.15}$$

Taking into account that

$$\dot{H}_0 = -\Gamma_1^2\left(k_{a_1}\omega^4(\eta_1 - \eta_{10})^2 + k_{a_2}(\eta_2 - \eta_{20})^2\right) \leq 0, \tag{3.16}$$

by using the LaSalle invariance principle it can be seen that, for all initial conditions except the center of the ellipse, the trajectories of the system tend to the curve $\Gamma_1 = 0$. Figure 3.2 shows this energy-like function.

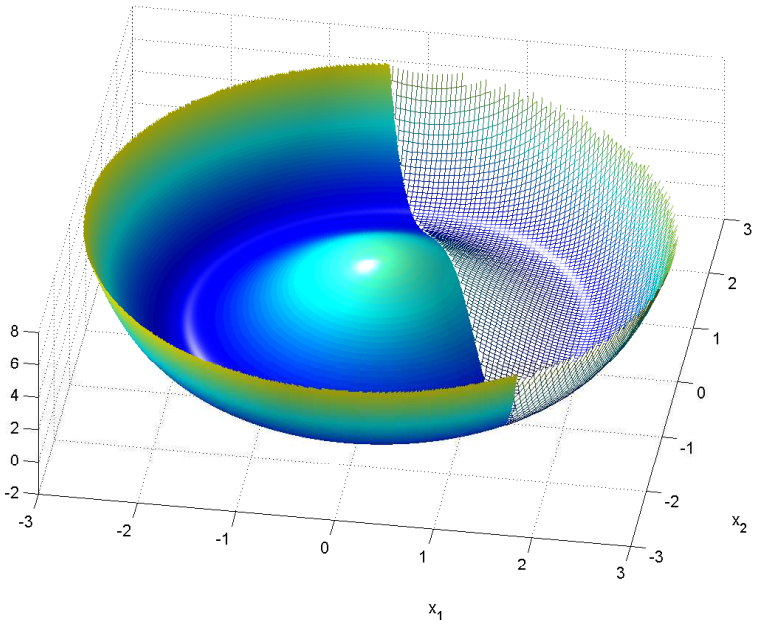


Figure 3.2: Desired energy function: mexican-hat.

The behavior of the target system ($\Gamma_1 = 0$) corresponds to the desired sinusoidal behavior for the DC-AC converter. Constants ω, η_{10}, η_{20} and μ are design parameters for the frequency, bias and amplitude of the desired behavior, while k_{a_1} and k_{a_2} define the speed of the transient response.

Note that $\dot{\eta}_1$ and $\dot{\eta}_2$ are in this case time derivatives of η_1 and η_2 with respect to $\tilde{t}$, in order to work with the normalized averaged model (3.7)–(3.8).

3.2.2 Controller design

System (3.7)–(3.8) can not be directly transformed to the form of system (3.14)–(3.15), but this can be done using the new change of coordinates given below:

$$\zeta_1 = \frac{x_1^2 + x_2^2}{2} \tag{3.17}$$

$$\zeta_2 = x_1 - ax_2^2 + ax_2x_4 + \zeta_{20} \tag{3.18}$$

where ζ_{20} is an offset term that will be a tuning parameter. From (3.17)–(3.18), it is easy to see that

$$\dot{\zeta}_1 = \zeta_2 - \zeta_{20} \tag{3.19}$$

$$\dot{\zeta}_2 = 1 + 2a^2x_2^2 - 3a^2x_4x_2 + a^2x_4^2 + ax_2\dot{x_4} - u_1(x_2 + 2ax_1x_2 - ax_4x_1). \tag{3.20}$$

It is not easy to obtain simple relationships $x_1 = f(\zeta_1, \zeta_2)$ and $x_2 = f(\zeta_3, \zeta_4)$ from (3.17)–(3.18) due to the quadratic terms. Nevertheless, this change of variables is a diffeomorphism if and only if $x_2 + 2ax_1x_2 - ax_4x_1 \neq 0$, as follows from the inverse function theorem. In Chapter 5 it will be seen that this constraint restricts the domain of attraction of the desired limit cycle when the controller obtained below is applied.

Looking at target system structure (3.14)–(3.15) and comparing it with (3.19)–(3.20) the choice $k_{a_1} = 0$ is obvious, resulting in the target system

$$\dot{\zeta}_1 = \zeta_2 - \zeta_{20} \tag{3.21}$$

$$\dot{\zeta}_2 = -\omega^2(\zeta_1 - \zeta_{10}) - k_1\Gamma_1(\zeta_2 - \zeta_{20}), \tag{3.22}$$

where, for sake of simplicity, k_{a_2} has been denoted as k_1. The attraction of curve $\Gamma = 0$ can still be proved by the LaSalle invariance principle.

The control law, u, that matches (3.19)–(3.20) and (3.21)–(3.22) is

$$u_1 = \frac{1 + 2a^2x_2^2 - 3a^2x_4x_2 + a^2x_4^2 + ax_2\dot{x_4} + k_1\Gamma_1(\zeta_2 - \zeta_{20}) + \omega^2(\zeta_1 - \zeta_{10})}{x_2 + 2ax_1x_2 - ax_4x_1}. \tag{3.23}$$

Indeed, u_1 varies dependently on x, as can be noted from Eq. (3.17)– (3.18). This controller has several problems. First, the denominator in (3.23) may be zero (this is the same necessary condition for (3.19)–(3.20) to be a diffeomorphism). Furthermore, in other cases, the resulting u_1 can violate the constraint $0 \leq u_1 \leq 1$. In Chapter 5, an estimation for the region of attraction of the desired limit cycle will be obtained by taking these problems into account. It is assumed that a starting strategy will bring the state of the system into this region of attraction [13, 91, 156].

Parameters η_{10}, η_{20} and μ have to be defined as a function of the desired behavior. For this, it is necessary to obtain an analytical expression of the desired objective curve in plane $x_1 - x_2$. Assume that the desired time evolutions for x_2 and x_4 are

$$x_2^* = A\sin\omega t + B \tag{3.24}$$
$$x_4^* = -A\sin\omega t + B, \tag{3.25}$$

where A, B and ω take pre-specified values to obtain the desired evolution for v_1 and i_{L_1} using (3.1)–(3.4), (3.5) and (3.6). In addition, note that these desired evolutions allow us to remove the bias in the output. The origin of time in (3.24)–(3.25) is arbitrary in such a way that no phase shift value is imposed (signal synchronization will be achieved below). Assume that the desired steady state for x_1 can be approximated by

$$x_1^* = a\alpha_0 + \alpha_1\cos\omega t + \beta_1\sin\omega t \tag{3.26}$$

This assumption is very common in the field of electronics [20, 37, 48, 60].

By substituting (3.24)–(3.25) and (3.26) in (3.11)

$$a\alpha_0 + (\beta_1 + a\alpha_0\alpha_1\omega)\sin\omega t + (\alpha_1 - a\alpha_0\beta_1\omega)\cos\omega t + \frac{1}{2}\omega(\alpha_1^2 - \beta_1^2)\sin 2\omega t$$
$$-\alpha_1\beta_1\omega\cos 2\omega t = aA^2 - 2aAB\sin\omega t - \omega AB\cos\omega t + \frac{1}{2}\omega A^2\sin 2\omega t - aA^2\cos 2\omega t.$$

If the second order harmonics are neglected, the corresponding coefficients can be equated:

$$a\alpha_0 = aA^2$$
$$\beta_1 + a\alpha_0\alpha_1\omega = -2aAB$$
$$\alpha_1 - a\alpha_0\beta_1\omega = -\omega AB.$$

When this system is resolved for α_0, α_1 and β_1,

$$\alpha_0 = A^2 \tag{3.27}$$
$$\alpha_1 = \frac{\omega AB(2a^2A^2+1)}{1+a^2A^4\omega^2} \tag{3.28}$$
$$\beta_1 = -\frac{aAB(\omega^2A^2-2)}{1+a^2A^4\omega^2}. \tag{3.29}$$

The next problem is to show that the desired behavior for ζ_1 and ζ_2 is an ellipse and defining the ellipse parameters (ω, ζ_{10}, ζ_{20} and μ) in terms of the desired behavior for x_2. For this, it is necessary to obtain the desired evolution for ζ_1 and ζ_2 by applying the change of variables (3.17)–(3.18) to (3.24)–(3.25) and (3.26).

$$\zeta_1 = \frac{1}{2}[(a\alpha_0 + \alpha_1\cos\omega t + \beta_1\sin\omega t)^2 + (A\sin\omega t + B)^2] \tag{3.30}$$
$$\zeta_2 = a\alpha_0 + \alpha_1\cos\omega t + \beta_1\sin\omega t - a(A\sin\omega t + B)^2 + a(-A^2\sin^2\omega t + B^2) + \zeta_{20} \tag{3.31}$$

Expanding these expressions in Fourier terms yields

$$\zeta_1 = \zeta_1^{(0)} + \zeta_1^{(11)}\cos\omega t + \zeta_1^{(12)}\sin\omega t + \zeta_1^{(21)}\cos 2\omega t + \zeta_1^{(22)}\sin 2\omega t \tag{3.32}$$

$$\zeta_2 = \zeta_2^{(0)} + \zeta_2^{(11)}\cos\omega t + \zeta_2^{(12)}\sin\omega t + \zeta_2^{(21)}\cos 2\omega t + \zeta_2^{(22)}\sin 2\omega t. \tag{3.33}$$

By equating (3.30)–(3.31) with (3.32)–(3.33) the following Fourier coefficients, are obtained

$$\begin{aligned}
\zeta_1^{(0)} &= \frac{2a^2\alpha_0^2 + \alpha_1^2 + \beta_1^2 + A^2 + 2B^2}{4} \\
\zeta_1^{(11)} &= a\alpha_0\alpha_1 \\
\zeta_1^{(12)} &= a\alpha_0\beta_1 + AB \\
\zeta_1^{(21)} &= \frac{\alpha_1^2 - \beta_1^2 - A^2}{4} \\
\zeta_1^{(22)} &= \frac{\alpha_1\beta_1}{2} \\
\zeta_2^{(0)} &= \zeta_{20} \\
\zeta_2^{(11)} &= \alpha_1 \\
\zeta_2^{(12)} &= \beta_1 - 2aAB \\
\zeta_2^{(21)} &= aA^2 \\
\zeta_2^{(22)} &= 0.
\end{aligned}$$

Assuming that the double frequency terms $\zeta_1^{(21)}$, $\zeta_1^{(22)}$, $\zeta_2^{(21)}$ and $\zeta_2^{(22)}$ can be neglected, these expressions can be approximated by an ellipse in the plane ζ_1, ζ_2 since (3.30)–(3.31) yields

$$\omega\zeta_1^{(11)} = -\zeta_2^{(12)} \tag{3.34}$$

$$\omega\zeta_1^{(12)} = \zeta_2^{(11)}. \tag{3.35}$$

The parameters of this ellipse are given by

$$\zeta_{10} = \zeta_1^{(0)} \tag{3.36}$$

$$\zeta_{20} = \zeta_2^{(0)} \tag{3.37}$$

$$\mu = \omega^2((\zeta_1^{(11)})^2 + (\zeta_1^{(12)})^2). \tag{3.38}$$

3.2.3 Control law for the full system

The boost inverter is composed of two DC-DC converters. Therefore, it has two control signals. For that, the previous control law, which is used for a part of the system, is used in

order to obtain the control law for the other part of the system.

By comparing the normalized full model Eqs. (3.7)–(3.10) and (3.7)–(3.8) there is a similar structure for the pairs of current and voltage of both boost DC-DC converters. Therefore, the two control laws are easily obtained. Control law u_2 is obtained by using symmetry. The control laws are

$$u_1 = \frac{1+a^2(2x_2^2-3x_2x_4+x_4^2+x_2\dot{x}_4)+k_1\Gamma_1(\zeta_2-\zeta_{20})+\omega^2(\zeta_1-\zeta_{10})}{x_2+2ax_1x_2-ax_4x_1} \triangleq \kappa_1(x) \quad (3.39)$$

$$u_2 = \frac{1+a^2(2x_4^2-3x_2x_4+x_2^2+x_4\dot{x}_2)+k_2\Gamma_2(\zeta_4-\zeta_{40})+\omega^2(\zeta_3-\zeta_{30})}{x_4+2ax_3x_4-ax_2x_3} \triangleq \kappa_2(x), \quad (3.40)$$

where

$$\Gamma_1(\zeta_1,\zeta_2) = \omega^2(\zeta_1-\zeta_{10})^2+(\zeta_2-\zeta_{20})^2-\mu \quad (3.41)$$

$$\Gamma_2(\zeta_3,\zeta_4) = \omega^2(\zeta_3-\zeta_{30})^2+(\zeta_4-\zeta_{40})^2-\mu. \quad (3.42)$$

The expressions for the time derivatives $\dot{x}_2$ and $\dot{x}_4$ are taken directly from the normalized equations of the boost inverter.

The stability is proved taking:

$$H = \frac{1}{4}(\Gamma_1^2+\Gamma_2^2),$$

whose differetation is:

$$\dot{H} = -\Gamma_1^2 k(\zeta_2-\zeta_{20})^2-\Gamma_2^2 k(\zeta_4-\zeta_{40})^2 \leq 0.$$

3.2.4 Simulation results

The following simulation shows how the controller is applied in a practical case. It is desired to obtain an output voltage $V_o = 220\frac{2}{\sqrt{2}}\sin(50\cdot 2\pi t)$ from an input voltage $V_{in} = 48V$.

These simulations are performed considering, $R = 100\Omega$, $L = 250\mu H$, $C = 250\mu F$. The desired frequency and voltage amplitude are $f = \frac{1}{T} = 50Hz$ and $220V_{rms}$, respectively.

Note that, $\omega_n = 4\cdot 10^3\frac{rad}{s}$ and $\varpi = 2\pi f = 3.14\cdot 10^2\frac{rad}{s}$, i.e., $\omega_n > 5\varpi$ and $\frac{a}{2} = 0.01 \ll 1$.

Parameter A in Eqs. (3.24)–(3.25) has to be the half of the desired output voltage amplitude, and B is chosen so that x_2 and x_4 are always positive. In order to obtain this voltage, the parameters are $A = 3.33$ and $B = 9.37$ with $\omega = 0.078$ in the normalized variables (x_1, x_2).

Figure 3.3 shows the results of a simulation using a commutation frequency of $50KHz$ and employing a sample time of $0.1T$ s (remind that T is the commutation frequency period). Both DC-DC converters achieve the desired limit cycle.

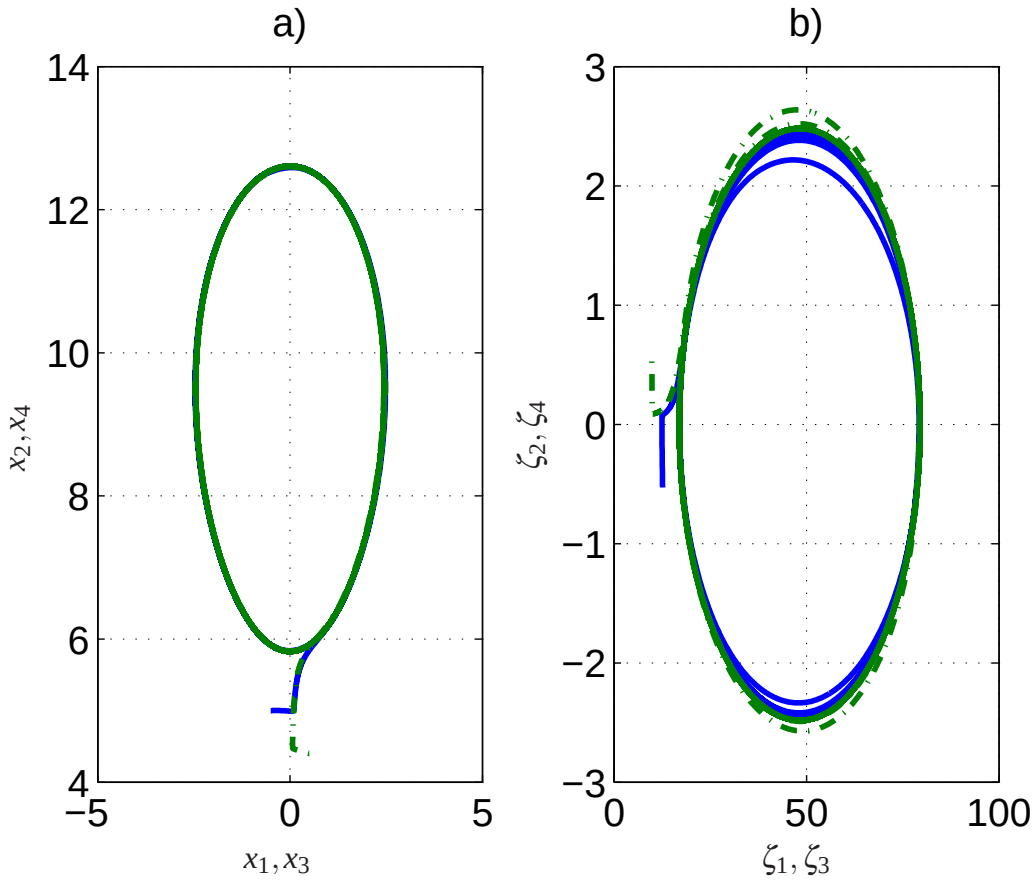


Figure 3.3: a) Evolution of (x_1, x_2) (solid) and (x_3, x_4) (dashed); b) evolution of (ζ_1, ζ_2) (solid) and (ζ_3, ζ_4) (dashed).

Figure 3.4 shows the boost inverter output voltage. Note that the system does not show overshoot, converging to the desired behaviour very fast. It can be seen that the desired amplitude is not achieved. The reason is that the previous design does not force the phase shift between signals v_1 and v_2 to be in anti-phase (180° phase shift). Figure 3.5 shows that, as a result, this goal is not achieved. The next section deals with this problem.

The control signals are shown in Fig. 3.6. For the parameter chosen in the application, the control law signal oscillates between 0.08 and 0.17. As pointed out by the jury member this signal has values smaller than 0.1, what is not good for the implementation. This is a circuit design problem. If the circuit is designed for more suitable values of the duty cycle, the proposed controller would also lead to satisfactory results.

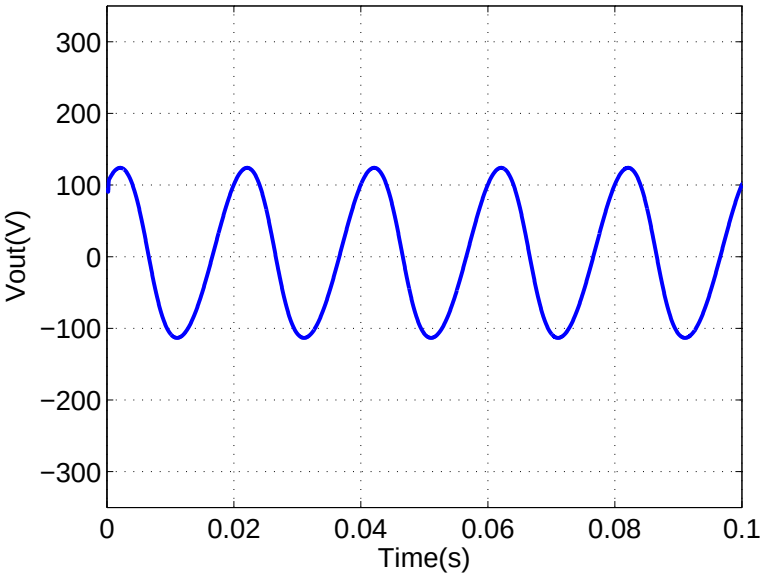


Figure 3.4: Output voltage of the boost inverter.

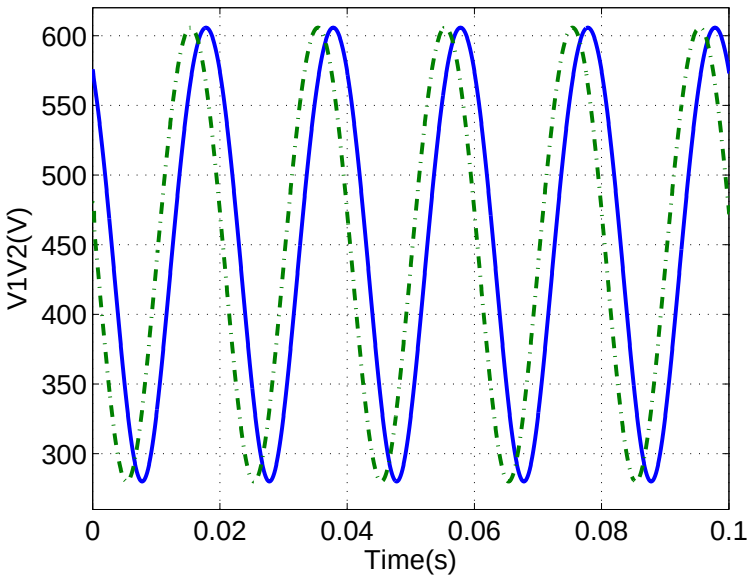


Figure 3.5: Output voltages of the first (solid) and second (dashed) boost DC-DC converters.

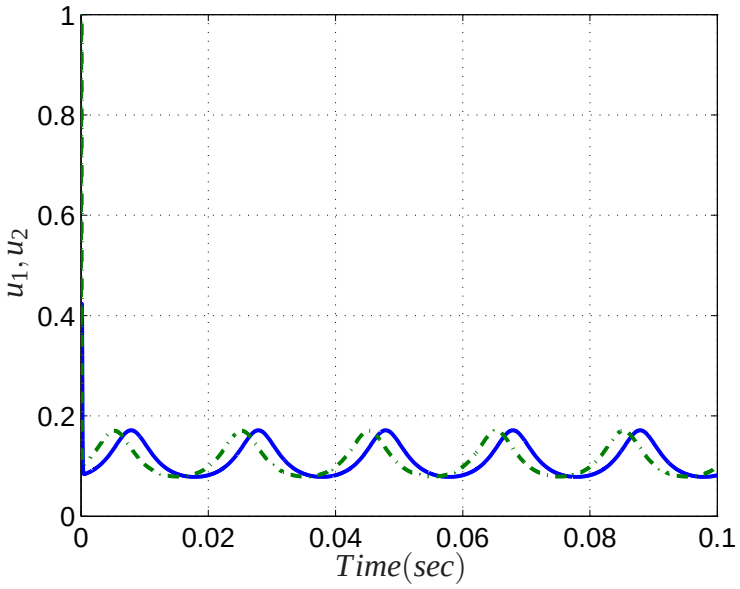


Figure 3.6: Time evolution of the control laws.

3.3 Synchronization problem

The controllers developed above for boost inverters do not synchronize the two parts of the circuit with a phase shift of 180° since each one controls independently a DC-DC converter. Therefore, in the above design, the voltage signal did not present the phase shift mentioned before. In order to get the desired output voltage, it is necessary to synchronize these signals, in such a way that they present a phase shift to 180°. In this section, a phase controller (PHC), inspired by the configuration of a phase-lock loop (PLL) [66]– [1], is added. The PHC allows us to achieve the desired phase shift between the output of the two DC-DC converters as well as to synchronize the boost inverter output with respect to a specified voltage signal, as in the case of synchronization with the electrical grid.

3.3.1 Boost inverter synchronization

The objective is to synchronize voltage signals x_2 and x_4 in anti-phase. The method is illustrated in Fig. 3.7. The normalized voltage of the second DC-DC converter, x_4, is taken as a reference signal and the normalized voltage of the first DC-DC converter, x_2, is the signal to be synchronized with x_4 in anti-phase. These are the inputs to the PHC. The output is a frequency variation, $\tilde{\omega}$, which is added to the nominal frequency, ω, in the Control 1 block and the resultant frequency is entered in (3.39). The output of the converter is a sinusoidal signal of that resulting frequency.

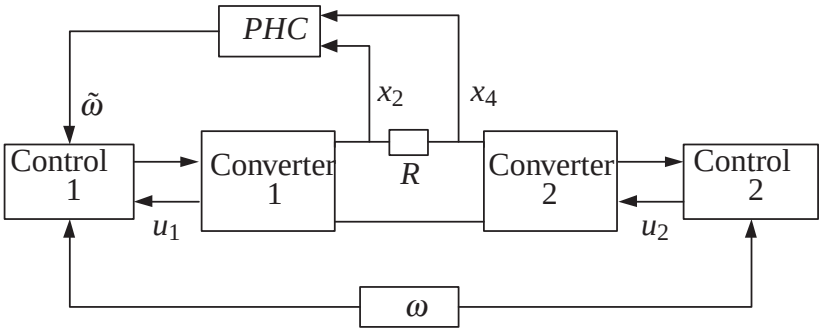


Figure 3.7: Block diagram of boost DC-AC converter with output voltages in anti-phase by the PHC.

The PHC block diagram appears in Fig. 3.8. The multiplier obtains the product, $x_2' \times x_4'$, in such way that its output, once filtered by a low pass filter (LPF), is a measure of the deviation of the phase shift with respect to 90°, [66]. For this reason, one of the inputs of the multiplier, e.g. x_2', is obtained by passing voltage x_2 through a high pass filter (HPF) in order to eliminate its continuous component. Likewise, x_4' is obtained after passing x_4 through another HPF, changing its sign and integrating it.

In the following, an intuitive explanation of the correct behavior of the full system is presented. It is assumed that $\tilde{\omega}(t)$ is small and varies slowly. Under this assumption it can be expected that the introduction of the PHC does not affect the normal behavior of the controllers (3.39) and (3.40) (apart from the phase shift between x_2 and x_4 as desired). In this way, it can be assumed that, after a transient period, x_2 and x_4 evolve as sinusoidal signals:

$$x_2 = A\sin((\omega + \tilde{\omega}(t))t + \varphi_i') + B \approx A\sin(\omega t + \varphi_i(t)) + B \tag{3.43}$$
$$x_4 = A\sin(\omega t + \pi) + B \tag{3.44}$$

where the origin of time has been chosen in such a way that $\varphi_i(t)$ represents the phase shift between x_2 and the desired behavior for x_2. Note, φ_i' is constant. Likewise, it is desired that $\varphi_i = 2n\pi$ with $n \in \mathbb{Z}$.

Assuming that both HPFs eliminate the bias terms, the signals that enter into the multiplier in Fig. 3.8 are

$$x_2' \approx A\sin((\omega t + \varphi_i(t))$$
$$x_4' = A\cos(\omega t + \pi) + C_{PHC}$$

where C_{PHC} is generated by the integrator, being eliminated by the LPF.

Assuming that the LPF filters out every sinusoidal signal of frequency greater or equal than ω, then

$$\tilde{\omega}(t) = \frac{A^2 K_{vd}}{2}\sin(\varphi_i(t) - \pi) = -\frac{A^2 K_{vd}}{2}\sin(\varphi_i(t)).$$

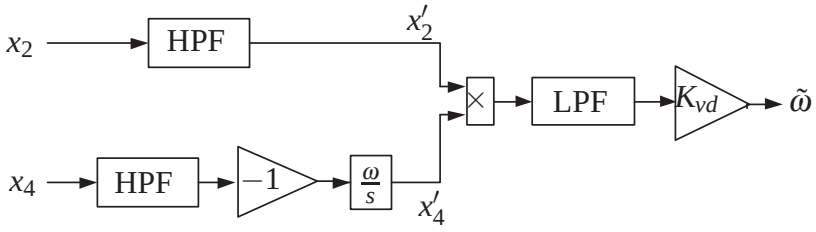


Figure 3.8: Conceptual block diagram of the PHC.

where K_{vd} is a positive design parameter. In this expression, $\sin(\alpha)\cos(\beta) = \frac{1}{2}(\sin(\alpha+\beta)+\sin(\alpha-\beta))$ has been employed. On the other side, from Eq. (3.43), it is easy to obtain $\dot{\varphi}_i \approx \tilde{\omega}$, and thus,

$$\dot{\varphi}_i \approx -\frac{A^2 K_{vd}}{2}\sin(\varphi_i(t)).$$

Obviously $\varphi_i(t)$ converges to $2n\pi$ with $n \in \mathbb{Z}$, which corresponds to the desired behavior.

Simulation results The previous values are used for the boost inverter parameters. The high pass filter applied is:

$$\frac{1.4s}{s+\omega}.$$

The LPF is a second order Butterworth filter [69]:

$$\frac{1}{(s+0.008(\frac{\sqrt{2}}{2}-\frac{\sqrt{2}}{2}j))(s+0.008(\frac{\sqrt{2}}{2}+\frac{\sqrt{2}}{2}j))}. \tag{3.45}$$

The value of the PHC gain is $K_{vd} = 5\cdot 10^{-4}$.

The results of the PHC application are shown in Fig. 3.9. Voltages v_1 and v_2 in anti-phase. In Fig. 3.10 the boost inverter output voltage is represented.

Figure 3.11 shows the ripple in the inductance currents, which is quite acceptable.

The output signal has a total harmonic distortion (THD) below 0.22% for a 50-Hz output voltage. Figure 3.12 shows the signal spectrum of the signals v_2 and v_4. As can be seen, the harmonics of the fundamental frequency wave of the obtained output is quite satisfactory.

This result justifies the first harmonic approximations carried out during the design of the control law. Of course, this is only valid for the chosen parameters and it does not prove the usefulness of the law in a general sense. In fact, the approximation does not work when the circuit parameters are not chosen adequately, but it is thought that, when

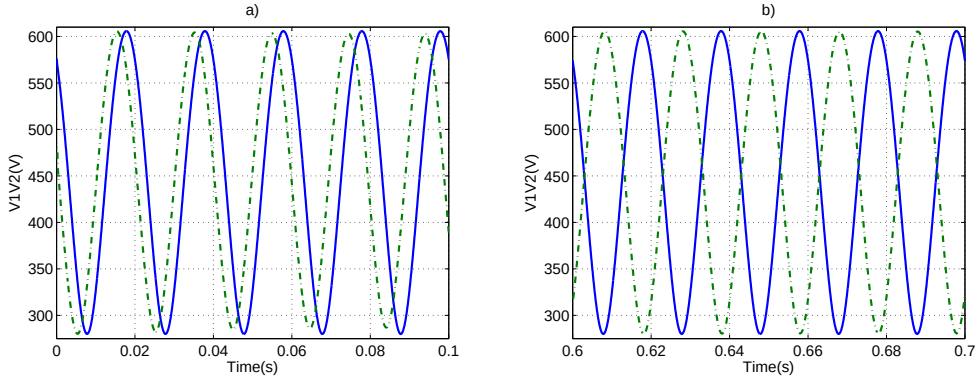


Figure 3.9: Output voltage of the first (solid) and second (dashed) boost DC-DC converters. In a) the transient time is shown and in b) the steady-state is shown.

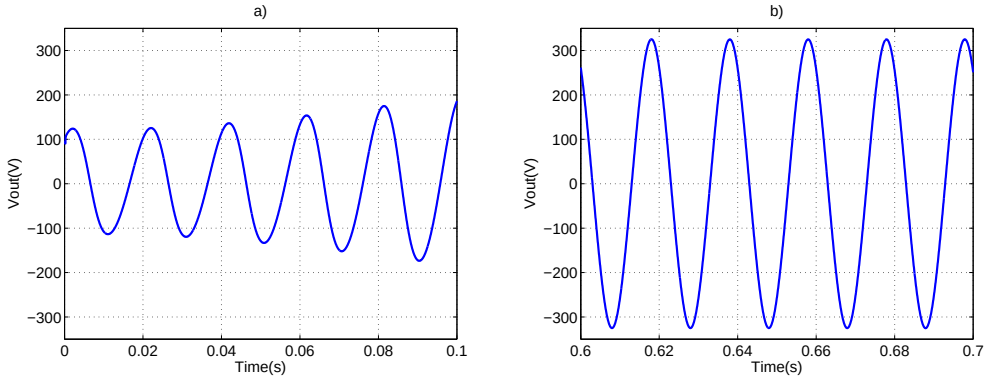


Figure 3.10: Output voltage with PHC. In a) the transient time is shown and in b) the steady-state is shown.

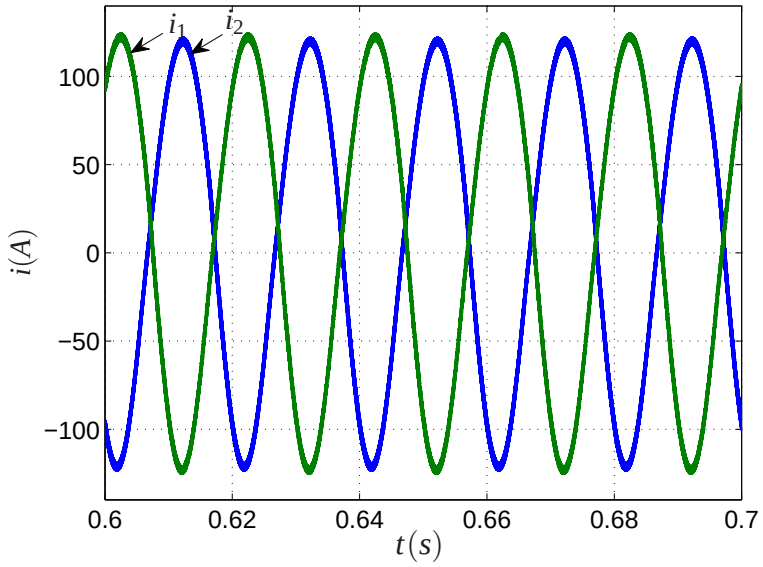


Figure 3.11: Inductance currents.

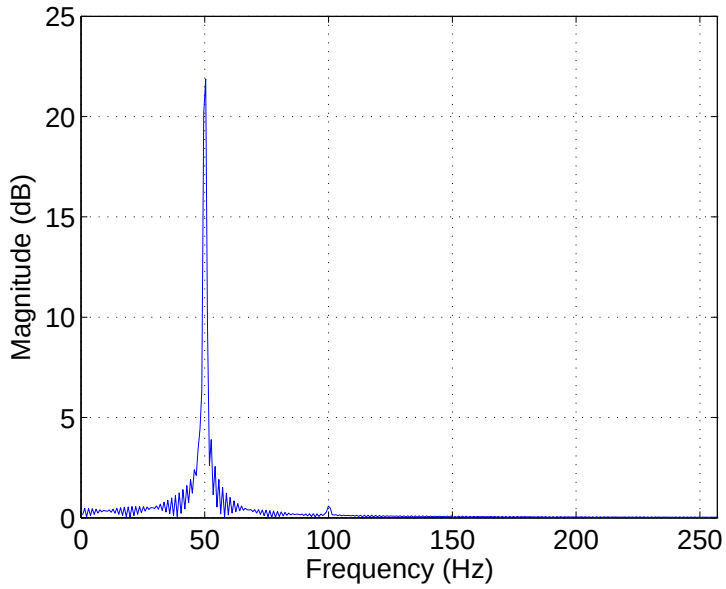


Figure 3.12: Output voltage signal spectrum.

the circuit is designed properly (taking into account the voltage, current and power levels), the approximations will yield good results. Notice once more that these approximations are common in the literature [47, 48].

3.3.2 Synchronization with the electrical grid

In some applications, such as renewable energy plants, an inverter is necessary to inject energy from production plants into the electrical grid. In this case, the problem is to synchronize the voltage output signals with the pre-specified signal. For this, the normalized voltage signals of both DC-DC converters (x_2, x_4) are treated with two PHCs, as is shown in Fig. 3.13. x_2 is synchronized with the grid voltage using a phase shift of 180° by using PHC1, whose structure is shown in Fig. 3.14 and which is similar to the PHC in Fig. 3.8. Signal x_4 is synchronized with the grid voltage using a zero phase shift by means of PHC2 shown in Fig. 3.15. In this case, $g' = \frac{A}{\omega}\sin\left(\omega t - \frac{\pi}{2}\right)$.

For simplicity, the stability analysis of the full system is not delivered, which is similar to the previous subsection.

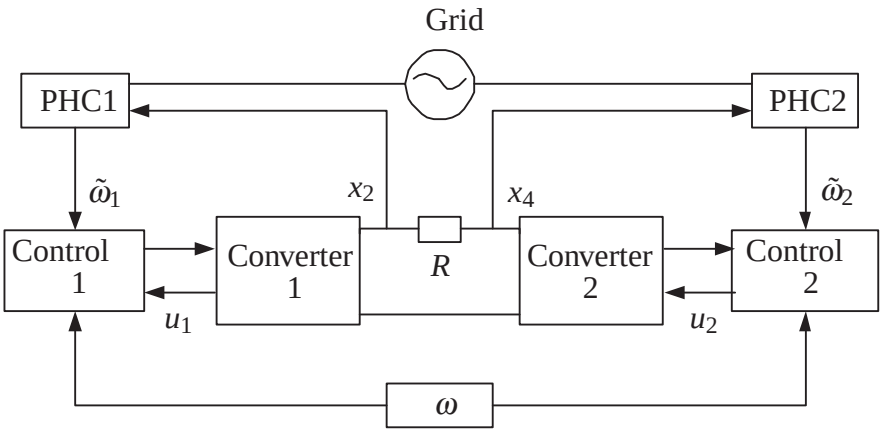


Figure 3.13: Block diagram of boost DC-AC converter with output voltage synchronized with the electrical grid.

Simulation results The grid voltage is

$$V_{grid} = 220\frac{2}{\sqrt{2}}\sin(100\pi t) \tag{3.46}$$

The values used in this simulation for the filter parameters and gain, K_{vd}, are the same ones used previously.

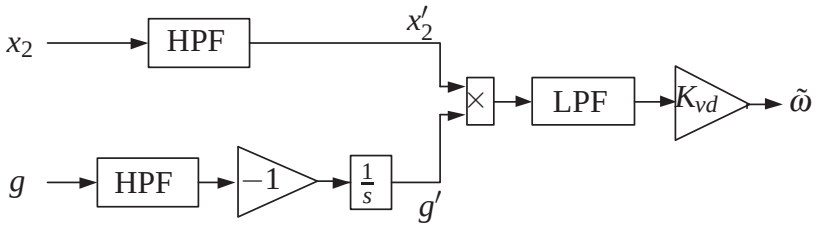


Figure 3.14: Conceptual block diagram of PHC1.

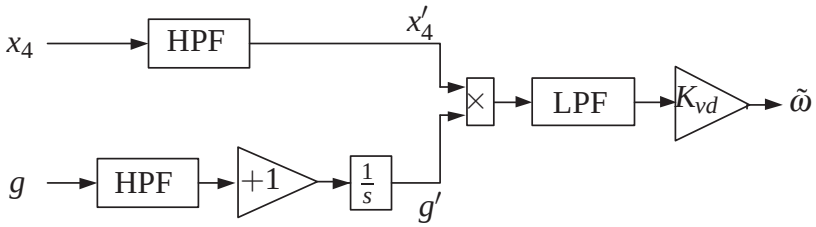


Figure 3.15: Conceptual block diagram of PHC2.

The performance of the synchronization of the boost DC-AC converter with the electrical supply voltage is represented in Fig.3.16 showing satisfactory behavior.

3.4 Conclusion

A control strategy for the complex nonlinear boost inverter was presented. The method is based on energy-shaping methodology, which generates a limit cycle guaranteeing the system stability. The obtained control law is a complex expression. Nevertheless, it has an important relevance: the system does not require any external reference signals. The resulting controller achieves the objective by adding a phase controller. The same idea is used in order to solve the problem of grid electrical synchronization.

The control laws designed in this chapter depends on the value of the resistive load, which is not necessarily known. Next chapter will deal with unknown and/or slowly varying loads, which are supposed to be constant.

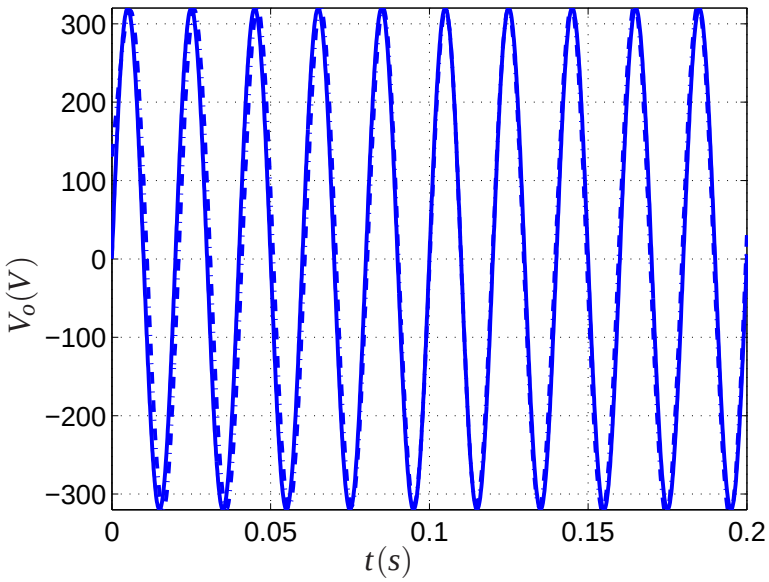


Figure 3.16: Electrical supply voltage (solid) and simulated output voltage synchronized with PHCs (dashed).

Chapter 4

Adaptive control

In the previous chapter, a control law for the nonlinear boost inverter has been designed, which guaranties the system stability. Likewise, a phase controller has been proposed in order to achieve the desired phase in the output voltage signal. This development has been performed assuming known load. Nevertheless, it is usual, that the load is unknown or/and change slowly.

In this chapter an adaptive control is designed for the boost inverter in order to cope with unknown and/or varying resistive load (see Fig. 4.1). This is a common problem in the field of electronics. Different control strategies have been applied to provide a solution to this standard problem in switched-mode converters [28, 63, 64, 94, 135]. Adaptation mechanism for similar controllers, as the one presented in previous chapter, were used in [108] for the case of the boost converter. The fact that the boost converter model is a 4^{th}-order system makes the design of the adaptation law more involved. A state observer for some of the converter variables is designed even when the state variables are measured. In order to analyze the stability of the full system singular perturbation analysis is used [76]. For simplicity, the phase-lock system is not considered in this analysis.

The resultant adaptive control is tested by means of simulations.

4.1 Design of an adaptive control

An adaptive law (or a load observer) is proposed to cope with load variations and/or load uncertainties. This observer is designed based only on a one-sided circuit, which contains enough information to make this parameter observable. Therefore, the study of the full two-sided circuit is avoided due to symmetry considerations.

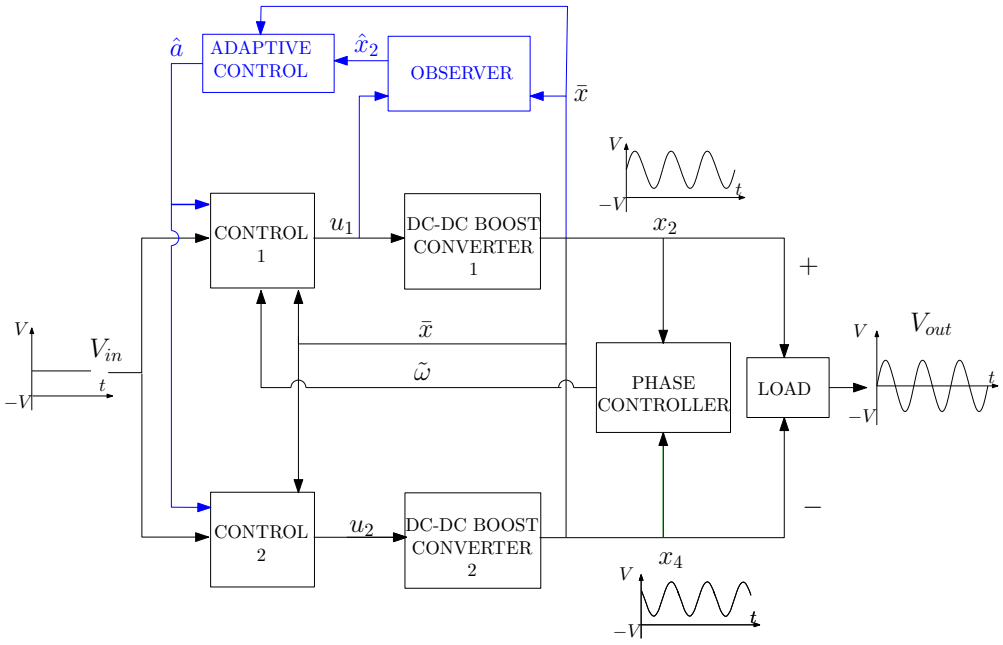


Figure 4.1: Controlled boost inverter with observer.

The model problem for one-sided circuit (left part of the Fig. 2.3) (3.7)-(3.8), can be rewritten compactly as:

$$\dot{x}_l = U_l x_l + aD_l y + E_l \tag{4.1}$$
$$\dot{a} = 0 \tag{4.2}$$
$$y = x_2 - x_4 \tag{4.3}$$
$$y_m = Mx_l \tag{4.4}$$

with $x_l = [x_1, x_2]^T$; x_4 can be considered as an input, and

$$U_l = \begin{bmatrix} 0 & -u_1 \\ u_1 & 0 \end{bmatrix}, D_l = \begin{bmatrix} 0 \\ -1 \end{bmatrix}, E_l = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, M = I_{2\times 2}.$$

Note, that $y \in \mathbb{R}^1$ and $y_m \in \mathbb{R}^2$.

Remark 4.1 *In what follows, it is assumed that both voltage and current, y_m, are measurable, and thus accessible for control use.*

Remark 4.2 *From remark 4.1, note that x_l and y are measurable variables.*

4.1.1 Adaptation law

The proposed adaptation law is comprised of a state observer for one side of the inverter boost, plus an adaptation law for parameter a.

From Eq. (4.4): $K_0(y_m - \hat{y}_m) = K_0(Mx_l - M\hat{x}_l) = K(x_l - \hat{x}_l)$ where $K_0, K \in \mathbb{R}^{2\times 2}$ are constant design matrix.

Therefore, the adaptation law has the following structure:

$$\dot{\hat{x}}_l = U_l x_l + \hat{a} D_l y + E_l + K(x_l - \hat{x}_l) \tag{4.5}$$
$$\dot{\hat{a}} = \beta(x_l, \hat{x}_l), \tag{4.6}$$

where $\beta(x_l, \hat{x}_l)$ is the adaptation law to be designed, $\hat{x}_l$ is the estimated state of x_l and $\hat{a}$ is the estimated value of a. From remark 4.2, the real state of x_l and y in Eq. (4.5) can be used. Note that even if x_l is accessible, the adaptation law designed here requires the additional (or extended) state observer. This will become clear during the analysis of the error equation system, as will be shown below.

4.1.2 Error equation

Assume that a is a constant parameter ($\dot{a} = 0$) or that it changes slowly ($\dot{a} \approx 0$) and define the following error variables:

$$\tilde{x}_l = x_l - \hat{x}_l, \quad \tilde{a} = a - \hat{a}, \quad \dot{\tilde{a}} = -\dot{\hat{a}}.$$

Error equations are now derived from (4.1)–(4.4) together with (4.5)–(4.6)

$$\dot{\tilde{x}}_l = -K\tilde{x}_l + \tilde{a} D_l y \tag{4.7}$$
$$\dot{\tilde{a}} = -\beta(x_l, \hat{x}_l). \tag{4.8}$$

Let K be of the form,

$$K \triangleq \alpha I, \quad \alpha > 0$$

and $P = I$ be the trivial solution of $PK^T + KP = -Q$, with $Q = 2\alpha I$.

Now, introducing

$$V = \tilde{x}_l^T P \tilde{x}_l + \frac{\tilde{a}^2}{\gamma} \tag{4.9}$$

it follows that

$$\begin{aligned}\dot{V} &= -\tilde{x}_l^T Q\tilde{x}_l + 2\tilde{a}\left(\tilde{x}_l^T PD_l y + \frac{\dot{\tilde{a}}}{\gamma}\right)\\ &= -\tilde{x}_l^T Q\tilde{x}_l + 2\tilde{a}\left(\tilde{x}_l^T PD_l y - \frac{\dot{\hat{a}}}{\gamma}\right).\end{aligned}$$

The adaptation law is now designed by canceling the terms in parentheses, i.e.

$$\dot{\hat{a}} = \gamma(D_l^T P\tilde{x}_l)y. \tag{4.10}$$

4.1.3 Stability properties

The observer and the adaptive law error equations are now fully defined. These equations are:

$$\dot{\tilde{x}}_l = -K\tilde{x}_l + \tilde{a}D_l y \tag{4.11}$$
$$\dot{\tilde{a}} = -\gamma(D_l^T P\tilde{x}_l)y. \tag{4.12}$$

The stability properties of these equations follow from the Lyapunov function, V, defined above. Note that with choice (4.10), it follows

$$\dot{V} = -\tilde{x}_l^T Q\tilde{x}_l$$

From standard Lyapunov arguments [76], it is proved that error variables $\tilde{x}_l$ and $\tilde{a}$ are bounded. Moreover, asymptotic stability is established by LaSalle's invariance principle [76]. For this, consider the level set $V_c = V(\tilde{x}_l, \tilde{a}, y) \leq c_0$ for sufficiently large $c_0 > 0$ and where $\dot{V}(\tilde{x}_l, \tilde{a}, y) \leq 0$.

From Eqs. (4.11)–(4.12), note that $\dot{V}(\tilde{x}_l, \tilde{a}, y)$ is negative everywhere, except on the line $\tilde{x}_l = 0$. Note that $\tilde{x}_l \equiv 0$ that implies $\dot{\tilde{x}}_l \equiv 0$, is only obtained if

$$\tilde{a}(t)D_l y(t) \equiv 0. \tag{4.13}$$

In addition, observe that if y behaves as a sinusoidal (as is expected from the control problem formulation) the unique asymptotic solution for $\tilde{a}$ is $\tilde{a} = 0$, as long as $y \not\equiv 0, \forall t \geq 0$.

Consequently, the maximum invariant set in $\dot{V}_c(\tilde{x}_l, \tilde{a}, y) = 0$ corresponds to the single point $(\tilde{x}_l = 0, \tilde{a} = 0)$ Therefore, every solution starting in V_c approaches this point as $t \to \infty$.

The following lemma summarizes the above results, assuming that $y \not\equiv 0$. Note, that the manifold $y(t) \equiv 0$ has to be carefully analyzed since can cause problems (e.g. in Eq. 4.13).

An intuitive explanation about the right system performance (as will be seen by simulation below) is the PHC introduction, see Chapter 3. The PHC objective is to achieve $x_2 + x_4 = 0$, thus avoiding $y(t) = x_2 - x_4 = 0$. A rigorous explanation has not been possible to provide it a cause of the system and control nature.

Lemma 4.3 *Consider the open-loop system (4.1)–(4.4), and the observer (4.5)–(4.6) with $K = \alpha I$ such that K is a solution for $PK^T + KP = -Q$, then the observer states have the following properties:*

i) *The estimated states $\hat{x}_l$, $\hat{a}$ are bounded.*

ii) $\lim_{t\to\infty} \hat{x}_l(t) = x(t)$.

iii) $\lim_{t\to\infty} \hat{a}(t) = a$, *if* $y(t) \not\equiv 0, \forall t \geq 0$.

4.2 Stability considerations of the full closed-loop system

In the previous section, the stability properties have been presented for the extended observer. These properties are independent of the evolution of the system state variables. The stability of the complete system is analyzed in this section.

The open-loop two-sided inverter (3.7)-(3.8) plus (2.7)-(2.8) normalized, can be compactly rewritten as:

$$\dot{x} = U(u_1, u_2)x + aDy + E \tag{4.14}$$

$$y = x_2 - x_4 \tag{4.15}$$

with $x = [x_1, x_2, x_3, x_4]^T$, and

$$U = \begin{bmatrix} 0 & -u_1 & 0 & 0 \\ u_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -u_2 \\ 0 & 0 & u_2 & 0 \end{bmatrix}, D = \begin{bmatrix} 0 \\ -1 \\ 0 \\ 1 \end{bmatrix}, E = \begin{bmatrix} 1 \\ 0 \\ 1 \\ 0 \end{bmatrix}.$$

4.2.1 Tuned system

The *tuned system* is defined as the ideal *closed-loop* system controlled by the *tuned feedback laws* $u_1^* = \kappa_1(x, a^*)$ and $u_2^* = \kappa_2(x, a^*)$, (from Eq. (3.39) and Eq.(3.40), respectively), where a^* is the *exact* value of a.

The tuned system given in (3.24)–(3.25) and (3.26) states

$$\dot{x} = U(u_1^*, u_2^*)x + aDy + E \tag{4.16}$$
$$= U(\kappa_1(x, a^*), \kappa_2(x, a^*))x + aDy + E \tag{4.17}$$
$$\triangleq f(x) \tag{4.18}$$

and, it achieves an asymptotically orbitally stable periodic solution, i.e.

$$x^*(t) = x^*(t+T).$$

In Section 3, it has been shown that functions Γ_1 and Γ_2 defined in (3.41)–(3.42) tend to zero. They correspond to periodic sinusoidal solutions of period $T = 2\pi/\omega$. Consequently, $y^* = x_2^* - x_4^*$ is also sinusoidal.

4.2.2 Closed-loop system

In practice, the control laws that are effectively applied depend on the estimation, $\hat{a}$, of parameter a. This control laws are denoted as $\hat{u}_1 = \kappa_1(x, \hat{a})$ and $\hat{u}_2 = \kappa_2(x, \hat{a})$, respectively. Note that these control laws depend on state x and not on their estimations, $\hat{x}_l$, because state x is directly measured. The role of $\hat{x}_l$ is to make possible the design of the adaptation law for parameter a.

The closed-loop equation resulting from the use of $\hat{u}_1 = \kappa_1(x, \hat{a})$, $\hat{u}_2 = \kappa_2(x, \hat{a})$, $u_1^* = \kappa_1(x, a^*)$ and $u_2^* = \kappa_2(x, a^*)$ is written as

$$\dot{x} = U(\hat{u}_1, \hat{u}_2)x + aDy + E + U(u_1^*, u_2^*)x - U(u_1^*, u_2^*)x \tag{4.19}$$
$$= f(x) + [U(\hat{u}_1, \hat{u}_2) - U(u_1^*, u_2^*)]\,x, \tag{4.20}$$

Let us assume that $\hat{a} \in [\hat{a}_m, \hat{a}^M]$ and denote $\tilde{a} \triangleq a^* - \hat{a}$. Applying mean-value theorem [76] yields

$$U(u_1^*, u_2^*) - U(\hat{u}_1, \hat{u}_2) = \mathscr{T}(x)\tilde{a},$$

being

$$\mathscr{T}(x) \triangleq \begin{bmatrix} \mathbb{I}\frac{\partial u_1}{\partial a}\Big|_{a=\tilde{a}} & 0 \\ 0 & \mathbb{I}\frac{\partial u_2}{\partial a}\Big|_{a=\tilde{a}} \end{bmatrix},$$

where, $\tilde{a}$ takes any value belonging to the interval $\mathscr{A} \triangleq [\min\{a^*, \hat{a}_m\}, \max\{a^*, \hat{a}^M\}]$, and

$$\mathbb{I} \triangleq \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}.$$

The term $\mathscr{T}(x)\tilde{a}$ captures the mismatch between the estimated and the true value of the load. In view of the discussion above, this term has the following property:

Property 4.4 *For small enough constants $\varepsilon_x > 0$ and $\varepsilon_a > 0$. Let $\mathbb{M} = \{(x,\tilde{a}) : dist(x,x^*) \leq \varepsilon_x, |\tilde{a}| \leq \varepsilon_a\}$ be a compact domain that includes the asymptotic periodic solutions from the tuned system and the exact value of a i.e. a^*. Then, $\mathscr{T}(x)\tilde{a}$ has $\forall(x,\tilde{a}) \in \mathbb{M}$, the following properties:*

i) *it is continuous, analytic, and free of singularities*

ii) $\lim_{\tilde{a}\to 0} \mathscr{T}(x)\tilde{a} = 0$.

Putting (4.20) together with the observer error system yields the complete set of closed-loop equations, with $y = y(x)$

$$\dot{x} = f(x) - \mathscr{T}(x)\tilde{a}x \tag{4.21}$$
$$\dot{\tilde{x}}_l = -\alpha\tilde{x}_l + \tilde{a}D_l y \tag{4.22}$$
$$\dot{\tilde{a}} = -\gamma(D_l^T P\tilde{x}_l)y, \tag{4.23}$$

remain that $K = \alpha I$. The stability consideration discussed here will be based on the time-scale separation. The main idea is that with the suitable choice of gains (as discussed below), observer equation (4.22)-(4.23) can be seen as the fast subsystem and equation (4.21) as the slow subsystem. Note again that this time-scale separation should be enforced by a particular choice of the observer and adaption constants α and γ, respectively.

4.2.3 Singular perturbation form

In order to rewrite the system above in the standard singular perturbation form, it is necessary to follow the next steps:

- introduce $\bar{a} = \frac{\tilde{a}}{\alpha}$,
- select $\gamma = \alpha$
- define $\varepsilon = \frac{1}{\alpha}$

With these considerations, Eqs. (4.21)–(4.23) are rewritten:

$$\begin{aligned}\dot{x} &= f(x) - \mathscr{T}(x)\alpha\overline{a}(\tilde{a})x \\ \varepsilon\dot{\tilde{x}}_l &= -\tilde{x}_l + \overline{a}(\tilde{a})D_l y, \\ \varepsilon\dot{\tilde{a}} &= -(D_l^T P\tilde{x}_l)y,\end{aligned}$$

where $\varepsilon > 0$ is small parameter (for a larger value of α). Note that, this particular selection of gains imposes relative gains for the adaptation, γ, and defines precisely, how the observer gain is related to γ.

Remark 4.5 *The perturbed variable parameter, $\varepsilon = \varsigma(\tilde{a})$, and for a side effect, the adaptation gain, γ, must fulfill*

$$\varepsilon \ll \min\left\{\frac{1}{\omega^2}, \frac{1}{k}\right\}$$

$$\gamma \gg \max\left\{\omega^4, k^2\right\}.$$

These relationships with respect to the tuning parameter, k, and desired frequency, ω, ensures the convergency of the observer and adaptation parameter, a.

Letting $z = [\tilde{x}_l, \overline{a}(\tilde{a})]^T$ yields the general form

$$\dot{x} = f(x) - \mathscr{T}(x)\alpha\overline{a}(\tilde{a})x \tag{4.24}$$

$$\varepsilon\dot{z} = g(x,z) \tag{4.25}$$

with $x(t_0) = x^0, x \in \mathbb{R}^4$, $z(t_0) = z^0, z \in \mathbb{R}^3$, and

$$g(z,x) = \begin{bmatrix} -\tilde{x}_l + \overline{a}(\tilde{a})D_l y \\ -(D_l^T P\tilde{x}_l)y \end{bmatrix}$$

According to the singular perturbation analysis, the next steps must be followed:

1. Find a stationary solution of the *fast* subsystem (4.25) by finding the roots of the equation $g(x,z) = 0$, i.e. $z = \phi(x)$.

2. Replace this solution in the *slow* subsystem (4.24), and find the resulting slow system

$$\dot{x} = f(x) - \mathscr{T}(x)\phi(x)x.$$

3. Check the boundary layer properties of the fast subsystem along one particular solution of

$$\dot{x} = f(x) - \mathscr{T}(x)\phi(x)x.$$

4.2.4 Slow sub-system

The previous step 1 requires to find the roots of

$$\begin{aligned}\tilde{x}_l &= \bar{a}(\tilde{a})D_l y\\ 0 &= -\bar{a}(\tilde{a})D_l^T P D_l y^2.\end{aligned}$$

Note that $D_l^T P D_l = 2$, and that the above equation has multiple solutions, i.e

$$\begin{aligned}\tilde{x}_l &= 0\\ \bar{a}(\tilde{a})y^2(x) &= 0\end{aligned}$$

which means that if $y \equiv 0$, there is one solution for $\tilde{x}_l = 0$, and infinite solutions for $\bar{a}$. However, if $y \not\equiv 0$, for instance, in the particular *tuned* solution $y^* = A\cos(\omega t)$, then

$$z = \phi(x) = \begin{bmatrix}\tilde{x}_l\\ \bar{a}(\tilde{a})\end{bmatrix} = 0$$

becomes an isolated root.

Now, step 2 is considered. For the previous particular solution, and taking into account that $\bar{a} = \frac{a-\hat{a}}{\alpha} = 0$, i.e. $\hat{a} = a$, the slow model is written as:

$$\dot{x} = f(x) - \mathscr{T}(x)\cdot 0 \cdot x = f(x), \tag{4.26}$$

which is nothing other than the tuned system whose solutions $x(t) = x^*(t)$ are sinusoidal.

4.2.5 Boundary layer fast subsystem

The next step is to evaluate the stability of the boundary layer system in the finite time interval $t \in [t_0, t_1]$. This is obtained by evaluating the fast subsystem (4.25) along one particular solution of the quasi-steady-state $x_p(t)$, and by re-scaling time t to the stretched time coordinates $\tau = (t - t_0)/\varepsilon$. The fast subsystem (4.25) evaluated along this trajectory is

$$\begin{aligned}\frac{d}{d\tau}\hat{\tilde{x}}_{l_1} &= -\hat{\tilde{x}}_{l_1}\\ \frac{d}{d\tau}\hat{\tilde{x}}_{l_2} &= -\hat{\tilde{x}}_{l_2} - \tilde{\bar{a}}(\tilde{a})y_p\\ \frac{d}{d\tau}\tilde{\bar{a}} &= \hat{\tilde{x}}_{l_2} y_p,\end{aligned}$$

which can be rewritten as:

$$\frac{d}{d\tau}\hat{z} = J(y_p)\hat{z} = J(\tau, \omega, \varepsilon)\hat{z}. \tag{4.27}$$

with

$$J = \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & -y_p \\ 0 & y_p & 0 \end{bmatrix} \tag{4.28}$$

Under these conditions, system (4.27) is reduced to the autonomous linear system

$$\frac{d}{d\tau}\hat{z} = J(\tau, \omega, 0)\hat{z} = J(y_{p_0})\hat{z}. \tag{4.29}$$

Consider the $y_{p_0} \in \mathscr{D}_x$, with $\mathscr{D}_x \triangleq \{x : |y| = |x_2 - x_4| > \varepsilon_0\}$. The above system has the following properties.

Property 4.6 *The eigenvalues of $J(y_p)$, for $[t, x_p, z] \in [t_0, t_1] \times D_x \times \mathbb{R}^3$, are all strictly negative, i.e.*

$$\lambda_1 = -1 \tag{4.30}$$

$$\lambda_2 = Re\left\{\frac{-1 + \sqrt{1 - 4{y_p}^2}}{2}\right\} < 0 \tag{4.31}$$

$$\lambda_3 = Re\left\{\frac{-1 - \sqrt{1 - 4{y_p}^2}}{2}\right\} < 0, \tag{4.32}$$

where $\varepsilon_0 > 0$ is a constant.

Therefore $J(y_p)$ is Hurwitz in the considered domain. As a result, there exists a matrix $P(y_p) = P(y_p)^T > 0$ and a $Q(y_p) > 0$ such that the standard Lyapunov equation holds:

$$P(y_p)J(y_p) + J(y_p)^T P(y_p) = -Q(y_p).$$

From standard Lyapunov arguments, it follows that for all $t \in [t_0, t_1]$,

$$||\hat{z}(t, \varepsilon)|| \leq c_1 \exp\left\{-\lambda_{min}(Q(y_p))\left(\frac{t - t_0}{\varepsilon}\right)\right\}.$$

Tikhonov's theorem [76] can now be used to summarize the previous result.

Theorem 4.7 *There exists a positive constant ε^* such that for all $y_{p_0} \in \mathscr{D}_x$, and $0 < \varepsilon < \varepsilon^*$, the singular perturbation problem of (4.24)-(4.25) has a unique solution, $x(t, \varepsilon)$, $z(t, \varepsilon)$ on $[t_0, t_1]$, and*

$$x(t, \varepsilon) - x_p(t) = O(\varepsilon) \tag{4.33}$$

$$z(t, \varepsilon) - \hat{z}_p(t/\varepsilon) = O(\varepsilon) \tag{4.34}$$

hold uniformly for $t \in [t_0, t_1]$, where $\hat{z}_p(\tau)$ is the solution of the boundary layer model (4.29). Moreover, given any $t_b > t_0$, there is $\varepsilon^{**} \leq \varepsilon^*$ such that

$$z(t, \varepsilon) = O(\varepsilon)$$

holds uniformly for $t \in [t_b, t_1]$ whenever, $\varepsilon < \varepsilon^{**}$.

In order to extend this result to an infinite time interval, it is necessary that the boundary layer system is exponentially stable in a neighborhood of the tuned slow solution $x_p(t)$ for all $t \geq t_0$. This may not be a simple proof, and it will be left for future investigation. Instead, the effectiveness of this approach is shown below using simulation.

An intuitive yet not completely rigorous explanation for the resulting good behavior in the infinite time interval can be given with the help of Fig. 4.2. Notice that the Hurwitz nature of Jacobian (10.13) is only lost when $y = x_2 - x_4 = 0$. Since the fast motion, z, evolves with almost constant y (vertical lines in Fig. 4.2), y will not reach the value zero during this motion provided that y is initially far enough from zero. Once the slow manifold is reached, the slow variable will evolve in the domain $z = 0$. This domain corresponds to the case when the adaptation mechanism has reached its objective and parameter a is correctly estimated. In this domain y may reach the value zero but, intuitively, it is assumed that the system, once the adaptation law has reached the correct value, will present a behavior that is similar to the known load case, whose stability is proved in Chapter 3.

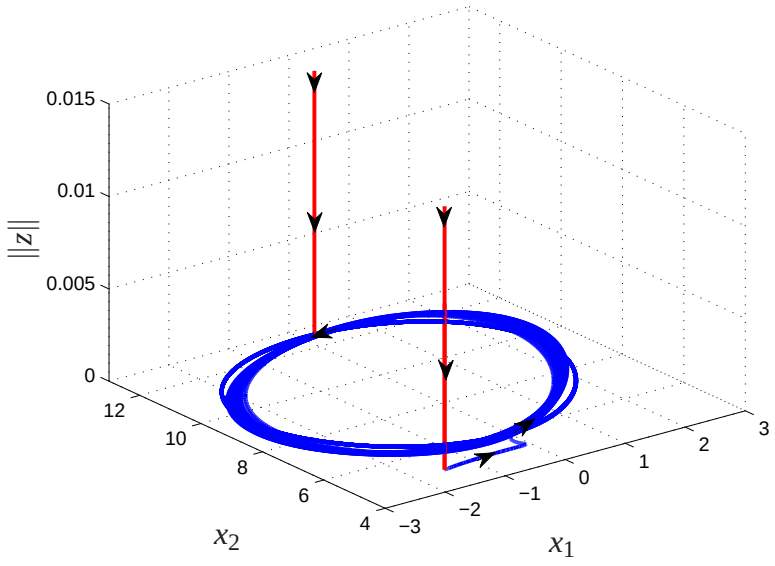


Figure 4.2: Evolution of two trajectories in the state subspace $(x_1, x_2, \|z\|)$. The last part of the trajectory is in the plane $\|z\| = 0$.

4.2.6 Simulations

The inverter parameter values are the same as those for the known load case given in the Subsection 3.2.4, where the load resistance has been 50Ω and, therefore, $a = 0.01$. The desired output is

$$V_o = 220\frac{2}{\sqrt{2}}\sin(100\pi t).$$

At time $t = 0s$, the chosen value for the adaptation parameter is $\hat{a} = 0.001$ (which corresponds to $R_0 = 1000\Omega$, i.e. the relative error is 90%). Later, at time $t = 0.5s$, a load variation is produced from $R = 100\Omega$ to $R_0 = 1000\Omega$, such that, parameter a is again equal to 0.01

Once again, a commutation time of $50KHz$ is employed resulting a sample time of $0.1T$ s.

Figures 4.3 and 4.4 show the evolution of the output voltage and the voltages of every boost DC-DC after $t = 0s$, respectively. Note that the circuit tends to the desired behavior. During this period the adaptation mechanism does not destabilize the system.

Figures 4.5 and 4.6 show the evolution of the output voltage and the voltages of every boost DC-DC around $t = 0.5s$, respectively. Note that the circuit continues with the desired behavior. The time scale is the real time scale before the change of variable. Note that during this time, when the perturbation in the resistance and, thus, the corresponding adaptation mechanism is activated, the output signal does not undergo any significant variation.

The adaptation of parameter a is represented in Figs. 4.7 and 4.8 where the load-change instants in the transition and steady-state are zoomed respectively. Note that the adaptation is very fast relative to the time scale of the system. In each of these graphs two evolutions are presented for two different values of ε. Note the smaller ε is, the faster the adaptation is.

4.3 Conclusions

In this chapter an adaptation law is added to the previous control law in order to deal with a common and important problem in the field of electronics: slowly varying and/or unknown loads. For that, an adaptive control for unknown load is developed, which adapts the load very fast with respect to the time evolution of the system. The method is based on using a state observer on one-sided inverter and assuming that the state variables are measured.

The stability of the complete system is proved by rewriting the system in the standard sin-

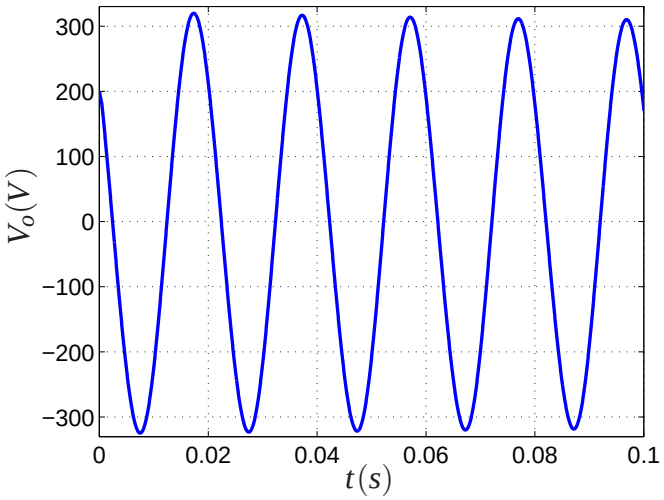


Figure 4.3: Output voltage with the adaptation of an unknown load in $t = 0s$.

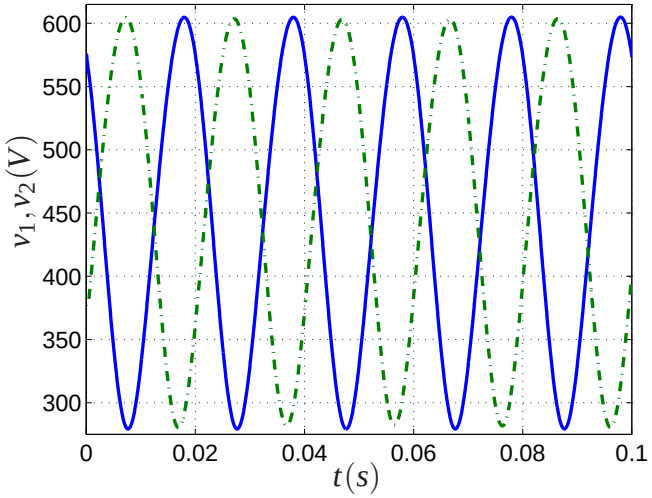


Figure 4.4: Output voltages of the first (solid) and second (dashed) boost DC-DC converters with the adaptation for an unknown load in $t = 0s$.

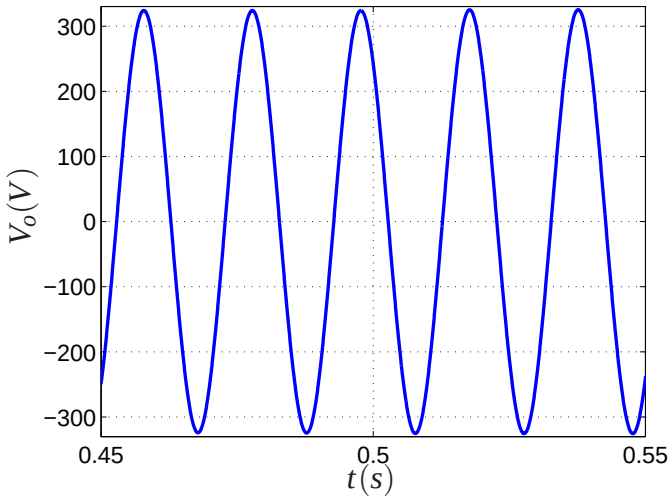


Figure 4.5: Output voltage with the adaptation of an unknown load in $t = 0.5s$.

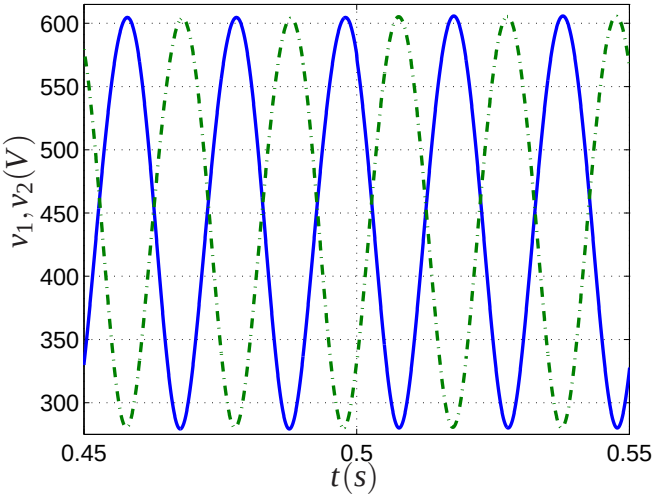


Figure 4.6: Output voltages of the first (solid) and second (dashed) boost DC-DC converters with the adaptation for an unknown load in $t = 0.5s$.

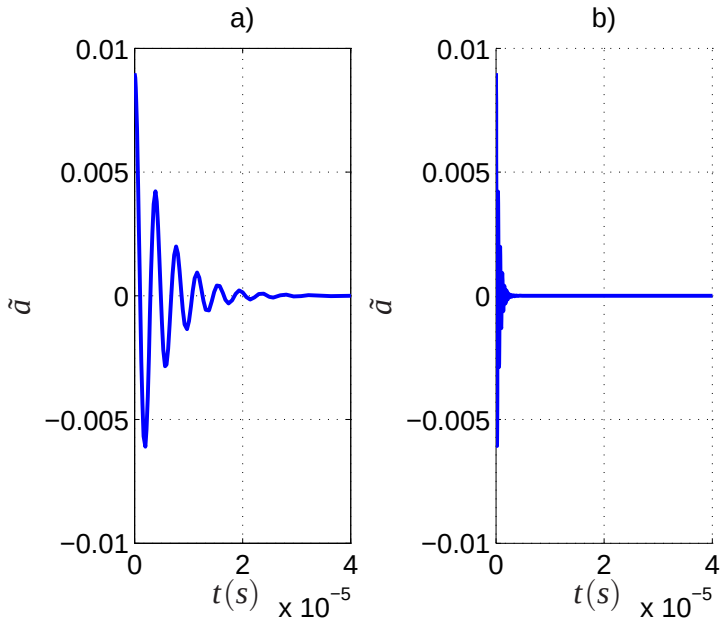


Figure 4.7: Time-evolution of the fast variable $\tilde{a}$ with $\varepsilon = 0.01$ in $a)$ and $\varepsilon = 0.001$ in $b)$. The perturbation is at $t = 0s$.

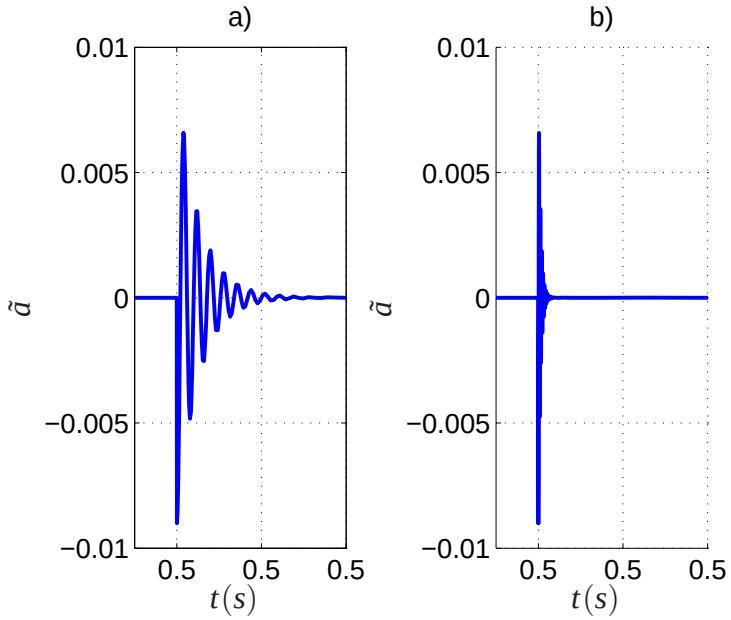


Figure 4.8: Time-evolution of the fast variable $\tilde{a}$ with $\varepsilon = 0.01$ in $c)$ and $\varepsilon = 0.001$ in $d)$. The perturbation is at $t = 0.5s$.

gular perturbation form; hence some relationship between the adaptation gain, γ, the observer matrix parameter, α, and the perturbed variable parameter, ε, are achieved. Another important relationship between the perturbed variable parameter, ε, and the system frequency, ω, is achieved in the analysis of the boundary layer fast subsystem. Finally, the stability is established by means of Tikhonov's theorem [76]. The stability proof extension for an infinite time interval, will be an objective for further investigation.

The assumption that voltage and current are measurable simplifies the observation problem. No persistant signals are required to prove the stability and the no noise is included in the measurable signals. As future work, an extension of this development could be done assuming that only the currents are measurable and including experimental results in order to validate all assumptions established in this work.

Chapter 5

Estimation of the attraction domain

In the previous chapter, a controller has been developed for the boost inverter. Global stability of the closed-loop system has been guaranteed by a Lyapunov function. However, state and control-signal constraints including saturations have been disregarded.

In this chapter, the objective is to estimate a satisfactory attraction domain for the boost inverter taking into account physical system constraints, containing control signal saturations. That is, to estimate a region composed of all initial conditions corresponding to trajectories that converge towards the right system behavior. The system will be driven into this attraction domain by a starting phase; this is common on the field of electronics [13,91,156]. This attraction region is estimated by using a novel method developed in this chapter.

Estimating an attraction domain may be involved if there are physical system constraints. This problem may present a high degree of difficulty due to the system and control-law nonlinearities, including saturation-like constraints. The term saturation-like constraints is used for non-linear functions $\gamma(u)$ that appear in the system model and they become the identity, $\gamma(u) = u$, in certain regions of the state space that include the desired behavior, (those regions are referred to regions in which such constraints are not active). Functions of this sort include typical control signal saturation as well as others, such as rate limiters, for example. Other constraints on the state variables can be considered as well.

There exist many published methods to estimate the region of attraction (see, for example [54, 76] and the references therein). A kind of such methods is based on Lyapunov theory: closed Lyapunov-function level surfaces enclose (conservative) estimations for the region of attraction [76]. These methods often employ polynomial systems [85, 124, 146]. There exist powerful mathematical tools that can be used in the computation of the maximum acceptable level for polynomial systems [32, 68, 111, 151]. Some of these tools could be further developed for application to non-polynomial systems as well [31]. Application of

these methods would imply to seek for Lyapunov functions in order to be able to deal with the constraints. The search for a Lyapunov function by means of the numerical estimation method may be seen as an advantage as the user would not be required to propose a Lyapunov function. In cases like these, however, the computational method has to solve a much more difficult problem and it will be hard to tackle with systems of moderate complexity. Furthermore, saturation-like functions, which are one of the most common nonlinearities in practice, are usually out of the scope of these techniques. Usually saturation-like functions are only considered in the case of linear systems [5, 21, 110, 114].

A simple idea that solves the problem of estimation of the attraction domain for polynomial non-linear systems (and some others) with saturation-like constraints and state constraints is presented. The idea is to take advantage of the unconstrained global stability analysis and use this result to obtain a 'conservative' estimation of the region of attraction for the constrained case. Using the Lyapunov function of this analysis, there is no need to look for a Lyapunov function while estimating the domain of attraction and, thus, this problem becomes much simpler. On the other hand, the estimated attraction region is included in the domain where the saturation-like constraints are not active and, therefore, the method introduces a new source of conservatism. This obvious idea may be successful in hard problems when all other methods fail.

In this chapter, this approach is employed to the boost inverter to estimate an attraction region. The application of the method produces good, albeit conservative, results. However, certain difficulties should be mentioned here: 1) the system equations are quite involved and can even present non-polynomial terms, namely rational functions; 2) the desired attractor is not an equilibrium point but a limit cycle. Both complications make the use of any other analysis method a formidable task.

For sake of simplicity, in the application of this method to the boost inverter, the phase controller dynamic is not taken into account either the adaptation law.

5.1 Problem statement

In Section 3.2 a control law (Eqs. (3.39)–(3.40)) for boost inverter not has been only designed, but has been also proved that for all initial conditions except the origin, the trajectories of the system tend to the curves $\Gamma_i = 0$ for $i = 1, 2$. Nevertheless, there are several constraints in the state variable that make this analysis useless from the practical point of view. These constraints are of several types:

C1. Saturation-like constraint: $\text{sat}_0^1(u_i)$ for $i = 1, 2$, makes control law (3.39)–(3.40) not to be feasible in the full state space. Therefore, this constraint is 'soft' in the sense that if

the system arrives at a point where the constraints are violated, the analysis of Section 3.2 is no longer valid for the system with constraints. The point may nonetheless still lie inside the attraction domain of the desired limit cycle. Therefore, these constraints are saturation-like.

C2. Capacitor voltages must be strictly positive in this circuit, which implies $x_i > 0; \quad i = 2,4$. This is a 'hard' constraint since this situation should be avoided.

C3. Finally, the control law is not feasible when any of the denominators in (3.39)–(3.40) are zero. This constraint is actually contained in C1, since denominators close to zero would imply large (positive or negative) values for $u_i; \quad i = 2,4$.

The objective of this work is to obtain a (possibly conservative) estimation for the region of attraction of the resultant system taking these physical constraints into account.

5.2 An approach of estimation of the attraction domain.

Normally, in every control system, the control signal is subject to physical constraints such as saturations, rate-limiters, etc. As for control designs, such constraints are typically disregarded and the resulting control law is applied to the actuator. In this way, if the designed control law is $u_d = \alpha(x)$, where x is the state variable, the actual control signal is $u = \gamma(u_d) = \gamma(\alpha(x))$, where $\gamma(\cdot)$ is a saturation-like function. This approach is valid when the actual expression for u is used in the stability analysis of the resultant system. It is however quite common to neglect the actuator constraints in the stability analysis so as to simplify the analysis. In fact, the local stability property is not usually affected by these constraints, since in a neighborhood $\mathscr{D}$ of the desired attractor they are not active, that is, $\gamma(\alpha(x)) = \alpha(x)\ \forall x \in \mathscr{D}$. However, the resulting attraction domain may be affected by constraints γ. This study deals with the estimation of this attraction domain based on a stability analysis that neglects the constraints.

The analysis can also take into account state variable constraints in the following sense. Assume that there exists a 'forbidden' region in the state space. This means that the system state must remain within the boundaries of a pre-specified admissible ('safe') region. The estimation of the domain of attraction should take into account these constraints.

Formally, the problem can be stated as follows:

Actual system. Consider a control system type defined as such:

$$\dot{x} = f_a(x,u), \tag{5.1}$$

where $x \in \mathscr{S} \subset \mathbb{R}^n$, $u \in \mathbb{R}^{n_u}$. Function f_a may include saturation-like functions. Furthermore, due to physical considerations, the state of the system must not go out of an admissible region $\mathscr{T}$. □

Unconstrained system Assume that an approximate model of the system is

$$\dot{x} = f(x,u), \tag{5.2}$$

where function $f : \mathbb{R}^n \to \mathbb{R}^n$ and, besides, in $\mathscr{D}$, $f(x,u) \equiv f_a(x,u)$. The reader can consider that this approximate model includes neither the saturation-like functions nor the state constraints. □

Assume that a control law $u = \alpha(x)$ has been designed for the unconstrained model (5.2) for a given control objective.

Remark 5.1 *The control objective is not necessarily the stabilization of an equilibrium point, but perhaps the stabilization of limit cycles, for instance, as seen in the examples in Section 3.2, can be considered.*

Assumption 5.2 *There is a widely known radially unbounded Lyapunov function $V(x)$, in which a compact positively invariant set Ω, $\frac{\partial V}{\partial x} f(x,\alpha(x)) \leq 0$. Let $\mathscr{M}$ be the largest invariant subset of the set for which $\dot{V} = 0$ in Ω.*

By the LaSalle invariance principle, assumption 5.2 guarantees that the trajectories of the unconstrained model tend to $\mathscr{M}$. It is implicitly assumed that this is the desired behavior. Notice that if the original Lyapunov theorem is used to prove global stability, the previous assumption is also fulfilled.

Assumption 5.2 also guarantees local stability for system (5.1). The problem lies in the estimation of the domain of attraction.

The key is clearly to ensure that the system state remain within the boundaries of the region where saturations are not active, thus introducing new constraints. A conservative estimation of the region of attraction can then be easily obtained. The advantage of the relative ease with which it is obtained, however, is compromised by the fact that it may be far too conservative. Nevertheless, in many problems this simple idea may give satisfactory results.

Assumption 5.3 *Consider system (5.1) with control law $u = \alpha(x)$. Let be $\mathscr{A} \stackrel{\triangle}{=} \mathscr{D} \cap \mathscr{T}$, that is, the intersection between the safe region and the region where the saturation-like functions are not active. It is assumed that this set can be estimated by a set of inequalities $g(x) \geq 0$, where $g : \mathbb{R}^n \to \mathbb{R}^{n_g}$.*

Now the problem can be transformed as follows:

> Given a control system $\dot{x} = f(x,u)$ with constraints in both the state variables and the control input $g(x) \geq 0$, assume that a control law $u = \alpha(x)$ has been designed such that global stability is confirmed when no constraints are taken into account. The problem lies in estimating a region of attraction for the real system with constraints when this control law is applied.

A 'conservative' estimation for the attraction domain of the system with constraints is given by the following theorem:

Theorem 5.4 *Under assumptions 5.2 and 5.3, assume that there exists a constant $c > 0$ such that in the set $\Omega_c = \{x : V(x) \leq c\}$, the constraints $g(x) \geq 0$ are satisfied. Then, all trajectories of the system with constraints starting at Ω_c tend to $\mathscr{M} \cap \Omega_c$.*

Proof: Since in Ω_c the saturation-like constraints are satisfied, the results for the unconstrained system are valid in Ω_c. Therefore, $\dot{V} \leq 0$ in Ω_c and Ω_c is positively invariant. Furthermore, since $V(x)$ is radially unbounded Ω_c is compact. The statement can be validated by applying LaSalle's invariance principle. ■

Remark 5.5 *Since $\mathscr{M} \cap \Omega_c \subset \mathscr{M}$, the theorem guarantees the desired asymptotic behavior for the system with constraints.*

Remark 5.6 *As with other techniques for estimation of attraction domain, the present method is conservative. In this case the conservativeness is mainly due to two facts:*

- *The estimation of the region of attraction is restricted to domains in which $V \leq c$.*
- *The method considers the saturation-like functions as hard constraints. Nevertheless, there may be points where the saturations are active in the actual attraction domain.*

Using Theorem 5.4, the problem is reduced to finding a value $c > 0$ such that $g(x) \geq 0$ at the points where $V(x) \leq c$. In order to use numerical tools for the determination of c, as will be seen in the next sections, the optimization problem can be stated as follows:

Problem 5.7 *Maximize c*

subject to:

$$(V(x)-c)+p_i(x)g_i(x)-\varepsilon_i \geq 0 \quad i=1,\ldots,N, \tag{5.3}$$

where $p_i(x)$ are unknown semi-definite positive functions and $\varepsilon_i > 0; \quad i=1,\ldots,N$. The purpose of constraint (5.3) is to validate the Theorem 1 hypothesis. To observe this, notice that at the boundary of the set Ω_c, $V(x)=c$ and, thus, the above constraints are reduced to $p_i(x)g_i(x) \geq \varepsilon_i > 0$. As functions $p_i \geq 0$, the constraints $g_i(x) \geq 0$ are satisfied at the points on the boundary of Ω_c. Furthermore, in the interior of this set, $V(x)-c<0$ and, thus, these constraints are also satisfied. The p_i functions lend even more degrees of freedom, thereby increasing problem feasibility. The small ε_i constants are pre-specified and are necessary in order to avoid problems at the points where $p_i(x)=0$. The introduction of ε_i parameters constitute a new source of conservatism.

Remark 5.8 *The region of attraction is estimated without the necessity of computing* $\dot{V}$.

In this work, sum-of-squares optimization is used in order to solve this problem. For this, a new assumption is needed.

Assumption 5.9 *Functions* $f(x,u)$ *and* $g(x)$ *are polynomial.*

5.2.1 Sum of squares optimization

Sum of squares optimization is an optimization technique based on the Sum Of Squares (SOS) decomposition for multivariate polynomials. A multivariate polynomial $p(x)$ is said to be a SOS, if there exist polynomials $f_1(x),\ldots,f_m(x)$, such that:

$$p(x)=\sum_{i=1}^{m} f_i^2(x)$$

and therefore, $p(x) \geq 0$ [117].

A SOS program has the following form [117]:

Minimize the linear objective function

$$r^T c,$$

where c is a vector formed from the (unknown) coefficients of:

- polynomials $p_i(x)$, for $i = 1,2,...,N_1$
- sum of squares $p_i(x)$, for $i = N_1+1,...,N_2$

such that

$$g_{0,j}(x) + \sum_{i=1}^{N} p_i(x) g_{i,j}(x) = 0 \qquad \text{for } j = 1,2,,\ldots,M_1,$$

$$g_{0,j}(x) + \sum_{i=1}^{N} p_i(x) g_{i,j}(x) \text{ are SOS}, \qquad \text{for } j = M_1+1,\ldots,M_2,$$

where w is the linear objective function weighting coefficients vector, and $g_{i,j}(x)$ represent certain scalar constant coefficient polynomials.

Currently, SOS programs are solved by reformulating them as semi-definite programs (SDPs), which in turn are solved efficiently, e.g., using interior point methods. Several commercial as well as non-commercial software packages are available to solve SDPs. SOSTOOLS [116] is a Matlab toolbox that performs this conversion automatically, calls the SDP solver, and converts the SDP solution back to that of the solution of the original problem.

The problem stated in the previous section can be addressed solving the following SOS problem:

Problem 5.10 *Maximize c*

subject to:

$$(V(x) - c) + p_i(x) g_i(x) - \varepsilon_i \quad \textit{are SOS}; \quad i = 1,\ldots,N, \tag{5.4}$$

where p_i are unknown SOS polynomials. This problem is more restricted than that presented in the previous section. Nevertheless, any solution to SOS problem 5.10 is a solution to problem 5.7.

Remark 5.11 *Assumption 5.9 can be relaxed since other types of functions, such as trigonometric functions [109] or rational functions (e.g., the application examples in the next section) can be considered.*

5.3 Application to the boost inverter

The method developed before is used in order to obtain an estimation of the attraction domain for the boost inverter when system physical constraints are taken into account. This method

is useful because the model and control law have a relative high degree and complexity. Furthermore, the global stability proof for the unconstrained problem is available by means a Lyapunov approach.

In Chapter 5.1 it has been proved that, under no constraints, all trajectories (except the one starting at the origin) of system (2.5)–(2.8) with control laws (3.39)–(3.40) tend to the desired limit cycle. Remind that the Lyapunov function used is:

$$V = \frac{\Gamma_1^2}{2} + \frac{\Gamma_2^2}{2}. \tag{5.5}$$

The constraints are (only constraints C1 and C2 are presented here; constraint C3 will be discussed later):

- $u_i(x) \leq 1 \quad i = 1,2$
- $u_i(x) \geq 0 \quad i = 1,2$
- $x_2 > 0$
- $x_4 > 0.$

The expressions for u_1 and u_2, which are given by (3.39) and (3.40) are not polynomial but rational functions. Nevertheless, writing them as quotient of polynomials $u_i(x) = n_i(x)/d_i(x)$ all the constraints can be formulated in standard form. For this, it can be assumed that polynomial $d(x)$ does not vanish at any point of the objective curve $\Gamma_i(x) = 0 \quad i = 1,2$. Otherwise, control laws (3.39)–(3.40) are not valid for this problem. Therefore, the sign of $d(x)$ is constant along $\Gamma_i(x) = 0$ and, by continuity, in a neighborhood of this curve. By numerical inspection, it can be checked that, for the circuit parameters given below, $d(x) > 0$ on $\Gamma_i(x) = 0$. With this consideration in mind, constraints (1)–(3) can be written as polynomial constraints:

- $d_i(x) - n_i(x) \geq 0 \quad i = 1,2$
- $n_i \geq 0 \quad i = 1,2$
- $x_2 > 0$
- $x_4 > 0$

Thus, the problem to solve is

$$\text{minimize } (-c) \tag{5.6}$$

subject to:

$$(V(x)-c)+p_1(x)(d_1(x)-n_1(x))-\varepsilon_1 \geq 0 \tag{5.7}$$
$$(V(x)-c)+p_2(x)(d_2(x)-n_2(x))-\varepsilon_2 \geq 0 \tag{5.8}$$
$$(V(x)-c)+p_3(x)n_1(x)-\varepsilon_3 \geq 0 \tag{5.9}$$
$$(V(x)-c)+p_4(x)n_2(x)-\varepsilon_4 \geq 0 \tag{5.10}$$
$$(V(x)-c)+p_5(x)x_2-\varepsilon_5 \geq 0 \tag{5.11}$$
$$(V(x)-c)+p_6(x)x_4-\varepsilon_6 \geq 0 \tag{5.12}$$

Notice that constraints C3 are considered in the previous set of constraints. Indeed, constraints (5.9)–(5.10) implies $n_1(x) \geq \varepsilon_3 > 0$ and $n_2(x) \geq \varepsilon_4 > 0$, respectively, for $V(x) \leq c$, while constraints (10.15)–(10.16) implies $d(x) \geq n_1(x)+\varepsilon_1$ and $d(x) \geq n_2(x)+\varepsilon_2$, respectively, for $V(x) \leq c$. This implies that $d(x) > 0$ in $V(x) \leq c$.

The following analysis can be directly modified for the case when $d(x) < 0$.

Results

The values of the circuit parameters are taken from Subsection 3.2.4.

Software SeDuMi [144] was used as the SDP solver under SOSTOOLS. The values for parameters ε_i are chosen equal to 10^{-6} while the chosen order for the unknown polynomials p_i is 3. The solution is obtained in approximately ten minutes on a PC (1.66 GHz Intel Core2): 23.26. This result is probably conservative as has been pointed out in Remark 5.6. As a way to corroborate this result, by numerical inspection, it has been found that for $x^{(1)} = (0 \quad -0.1 \quad 0.2 \quad 5.8)^\top$, which corresponds to $V(x^{(1)}) = 33.02$, the constraint $x_2 \geq 0$ is violated.

5.4 Conclusions

The problem considered in this chapter is the estimation of the attraction domain for the boost inverter with the control law proposed in Chapter 3, which does not present a global stability due to certain physical constraints. For this a method for the estimation of the attraction region considering general physical constraints is presented. This approach can be applied to systems with a global Lyapunov stability achieved without considering saturations and other kind of limitations. This is a common situation since, saturations are neglected in many stability analysis. The idea is to take advantage of the Lyapunov level sets, finding the maximum Lyapunov level in such a way that constraints are fulfilled inside it. This makes that the computed attraction domain is a 'conservative' estimation. This method is useful even when the degree and complexity of the equations is high.

For application of the method, powerful computational tools exist when the system is polynomial, such as SOS. Therefore, the closed-loop system needs to be polynomial or rational (however, there exist cases where SOS programming have been applied to trigonometrical and other terms [109]). Consequently, the problem is transformed in a sum of squares optimization problem. Conservativeness of the method has also been discussed.

In the application to the boost inverter the system as the constraints are rewritten in a polynomial form, as the method requires. For simplicity reasons neither phase controller nor adaptive control has been taken into account.

Part II

Controlling a DC-DC Vdd-Hopping converter

Chapter 6

Introduction

The development of low-power electronic devices has raised up in recent years. Very-Large-Scale Integration (VLSI) is mostly used in products related to information technology, such as PCs, mobile devices and digital consumer equipments. Motivated by the Moore's law and market evolutions [132], ARAVIS project (Architecture avancée Re-configurable and Asynchrone pour Video et radio logicielle Intégrée Sur puce) sponsored by Minalogic[1], looks for architecture and design solutions that allow the production of embedded computational platforms in its scalability limit. It proposes a generalization of certain techniques in order to obtain a solution to the technology variability problem in 32nm, what will represent an input toward the development of a new paradigm. This part of the thesis is included in the ARAVIS project context.

Currently System on Chips (SoCs) technology: 90nm, 65nm and, even, 45nm can not be applied any more to the technology of 32nm due to the semiconductor material behavior in small scale. The main problem in this kind of scale is the occurrence of technology variability phenomenon [154], that generates quite disparate performances in a same chip. Consequently, a new architecture must be developed in order to answer to this issue. In Fig. 6.1, an example of this problem is shown. It presents a fault or low performance of a computational node[2] in high speed.

The ARAVIS project is focused on three technology keys:

- re-configurable structure with respect to applicability requirements. It can be accomplished by programming the flexible interconnections between the clustered nodes of the SoC computational unit [113].

[1] http://www.minalogic.com/

[2] The common computational unit of a SoC is composed of clustered nodes [74]

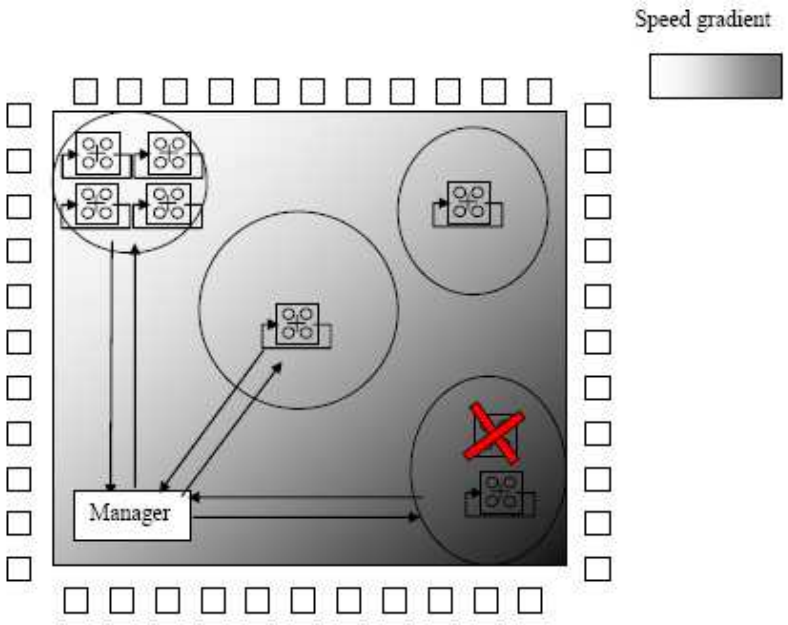


Figure 6.1: Technology variability problem in a chip in a computational node working in high speed.

- Globally asynchronous locally synchronous method [92], in order to release the communication constraints between remote points, and
- dynamic management of the power consumption and activity with respect to constraints are achieved by control theory application [30, 65, 122].

The last key looks for achieving a good trade-off between activity, power consumption and Quality of Service (QoS), what is one of the challenges in future embedded architecture. This dynamic management is especially difficult for 45nm and 32nm, which are at the limit of the scalability. Figure 6.2 shows chips integration in 32nm scale.

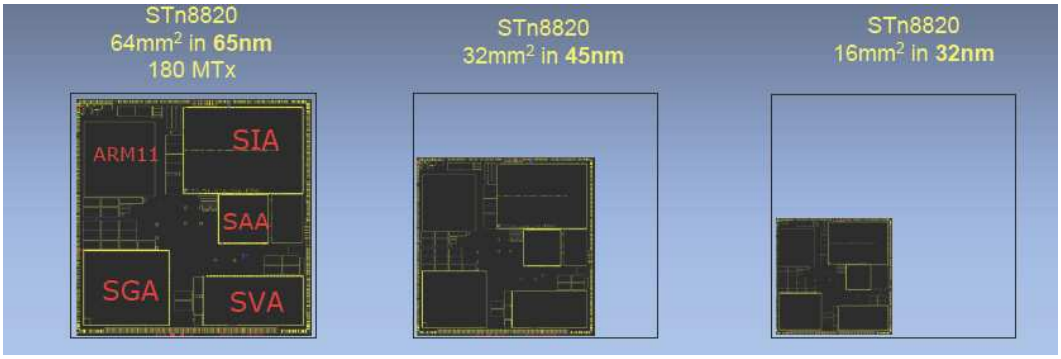


Figure 6.2: Integration of future 32 nm chips.

Advanced control strategies have, therefore, to be designed in order to make the performance fits the requirement, minimizing the energy losses on a chip. This second part of the

thesis focuses on designing control strategies for certain loop of the chip that optimizes the energy consumption.

6.1 Optimization of the energy consumption in SoCs

As has been mentioned before, one of the challenges in the ARAVIS project is the energy-consumption reduction in SoCs, which can be got by means of automatic control methods. Control loops can be applied in different architecture levels: cluster frequency and voltage supply, cluster computational power and management of the quality of service provided by the application [30]. Figure 6.3 shows these different control loops.

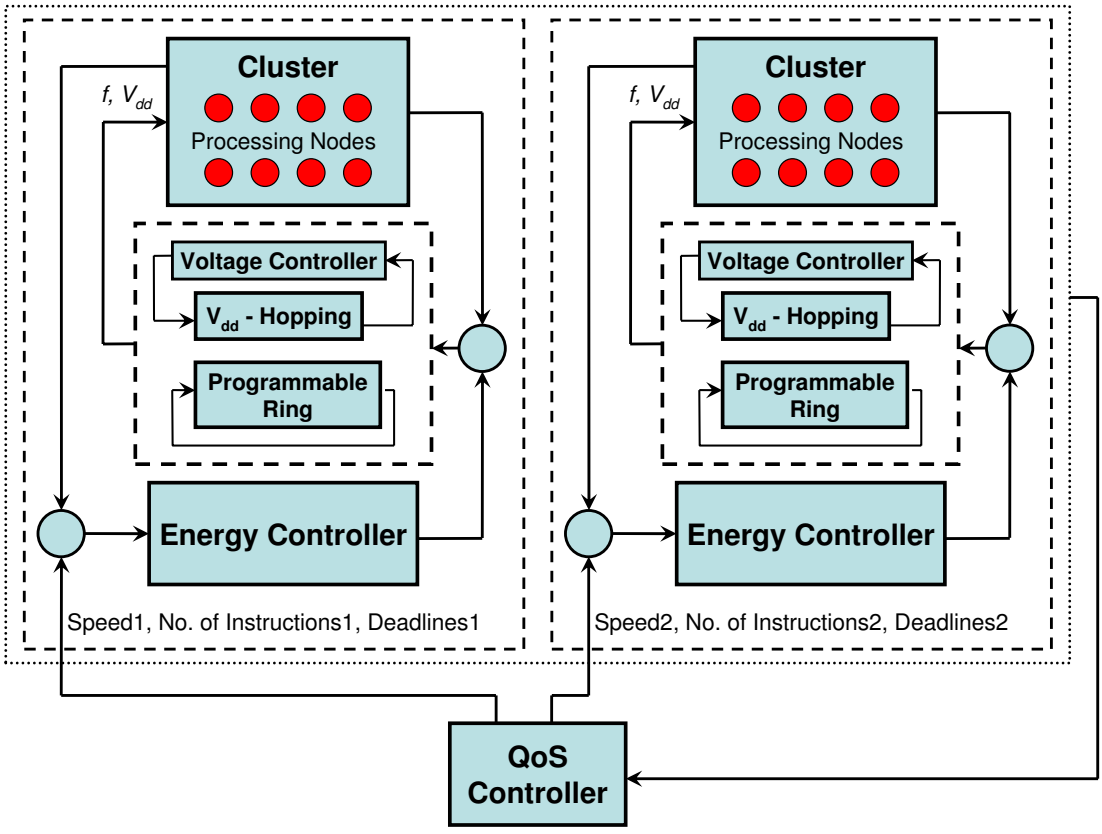


Figure 6.3: Sketch of the three control loops.

Generally, the power consumption can be reduced if the local core voltage or/and the clock frequency are decreased. For this dynamic control loop in frequency and voltage is more and more important in the embedded systems [122]. Thus, these control loops allow the adaptation of computational power in the cluster level, and hence, the power-saving.

Another control loop is used in order to achieve an energy-performance trade-off. The system must not always work in the maximum power level if it can work in other lower power levels. This is possible if each task is performed before to certain deadline [45]. In [39], a control solution has been presented, applying 'robust control'. This solution reaches a control that can reduce or, even, reject the influence of the variability problem.

The last control loop employed in this kind of architecture looks for a trade-off between QoS, computational limitations and global energy consumption.

6.2 Vdd-Hopping DC-DC converter

Microprocessors in SoC have a computational load that requires a time-varying performance. Consequently, the SoCs can achieve a substantial energy efficiency, if they reach to operate at the minimum performance level required by the active software processes.

Dynamic Voltage Scaling (DVS) is a known technique that manages the system power consumption [27, 89, 136]. The operation principle is to adjust the processor supply voltage to the minimum level of performance required by the system application. Therefore, DC-DC converters are a key element in a DVS mechanism, since they can adapt this supply voltage. However, these converters have a different structure than the standards ones, because they must change the operating voltage in a dynamic way [23].

A dynamic continuous buck converter for DVS systems was presented in [88], which provides good performance. It, however, limits SoC scaling properties due to the size of inductive component. In the framework of SoC miniaturization, a Vdd-Hopping DC-DC converter was developed, whose basic structure is showed in Section 6.4. Note that this converter is composed by two supply sources and a Power Supply Selector (PSS) [99]. In this structure, the inductive element is replaced by a set of PMOS transistors[3], reducing the converter required size.

Vdd-Hopping converter is specially interesting, because it may deal with Local Dynamic Voltage Scaling (LDVS) [23, 157] adapted to Globally Asynchronous and Locally Synchronous Systems (GALS) systems [92]. The main idea for GALS systems is to replace the global clock by several independent synchronous blocks. Every synchronous block operates with an own internal clock and they are communicated asynchronously by each other. This mode of operation provides additional flexibility. This fact allows to use energy-aware converter structures such as DVS architectures. DVS is applied in every synchronous block, that is why, it is called LDVS.

[3] P-channel Metal-Oxide-Semiconductor field-effect transistor.

The Vdd-Hopping converter, as has been mentioned before, is basically made up of a PSS and two external supply voltages. A high voltage supply, V_h, for a unit running at nominal speed and a low voltage supply, V_l, for a unit running at reduced speed. v_c is the output voltage of the system.

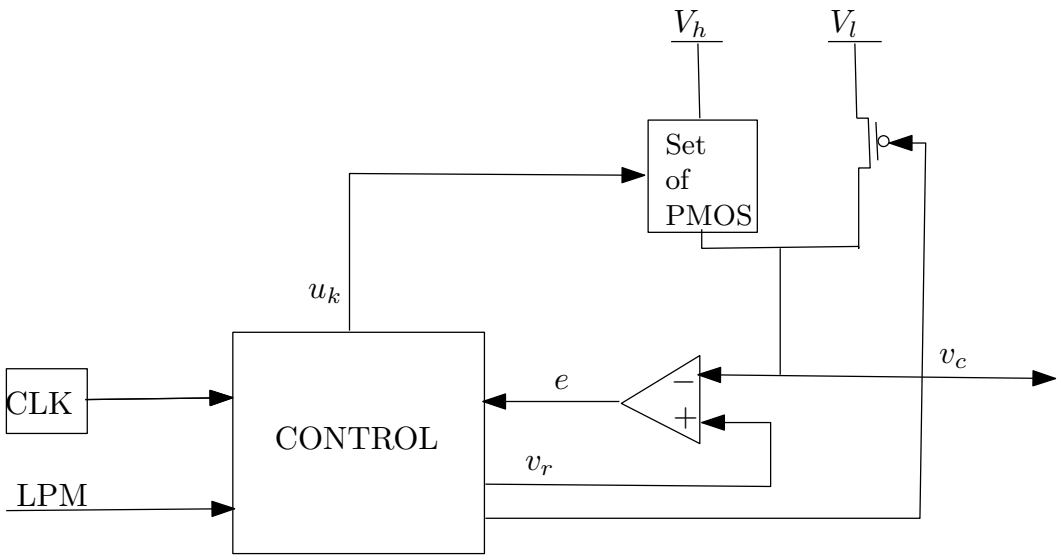


Figure 6.4: DC-DC Vdd-Hopping converter structure.

A PSS is constituted by a group of PMOS transistors connected in parallel with common drain, source and bulk, but separated gates in order to scale the output voltage from a low voltage level to a high voltage level (rising transient-period) and from a high voltage level to a low voltage level (falling transient-period). Furthermore, the PMOS transistor that connects the V_l to the voltage output v_c is switched on when V_l is the selected power supply. This reduces the dissipated energy when the unit running is at low speed. Other component in the PSS is a control block that provides a control signal u_k for the PMOS transistors. Besides it generates a reference signal v_r. Likewise, this control block has as inputs: a clock signal (CLK), a local power manager signal (LPM), that orders to the PSS to start the hopping sequence and the error voltage signal from a comparator e.

Load model

The load model taken in this work is an impedance which depends on the core voltage, v_c, and sometimes, also on the clock frequency, ω_n [98]. In this thesis, the load model provided in [98] is employed. This model approaches a low frequency in function of the core voltage, thus the load only depends on the voltage v_c. It is composed of a current supply, I_{leak}, a capacitance, C, and a dynamic resistance, r_L, representing the dynamic and short-circuit consumption. It is shown in Fig. 6.5.

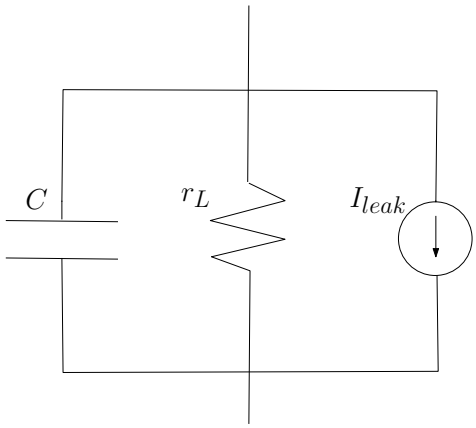


Figure 6.5: Load model.

6.3 Non-linear control application to Vdd-Hopping DC-DC converter

Control objective for this kind of discrete DC-DC converter is to achieve the target voltage providing a correct and reliable operation during the switching transitions, allowing to accomplish the main ARAVIS projet objective: SoCs miniaturization. Therefore, the control must achieve:

- high energy efficiency,
- system stability,
- small current peaks,
- fast transient periods,
- robustness with respect to parameter uncertainty,
- robustness with respect to delays and
- easy implementation.

Figure 6.6 shows the control problem for the DC-DC Vdd-Hopping converter.

A simple discrete controller was proposed in [99] to handle the two voltage levels of the Vdd-Hopping technique. In this control structure only one transistor can be switched at each sampling time. This limits the ability of the converter to make fast transient-periods, and hence the possibility to optimize the energy consumption. In addition, the employed voltage reference was a ramp with a computed slope to obtain the smallest possible current peaks.

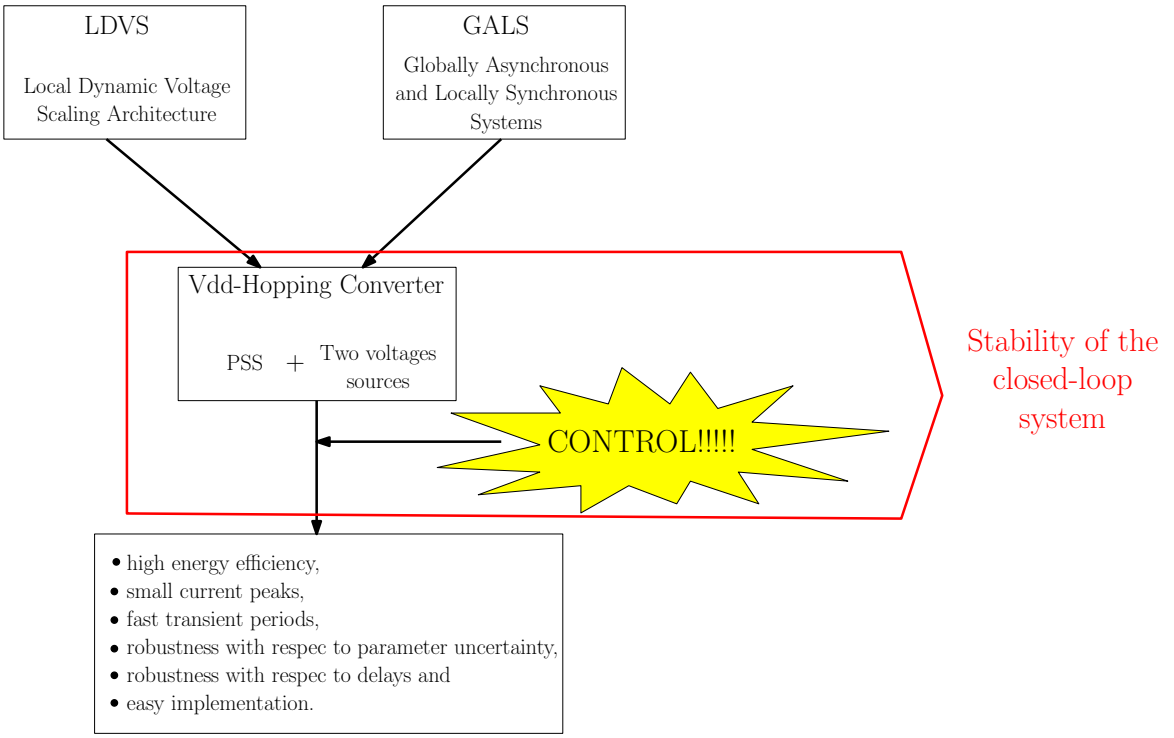


Figure 6.6: DC-DC Vdd-Hopping converter control problem.

6.3.1 High-performance controllers

In Chapter 7, a set of high-performance control laws for the DC-DC Vdd-Hopping converter is developed, without the constraint that only one transistor can be switched at each sampling time. [8]. This allows to obtain a richer set of control sequences and, thus, a better expected performance with respect to the issues previously mentioned. The controllers are developed in order to improve the tracking capability and its regulation characteristic. As a side effect, it is also observed that the transient current peaks are reduced. However, the computational cost is increased.

The different controllers are compared in terms of: transient response, quality of the induced load current and power consumption. It will be seen that the most suitable controller is the one based on Lyapunov theory. However, this controller is enhanced in order to achieve a high energy saving, minimum current peaks and a suitable performance with unknown load resistive parameter, which are very common properties in the field of microelectronics [70, 103]. Firstly, an optimal evolution of the voltage reference will be computed applying optimal control theory [80, 86, 155]. This optimal voltage reference is computed looking for minimizing the current peaks as well as energy losses. Secondly, an adaptive controller is proposed for an unknown load resistive component, offering a suitable system performance by simulation even if it is time-varying. Figure 6.7 shows a sketch of this high performance controller.

In spite of the good advantages that this enhanced controller offers, it presents much more computational blocks (more complex implementation) than the controller proposed in [99] and thus, although, it reduces notably energy consumption, it does not corresponds to a feasible solution for the ARAVIS project context. For this, another controller is developed in Chapter 8 based on the one that presents the easiest implementation from the set of controllers previously presented. This new developed controller must be easy to implement and maintain all the good characteristics obtained by the controller mentioned previously in Chapter 7.

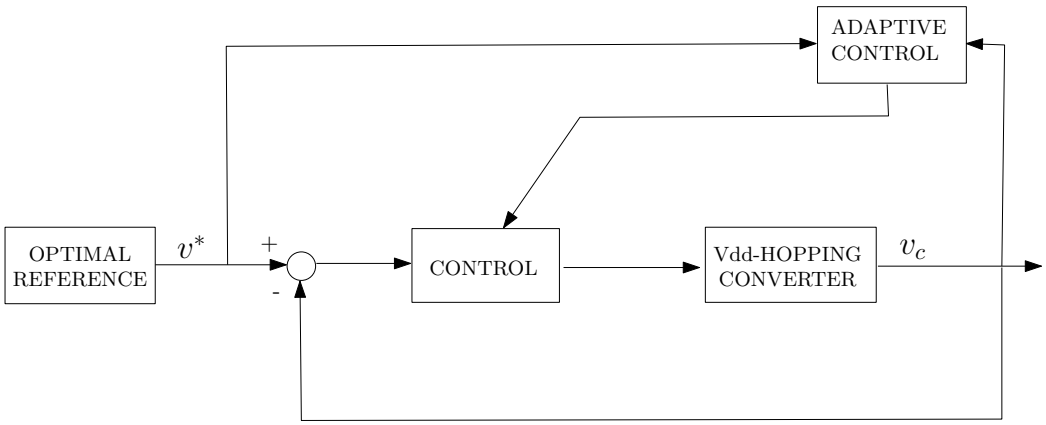


Figure 6.7: Vdd-Hopping converter closed-loop with optimal reference and adaptation parameters.

6.3.2 Energy-aware controller

The previous proposed controller provides very suited properties. The only drawback is that it has a complex implementation, what can exclude it from the ARAVIS project scope. Among the set of controllers presented before, there is one with a simple implementation. In Chapter 8, this controller is selected and developed taking into account the objectives given before to obtain a suitable controller for the ARAVIS project.

The controller with a feasible structure is a 'linear controller, what makes it to present a simple implementation. Hence, it takes a relevant interest in the industrial applications [17, 84, 87, 120]. Nevertheless, this controller does not provide the best system performance. Now, from this structure, an 'advanced linear controller' is developed in Chapter 8. An innovative approach based on saturations with time-varying limits that manages the current peaks during the transient periods is proposed for this controller. Furthermore, energy-efficiency is improved when a step voltage reference is used instead of a ramp voltage reference. Consequently, it does not only reduces the current peaks but achieves also a fast transient response and reduces energy dissipation. In summary, this proposed 'advanced linear controller' is focused on limiting the current peaks while transient periods are reduced, being energy-aware.

Generally, controllers applied in the industry are implemented in discrete-time. Hence that, the previous advanced controller is discretized. This control law is patent pending under the name of ENergy-AwaRe Control (ENARC) [6].

In order to show the consumption energy saving that this controller may achieve, a comparison with a previous controller published in [99] is performed. It is shown that this controller can diminish the energy consumption 96% with respect to the previous published controller. In addition, other control objectives are achieved: faster transients, small current peaks, and easy implementation. For the last characteristic, it is remarked that this controller needs less computational blocks than the other controllers presented above. The stability property is analyzed in Chapter 9. Thanks mainly to its innovative current-peak aware the ENARC control becomes attractive for industrial applications.

These results will be validated in the ARAVIS project by using VHDL-AMS[4] simulator, since the Vdd-Hopping system with the load is an hybrid system between analog and digital elements (the controller will be implemented digitally). It is expected that the ENARC controller is physically implemented in the new generation of SoCs of 45nm and/or 36nm developed in the project context.

6.3.3 Approximate stability analysis for the energy-aware controller

In Chapter 9, an approximate global stability analysis of the equilibrium is developed for the Vdd-Hopping system with the continuous-time version of the ENARC controller [9]. This controller coincides with the 'advanced linear controller' mentioned before. For sake of simplicity, this analysis is performed in continuous-time and it is not rigorous. This analysis allows to have an intuition of the closed-loop system behaviour with the discrete ENARC controller. This assumption is very common [71, 152].

As the Vdd-Hopping model as the continuous-time version of the ENARC controller are nonlinear. Among their nonlinearities, there is a saturation with limits depending on system state. This makes the analysis involve.

For simplicity, a preliminary stability analysis is performed for the Vdd-Hopping system with the 'linear controller' proposed in the set of high-performance controllers developed in Chapter 7. This analysis is based on LaSalle's invariance principle [76]. Then, it is extended to the continuous-time version of the ENARC.

This continuous-time controller has a saturation mechanism, the system can work in three

[4]It is a hardware description language used in electronic design automation. It is capable to define the behavior of mixed-signal systems, because it describes digital systems as well as analog systems. This is a very used powerful software.

operating-modes: non-saturated system (Region I), saturated system in the upper limit (Region II) and saturated system in the lower limit (Region III). It is proved that the equilibrium is placed in Region I. The stability proof is performed in two parts. Firstly, it is proved that the system in saturated mode converges to the non-saturated mode in finite time, and that, it crosses the saturation limit to the Region I without being able to return towards the saturated mode. Secondly, it is also proved that the system converges to the desired point in Region I. This analysis applies LaSalle's invariance principle for a bounded domain limited by a Lyapunov level curve and the saturation limit lines. Figure 6.8 represents this idea.

Once the global stability analysis is ensured for the ENARC controller, the control objective that must be dealt with are: the robustness under delay presence and parameter uncertainties.

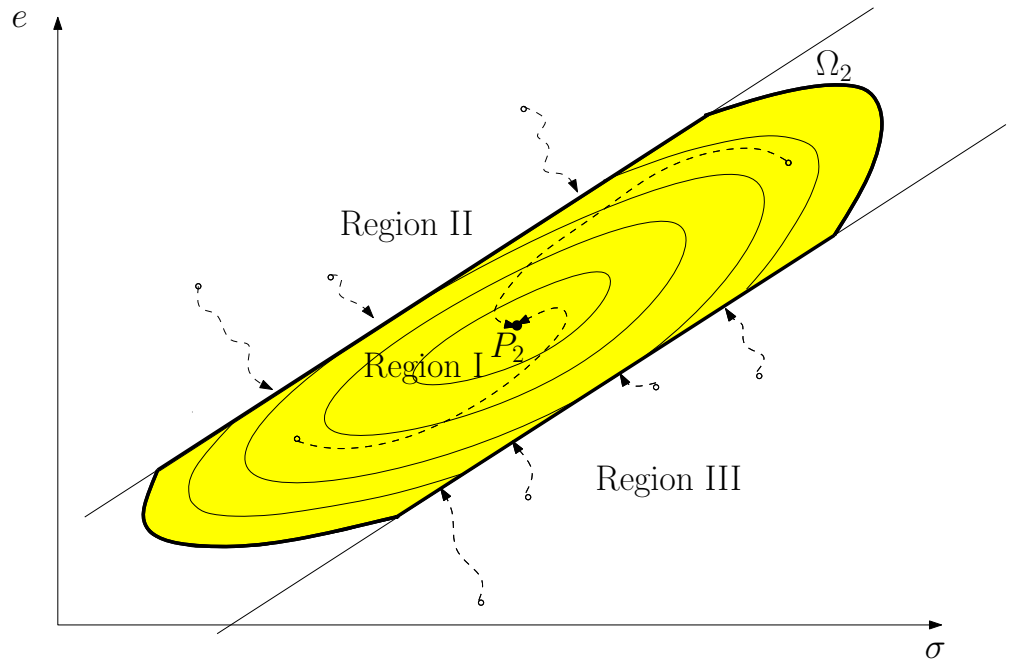


Figure 6.8: Representation of the system operating regions

6.3.4 Advanced energy-aware controller

Previously, an energy-aware controller has been presented, which not only satisfies certain requirements for SoCs, but their stability properties have been also proved. Now, in Chapter 10, this controller is improved in order to satisfy the control objective of achieving robustness with respect to uncertain parameters and delays. The delays are presents in the input and output of the control block for computational and synchronization issues, respectively.

So far, delays and parameter uncertainties have not been considered in the Vdd-Hopping

system. In SoC, however, these issues are very usual [112, 140]. The controller presents delays due mainly to two reasons: synchronization issues and power-performance trade-off [45]. In addition, another point to take into account is the parameter uncertainties, which can cause an unpredictable impact on the power, performance and reliability of the system [34, 93].

In Chapter 10, the ENARC controller is improved dealing with delays and parameter uncertainties. A sub-optimal 'conservative' control tuning approach for the control gains is presented based on linear control theory. This method is sub-optimal because, for simplicity, it is developed for an approximate ENARC controller version that does not consider the current-peaks management. The sub-optimal control gains are obtained solving a H_∞ control problem [26, 53, 101]. This problem is dealt with Lyapunov Krasovskii theory [53, 138], which provides some stability conditions through Linear Matrix Inequalities (LMIs). Consequently, a robust equilibrium stability as well as a robust disturbance rejection under parameter uncertainties are ensured for a delay-time system. This kind of approach are used in industrial applications [14, 129].

In this chapter, the robustness properties achieved by the closed-loop system with the sub-optimal constants applied to the ENARC controller are shown by simulations.

In summary, the ENARC controller with the sub-optimal constants applied to the Vdd-Hopping DC-DC converter can satisfy all the control objectives mentioned before for low-power technology. Therefore, it can have an important impact in the recent trends in the miniaturization of electronic devices.

Chapter 7

High-performance control for the DC-DC Vdd-Hopping converter

The development of low-power electronic devices has raised up in recent years. Very-Large-Scale Integration (VLSI) is mostly used in information technology related products, such as PCs, mobile devices and digital consumer equipments. In a System on Chip (SoC), several levels of supply voltages are required to reduce power consumption. It can be reached applying the Dynamic Voltage Scaling (DVS) concept, which is an interesting method that manages dynamically the microprocessor supply voltage V_{dd} according to various loading conditions.

DC-DC converters may be used in order to apply the DVS concept. Among this kind of converters, a high efficiency discrete converter is found: the DC-DC Vdd-Hopping converter [99], which is implemented applying, as its name references, the Vdd-Hopping approach [75, 106, 128]. This technic delivers two distinct small voltage levels with a very small current, according to the required performance level. Consequently, it achieves a high energy-efficiency. Therefore, its operation principle is to vary the voltage from a low voltage level to a high voltage level, and reciprocally.

A controller for this DC-DC converter must be developed taking into account the context where it will be implemented. One of the main control problem in low-power DC-DC converters is to achieve a high energy-efficiency. Furthermore, DC-DC Vdd-Hopping converters must be able to adapt to various loading conditions and achieve high efficiency over a wide load-current range, which is critical for extended battery life. Moreover, to keep the rate of change of the device voltage providing a correct and reliable operation during the switch transition is also important.

In this chapter, a set of controllers for the Vdd-Hopping converter is developed, obtaining

a high-performance. Among these proposed controllers, the one that offers a best transient performance is selected and enhanced with the aim to deal with the unknown resistive component of the load as well as to minimize the dissipated energy and current peaks, what is very important in the field of microelectronics. Current peaks and power consumption are minimized by computing an optimal evolution for the voltage reference. Likewise, an adaptive controller is proposed to deal with the unknown load resistive parameter. Consequently, the obtained high performance controller can acquires a high consideration on electronic devices.

Generally, the power consumption in a SoC can be reduced if the local core voltage or/and the clock frequency are decreased, that is why a GALS systems is developed in the ARAVIS project where the Vdd-Hopping converter is embedded. Likewise, the clock frequency has to satisfy that the task (for instance, the execution of the control laws designed here) is performed before a deadline and that the minimum required local clock frequency that guaranties the critical path (longest path delay) of the whole chip is fulfilled [45]. Normally, in order to take into account all of these issues in a GALS system when the frequency and voltage have to rise, firstly the voltage is rising and later the frequency is rising. On the contrary, when the frequency and voltage have to fall, firstly the frequency is fallen, and later the voltage is fallen.

7.1 Mathematical model of Vdd-Hopping mechanism

The discrete DC-DC Vdd-Hopping converter presented in [99] for SoCs shows several advantages: high efficiency and reduced size, since it does not need passive components. This converter uses the Vdd-Hopping technique [75, 106, 128] in order to obtain a LDVS architecture for a GALS system. Figure. 6.4 shows this connected Vdd-Hopping structure.

7.1.1 Mathematical model for control design

For simplicity the low voltage supply, V_l, is disregarded for control design purposes (see Fig. 6.4). The main objective is that the core voltage v_c achieves the high and low voltage levels by switching the PMOS transistors. In this configuration,, at least, one transistor must always be switched on.

Figure 7.1 shows an electrical representation of the Vdd-Hopping converter without the low voltage supply, V_l, connected to the load that has been described in Section 6.2.

Assumption 7.1 *PMOS transistors are modeled as ideal resistors when they are switched*

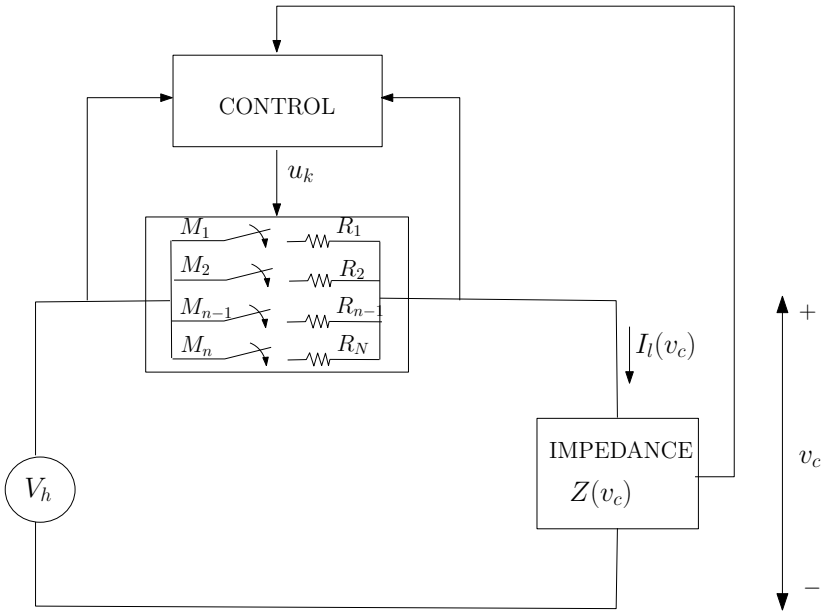


Figure 7.1: Vdd-Hopping, voltage supply and load.

on and as resistors with infinite resistance when they are switched off. They are considered to have the same electrical characteristic.

The voltage loop equation yields the relationship

$$I_l(v_c) = \frac{V_h - v_c}{R_{u_k}}, \quad \text{where} \quad R_{u_k} \triangleq \frac{R_0}{u_k}. \tag{7.1}$$

u_k is the number of transistors switched on, thus, $u_k \in \mathscr{U} = \{1, 2, ..N\}$ and it is the control variable. Likewise, R_0 is the PMOS transistor resistance. In this kind of system, it can be assumed that all transistors have the same transistor resistance $R_0 = R_1 = R_2 = \ldots = R_N$.

The current through the set of PMOS transistors, I_l, depends on voltage v_c and control signal u_k. Thus, I_l varies during the hopping transients.

In this work, as mentioned in Section 6.2, the load model presented in [98] is employed:

$$I_l = f(v_c, f_{clk}) = I_{dyn} + I_{short} + I_{stat} + I_{cap} \tag{7.2}$$
$$I_{dyn} = K_{dyn} f_{clk} v_c \tag{7.3}$$
$$I_{short} = K_{short} f_{clk} (v_c - 2V_{th})^3 \tag{7.4}$$
$$I_{leak} = K_{leak} \tag{7.5}$$
$$I_{cap} = C \frac{dv_c}{dt}, \tag{7.6}$$

where C, K_{dyn}, K_{stat} and K_{leak} depending on the real consumption estimation. V_{th} is the

threshold voltage, which must fulfill $v_c > 2V_{th}$. And f_{clk}, which represents the clock frequency, may be approximated as a function of the core voltage, v_c.

Figure 7.2 shows the representation of the load model used in this research. r_L represents the dynamic resistance. For simplicity reasons, firstly, an constant average value of r_L is taken in order to design controllers. Later, the real time-varying parameter, r_L, will be taken into account.

The averaged load resistance R_L is given by

$$R_L \triangleq \frac{1}{t_f - t_0} \int_{t_0}^{t_f} r_L dt.$$

where t_0 and t_f are the initial and final time, respectively, in the rising transient period. Assume that R_L has the same value in the falling transient period.

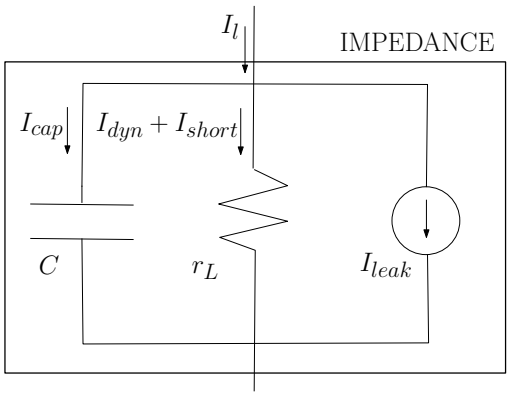


Figure 7.2: Load model.

Let us combine the specific form of the load, Eqs. (7.2)–(7.6), with system (7.1). The voltage equation can be expressed as

$$\dot{v}_c = -\beta v_c + b(V_h - v_c)u_k - \delta, \tag{7.7}$$

where

- $\beta \triangleq \frac{1}{CR_L} > 0$ and $\delta \triangleq \frac{I_{leak}}{C} > 0$ depend on the load.
- $b \triangleq \frac{1}{CR_0} > 0$ depends on PMOS resistance, R_0, and on load parameter C.

Define the voltage error as: $e \triangleq v_r - v_c$, where v_r is a voltage reference. Thus, the associated error voltage equation is

$$\dot{e} = -\beta e + b(v_r - V_h)u_k - bu_k e + \beta v_r + \delta + \dot{v}_r. \tag{7.8}$$

7.2 Control laws

The objective of this section is to present some high-performance control laws for the Vdd-Hopping converter, fulfilling the requirements mentioned before. All these controllers are designed to provide stable behaviors, and different control methodologies are used in each case.

Some simulations are performed, such that the behavior of the closed-loop system with the different controllers are shown. In these simulations, $N = 24$ is taken as the total number of PMOS transistors in the model shown in Fig. 7.1. Note that, at least, one active transistor must be always switched on. The voltage supply is $V_h = 1.2V$. The reference signal, v_r, follows a linear time evolution between the low voltage level $V_l = 0.8V$ and the high voltage level $V_{c_h} = 1.2 - \Delta_h$. This signal has a slope specified by the designer, which is inspired by [99].

Remark 7.2 *For physical reasons, the maximum voltage achieved, v_c, must be $V_{c_h} = V_h - \Delta_h$ where $\Delta_h \in \mathbb{R}$ and is small. Δ_h depends on the voltage supply, PMOS resistance and load parameter.*

The system resistances are $R_L = 27.7\Omega$ and $R_0 = 31.41\Omega$, the capacitance is $C = 9nF$ while $K_{leak} = 1.67 \cdot 10^{-3}$, the threshold voltage is $V_{th} = 0.4V$, and system clock frequency is $\omega_n = 500MHz$. The sampling frequency has the same value that the clock frequency. The difference between the high voltage supply, V_h, and the high core voltage, V_{ch}, is $\Delta_h = 0.08V$ and the slope of the reference signal, v_r, is $1.067 \cdot 10^6 V/s$.

7.2.1 Control proposed in [99]

The development of the set of the high performance controllers for the Vdd-Hopping converter is inspired by the 'intuitive control' used in [99], under the form:

$$u_k = \text{sat}_1^N \{u_{k-1} + \text{sign}(e)\} \tag{7.9}$$

In this law, no more than one transistor switches at each sampling time according to the sign of the voltage error. Previously to the works developed in this thesis [8, 9], control (7.9) was the only published controller. Therefore, this controller has the limitation that one only transistor can be switched on or off at every sampling time. Figure 7.3 shows the implementation of this controller. Likewise, Fig. 7.4 shows a simulation for this controller by using Matlab. Note that the performance presents an oscillatory behavior, with important current peaks.

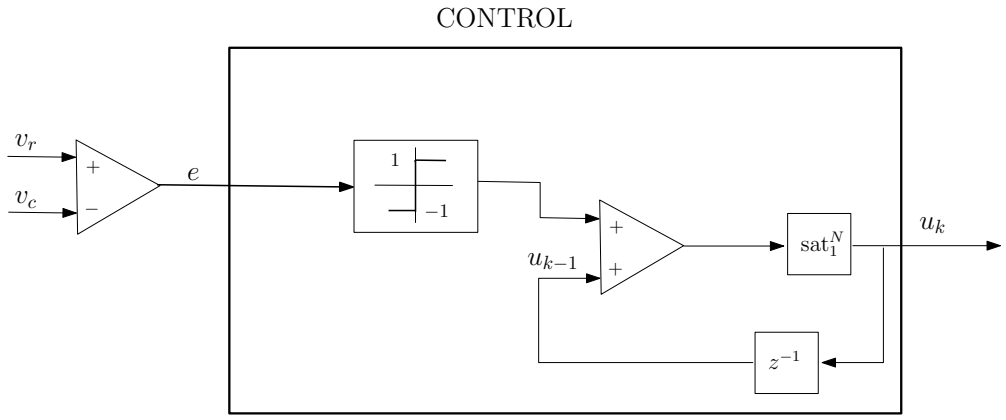


Figure 7.3: Intuitive control from [99].

In what follows, other control alternatives are proposed without the constraint that only one transistor can be switched on or off, as long as the number of transistor is limited by 1 and N. This introduces a saturation in every control law for the Vdd-Hopping converter.

Remark 7.3 *Every control law is designed in such a way that the desired output voltage corresponds to one of the saturation bounds* 1 *or* N*, since they corresponds to the lower or higher voltage level, respectively.*

Assumption 7.4 *The sampling time is chosen in such a way that the controllability and observability properties are preserved.*

Control laws will be designed using directly the nonlinear continuous-time equation (7.8). This will lead to a continuous-time controller expression that will be approximately discretized. This approach is very common in the field of automatic control [71, 81]. The implementation of these discrete-time controllers are shown by block diagrams.

The time evolution for the reference signal employed in [99] is maintained in the simulations of each developed controller in this section. However, later, it will be seen that, by means of choosing an suitable reference, the closed-loop system performance can be enhanced.

7.2.2 Controller No. 1: linear controller

The first proposed controller is based on a linear structure, namely a PI (Proportional-Integral) controller. This controller is the most common industrial control solution [17, 84, 120]. It has to be designed to cope with possible steady-state errors.

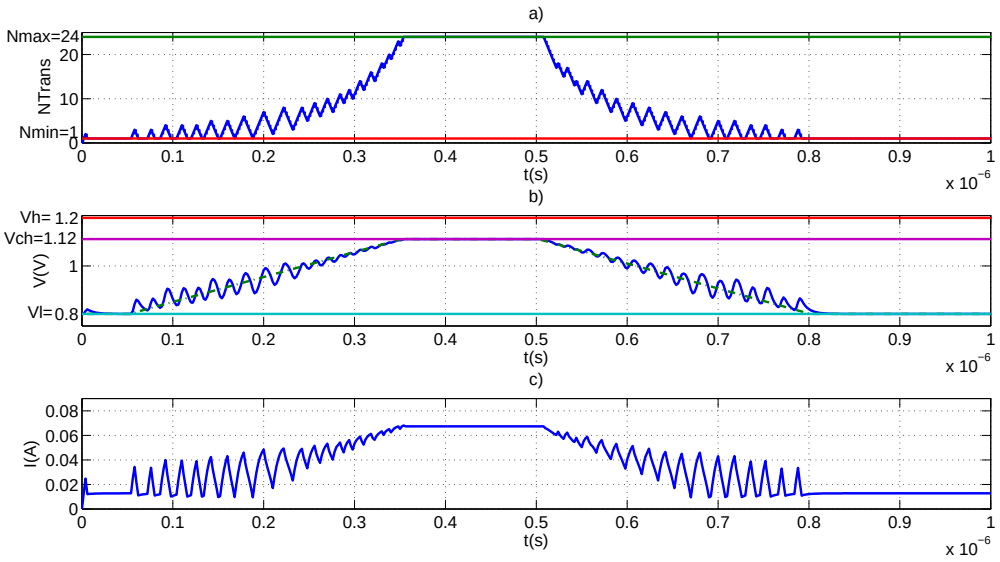


Figure 7.4: Intuitive control. Evolution of: a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid), c) current. I_l.

The proposed control law is:

$$u_k = \text{sat}_1^N \text{round}\{K_1 e + K_2 \sigma\}, \tag{7.10}$$

where σ corresponds to $\int_t^{t+T_s} e dt$ and being $T_s = \frac{1}{\omega_n}$ the sampling time.

The constants K_1 and K_2 are tuned off line. The tuning process must take into account the sampling frequency, low and high voltage level, number of transistors, load parameters and PMOS resistance.

A tuning method is proposed to ensure the right system performance. For this, the closed-loop system is linearized around a set point, such that, $K = [K_1, K_2]$ are defined by ensuring that $A + BK$ is Hurwitz. This tuning mechanism is

$$K_1 = \frac{2\xi\omega_n - (u_{k_l} b + \beta)}{b(V_h - V_l)} \tag{7.11}$$

$$K_2 = \frac{\omega_n^2}{b(V_h - V_l)}, \tag{7.12}$$

being u_{kl} the minimum value of transistors that have to remain switched on, i.e., the minimum value of u_k, $u_{kl} = 1$, and ξ is a design parameter. In Chapter 9, constraints on ξ are obtained, such that, the closed-loop system is asymptotically stable to the equilibrium point $[e, \sigma] = [0, \bar{\sigma}]$.

The closed-loop system with control (7.10) can suffer wind-up. This phenomenon has

not been studied and it is a future work. It is highlighted that in the performed simulations this effect has not displayed.

The discretization of this controller is:

$$u_k = sat_1^N \left\{ u_{k-1} + \text{round}(\bar{K_1}\Delta e_k + \bar{K_2} e_k) \right\}, \tag{7.13}$$

where

$$\bar{K_1} \triangleq K_1 - \frac{K_2}{2} \tag{7.14}$$

$$\bar{K_2} \triangleq K_2 T_s. \tag{7.15}$$

Equations (7.14)–(7.15) are common relationships between continuous- and discrete-time system [104].

Next up, Fig. 7.5 shows the approximate discretization of this controller, for digital implementation.

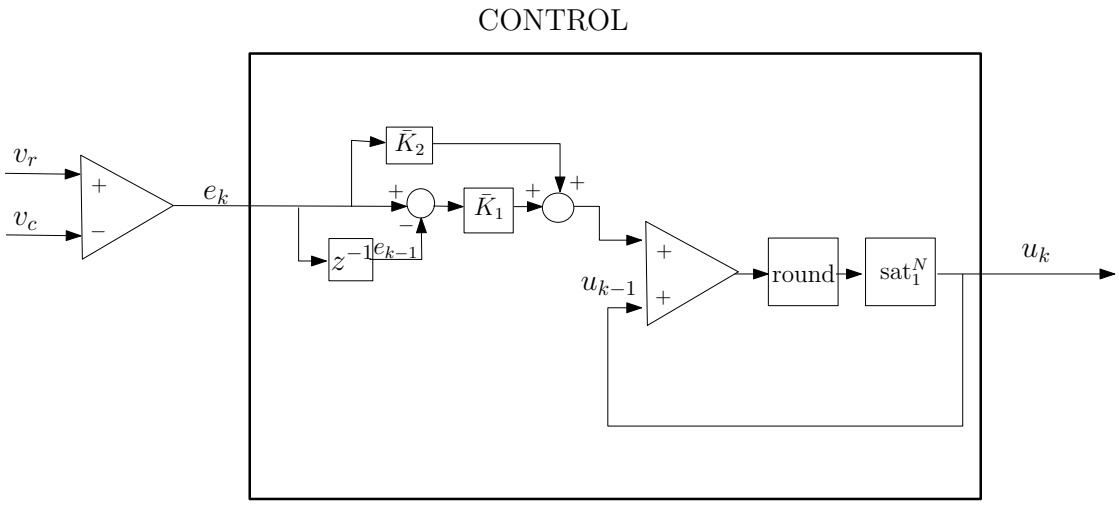


Figure 7.5: Digital PI controller.

Figure 7.6 shows a simulation of the system (7.8) with control (7.13). In this simulation is chosen as design parameter value $\xi = 0.05$. The interval I defined in Lemma 9.1 (in Section 9.1) results $[0.01, 0.08]$. Therefore, the equilibrium stability will be able to be guaranteed according to Chapter 9. This controller could be the most suitable for physical implementation not only because it requires a reduced number of computational blocks, but also because it does not require model information. Moreover, as it can be seen in Fig. 7.6, it provides better performance in both voltage and current variables with respect to the intuitive controller. Nevertheless, it still presents some peaks in the current signal.

In summary, this control law can make that the system achieve the suited stability properties, as will be seen in Chapter 9, with the characteristic to requires a reduced number of computational blocks.

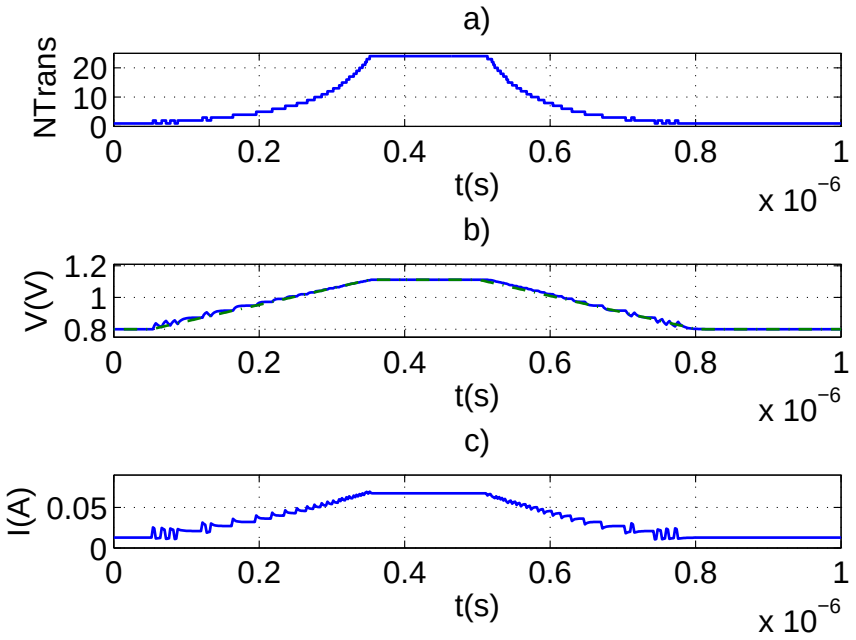


Figure 7.6: Control No.1. Evolution of: a) number of PMOS transistors switched on, b) the v_r (dashed) and v_c (solid). c) the current I_l.

7.2.3 Controller No.2: feedback linearization

The second proposed controller is designed by using feedback linearization technique. This leads to a continuous-time linear system in closed-loop. The aim of this method is that the closed-loop system becomes

$$\dot{e} = -K_3 e - K_4 \sigma,$$

which achieves the suited properties of a stable linear system. Remind that $\sigma = \int_t^{t+T_s} e dt$.

The controller has the following form:

$$u_k = \frac{K_3 e + K_4 \int_t^{t+T_s} e dt + \beta(v_r - e) + \dot{v}_r + \delta}{b(V_h + e - v_r)} \tag{7.16}$$

where K_3 and K_4 are positive constant.

Note that, if K_3 and K_4 are positive and the next Lyapunov function is chosen:

$$V_{lin} = \frac{e^2}{2} + K_4 \frac{(\int_t^{t+T_s} e dt)^2}{2},$$

which differentiation is

$$\dot{V}_{lin} = -K_3 e^2 \leq 0,$$

then the equilibrium stability with control (7.16) is guaranteed.

For physical implementation, the controller (7.16) has the next discrete-time approximation,

$$u_k = \text{sat}_1^N \text{round} \left\{ \frac{\bar{K_3}(e_k - e_{k-1}) + \bar{K_4} e_k + \beta T_s (v_{r_k} - e_k) + v_{r_k} - v_{r_{k-1}} + \delta T_s}{b T_s (V_h + e_k - v_{r_k})} \right\} \quad (7.17)$$

where $\bar{K_3}$ and $\bar{K_4}$ follow the similar change of parameter given for $\bar{K_1}$ and $\bar{K_2}$ in Controller No.1 (Eqs (7.14)–(7.15)), i.e.:

$$\bar{K_3} \triangleq K_3 - \frac{K_4}{2} \quad (7.18)$$

$$\bar{K_4} \triangleq K_4 T_s. \quad (7.19)$$

Note that, the saturation and rounding functions are necessarily considered in the discrete-time controller.

Figure 7.7 shows the implementation of the approximate discrete-time controller No. 2, Eq. (7.17).

The performance of the control (7.17) with $K_3 = 2.4$ and $K_4 = 1.44$ is displayed in Fig. 7.8. These constants have been tuned by ensuring that the closed-loop system is Hurwitz. Observe that the current peaks have been reduced with respect to the 'intuitive controller', obtaining a smoother current signal. Moreover, the voltage evolves towards the voltage reference with hardly oscillations. As a consequence, the dissipated energy will be reduced, as will be shown below. Nevertheless, this controller has two drawbacks, it directly uses model parameters and needs a larger number of computational blocks.

7.2.4 Controller No.3: Lyapunov-based design

The last controller is designed guarantying closed-loop Lyapunov stability conditions for the equilibrium, $e = 0$. Once again the design is performed employing the continuous-time error equation (7.8).

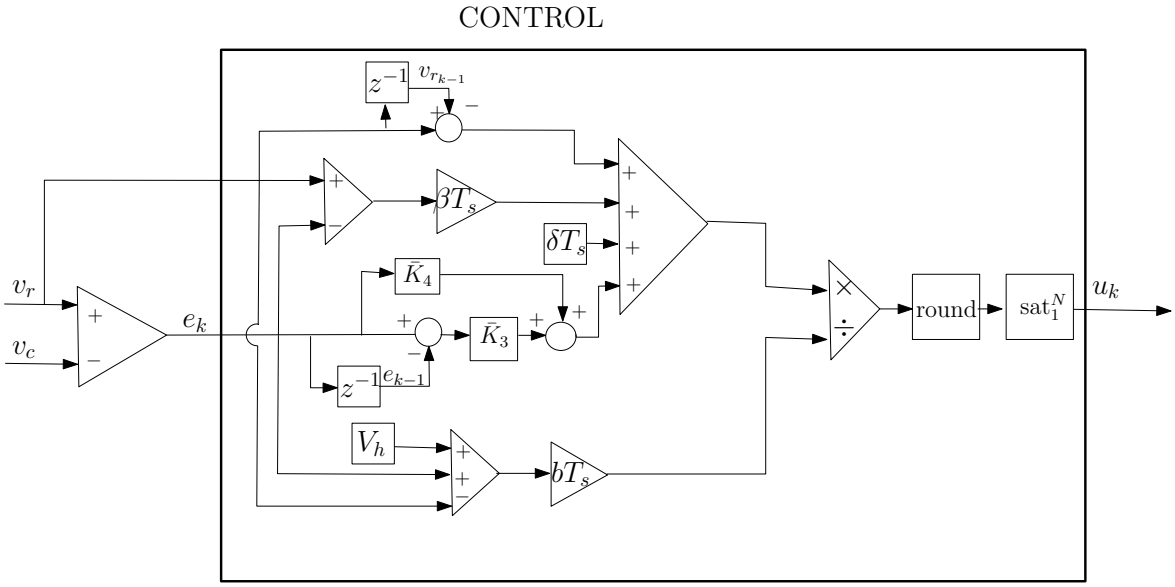


Figure 7.7: Digital feedback linearization control.

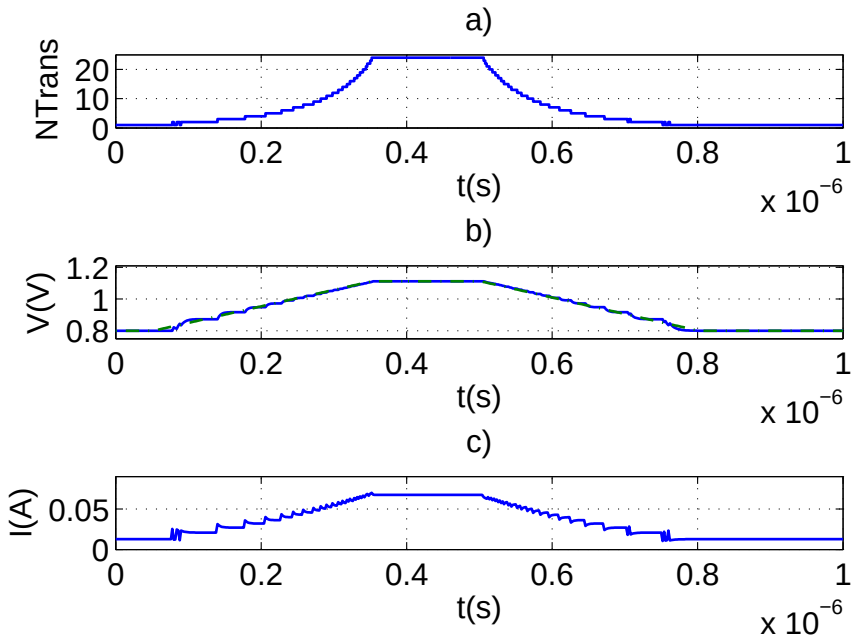


Figure 7.8: Control No. 2. Evolution of: a) number of PMOS transistors switched on, b) the v_r (dashed) and v_c (solid). c) the current I_l.

Consider the following Lyapunov function candidate

$$V_{lyap} = \frac{e^2}{2}.$$

Its time derivative is

$$\dot{V}_{lyap} = -\beta e^2 + (b(v_r - V_h)u_k - bu_k e + \beta v_r + \delta + \dot{v}_r)e. \tag{7.20}$$

The negativeness of $\dot{V}$ can be assured canceling the undesired terms. This can be done by choosing

$$u_k = \frac{\beta v_r + \dot{v}_r + \delta}{b(V_h + e - v_r)}, \tag{7.21}$$

then Eq. (7.20) will be

$$\dot{V}_{lyap} = -\beta e^2 \leq 0.$$

Therefore, $e = 0$ is asymptotically stable.

The approximate discrete-time version of Eq. (7.21) considering the saturation and rounding function for physical implementation purposes is:

$$u_k = \text{sat}_1^N \text{round}\left\{\frac{\beta T_s v_{r_k} + v_{r_k} - v_{r_{k-1}} + \delta T_s}{bT_s(V_h + e_k - v_{r_k})}\right\}, \tag{7.22}$$

Figure 7.9 shows a block diagram of this discrete-time controller.

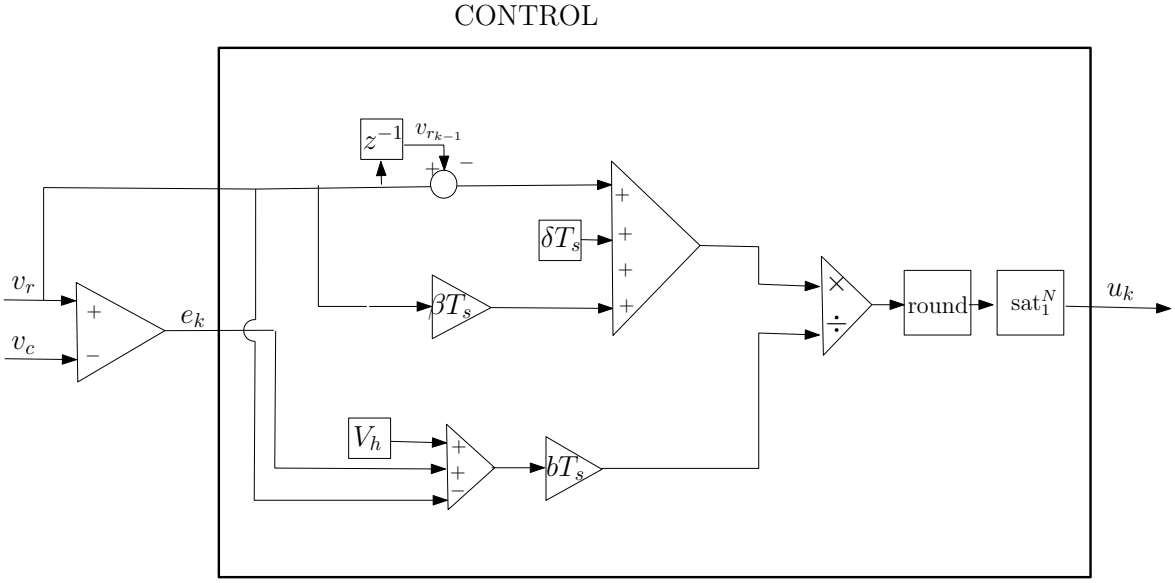


Figure 7.9: Digital Lyapunov control.

The performance of this controller is displayed by simulation in Fig. 7.10. Note that, the application of this controller to the Vdd-Hopping converter reduces the current peaks,

obtaining smoother voltage and current evolutions. Note that the obtained performance is similar to the one obtained with the feedback linearization controller (see Fig. 7.8). However, this controller presents less computational blocks. Compare Fig 7.7 and Fig. 7.9.

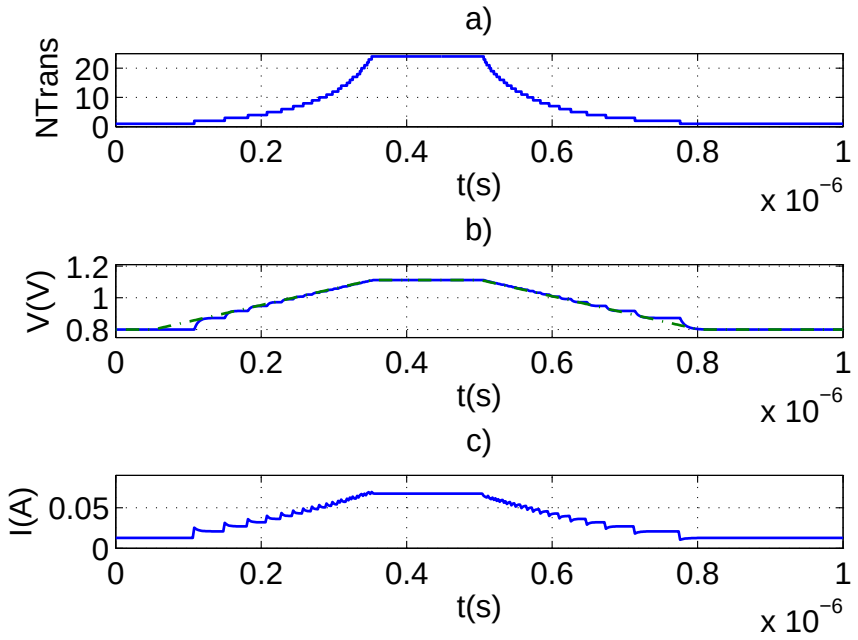


Figure 7.10: Control No. 3. Evolution of: a) number of PMOS transistors switched on, b) the v_r (dashed) and v_c (solid). c) the current I_l.

7.3 Performance evaluation

In this section a performance evaluation is performed for the resulting voltage and current signals, after applying the previous controllers. The voltage signal performance is evaluated by computing the mean and variance of the voltage error. Likewise, the current signal performance is evaluated by computing the maximum current peaks produced as well as its Power Spectral Density (PSD). This PSD is computed using all the recorded data, since this decomposition is computed after the simulation.

Table 7.1 presents the mean and variance of the voltage error signal and maximum peak of the current signal.

Note that, all the new proposed controllers improve the system performance with respect

	Mean Error	Var. Error	Max. Curr. Peak
Intuitive	$3.32 \cdot 10^{-3}$	$6.59 \cdot 10^{-5}$	$4.0 \cdot 10^{-2}$
Contr. No. 1	$2.4 \cdot 10^{-3}$	$2.54 \cdot 10^{-5}$	$2.5 \cdot 10^{-2}$
Contr. No. 2	$2.52 \cdot 10^{-3}$	$4.66 \cdot 10^{-5}$	$0.5 \cdot 10^{-2}$
Contr. No. 3	$2.24 \cdot 10^{-3}$	$3.37 \cdot 10^{-5}$	$0.5 \cdot 10^{-2}$

Table 7.1: Performance evaluation.

to the solution given in [99]. Furthermore, equilibrium stability has been guarantied for Controller No.2 and No.3 in the previous section. Likewise, equilibrium stability of Controller No.1 will be proved in a chapter dedicated to such purpose (Chapter 9) because of its complexity. From this point of view, among these new proposed controllers, the most interesting one is Controller No.3, since it provides the best voltage and current performance. This can be observed in Table 7.1 and in Fig. 7.11. Observe that controller No.3 ((d) in Fig. 7.11) provides a PSD smaller than the other controllers (see (a), (b) and (c) in Fig. 7.11).

7.3.1 Energy evaluation

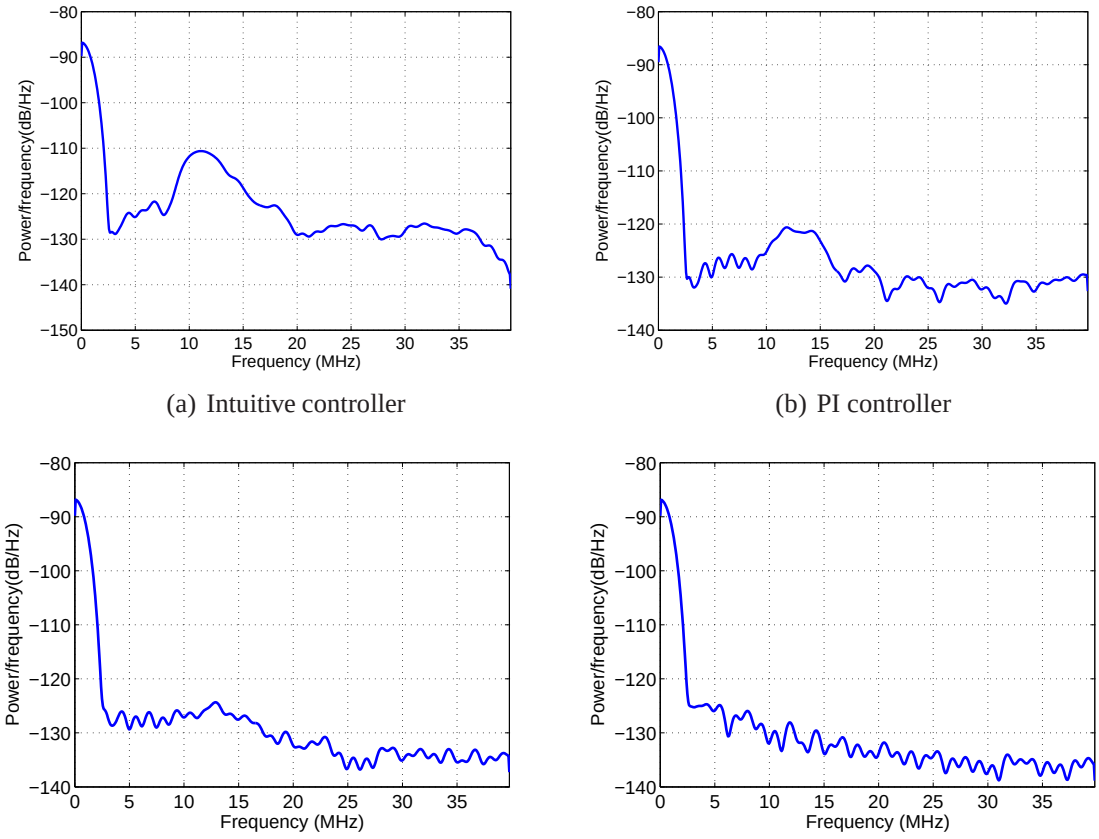
In the set of PMOS, the accumulated dissipated energy in the transient period depends on the control law employed, i.e., on the switching sequence. For instance, undesirable oscillatory current profile can be obtained with certain controllers. This non-smooth behavior of the transient current may result in a higher energy consumption. The purpose of this subsection is to evaluate the energy cost associated with each one of the controllers presented in previous section.

The estimation of the dissipated energy in the PMOS transistors during the transient-period is

$$E_d = \int_{t_0}^{t_f} (V_h - v_c) I_l dt$$

where t_0 is the initial time and t_f is the final time in such transient period. Figure 7.12 and Tab. 7.2 show the dissipated energy during the rising transient period.

Note that the energy consumption for all controllers presented above is improved with respect to the intuitive controller. This is due to the smoother behavior of voltage and current signals obtained with these controllers. Likewise, note that, the smallest dissipated energy is achieved with Controller No.3, since it provides the best performance.



(a) Intuitive controller

(b) PI controller

(c) Feedback linearization controller

(d) Lyapunov Controller

Figure 7.11: Power spectral density.

DISSIPATED TOTAL ENERGY (μJ)	
Intuitive control	7.2
Controller No.1	6.8
Controller No.2	6.2
Controller No.3	4.8

Table 7.2: Total energy dissipated in rising transient period.

7.3.2 Summary

The intuitive control proposed in [99] provides a reasonable tracking at the expense of an oscillatory behavior due to its own limitation. This involves that the current signal time profile presents a high frequency behavior with some substantial peaks, in particular when the total PMOS parallel resistances are larger. This seems to be the main cause of a larger dissipated energy.

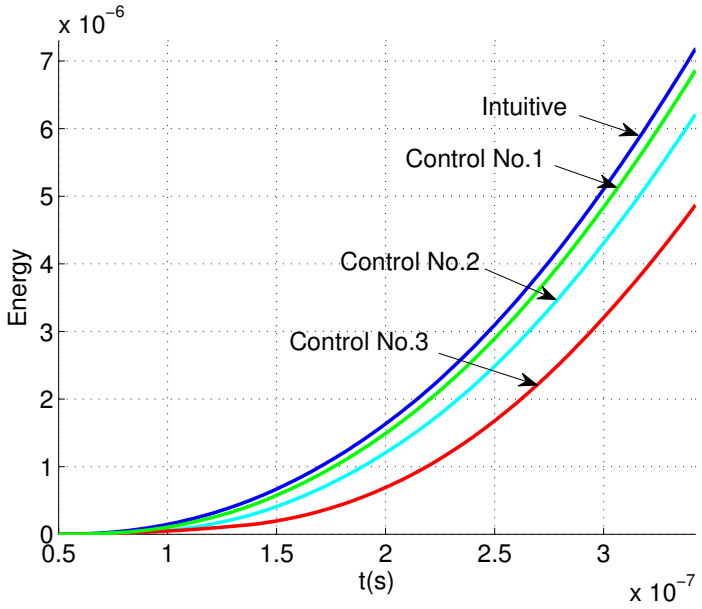


Figure 7.12: Energy dissipated during the rising transient period.

Linear control (Controller No.1) does not need model knowledge. This controller also reduces the current peaks with respect to the intuitive controller. The dissipated energy reduction according to this intuitive controller is 5%.

Control by linearization (Controller No.2) yields a smother current and voltage time-profiles, reducing the current peaks. However, it directly needs system knowledge and presents more computational blocks. In terms of energy consumption, this controller improves the 'intuitive control' by 14%.

Lyapunov's controller (Controller No.3) requires also model knowledge and a certain number of computational blocks. The highlight of this controller is its energy consumption reduction, which is due to the smoother behavior of the voltage and current time profiles. This involves that the controller reduces by 32% the energy consumption with respect to the 'intuitive control'.

Although the Lyapunovs controller presents very nice characteristics, they may be enhanced by changing the voltage signal reference and adapting the resistive load parameter. Firstly, a signal reference can be computed looking for minimizing the dissipated energy and the current peaks as well. And secondly, note that, the controller depends directly on the resistive load parameter. Therefore, an adaptive controller can be designed to cope with variations and/or uncertainties on this load parameter. These two issues will be seen in the next section.

Generally, the power consumption can be reduced if the local core voltage or/and the

clock frequency are decreased, that is why a GALS systems is developed in the ARAVIS project where the Vdd-Hopping converter is embedded. The frequency is chosen in such a way that the task (for instance, the execution of the control laws designed here) is performed before a deadline and that the minimum required local clock frequency that guaranties the critical path (longest path delay) on the corresponding clock domain [45]. Normally, in order to take care of this issue when the frequency and voltage have to rise, firstly the voltage is rising and later the frequency is rising. On the contrary, when the frequency and voltage have to fall, firstly the frequency is fallen, and later the voltage is fallen.

7.4 Advanced Lyapunov's controller

The Lyapunov's controller (Eq. (7.21)) presents very suited properties for the Vdd-Hopping converter. However, this controller can be improved.

On the one hand, minimization of energy consumption and current peaks are desired. This can be achieved finding an appropriate evolution for the voltage reference, $v_c^*(t)$, by applying optimal control theory [80, 86, 155].

On the other hand, note that the Lyapunov's controller depends on the resistance load parameter, β. However, this parameter is, in many occasions, difficult to estimate and may change with time, as mentioned in Section 7.1. Therefore, a second objective is to design an adaptation law in order to obtain an estimation $\hat{\beta}$ for the unknown parameter.

The proposed control architecture including the optimal reference and the adaptation mechanism is shown in Fig. 7.13.

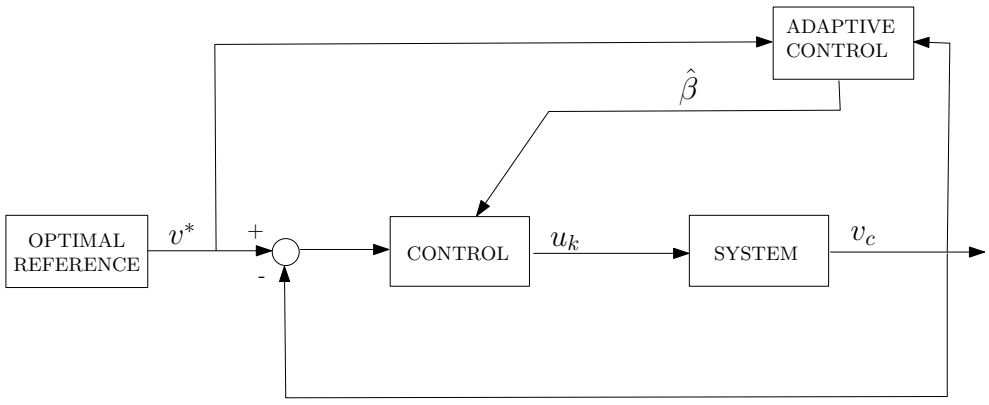


Figure 7.13: Vdd-Hopping closed-loop with optimal evolution of the reference and adaptation parameter.

7.4.1 Optimal voltage reference computation

Assume that the desired voltage is constant. The problem may be formulated as to find a continuous-time voltage reference trajectory from a voltage initial value $v_c(t_0)$ to set-point v_r, minimizing current peaks, ΔI, and the dissipated energy. This problem will be addressed applying continuous-time optimal control theory [80, 86, 155].

In order to optimize the current peaks, time derivative of the current $\dot{I}_l$ is included in the performance index. In every sampling time, a certain number of transistors will be switched on. The total number of PMOS transistors switched on at the previous sampling time is denoted by u_k^-, and the total number of PMOS transistors switched on at the current sampling time is denoted by u_k^+. Consequently, the number of PMOS transistors switched on or off in every sampling time is given by $\Delta u_k = u_k^+ - u_k^-$.

The current peaks are due to the sudden change of the PMOS resistance at the sampling times. These peaks $\Delta I_l = I_l^+ - I_l^-$ are given by

$$\Delta I_l = \frac{V_h - v_c}{R_0}(u_k^+ - u_k^-) = \frac{V_h - v_c}{R_0}\Delta u_k.$$

The same notation given above for u_k^+ and u_k^- is used here for variable I_l. Therefore, the continuous-time approximation for the current peaks is

$$\dot{I}_l \approx \frac{V_h - v_c}{R_0}\dot{u}.$$

Another way to achieve this same expression is taking time derivative of I_l given by Eq. (7.1). Rigorously, the time derivative of this current is

$$\dot{I}_l = \frac{V_h - v_c}{R_0}\dot{u} - \frac{\dot{v}_c}{R_0}u.$$

Nevertheless, it can be shown by simulation that during a typical transient-period, the last term is very small (see Fig. 7.14). This simulation is performed using the same parameters given in Section 7.2. This graph supports the previous argument.

Take the following performance index

$$J = \int_0^\tau L(e,u,t)dt, \tag{7.23}$$

where the final time τ is free and the Lagrangian $L(e,u,t)$ is chosen in order to penalize:

- voltage error e,

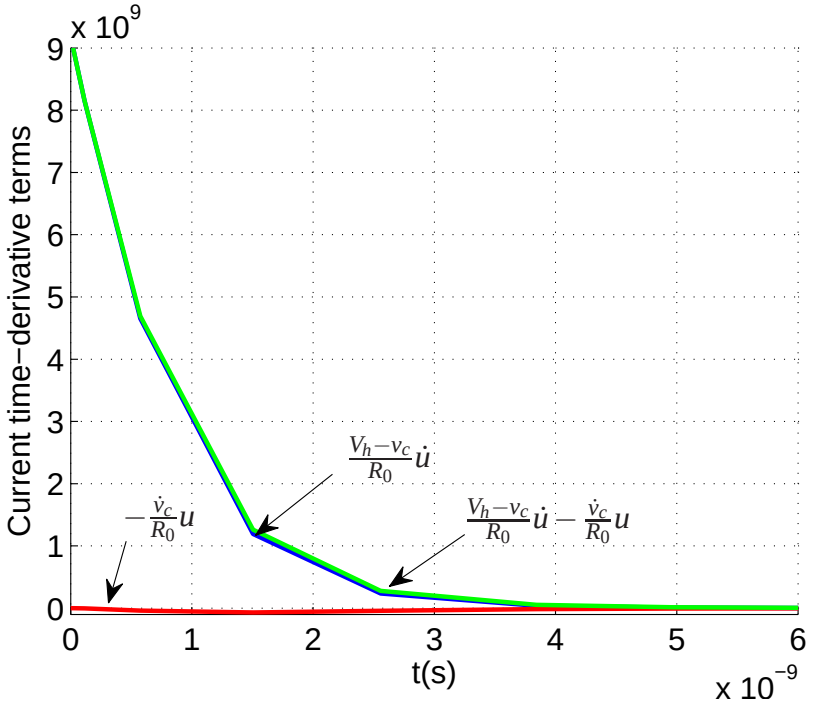


Figure 7.14: Current time-derivative terms.

- dissipated power $P = (V_h - v_c)I_l$ and
- current peaks $\dot{I}_l$.

For this, the following Lagrangian is chosen

$$L = q_1 e^2 + q_2 \left(\frac{(V_h - v_r + e)^2}{R_0} u \right)^2 + \left(\frac{V_h - v_r + e}{R_0} \dot{u} \right)^2, \tag{7.24}$$

where q_1 and q_2 are positive weighting constants. The first term of Eq. (7.24) penalizes the voltage error, the second one penalizes the dissipated power in the set of transistors and the last one, the current peaks. This dissipated power is modeled as $P_w = \frac{(V_h - v_c)^2}{R_0} u$, where $v_c = v_r - e$.

Let us consider a 2-dimensional optimal control problem $x = [e, u]$ with $\dot{x} = [\dot{e}, v]$, where $v \triangleq \dot{u}$. Thus, the Hamiltonian function is

$$H = q_1 e^2 + q_2 \frac{(V_h - v_r + e)^4 u^2}{R_0^2} + \left(\frac{V_h - v_r + e}{R_0} v \right)^2 + \lambda_1 [b(-V_h + v_r - e)u + \beta + \delta] + \lambda_2 v. \tag{7.25}$$

Solving the algebraic equation

$$\left.\frac{\partial H(e,v,\lambda_1,\lambda_2)}{\partial v}\right|_{v=v^*}=0,$$

the optimal $v^*(x,\lambda)$ is

$$v^*=\frac{-\lambda_2}{2}\left(\frac{R_0}{V_h-v_r+e}\right)^2,$$

which gives the optimal Hamiltonian expression

$$H^*(e,\lambda_1,\lambda_2)=q_1e^2+q_2\frac{(V_h-v_r+e)^4u^2}{R_0^2}-\frac{\lambda_2^2R_0^2}{2(V_h-v_r+e)^2}+\lambda_1[b(v_r-V_h-e)u+\beta+\delta]. \tag{7.26}$$

The optimal solution is associated with the set of differential equations:

$$\frac{\partial H^*}{\partial\lambda_1}=b(v_r-V_h-e)u+\beta+\delta=\dot{e} \tag{7.27}$$

$$\frac{\partial H^*}{\partial\lambda_2}=\frac{-\lambda_2}{2}\left(\frac{R_0}{V_h-v_r+e}\right)^2=\dot{u}=v \tag{7.28}$$

$$\frac{\partial H^*}{\partial e}=2q_1e+4q_2\frac{(V_h-v_r+e)^3}{R_0^2}u^2+\frac{(\lambda_2R_0)^2}{2(V_h-v_r+e)^3}-bu\lambda_1-\beta\lambda_1=-\dot{\lambda}_1 \tag{7.29}$$

$$\frac{\partial H^*}{\partial u}=\frac{2q_2u(V_h-v_r+e)^4}{R_0^2}+b\lambda_1(v_r-V_h-e)=-\dot{\lambda}_2 \tag{7.30}$$

with the boundary conditions,

$$e(0)=v_r-v_c(0) \tag{7.31}$$

$$e(\tau)=0 \tag{7.32}$$

$$u(0)=\text{number of transistors switched on in } t=0. \tag{7.33}$$

$$u(\tau)=\text{number of transistors switched on in } t=\tau. \tag{7.34}$$

and, the transversality condition

$$H^*(\tau)=0. \tag{7.35}$$

Note that, this is a nonlinear Boundary Value Problem (BVP) with a transversality condition, since the final time τ is unknown.

Solving (7.27)–(7.35), yields e^*, from which, the optimal voltage evolution $v_c^*=v_r-e^*$ can be derived. This evolution can be employed as reference for the controllers developed in Section 7.2.

Numerical solution

The problem raised before: finding a solution for (7.27)–(7.35) with (7.31)–(7.34) and (7.35), is a complex problem because it is a nonlinear BVP with a four dimensional character and it has a transversality condition. For this, a numerical solution is proposed. Nevertheless, finding this numerical solution is also an involved task. There is not so many tools that cope with this kind of problems. In this case the Matlab function'bvp4c' has been employed. Function bvp4c [130] combines the solution of Initial Value Problem (IVP) for Ordinary Differential Equations (ODEs) and the solution of algebraic equations, being a non-shooting code. The nonlinear algebraic equations are solved iteratively by linearization, providing an initial guess over a mesh and taking into account the boundary conditions. This is due to the fact that can have more than one solution and, thus, a guess for the desired solution must be provided by designers, which includes an initial mesh for this desired solution.

Function bvp4c controls the error of the numerical solution and adapts the mesh in every iteration to obtain an accurate numerical solution with a modest number of mesh points. Thus, obtaining an 'residual' error is common. If the residual error is small, then the solution provided by function bvp4c is a good solution.

Function bvp4c is not directly applicable for the present problem since it cannot handle the transversality condition. Thus, this function has been used iteratively in order to obtain a solution that fulfills condition (7.35). The system parameters given in Section 7.2 are reported. Furthermore, it is considered the rising transient period, i.e, when output voltage goes from the low voltage level to the high voltage level. Therefore, the next boundary conditions are selected:

$$e(0) = v_r - v_c(0) \tag{7.36}$$
$$e(\tau) = 0 \tag{7.37}$$
$$u(0) = 1 \tag{7.38}$$
$$u(\tau) = N \tag{7.39}$$

The following values for the weighting constants are chosen[1],

$$q_1 = 0.64 \tag{7.40}$$
$$q_2 = 0.32. \tag{7.41}$$

Using as initial guess

$$\begin{aligned} e(t) &= 0.3e^{-10^8 t} \\ u(t) &= 24 - 23e^{-10^8 t} \\ \lambda_1(t) &= 10^6 t + 10^5 \\ \lambda_2(t) &= -3.2 \cdot 10^7 t^2 - 3.2 \cdot 10^7 t + 100, \end{aligned}$$

[1] As usual in optimal control problems, they have been chosen in a trial-and-error procedure, checking by simulations the solutions obtained.

Note that this initial guess has a complex form and, because it has been difficult to obtain. As mentioned before, this problem is a complex problem, and finding a solution has been very involved. However, with the future numerical methods, it is expected that new tools for this kind of problem will be researched and developed.

The nonlinear BVP (7.27)–(7.30) with the specified boundary conditions (7.36)–(7.39) reaches the numerical solution shown in Fig. 7.15. Note that, the boundary conditions in e^* and u^* are satisfied when $\tau = 23.3 \cdot 10^{-9} s$. From e^*, the optimal evolution of the voltage reference v^* can be obtained.

Figure 7.16 shows the evolution of H^*, whose value at $\tau = 23.3 \cdot 10^{-9} s$ is close to zero, fulfilling the transversality condition.

Notice that, this voltage reference has been computed for the rising transient period. For the falling transient period, a similar procedure can be applied.

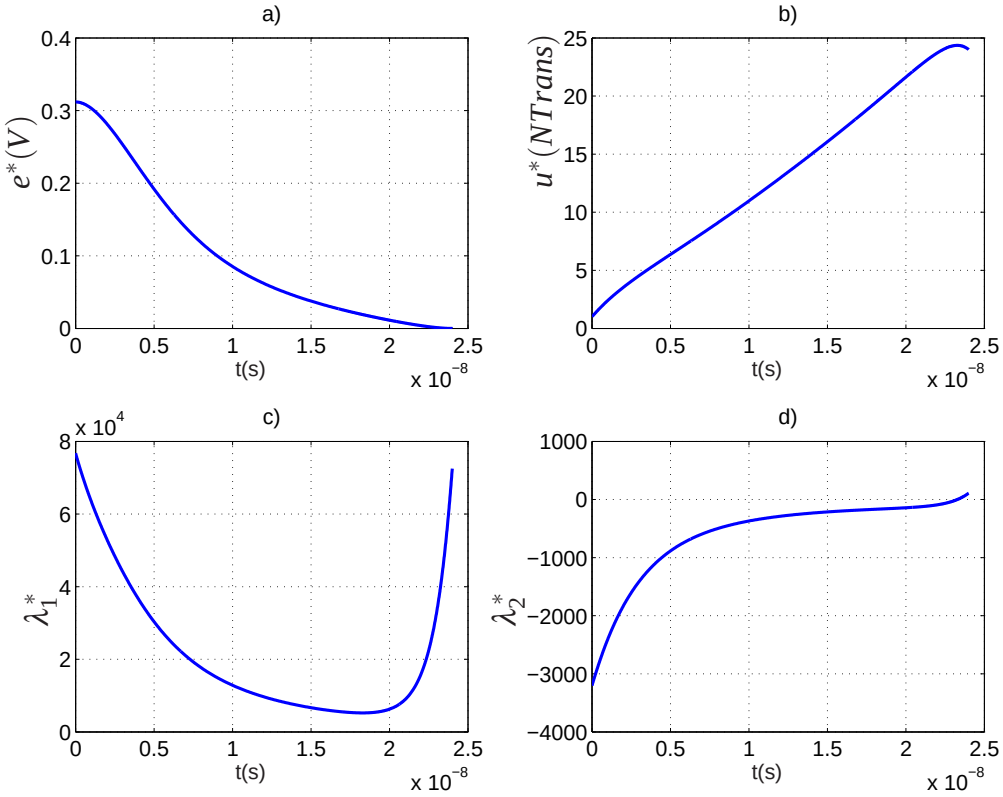


Figure 7.15: Optimal numerical solution. a) error evolution, b) control evolution, c) λ_1 evolution and d) λ_2 evolution.

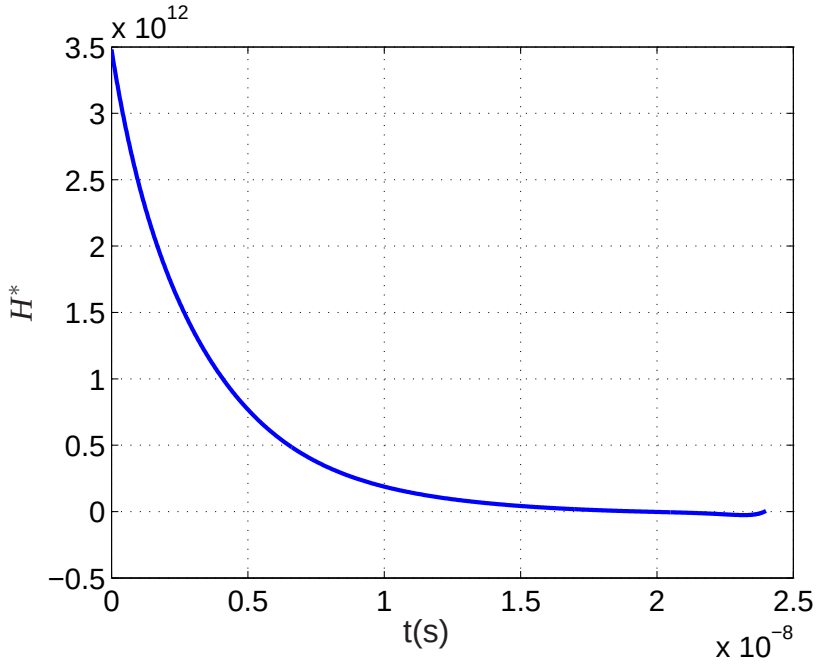


Figure 7.16: H^* evolution.

7.4.2 Adaptive feedback control design

The Lyapunov's controller (Section 7.2) has been designed under the assumption that the parameter β is known. In this section, an adaptive law is proposed in order to cope with the case when the load parameter β is unknown.

Let us denote $\hat{\beta}$ as the estimated value for the load parameter. This estimated parameter will be used in control law (7.21) instead of its real value. The application of this law to system (7.8) yields

$$\dot{e} = -\beta e + \beta v_r - \hat{\beta} v_r. \tag{7.42}$$

Let us assume that β is a constant parameter which involves $\dot{\beta} = 0$ (the case when β is time-varying will be discussed in next section) and define

$$\tilde{\beta} = \beta - \hat{\beta}, \quad \dot{\tilde{\beta}} = -\dot{\hat{\beta}}.$$

For the adaptive control system, the next Lyapunov function candidate is proposed

$$W = \frac{e^2}{2} + \frac{\tilde{\beta}^2}{2\gamma_1}, \tag{7.43}$$

where γ_1 is a positive design parameter that may define the adaptation speed.

Differentiating W with respect to time, yields

$$\dot{W} = -\beta e^2 + \tilde{\beta}\left(v_r e + \frac{\dot{\tilde{\beta}}}{\gamma_1}\right).$$

Note that $\beta > 0$, as has been seen above. The adaptive law is designed by canceling the term in brackets, i.e.:

$$\dot{\hat{\beta}} = -\dot{\tilde{\beta}} = \gamma_1 v_r e. \tag{7.44}$$

This achieves $\dot{W} = -\beta e^2$.

Asymptotic stability is established by LaSalle's invariance principle [76]. For this, consider the level set $W_c = W(e, \tilde{\beta}) \leq c_0$ for sufficiently large $c_0 > 0$, where $\dot{W} \leq 0$. This set is compact and positively invariant.

Note that $\dot{W} = 0$ on $e = 0$. Furthermore, note from Eq. (7.42), that

$$e(t) \equiv 0 \quad \Rightarrow \quad \dot{e}(t) \equiv 0 \quad \Rightarrow \quad \tilde{\beta}(t) \equiv 0.$$

Therefore, the maximum invariant set in W_c with $\dot{W} = 0$ corresponds to the single point $P_1 = (e = 0, \tilde{\beta} = 0)$, thus, every solution starting in W_c approaches the desired point P_1 as $t \to \infty$.

7.5 Simulation of the advanced Lyapunov's controller

In this section, some simulations using the parameter presented in Section 7.4 are performed.

The resulting controller (7.22) is

$$u_k = \text{sat}_1^N \text{round}\left\{\frac{\hat{\beta} T_s v_{r_k}^* + v_{r_k}^* - v_{r_{k-1}}^* + \delta T_s}{b T_s (V_h + e_k - v_{r_k}^*)}\right\} \tag{7.45}$$

where $v_{r_k}^*$ and $v_{r_{k-1}}^*$ comes from the discretization of the optimal voltage reference, which has been previously obtained. For implementation, the values of $v_{r_k}^*$ can be stored in a table. In the same way, $\hat{\beta}$ is adapted by the discrete-time approximation of the adaptation law (7.44):

$$\tilde{\beta}_k = \tilde{\beta}_{k-1} - T_s \gamma_1 v_{r_k}^* e_k$$

The data reported in Section 7.2 are used in the simulations. In order to perform more realistic tests, a more precise model for the load is considered in such a way that β depends on r_L, i.e., it is time-varying. The bounds on β are: $\beta_{min} = 1.38 \cdot 10^7$ for $v_c = V_l$ and $\beta_{max} = 5.9 \cdot 10^7$ for $v_c = V_h$. As initial estimated values is taken: $\hat{\beta} = 0$.

Figure 7.17 shows the closed-loop performance by employing the optimal voltage reference and the adaptation mechanism. Note that when the adaptation mechanism is implemented the system can achieve a similar performance to the case of known load. Although, the adaptive control introduces a delay in the system response, small current peaks and faster transient periods are obtained.

In addition, thanks to the obtained voltage reference the energy consumption is reduced. The accumulated dissipated energy in the rising transient period is $4.8\mu J$ using the Lyapunov controller (Eq. (7.22)) and $0.5\mu J$ using the advanced Lyapunov controller (Eq. (7.45)). That means 90% energy saving. Likewise, the transient period is reduced to $23.3ns$.

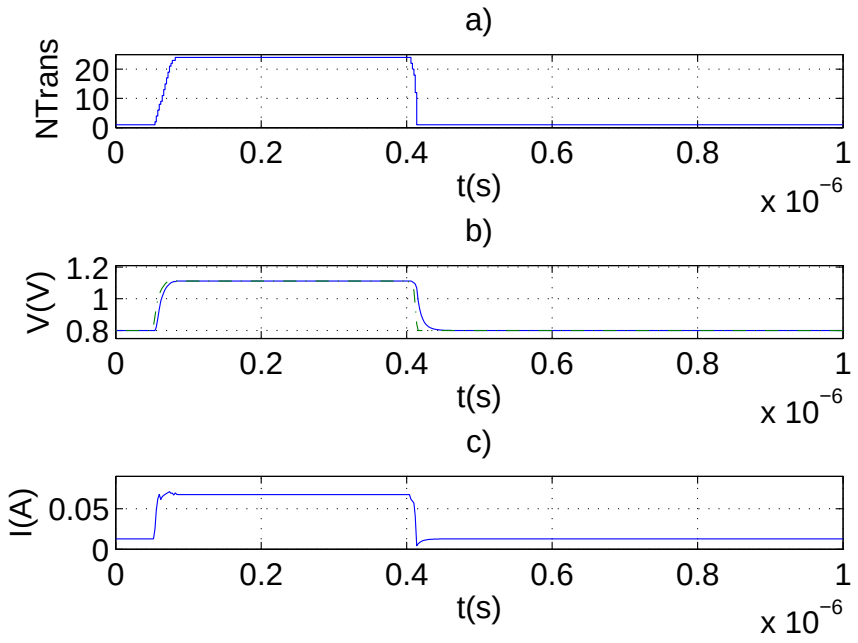


Figure 7.17: Vdd-Hopping with control (7.45) and adaptation $\hat{\beta}$. Evolution of a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid) and c) current I_l.

The adaptation of the load resistive component β is shown in Fig. 7.18. Note that β approaches its real value, in spite of the fact that β is time-varying. Observe that the time-evolutions of $\hat{\beta}$ and β are superimposed.

Consequently, the reliability and efficiency of the controller (7.45), which uses the optimal voltage reference and the adaptation mechanism, has been validated. Besides, the fact,

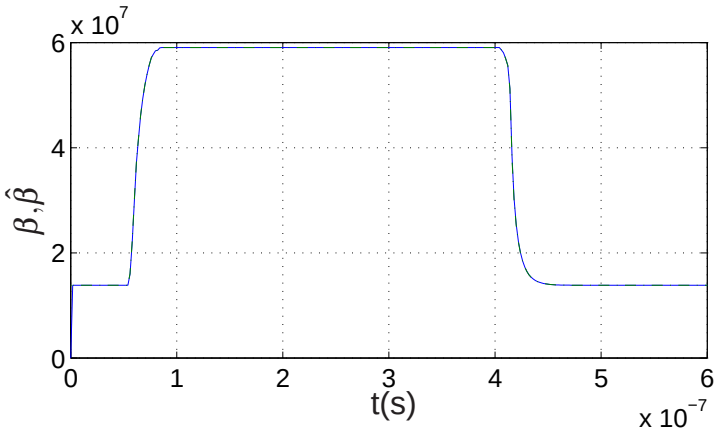


Figure 7.18: Time-evolution of $\hat{\beta}$ (solid) and β (dashed).

that there exists a time-varying load resistive component is not relevant for the right system performance. In addition, this controller has a small energy consumption as well as small current peaks and faster transient-periods.

7.6 Conclusion

In this work, a set of controllers has been designed for a Vdd-Hopping converter. Most of these controllers improve performance over the one used in [99] in terms of transient responses, as has been seen in Section 10.5. This controller is a very simple controller with a strong limitation: only one transistor can be switched on or off in every sampling time. The good results obtained with the set of controllers developed in this chapter come from applying control theory as well as the possibility to let such controllers to switch more than one transistor at once.

In a performance evaluation presented in Section 10.5 to the set of controllers, it has been concluded that the best one seems to be Lyapunov's controller. This is not only for a better signal performance but also for a better energy consumption. Nevertheless, this controller can be enhanced, if both optimal and adaptive control are developed. These control approaches allow to diminish energy consumption and current peaks and deal with unknown load parameters, respectively.

A method to obtain an optimal reference has been developed applying optimal control theory [80, 86, 155]. Nevertheless, the problem stated for this method presents a high complexity, because it is a BVP with transversally condition for a 4^{th}-order optimal problem. Hence, that an optimal reference has been computed from of this problem. This numerical solution has been obtained using the Matlab function bvp4c. It has been a involved task, and

it is expected that new mathematic tools will be developed to make easier to compute this voltage reference. This result achieves a reduction of current peaks and 90% energy saving with respect to the previous Lyapunov controller. This fact makes that the total energy saving with respect to the intuitive controller used in [99] is 93% reduction.

In addition, an adaptive strategy is developed in order to deal with the load modeling error. Moreover, in order to prove the reliability of this adaptive controller, it has been introduced by simulation that parameter β is time-varying, as is common in practice.

The suited performance of the results in the Vdd-Hopping converter has been shown by simulations.

In summary, an advanced controller which does not need knowledge of the load resistive parameter has been obtained. This controller reduces energy consumption as well as current peaks and transient-periods. Nevertheless, it presents a more complex physic implementation, since it requires more computational blocks.

Next chapter, a new controller will be developed to cover this drawback, at the same time that all nice achieved properties are maintained.

Chapter 8

Energy-aware controller for the Vdd-Hopping converter

In the previous chapter a set of high-performance controller has been designed for the DC-DC Vdd-Hopping converter. From the set of controllers, the one that provides a better performance has been selected and some developments have been done to fulfill with low-power technology requirements. Nevertheless, it presents some number of computational blocks, what can be translated in a complex implementation in certain industrial applications, as in the ARAVIS project. That is why the controller with presents the less number the computational blocks from the set of controller proposed before is chosen and enhanced in order to accomplish all control objectives. It is based on a PI structure [84, 120].

From this controller, an optimal nonlinear energy-aware controller is obtained. The proposed solution is a discrete-time control mechanism, which does not need to track any time-indexed voltage reference. This control law only needs to know the set-point. As an important innovation, the proposed a control introduces a saturation with time-varying limits, which reduces the current peaks. These facts involve an important diminishing of energy consumption. Moreover, its computing cost have been reduced. It is patented under the name of ENergy-AwaRe Control (ENARC) [6].

In the ARAVIS project, this controller will be simulated in VHDL-AMS. In addition, it is expected that it is implemented in the innovated 45nm or/and 36nm SoC developed in ARAVIS.

8.1 Control design without current-peak managing

In this section, a controller based on linear control theory is designed to cope with possible steady-state errors [105]. The relevant characteristic of this controller is that presents a relative low number of computational blocks. This makes it interesting in industry. Previously, it has been enhanced assuming that more than one transistor is switched at once and, dealing with a tracking problem. Now, let us consider a stabilization point problem. Therefore, the reference will be constant, i.e., a step. This looks for making faster transient periods. Nevertheless, important current peaks can be generated being able to damage the system.

The 'linear control' proposed in Section 7.2 (Eq. (7.10)) has been:

$$u_k = \text{sat}_1^N \{\text{round}(K_1 e + K_2 \sigma)\}, \tag{8.1}$$

where σ corresponds to $\int_t^{t+T_s} e dt$, which can be considered as a new variable that augmentes the system dimension. Constants K_1 and K_2 are chosen with the tunning mechanism (7.11)–(7.12).

Figure 8.1 shows a simulation to display the stability properties of this control law. The data reported in Section 7.2 are employed in this simulation. The time-varying reference is changed by a step reference, what makes to obtain faster transient periods. Nevertheless, the constant reference generates a no-desired important current-peak (as has been predicted before), which may increase the dissipated energy as well as can damage the physical system. Note that this current peak is not symmetric when system is falling down. It is due to the current definition (Eq. (7.1) in Section 7.1). Observe that current variable directly depends on the number of PMOS transistors switched on, u_k, that is, smaller current for lower voltage.

8.2 Control redesign with current-peak managing

The controller presented before is modified in order to achieve a high-performance from a point of view of current-peaks. Current-peaks can be managed by introducing a pre-specified maximum admissible current-peak constraint, e.g., introducing an on-line saturation mechanism. This current-peak constraint is defined in the Vdd-Hopping system by $\Delta I_{l_{max}}$.

In Section 7.4, an expression that relates the current variation with the number of transistor switched on or off in every sampling time has been given. In order to make easier the reading, this expression is here advocated

$$\Delta I_l = \frac{V_h - v_c}{R_0} \Delta u_k. \tag{8.2}$$

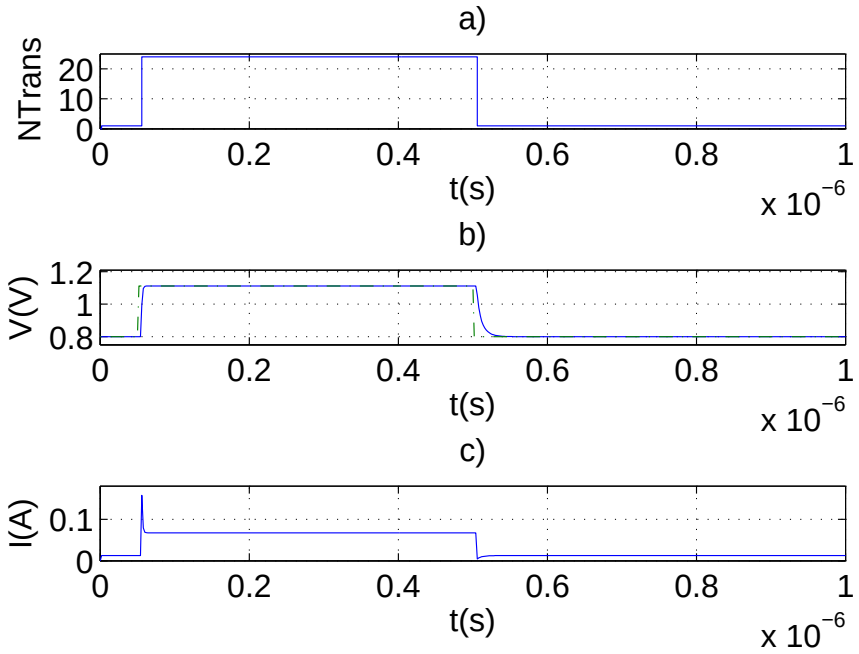


Figure 8.1: Control (8.1) with step reference. Evolution of a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid) and c) current I_l.

It comes from the discrete property of the Vdd-Hopping converter, while that its core voltage is a continuous-time variable, as is seen in [99].

Assume that a maximum admissible current variation for Eq. (8.2) is defined as $\Delta I_{l_{max}}$, in such a way that

$$\Delta I_{l_{max}} \leq \frac{V_h - v_c}{R_0} \Delta u_k \leq \Delta I_{l_{max}}. \tag{8.3}$$

This constraint can be introduced in the system by saturating the maximum and minimum PMOS transistors that can be switched on or off and every sampling time, i.e., the maximum in minimum admissible Δu_k are

$$\Delta u_k^M = \frac{R_0}{V_h - v_c} \Delta I_{l_{max}} \triangleq \alpha_k^M \tag{8.4}$$

$$\Delta u_k^m = -\frac{R_0}{V_h - v_c} \Delta I_{l_{max}} \triangleq \alpha_k^m, \tag{8.5}$$

being $\alpha_k^M > 0$ and $\alpha_k^m < 0$. Note that the saturation limits depends on the output voltage. Thus, control (8.1) is modified in order to consider current-peaks

$$u_k = \text{sat}_1^N \left\{ \text{round}(\text{sat}_{\bar{\alpha}_k^m}^{\bar{\alpha}_k^M} (K_1 e + K_2 \sigma)) \right\}, \tag{8.6}$$

where the current-peak constraints are employed according to next expressions:

$$\bar{\alpha}_k^M \triangleq u_{k-1} + \alpha_k^M \tag{8.7}$$
$$\bar{\alpha}_k^m \triangleq u_{k-1} + \alpha_k^m. \tag{8.8}$$

Remark 8.1 *The current peak constraint must allow to switch, at least, one transistor in order to guarantee that the system achieves the desired voltage level. Therefore, the admissible current peak constraint has to be larger than a minimum bound guaranteeing this condition. From Eq.* (8.3)*, it can be obtained*

$$\Delta I_{l_{max}} \geq \frac{V_{c_h} - V_{low}}{R_0} \min(\Delta u_k) = \frac{V_{c_h} - V_{low}}{R_0} 1$$

where $\min(\Delta u_k)$ *is the minimum number of PMOS transistors that can be switched on or off in every sampling time. As* u_k *is determined by a rounding function, the minimum of* (Δu_k) *must be larger or equal than* 1 *in order to have that the constraint* $\Delta I_{l_{max}}$ *allows switching at least one transistor.*

The aware management of the current-peaks makes Control (8.6) to be an innovated controller for the Vdd-Hopping converter. As a side effect, an important reduction of the dissipated energy is achieved by means of a trade-off between faster transient period and small current-peak as will be shown below. The optimization of the energy dissipation is a crucial point in the miniaturization of microsystems.

8.2.1 Time discretization

Usually, the controllers are implemented in discrete-time. That is why control (8.6) is approximately discretized, yielding the structure

$$u_k = sat_1^N \left\{ u_{k-1} + \text{round}(\text{sat}_{\alpha_k^m}^{\alpha_k^M}(\bar{K}_1 \Delta e_k + \bar{K}_2 e_k)) \right\}, \tag{8.9}$$

where $\bar{K}_1$ and $\bar{K}_2$ follows the transformation given in (7.14)–(7.15) in Section 7.2, and where α_k^m and α_k^M are given in Eqs. (8.4)–(8.5).

This controller is patent pending under the name of ENergy-AwaRe Controller (ENARC) [6].

The structure of the ENARC controller is shown in Fig. 8.2. This controller is composed of:

- two gains, $\bar{K_1}$ and $\bar{K_2}$, adjusted by a tuning method given by Eqs (7.11)–(7.12), in such a way that asymptotic stability of the equilibrium of the closed-loop system is guaranteed. The stability will be analyzed in Chapter 9.

- A current limit mechanism, that computes on-line the maximum and minimum number of PMOS transistors switched in every sampling time, Δu_k^M and Δu_k^m, respectively. The limits over the switched-transistor variation are necessary in order to ensure that a maximum admissible current peak $\Delta I_{l_{max}}$ is respected.

- A saturation mechanism that limits the maximum and minimum switched-transistor variation computed before.

- A rounding for digital control signal and

- an output saturation mechanism, that limits the minimum and maximum PMOS transistor number switched on at every sampling time.

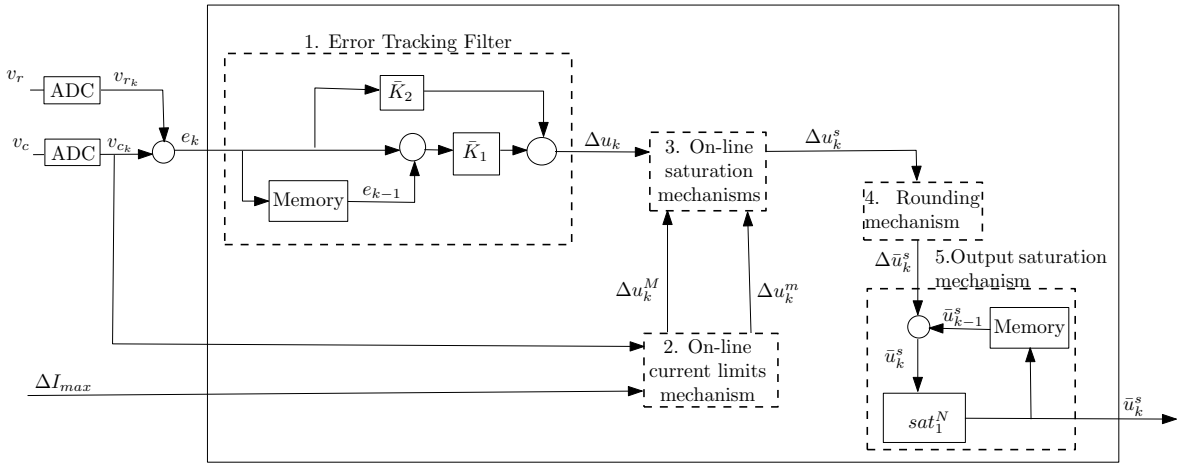


Figure 8.2: ENARC structure patented in [6].

8.2.2 Simulation of ENARC controller in the Vdd-Hopping system

Now, some simulations are performed to display system signal evolutions. The reference signal is a step, as has been chosen in Section 8.1. For implementation, some values of α_k^m and α_k^M can be stored in a table. For this, the reported parameter values from Section 7.2 are chosen. Consequently, from Eqs. (7.14)–(7.15) and Eqs. (7.11)–(7.12)

$$\bar{K_1} = -19.3 \tag{8.10}$$

$$\bar{K_2} = 39.27. \tag{8.11}$$

The maximum admissible current peak constraint is chosen according to the equation given in Remark 8.1

$$\Delta I_l = \frac{V_{c_h} - V_l}{R_0} 0.6.$$

Figure 8.3 shows a simulation of the resultant closed-loop system with Eq.(8.9). Note, that the system response obtains faster transient period and reduces considerably the current peak with respect to the previous controller (see Fig. 8.1).

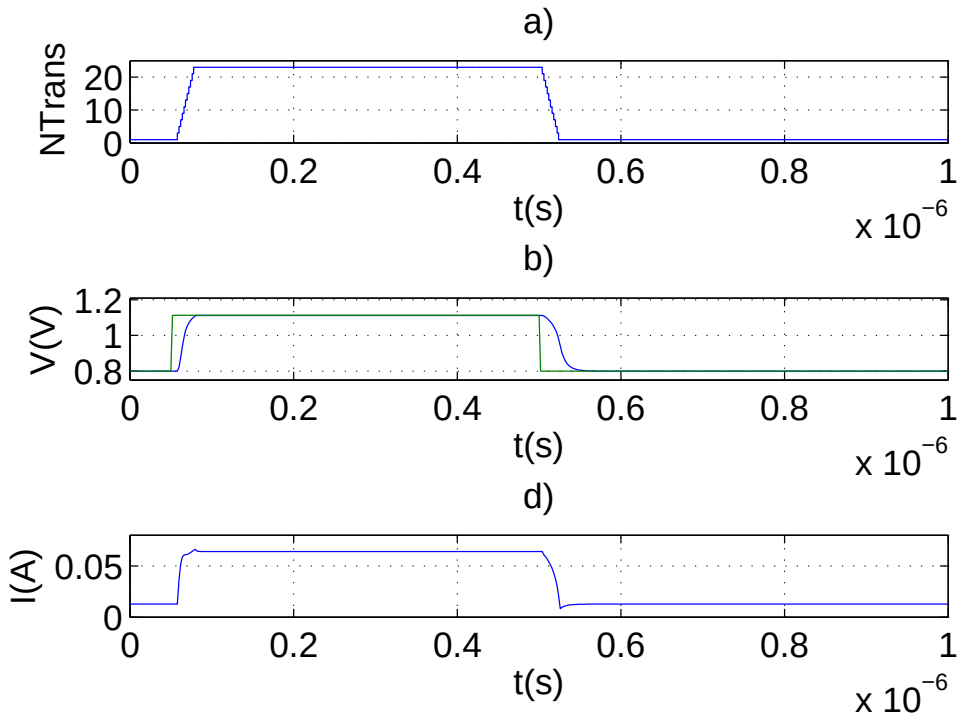


Figure 8.3: ENARC with step reference. Evolution of the: a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid), c) current. I_l.

Energy-consumption evaluation.

Now, let us discuss the main objective concerning to the controller: the energy consumption.

The cumulated dissipated energy in the set of PMOS during the rising transient time depends on the type of control law employed, and thus, on the switching sequence. Remember that in the control structure published in [99] only one transistor can be switched at each sampling time and a ramp reference has been employed. However, with the ENARC controller more than one transistor may be switched in every sampling-time and a step reference

has been employed. The energy consumption during the rising transient time has been reduced from $7.2\mu J$ (with the control published in [99]) to $0.26\mu J$ (with ENARC), i.e., 96% reduction.

The energy consumption is much higher using the 'intuitive' controller than using the ENARC controller. Note, thus that, a non-smooth behavior of the current signal and a larger transient time may result in a higher energy consumption.

8.3 Conclusions

In this chapter, some important advances have been developed for the 'linear controller' (Controller No.1, in Section 7.2) proposed for the Vdd-Hopping system. The 'linear controller' has a relevant interest due to its simple implementation, since it requires a relative low number of computational blocks.

A nonlinear discrete-time controller has been designed for the Vdd-Hopping system with the aim of reducing the dissipated energy. This controller has an energy-aware management of current-peaks in the set of PMOS transistors. In addition, a step reference has been used, thus, it only needs to know the two desired voltage levels. This result comes from the possibility to control more than one transistor at once, i.e., to switch more than one transistor in a same sampling time. As a side effect the transient-periods are diminished. This controller has been compared with the 'intuitive' control used in [99]. In this context, the ENARC controller reduces the energy consumption a 96%.

The ENARC controller does not only have the same properties that the high-performance Lyapunov controller developed in Chapter 7; but it also has a simple implementation. And thus, it may present special interest for industrial applications in the fields of microelectronics.

This mechanism is an innovative controller for the discrete Vdd-Hopping converter applied in the ARAVIS project. It is focused on achieving the project global objective.

The features that have not yet been studied are the presence of delay as well as parameter uncertainty, which will be taken into account in Chapter 10. In addition, the closed-loop stability of Vdd-Hopping with ENARC will be studied in next chapter.

Chapter 9

Approximate stability analysis of the DC-DC Vdd-Hopping converter

In Chapter 8, a controller has been developed based on a linear structure. This is a nonlinear discrete-time energy-aware controller called ENARC, which may fulfill most of the specific control objectives for the Vdd-Hopping converter, mentioned in Chapter 6. Among them its low computational cost can be highlighted. This characteristic makes it attractive for industrial applications [17, 84, 120]. However, in that chapter, the equilibrium stability of the system with the ENARC has been not studied. Therefore, the convergence and stability of the equilibrium of the closed-loop Vdd-Hopping is not reliable.

This chapter focuses on studying the stability of the nonlinear system (7.7) with the ENARC controller developed in Chapter 8. As Vdd-Hopping model is continuous, the stability analysis is performed in continuous-time, assuming that the ENARC stability property is ensured through its continuous-time version (this continuous-time version of the ENARC has been presented in control (8.6)). This is a very common assumption [71, 152].

For simplicity, a preliminary equilibrium stability analysis of the closed-loop system is studied when the controller does not consider the current peak issues. This controller has been the 'linear controller' presented in Section 7.2 (Eq. (7.10)). Then, a stability analysis is performed when control (8.6) is employed. This controller introduces a type of nonlinearity: a saturation with dynamic limits. This fact makes that the nonlinear closed-loop system works in three operating-modes: non-saturated system, saturated system in the upper limit and saturated system in the lower limit. It is seen that the equilibrium is in non-saturated mode. The stability analysis is based on LaSalle's invariance principle [76].

The stability analysis presented here is not rigorous because it is based on some system approximations in continuous time. The complexity of the discrete system with the ENARC

does not allow to find another simple way to prove the global stability.

9.1 Stability with control (7.10)

In this section, a stability analysis is performed for the nonlinear model (7.7) of the Vdd-Hopping converter with control (7.10) developed in Section 8.1. For simplicity, the saturation that limits the number of the PMOS transistors switched on as well as the rounding function are disregarded. This analysis is based on LaSalle's invariance principle [76].

To help the reading of the thesis, the equation of the control is recalled,

$$u_k = K_1 e + K_2 \sigma \tag{9.1}$$

Remember that $\sigma = \int_t^{t+T_s} e dt$ and the control parameters K_1 and K_2 are constant and chosen according to the tuning mechanism (7.11)–(7.12) described in Chapter 7. These tuning equations depend on a design parameter ξ. The following lemma deals with tuning the parameter ξ, such that, K_1 and K_2 have certain desired properties.

Lemma 9.1 *Consider the interval*

$$I = \left[\frac{u_{k_l} b + \beta}{2\omega_n}, \qquad \frac{u_{k_l} b + \beta}{2\omega_n} + \frac{\omega_n}{2(b u_{k_h} + \beta)} \right].$$

If ξ is chosen in I, then the following inequalities are satisfied

$$K_1 > 0 \quad \text{and} \quad K_1 (b u_{k_h} + \beta) - K_2 < 0,$$

where u_{k_h} is the upper-bound of u_k, i.e., $u_{k_h} = N$.

Notice that $K_2 > 0$ from Eq. (7.12).

Remark 9.2 *The term*

$$\frac{\omega_n}{2(b u_{k_h} + \beta)}$$

is always positive from the parameter properties given in Section 7.1, thus it is clear that the interval I is not empty. Then, there is always a possibility to find the suitable values for the control parameters K_1 and K_2.

Assume that the tuning of these control parameters is achieved according to the previous rules. The next step concerns the stability analysis of the closed-loop system. The following theorem establishes the global stability of system (7.7) under the control law given in (9.1).

Theorem 9.3 *Consider system (7.7) with the controller (9.1). Then, if K_1 and K_2 are positive, the equilibrium of the system is globally stable.*

Proof: From the dynamics of system (7.7), its equilibrium satisfies the equation

$$0 = (v_r - V_h)b\bar{u_k} + \beta v_r + \delta.$$

Thus, an expression of the control input at the equilibrium is straightforwardly obtained:

$$\bar{u_k} = \frac{\beta v_r + \delta}{(V_h - v_r)b} = K_2\bar{\sigma}, \tag{9.2}$$

where $\bar{v_c}$ and $\bar{\sigma}$ are the equilibrium values of v_c and σ, respectively. Note that $\bar{u_k}$ corresponds to the saturation bounds 1 and N when the set point is the lower and higher values, respectively, as has been defined in Remark 7.3. Now, the new variable w_k, which represents the difference between the control u_k considered at any position and at the equilibrium, is introduced:

$$w_k \triangleq u_k - \bar{u_k}. \tag{9.3}$$

Rewriting the dynamic of system (7.7) using this new variable, yields:

$$\dot{e} = -(\beta + bu_k)e + (v_r - V_h)bw_k + (v_r - V_h)b\bar{u_k} + \beta v_r + \delta, \tag{9.4}$$

Substituting the expression of $\bar{u_k}$ from (9.2) into the right-hand side of (9.4), the following equation is obtained

$$\dot{e} = -(\beta + bu_k)e + (v_r - V_h)bw_k.$$

According to the assumption of the theorem, the control constant K_2 is positive. Moreover, from Section 7.1, the positivity of β and b is guaranteed. Since the control u_k is equal to $\text{sat}_1^N\{\text{round}(K_1e + K_2\sigma)\}$, it is clear that u_k is positive and consequently so is $\beta + bu_k + K_2$.

The next step of the proof is based on the Lyapunov's theorem. Consider the Lyapunov function candidate of the form:

$$V(e,\sigma) = \frac{e^2}{2b(V_h - v_r)} + \frac{(\sigma - \bar{\sigma})^2}{2}K_2,$$

Notice that, the reference voltage v_r is constant. From the system properties, the high voltage V_h is greater than the reference voltage v_r. As has been seen just before, b is positive. Thus, V is indeed a positive definite function of e and σ.

Thanks to (9.1) and (9.2), V can be expressed as follows

$$V(e,\sigma) = \frac{e^2}{2b(V_h - v_r)} + \frac{(u_k - \bar{u_k} - K_1e)^2}{2K_2}. \tag{9.5}$$

The differentiation of the function V along the trajectories of (9.1) leads to

$$\dot{V} = -\frac{(\beta + b(\bar{u_k} + w_k))e^2}{b(V_h - v_r)} - K_1 e^2 + \frac{1}{K_2}\left[(K_1\dot{e} + K_2 e) - (K_1\dot{e} + K_2 e)\right] \cdot \left[(K_1 e + K_2\sigma) - K_2\bar{\sigma} - K_1 e\right].$$

Introducing $(-K_1e^2 + K_1e^2)$ in the previous equality and assuming that the differentiation of $\dot{u}_k$ from Eq. (9.1) is

$$\dot{u}_k = K_1\dot{e} + K_2 e.$$

Then, the differatation of the function can be expressed as:

$$\dot{V} = -\left(\frac{(\beta + b(\bar{u_k} + w_k))}{b(V_h - v_r)} + K_1\right)e^2. \tag{9.6}$$

Note that K_1 and K_2 have been assumed positive, and $u_k = \bar{u_k} + w_k$ is assumed be positive, thus,

$$V(e,\sigma) \geq 0$$
$$\dot{V}(e,\sigma) \leq 0.$$

Asymptotic stability is established by LaSalle's invariance principle [76]. For this, consider the level set $\Omega_1 = V(e,\sigma) \leq c_1$ for sufficiently large $c_1 > 0$. This set is compact and positively invariant. This is represented in Fig, 9.1.

From Eq. (9.6), notice that $\dot{V}(e,\sigma)$ is negative everywhere, except on the line $e = 0$, where $\dot{V}(e,\sigma) = 0$. Unless $\sigma = \bar{\sigma}$, this is impossible from the closed-loop system (7.7) with control (9.1), since

$$e(t) \equiv 0 \quad \Rightarrow \quad \dot{e}(t) \equiv 0 \quad \Rightarrow \quad 0 \equiv -(v_r - V_h)bK_2\sigma + \beta v_r + \delta.$$

The last equation is satisfied in

$$\sigma \equiv \frac{v_r + \delta}{(V_h - v_r)bK_2} = \bar{\sigma}.$$

Consequently, the maximum invariant set in Ω_1 with $\dot{V}(e,\sigma) = 0$ corresponds to the single point $P_2 = (e = 0, \sigma = \bar{\sigma})$. Therefore, every solution starting in Ω_1 approaches P_2 as $t \to \infty$.

■

In summary, the global stability of the Vd-Hopping with Eq. (9.1) has been established. In next section, this result will be employed to analyze the global stability with control (8.6).

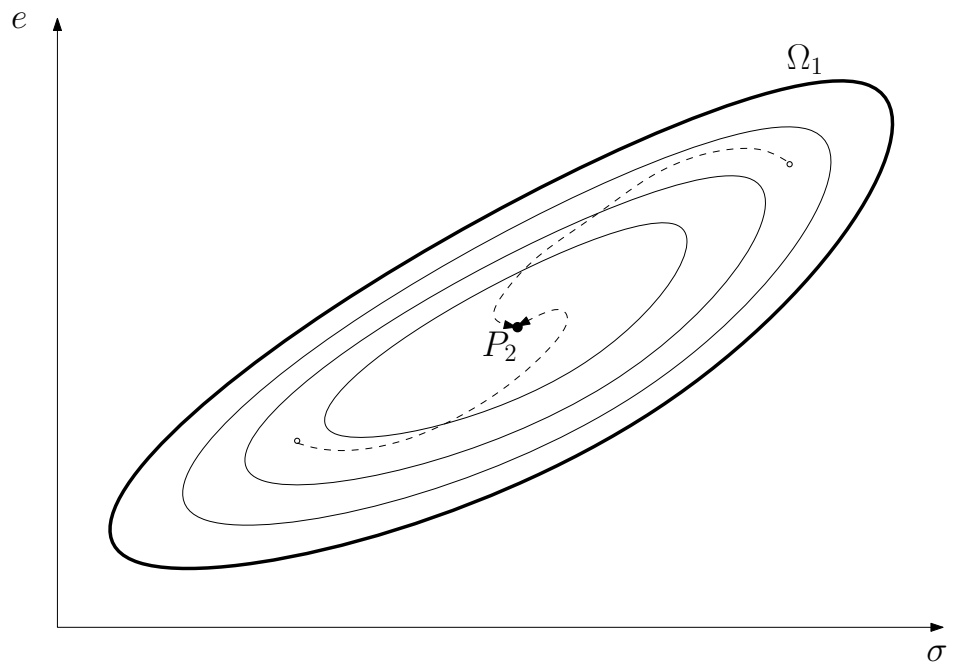


Figure 9.1: Representation of the compact set Ω_1.

9.2 Stability with control (8.6)

Based on the previous study, the objective of this section is to extend the proof before to control (8.6). Note that, it is the continuous-time version of the ENARC controller, and it is nonlinear due to control saturations. Here, the saturation that limits the number of the PMOS transistors switched on as well as the rounding function are also disregarded for simplicity reasons. An added difficulty is that the limits of the saturations depend on the state e.

The equation of control (8.6) is expressed here, to make easier the reading:

$$u_k = \text{sat}_{\bar{\alpha}_k^m}^{\bar{\alpha}_k^M}(K_1 e + K_2 \sigma), \tag{9.7}$$

with

$$\bar{\alpha}_k^M = u_{k-1} + \alpha_k^M = u_{k-1} + \frac{R_0}{V_h - v_c}\Delta I_{l_{max}} \tag{9.8}$$

$$\bar{\alpha}_k^m = u_{k-1} + \alpha_k^m = u_{k-1} - \frac{R_0}{V_h - v_c}\Delta I_{l_{max}}, \tag{9.9}$$

as has been defined in Eqs. (8.4)–(8.5) and Eqs. (8.7)–(8.8). The stability analysis comes from dividing the space (e, σ) in three regions (see Fig 9.2):

- **Region I**, where the system does not saturates.

- **Region II**, where the system saturates in the upper limit.
- **Region III**, where the system saturates in the lower limit.

Remark 9.4 *The equilibrium of system (7.7), i.e., $u_k = \bar{u_k}$, is in Region I.*

This is easy to see from Eq.(9.2) and Eqs. (9.8)–(9.9):

$$\bar{u_k} = \text{sat}_{K_2\bar{\sigma}-\frac{R_0}{V_h-v_c}\Delta I_{max}}^{K_2\bar{\sigma}+\frac{R_0}{V_h-v_c}\Delta I_{max}}(K_2\bar{\sigma}),$$

Notice that $V_h - v_c$ and R_0 are positive as it has been defined in Section 7.2 and that ΔI_{max} is also positive according to Section 8.2. Then, $\frac{R_0}{V_h-v_c}\Delta I_{max} > 0$.

The proof will be defined in two parts. In the first part, convergence to the non-saturated region in finite time will be proven. In the second part, convergence to the desired point, once the system is in Region I is proven.

For the first part, two properties are performed for the saturated cases (Region II and III), which define the convergence to the non-saturated region (Region I). These properties are based on the variable $\dot{u}_k$, since it is directly affected by the saturation limits: $\alpha_k^m(e)$ and $\alpha_k^M(e)$.

Assumption 9.5 *For system* (7.8) *with a suited sampling time, next expression in continuous-time can be taken into account*

$$\dot{u}_k = sat_{\bar{\alpha}_k^m}^{\bar{\alpha}_k^M}(K_1\dot{e} + K_2 e). \tag{9.10}$$

Equation before comes from Eq. (9.7) and Eqs. (9.8)–(9.9)

Firstly, next property is defined for Region II:

Property 9.6 *In Region II, if K_1 is constant and positive, system (7.7) satisfies*

- $\dot{u}_k > \alpha_k^M(e) > 0$
- $\ddot{u}_k \leq \varepsilon_M < 0 \quad being \quad \varepsilon_m \triangleq \frac{K_1\Delta I_{max}}{C} = constant$
- $e > 0$

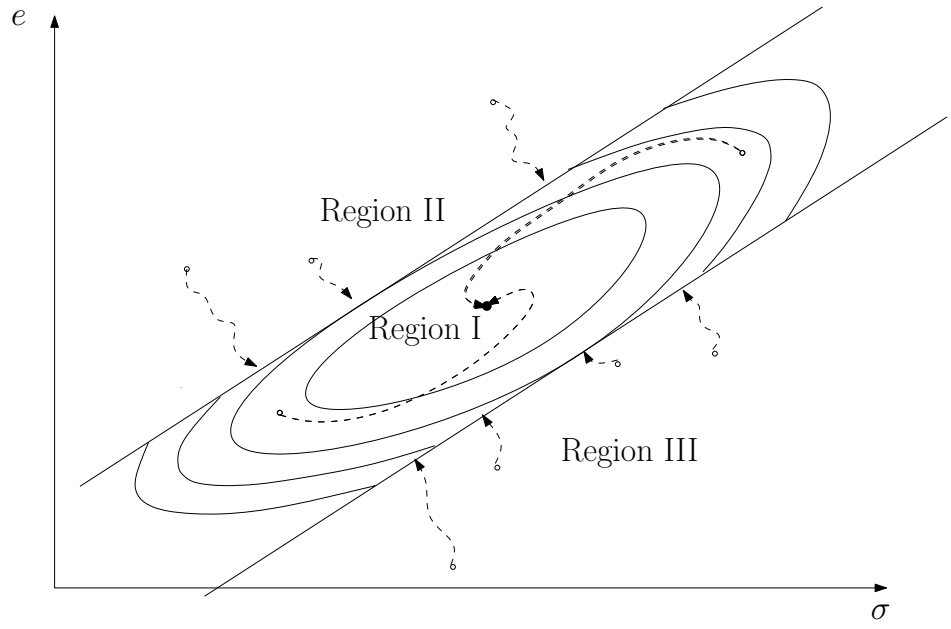


Figure 9.2: Representation of the system operating regions.

where $\alpha_k^M(e)$ is defined by Eq. (9.8) and $v_c \triangleq v_r - e$ (as has been seen in Section 7.1). Besides, ε_M comes from differentiating $\dot{u}_k$ and employing the definition of $\alpha_k^M(e)$ from Eq. (9.8). Parameters C and ΔI_{max} are positive according to Section 7.2 and Section 8.2, respectively.

Remark 9.7 *$\dot{u}_k$ is decreasing with time derivative that is bounded away from zero, as is shown in Property 9.6, and hence it will reach $\alpha_k^M(e)$ (see Eq. 9.8) in finite time.*

Secondly, the following property is defined for Region III:

Property 9.8 *In Region III, if K_1 is constant and positive, system (7.7) satisfies*

- $\dot{u}_k < \alpha_k^m(e) < 0$
- $\ddot{u}_k \geq \varepsilon_m > 0 \quad being \quad \varepsilon_m \triangleq \frac{K_1 \Delta I_{max}}{C} = constant$
- $e < 0$

where $\alpha_k^m(e)$ is defined by Eq. (9.9) and $v_c \triangleq v_r - e$ (as has been seen in Section 7.1). Besides, ε_m comes from differentiating $\dot{u}_k$ and employing the definition of $\alpha_k^m(e)$ from Eq. (9.9). Parameters C and ΔI_{max} are positive according to Section 7.2 and Section 8.2, respectively.

Remark 9.9 *$\dot{u}_k$ is creasing, with time derivative that is bounded away from zero, as is shown in Property 9.8, and hence it will reach $\alpha_k^m(e)$ (see Eq. 9.9) in finite time.*

These properties and remarks about the different regions allow to prove the convergence of variable $\dot{u}_k$ to the saturation limits. For this, next lemma can be stated

Lemma 9.10 *If the next conditions are satisfied:*

$$K_1 > 0, \quad K_2 > 0 \quad \textit{and} \quad K_1(bu_{k_h} + \beta) - K_2 < 0,$$

and taking into account the Assumption 9.5 then, system (7.7) with controller (9.7) saturated in the upper or lower saturation limit converges to the non-saturation region in a finite time.

Proof: Firstly, Region II (see Fig.9.3) is studied, i.e., the case when system saturates in the upper saturation limit.

Employing $\dot{u}_k$ which is affected directly by $\alpha_k^M(e)$, as has been seen in Eq. (9.10). It is desired to prove that:

$$\dot{u}_k \rightarrow \alpha_k^M(e)$$

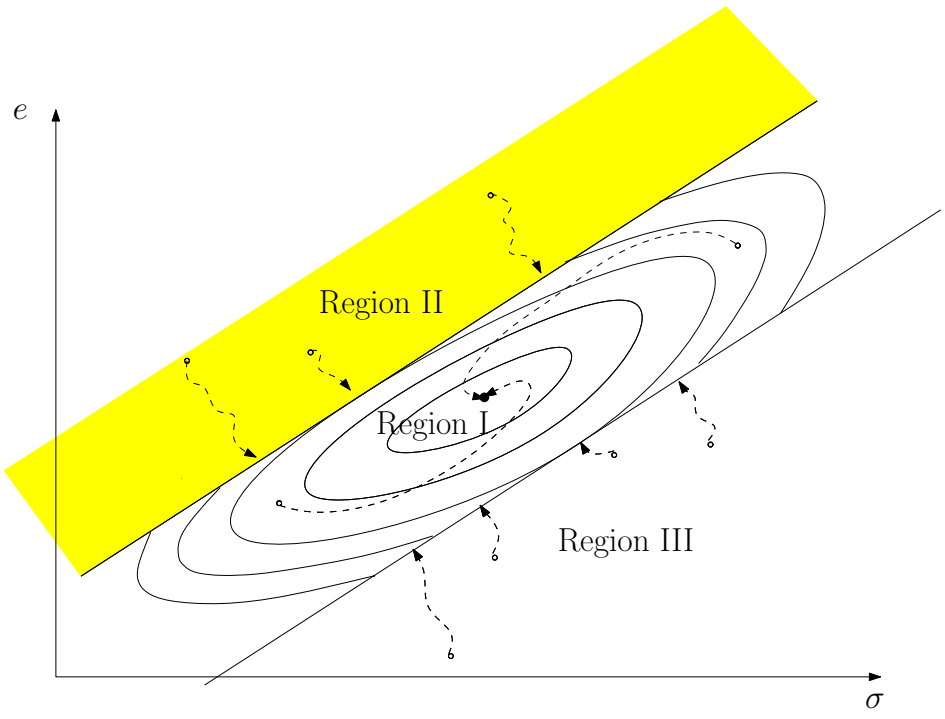


Figure 9.3: Region II in the representation of the system operating regions.

For this, the following Lyapunov function candidate is selected:

$$W = \dot{u}_k - \alpha_k^M(e) = K_1\dot{e} + K_2 e - \alpha_k^M(e) > 0.$$

Differentiating

$$\dot{W} = K_1\ddot{e} + K_2\dot{e} + \frac{\alpha_k^M(e)}{(V_h - v_r + e)}\dot{e}.$$

Next up, from Eq. (8.4), $\alpha_k^M(e)$ is differentiated

$$\dot{W} = -b(V_h - v_c)K_1\dot{u}_k + \left(-K_1(bu_k + \beta) + K_2 + \frac{\alpha_k^M(e)}{V_h - v_r + e}\right)\dot{e}. \tag{9.11}$$

Note that b and $(V_h - v_c)$ are positive from Section 7.2. Besides, from the statement the positivity of K_1 is also established. And Property 9.6 maintains $\dot{u}_k > 0$ in this region. Therefore, the first term on the right-hand side is negative for every time instant. For simplicity, this first term is defined as

$$\varsigma(e) \triangleq b(V_h - v_c)K_1\dot{u}_k > 0. \tag{9.12}$$

Rewriting Eq. (9.11), such that the next inequalities are satisfied

$$\begin{aligned}
\dot{W} &= -\varsigma(e) + \left(-K_1(bu_k + \beta) + K_2 + \frac{\alpha_k(e)}{V_h - v_r + e}\right)\dot{e} \\
&< -\varsigma(e) + \left(K_1(bu_k + \beta) - K_2 - \frac{\alpha_k(e)}{V_h - v_r + e}\right)\frac{K_2 e}{K_1} \\
&< -\varsigma(e) + \left(K_1(bu_{k_h} + \beta) - K_2 - \frac{\alpha_k(e)}{V_h - v_r + e}\right)\frac{K_2 e}{K_1} \\
&< 0.
\end{aligned}$$

The first inequality comes from applying $\dot{u}_k = K_1\dot{e} + K_2 e > 0$, thus $-\dot{e} < \frac{K_2 e}{K_1}$. Furthermore, form Property 9.6, it is known that $e < 0$. A maximum bound of u_k, u_{k_h}, is taken in the second inequality.

From Lemma 9.10, $K_1(bu_{k_h} + \beta) - K_2 < 0$ is fulfilled, then the last inequality is satisfied

$$\dot{W} < 0.$$

In addition, from Property 9.6, it is ensured that $\dot{u}_k$ converges to the boundary.

The proof for Region III (see Fig. 9.4) is symmetric to the one developed before for Region II, applying Property 9.8. ■

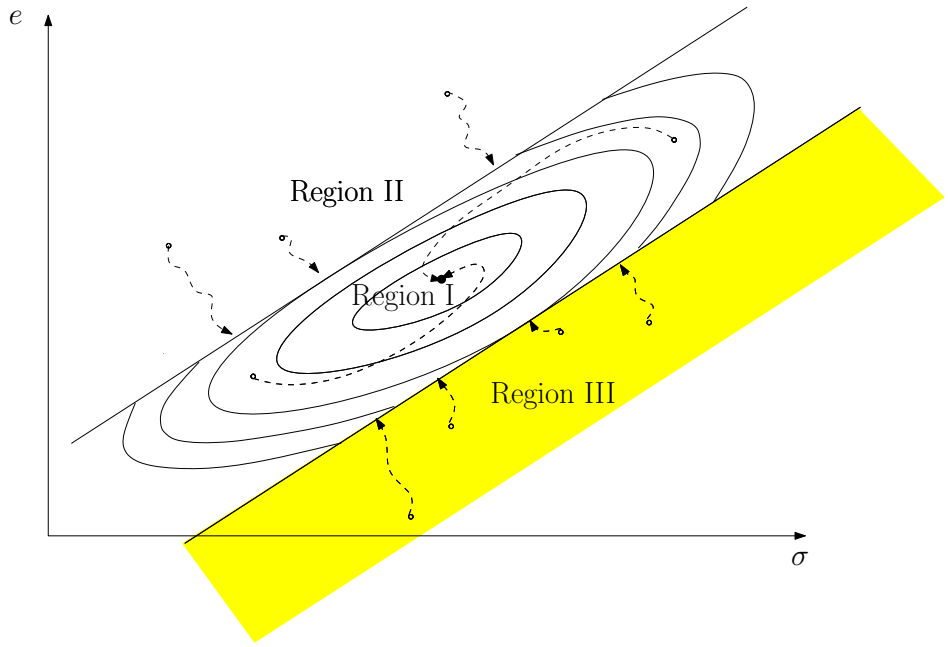


Figure 9.4: Region III in the representation of the system operating regions.

Finally, from the lemma stated before about the convergence of the saturated region to the non-saturated region, the equilibrium localization given in Remark 9.4 and the global stability property of the Region I established in Theorem 9.3, next theorem ensures the global stability property of the system (7.7) with controller (9.7).

Theorem 9.11 *If K_1 and K_2 are positive, and $K_1(bu_{k_h}+\beta)-K_2<0$, then the equilibrium of system (7.7) with controller (9.7) is globally stable.*

Proof: There exist two state space regions corresponding to the case when system saturates in the upper limit (Region II), and when the system saturates in the lower limit (Region III). By Lemma 9.10, the system operating in Region II or III converges to the non-saturated region (Region I) in finite time. In addition, Properties 9.6 and 9.8 guarantee that the system once is in Region I can not cross this saturation lines towards Regions II or III.

Now, the proof is concluded by using the assumptions K_1 and K_2 that are constant and positive, $K_1(bu_{k_h}+\beta)-K_2<0$ and by advocating the La Salle's invariance principle. There exists a set Ω_2 limited by the level curve $V(e,\sigma)=c_1$ for sufficiently large c_1 and the saturation limits, which is compact and positively invariant. Figure 9.5 represents the set Ω_2. From Lemma 9.10 the state of the system reaches Ω_2 in finite time.

As has been seen in Section 9.1, the maximum invariant set with $\dot{V}(e,\sigma)=0$ corresponds to the single point $P_2=(e=0,\sigma=\bar{\sigma})$. LaSalle principle establishes that every system evolution in Ω_2 approaches P_2 as $t\to\infty$.

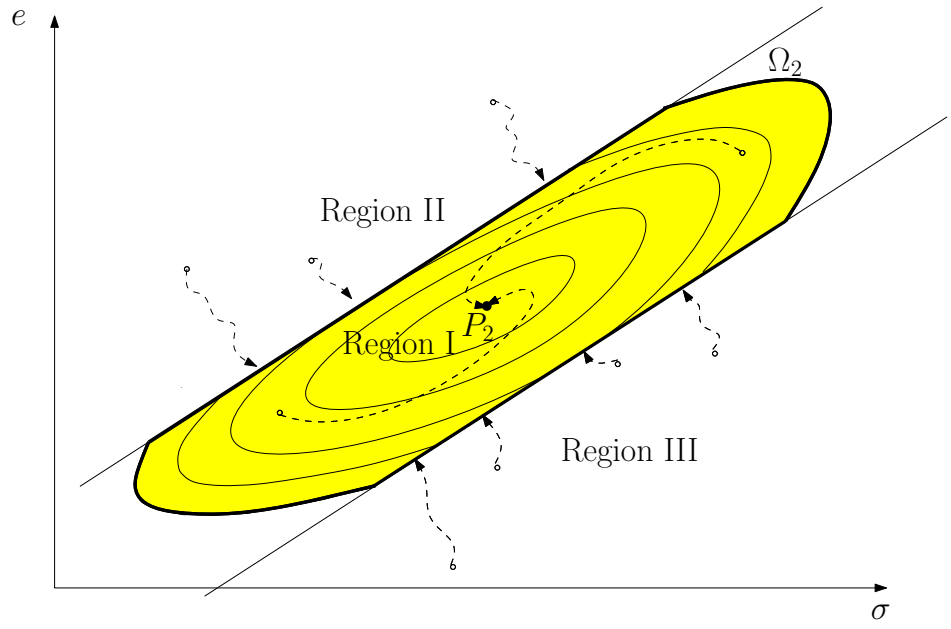


Figure 9.5: Representation of the invariant set Ω_2.

■

9.3 Conclusions

In this chapter the equilibrium stability of the nonlinear Vdd-Hopping system when control (9.1) has been analyzed . This controller does not manage the occurrence of current peak in the system. The proof of this stability analysis has been based on LaSalle's invariance principle.

Next up, the analysis has been extended to prove equilibrium stability with the innovative nonlinear controller (9.7). This controller manages current peaks through saturations. The saturation limits depends on the system state, making difficult to prove global stability. The rigorous global stability analysis deals with three operating modes: no saturated, saturated in the upper limit and saturated in the lower limit. It has been ensured that the equilibrium is located in the non-saturated mode. When system is saturated, it will converge to the non-saturated mode in finite time without being able to return to the non-saturated case. This analysis follows LaSalle's invariance principle for a domain bounded by Lyapunov level and the saturation lines.

The analysis presented here has been performed for a continuous-time version of the ENARC controller. It has been assumed that the stability property is maintained for the discrete-time ENARC controller. This kind of assumptions is very common in control theory

[71, 152].

The only control objectives that have not yet been considered is the equilibrium robustness in view of delays presence and parameter uncertainties that the system can suffer. These issues will be seen in Chapter 10.

Chapter 10

Sub-optimal control considering delays and parameter uncertainties

In Chapter 8, an energy-aware controller has been designed for the Vdd-Hopping converter. This converter satisfies control requirements for this low-power converter implemented in the ARAVIS project context. Furthermore, in Chapter 9 a stability analysis of the equilibrium has been performed. In order to cover all control requirements specified in Chapter 6, this chapter focuses on system robustness with respect to delays and parameter uncertainties in the Vdd-Hopping system at the same time that the stability is guaranteed. They are common issues in SoC [112, 140].

Figure 10.1 shows Vdd-Hopping mechanism including delays. The system has a computational h_2-sample-period delay at the control block input required to ensure that the system is synchronized with the cluster clock [77]. Likewise, there is a computational h_1-sample-period delay associated with computational issues in the control block output. The size of this last delay depends on a trade-off between power consumption and performance. Generally, the power consumption can be reduced if the local core voltage or/and the clock frequency are decreased. However, this fact produces that the computational speed diminishes, in such a way that the size of the existing delay decreases. Therefore, the h_1-sample-period delay depends on the local clock frequency[1] [38]. In many cases, applications do not require the full computational power at any time. The performance requirement is that the task is performed before a deadline. Therefore, it is possible to have a low frequency, which ensures system performance, and hence, to allow reducing the power consumption. On the other hand, there is a minimum required local clock frequency that guaranties the critical path (longest path delay) on the corresponding clock domain circuit [45]. That is why, a low frequency of $200MHz$ is taken here, for the local clock. This frequency introduces an one-sample-period delay in the control block output. In some cases, it is considered that the delays are fixed and

[1] The higher the clock frequency is, the longer the delay is.

known.

The other relevant issue in low-power technology are the parameter uncertainties, which can generate a non-desirable performance and lack of reliability of the system [34, 93].

In summary, delays presence and parameter uncertainties must be considered in the design of the controller.

The control design procedure given in Lemma 9.1 provides a range of values for parameter ξ that guarantees equilibrium asymptotic stability for system (7.7) for fixed parameters. This stability analysis has been performed in Chapter 9. Although this tuning method deals with the current peak management, it does not consider that some system parameters may be uncertain. Likewise, perturbation rejection and delays were not considered either.

In order to ensure the robustness of the Vdd-Hopping converter with respect to uncertain parameters and delays presence, a 'conservative' sub-optimal tuning approach for $\bar{K_1}$ and $\bar{K_2}$ is now developed for an approximate ENARC controller version that, for simplicity, disregards the current peak management. For this, the system is rewritten into a suitable state-space form to formulate a robust H_∞ problem that can be solved by using Lyapunov-Krasovskii theory [53, 62]. In this process, the saturation in the controller is considered [26, 50]. The designed controller guarantees asymptotic stability, disturbance rejection as well as robustness of the system with respect to delays and uncertain parameters. The problem is expressed in terms of Linear Matrix Inequalities (LMIs). Likewise, an attraction domain is estimated in such a way that a regional stabilization for the saturated control is guaranteed.

The robustness properties of the closed-loop system with the sub-optimal control tuning design applied to the ENARC controller are tested by simulations. In these simulations is taken into account that the load dynamic parameter is not constant R_L, but is time-varying r_L, as mentioned in Chapter 7. Remember that for control purposes, it has been taken as constant in Section 7.1.

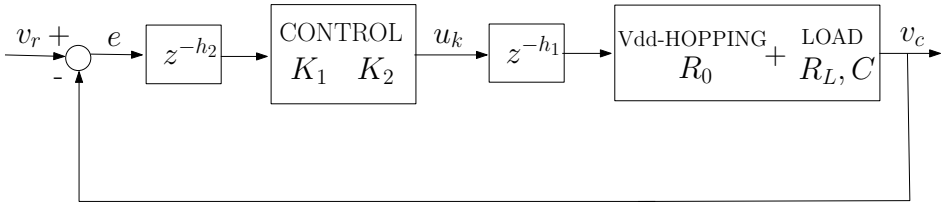


Figure 10.1: Sub-optimal control tuning for the ENARC controller.

An evaluation of the two control tuning approaches developed in this part of the thesis for the ENARC controller is performed.

10.1 Problem statement

In this section, we are going to formulate the problem rewriting the system (7.8) in an approximate discrete-time form considering both delays and uncertain parameters. This approximate time-discretization is performed by using forward euler method [104], by assuming that the sampling time is small enough to the system evolution. Likewise, for simplicity, an approximate version of the ENARC controller is taken.

From Fig. 10.1, note that h_1 and h_2 are the number of sampling periods in the input and in the output of the control block, respectively. Taking this notation and considering a small sampling period, T_s, the associated approximated discrete-time voltage error equation after employing forward Euler method is

$$e_{k+1} = (1 - T_s\beta)e_k + T_s b(v_r - V_h)u_{k-h_1} + T_s(\beta v_r + \delta) - bT_s u_{k-h_1} e_k. \tag{10.1}$$

Remember that the sampling frequency takes the clock frequency value, $T_s = \frac{1}{\omega_n}$.

Considering the state $x_k = [e_k \quad e_{k-1}]^T$, the applied control law is

$$u_{k-h_1} = \text{sat}_1^N\{u_{k-1-h_1} + Kx_{k-h}\}, \tag{10.2}$$

where $h \triangleq h_1 + h_2$ and $K = [\overline{K_1} \quad \overline{K_2}]$.

The parameters R_L, R_0 and C that correspond to β, b and δ and ω_n that defines the T_s in model (10.1), can be considered uncertain. Each uncertain parameter is within an uncertainty interval, whose corresponding extremes are

- $u_k \in [u_{k_l} = 1, u_{k_h} = N]$,
- $R_L \in [R_L^m, R_L^M]$,
- $R_0 \in [R_0^m, R_0^M]$,
- $T_s \in [T_s^m, T_s^M]$.

Remark 10.1 *The asymptotic stability of system (10.1) is guaranteed in a point within an uncertainty interval for the low level voltage, $\mathscr{I}_l$, and within an uncertainty interval for the high level voltage, $\mathscr{I}_h$, bounded by*

$$\mathscr{I}_l \triangleq \left[\frac{R_L^m(u_{k_l}V_h - R_0^M K_{leak})}{u_{k_l}R_L^m + R_0^M}, \quad \frac{R_L^m(u_{k_l}V_h - R_0^m K_{leak})}{u_{k_l}R_L^m + R_0^m}\right] \tag{10.3}$$

$$\mathscr{I}_h \triangleq \left[\frac{R_L^M(u_{k_h}V_h - R_0^M K_{leak})}{u_{k_h}R_L^M + R_0^M}, \quad \frac{R_L^M(u_{k_h}V_h - R_0^m K_{leak})}{u_{k_h}R_L^M + R_0^m}\right]. \tag{10.4}$$

Other added problem is that the system can suffer some exogenous disturbances.

Consequently, the main objective is to find the optimal gain K in such away that Control (10.2) is robust with respect to delays as well as parameter uncertainties. Likewise, this optimal K must guarantee asymptotic stability and disturbance rejection for the known constant delays, h_1 and h_2.

10.1.1 Alternative representation for the saturated control (10.2) and the error equation (10.1)

Firstly, some lemmas are given to rewrite the saturated control (10.2) and an alternative form.

Lemma 10.2 *[67], for x_k in $\mathscr{R}^n$, assume that there exist $K, G \in \mathscr{R}^{1\times n}$ such that $1 < u_{k-1-h_1} + Gx_{k-h} < N$, then*

$$sat_1^N \{u_{k-1-h_1} + Kx_{k-h}\} \in Co\left\{\alpha^{(m)}(u_{k-1-h_1} + Kx_{k-h}) + (1-\alpha^{(m)})(u_{k-1-h_1} + Gx_{k-h}), \quad m = 1,2,\right\}.$$

Lemma 10.3 *Assume that there exists $G \in \mathscr{R}^{1\times n}$, P_1[2] $> 0 \in \mathscr{R}^{n\times n}$ and $c > 0$ such that for any $x_k \in \mathfrak{X}$, where*

$$\mathfrak{X} = \left\{x_k : x_k^T P_1 x_k \leq c^{-1}\right\},$$

then, $1 < u_{k-1-h_1} + Gx_{k-h} < N$, and Control (10.2) admits the following representation

$$\begin{aligned} u_{k-h_1} &= \sum_{m=1}^{2} \lambda_{mk}\left[(\alpha^{(m)}(u_{k-1-h_1} + Kx_{k-h}) + (1-\alpha^{(m)})(u_{k-1-h_1} + Gx_{k-h})\right] \\ &= \sum_{m=1}^{2} \lambda_{mk}\left[u_{k-1-h_1} + \alpha^{(m)}Kx_{k-h} + (1-\alpha^{(m)})Gx_{k-h})\right], \end{aligned}$$

being $\sum_{m=1}^{2} \lambda_{mk} = 1$, with $\lambda_{mk} \geq 0$, for all $k > 0$.

Then, defining

$$\Omega_\alpha \triangleq \sum_{m=1}^{2} \lambda_{mk}\alpha^{(m)}, \quad \text{for} \quad \text{all} \quad 0 \leq \lambda_{mk} \leq 1, \quad \sum_{m=1}^{2} \lambda_{mk} = 1$$

where the vertices of the polytope are given by $\alpha^{(m)}$, Eq. (10.1) can be rewritten

$$\begin{aligned} e_{k+1} = (1 - T_s\beta)e_k + T_s b(v_r - V_h)(u_{k-1-h_1} + \alpha^{(m)}Kx_{k-h} \\ +(1-\alpha^{(m)})Gx_{k-h}) + T_s(\beta v_r + \delta) - bT_s u_{k-1-h_1} e_k \end{aligned} \tag{10.5}$$

for $m = 1,2$.

[2] P_1 is a positive matrix defined to guarante system stability.

10.1.2 State-space representation

The saturated control and error equation, as redefined before, allow to system (10.1) rewrite it in a state-space form. For this, an expression for the dynamic part of the controller, u_{k-1-h_1}, is obtained.

Next expression is achieved from (10.1)

$$u_{k-h_1} = \frac{e_{k+1} - (1 - T_s\beta)e_k - T_s(\beta v_r + \delta) + bT_s u_{k-h_1} e_k}{T_s b(v_r - V_h)},$$

and it is delayed one sampling period

$$u_{k-1-h_1} = \frac{e_k - (1 - T_s\beta)e_{k-1} - T_s(\beta v_r + \delta) + bT_s u_{k-1-h_1} e_{k-1}}{T_s b(v_r - V_h)}. \tag{10.6}$$

Now, Eq. (10.6) is applied to (10.5) obtaining

$$\begin{aligned} e_{k+1} = {} & (2 - T_s\beta)e_k - (1 - T_s\beta)e_{k-1} + T_s b(v_r - V_h)(\alpha^{(m)}K + (1 - \alpha^{(m)})G)x_{k-h} \\ & -T_s b(u_{k-h_1} e_k - u_{k-1-h_1} e_{k-1}), \qquad m = 1, 2. \end{aligned} \tag{10.7}$$

This can be rewritten in the following matrix form:

$$x_{k+1} = A(u_{k-h_1}, u_{k-1-h_1})x_k + B\bar{u}_{k-h}^{(m)} \quad m = 1, 2, \tag{10.8}$$

where

$$A = \begin{bmatrix} 2 - T_s\beta - T_s b u_{k-h_1} & T_s\beta - 1 + T_s b u_{k-1-h_1} \\ 1 & 0 \end{bmatrix},$$

$$B = \begin{bmatrix} T_s b(v_r - V_h) \\ 0 \end{bmatrix},$$

being $\bar{u}_{k-h}^{(m)} = (\alpha^{(m)}K + (1 - \alpha^{(m)})G)x_{k-h}$ for $m = 1, 2$, with $\alpha^{(m)} = [0, 1]$. u_{k-h_1} and u_{k-1-h_1} are treated as uncertain parameters, whose values will be inside the uncertainty interval $[1, N]$.

10.1.3 Stability and disturbance rejection problem

Equation (10.8) can be rewritten in the following explicit closed-loop form with an $\mathscr{L}_2$ perturbation added, in such a way that a H_∞ problem can be formulated.

$$x_{k+1} = Ax_k + B(\alpha^{(m)}K + (1 - \alpha^{(m)})G)x_{k-h} + B_w w_k \quad m = 1, 2, \tag{10.9}$$

$$x_l = \phi_l, \quad \forall l \in [-h, 0] \tag{10.10}$$

$$z_k = I_2 x_k, \tag{10.11}$$

with

$$B_w = \begin{bmatrix} b_{w_1 1} & b_{w_1 2} \\ b_{w_2 1} & b_{w_2 2} \end{bmatrix},$$

where $x_k, z_k, w_k \in \mathscr{R}^n$ are the state vector, controlled output and exogenous disturbance input, respectively. ϕ_k is the initial condition and $h \geq 0 \in \mathscr{R}$ is a fixed and known delay. Moreover,

Problem 10.4 *The problem is to find a $\mathfrak{X}(P_1, c)$, a vector G and K such that,*

a) Lemma 10.3 holds and, hence, the closed-loop system (10.8) *and*

b) there exists a Lyapunov-Krasovskii functional $V_k > 0$, such that $V_{k+1} - V_k$ along the solution of (10.9) *fulfills*

$$V_{k+1} - V_k < 0, \tag{10.12}$$

when the system is not perturbed, and for any perturbation input, there exists a minimum disturbance attenuation, $\gamma^* \geq 0$, such that, for all $\gamma \geq \gamma^*$ the $\mathscr{L}_2$ gain between the perturbation vector w_k, and the output vector z_k is less or equal to γ. i.e.

$$\begin{aligned} &\|z_k\|_2^2 - \gamma^2 \|w_k\|_2^2 < 0, \quad \forall w_k \in \mathscr{L}_2 \\ &for \quad \phi_l = 0, \quad -h \leq l \leq 0. \end{aligned} \tag{10.13}$$

The solution to this problem guarantees the system stability as well as the disturbance rejection for the time-delay system (10.9)–(10.11).

10.2 H_∞ control design

In order to cope with this problem a mathematical manipulation of Eq. (10.9) is performed via a descriptor model transformation [51]. The descriptor approach is just a variable change, which makes easier to work with Lyapunov-Krasovskii functional [52].

10.2.1 Descriptor model transformation

Equation (10.9) is manipulated in order to achieve the previous objectives. For this, a descriptor model transformation is applied.

Considering:

$$y_k \triangleq x_{k+1} - x_k, \quad \psi_k \triangleq \sum_{i=k-h}^{k-1} y_i.$$

Next, Eq. (10.9) is rewritten in the descriptor form [51]:

$$\begin{bmatrix} x_{k+1} \\ 0 \end{bmatrix} = \begin{bmatrix} y_k + x_k \\ -y_k + Ax_k - x_k + B(\alpha^{(m)}K + (1-\alpha^{(m)})G)x_k + B_w w_k \end{bmatrix}, \quad m = 1,2.$$

From $x_{k-h} = x_k - \psi_k$, this system can be compactly written as:

$$E\bar{x}_{k+1} = \bar{A}\bar{x}_k - \begin{bmatrix} 0 \\ B(\alpha^{(m)}K + (1-\alpha^{(m)})G) \end{bmatrix} \psi_k + \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_k, \quad m = 1,2, \tag{10.14}$$

where

$$\bar{A} \triangleq \begin{bmatrix} I_2 & I_2 \\ A + B(\alpha^{(m)}K + (1-\alpha^{(m)})G) - I_2 & -I_2 \end{bmatrix}, \quad E \triangleq \text{diag}\{I_2, 0\}, \quad \bar{x_k} \triangleq \begin{bmatrix} x_k \\ y_k \end{bmatrix},$$

$m = 1,2$.

10.2.2 Condition for state-space representation

Firstly, the condition a) of the Problem 10.4 is dealt with. From [49], it is seen that, in order to guarantee $1 < u^{(i)}_{k-1-h_1} + Gx_{k-h} < N$, for $i = 1,2$, where $u^{(i)}_{k-1-h_1} = \{1, N\}\ \forall x \in \mathfrak{X}$ given in (10.3), it is necessary that next equations are satisfied

$$2N \geq N(1 + cx^T_{k-h}P_1x_{k-h}) \geq 2(u^{(i)}_{k-1-h_1} + Gx_{k-h}) \tag{10.15}$$

$$2 \leq (1 + cx^T_{k-h}P_1x_{k-h}) \leq 2(u^{(i)}_{k-1-h_1} + Gx_{k-h}), \tag{10.16}$$

which correspond to

$$\begin{bmatrix} 1 & x^T_{k-h} \end{bmatrix} \begin{bmatrix} N - 2u^{(i)}_{k-1-h_1} & -G \\ * & cNP_1 \end{bmatrix} \begin{bmatrix} 1 \\ x_{k-h} \end{bmatrix} \geq 0, \tag{10.17}$$

for (10.15) and

$$\begin{bmatrix} 1\, x^T_{k-h} \end{bmatrix} \begin{bmatrix} -1 + 2u^{(i)}_{k-1-h_1} & G \\ * & cP_1 \end{bmatrix} \begin{bmatrix} 1 \\ x_{k-h} \end{bmatrix} \geq 0, \quad i = 1,2. \tag{10.18}$$

for (10.16).

These matrices can be rewritten in a suitable form by employing the Schur's complement. Likewise defining $Y = GQ_1$, applying $\bar{P_1} = Q_1P_1Q_1$ and pre and post-multiplying by $diag\{1, Q_1\}$, next LMIs from (10.17) and (10.18) are obtained

$$\begin{bmatrix} c & Y \\ * & (N^2 - 2Nu^{(i)}_{k-1-h_1})\bar{P_1} \end{bmatrix} \geq 0, \quad \begin{bmatrix} c & Y \\ * & (-1 + 2u^{(i)}_{k-1-h_1})\bar{P_1} \end{bmatrix} \geq 0, \quad i = 1,2, \tag{10.19}$$

respectively.

10.2.3 Control design

Now, the condition b) of the Problem 10.4 can be formulated in terms of Linear Matrix Inequalties (LMIs) [53]. Fulfillment of condition (10.12) plus condition (10.13) is looked for.

Take $\zeta \triangleq [\bar{x_k} \quad \psi_k \quad w_k]^T$, then objective (10.13) is satisfied if

$$V_{k+1} - V_k + x_k^T x_k - \gamma^2 w_k^T w_k \leq \zeta^T \Gamma_0 \zeta < 0. \tag{10.20}$$

Define $P \triangleq \begin{bmatrix} P_1 & P_2 \\ P_2^T & 0 \end{bmatrix}$, being P_2 Hermitian.

For this purpose, as Lyapunov-Krasovskii candidate is considered

$$V_k = V_{1,k} + V_{2,k} + V_{3,k}, \tag{10.21}$$

being

$$V_{1,k} = \bar{x}_k^T E P E \bar{x}_k, \quad P_1 > 0 \tag{10.22}$$

$$V_{2,k} = \sum_{n=1}^{h} \sum_{i=k-n}^{k-1} y_i^T R y_i, \quad R > 0 \tag{10.23}$$

$$V_{3,k} = \sum_{i=k-h}^{k-1} x_i^T S x_i, \quad S > 0, \tag{10.24}$$

where $V_{1,k}$ guaranties asymptotic stability of system (10.14) without delays. Delay-dependent as well as delay-independent criteria are considered in $V_{2,k}$ and $V_{3,k}$, respectively [53, 62].

Next, a sufficient condition for asymptotic stability and disturbance rejection is derived.

Theorem 10.5 *Consider system (10.9)–(10.11) with energy-bounded w_k and control law $\bar{u}_{k-h} = \alpha^{(m)} K x_{k-h} + (1-\alpha^{(m)}) G x_{k-h}$ for $m = 1,2$, where $h > 0 \in \mathscr{R}$ is a known constant delay and $K, G \in \mathscr{R}^{1\times n}$. If there exist $S, R, P_1 > 0 \in \mathscr{R}^{n\times n}$ such that the LMIs* (10.19) *plus the following LMIs are satisfied:*

$$\Gamma^{(m)} \triangleq \begin{bmatrix} \bar{A}^T P \bar{A} - EPE + diag\{I_n, hR\} & -\bar{A}^T P \begin{bmatrix} 0 \\ B(\alpha^{(m)} K + (1-\alpha^{(m)}) G) \end{bmatrix} + \begin{bmatrix} S \\ 0 \end{bmatrix} & \bar{A}^T P \begin{bmatrix} 0 \\ B_w \end{bmatrix} \\ * & -\frac{1}{h} R - S & 0 \\ * & * & -\gamma^2 I_n \end{bmatrix} < 0 \tag{10.25}$$

for $m = 1,2,$, then the equilibrium of the closed-loop system (10.9)–(10.11) is asymptotically stable and there is a value γ^* such that for $\gamma < \gamma^*$ condition (10.13) is fulfilled.

Proof: The goal is to satisfy $V_{k+1} - V_k + z_k^T z_k - \gamma^2 {w_k}^T w_k < 0$ for both disturbance rejection and asymptotic stability of the equilibrium for system (10.14).

Lyapunov-Krasovskii method yields:

$$\begin{aligned} V_{1,k+1} - V_{1,k} &= \bar{x}_{k+1}^T EPE\bar{x}_{k+1} - \bar{x}_k^T EPE\bar{x}_k \\ &= \left\{ \bar{x}_k^T \bar{A}^T - \psi_k^T [0 \quad \alpha^{(m)} K^T B^T + (1-\alpha^{(m)}) G^T B^T] + w_k [0 \quad B_w^T] \right\} \\ &\quad \times P \left\{ \bar{A}\bar{x}_k - \begin{bmatrix} 0 \\ \alpha^{(m)} BK + (1-\alpha^{(m)}) BG \end{bmatrix} \psi_k + \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_k \right\} - \bar{x}_k^T EPE\bar{x}_k \\ &= \bar{x}_k^T [\bar{A}^T P \bar{A} - EPE] \bar{x}_k + \eta_k + \nu_k, \quad m = 1,2. \end{aligned}$$

where

$$\eta_k = -\bar{x}_k^T \bar{A} P \begin{bmatrix} 0 \\ \alpha^{(m)} BK + (1-\alpha^{(m)}) BG \end{bmatrix} \psi_k - \psi_k^T [0 \quad \alpha^{(m)} K^T B^T + (1-\alpha^{(m)}) G^T B^T] P \bar{A}\bar{x}_k$$

$m = 1,2.$

$$\nu_k = w_k^T [0 \quad B_w^T] P \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_k + \bar{x}_k^T \bar{A} P \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_k + w_k [0 \quad B_w^T] P \bar{A}\bar{x}_k,$$

$$V_{2,k+1} - V_{2,k} = h y_k^T R y_k - \sum_{n=1}^{h} y_{k-n}^T R y_{k-n} \leq \bar{x}_k^T \begin{bmatrix} 0 & 0 \\ 0 & hR \end{bmatrix} \bar{x}_k - \frac{1}{h} \psi_k^T R \psi_k$$

This inequality is obtained developing Eq. (10.23) and applying Jensen Inequality [61].

$$V_{3,k+1} - V_{3,k} = x_k^T S x_k - x_{k-h}^T S x_{k-h} = x_k^T S \psi_k + \psi_k^T S x_k - \psi_k^T S \psi_k$$

These developed expressions are applied to inequality (10.20), in such a way that the LMIs (10.25) are obtained. ■

10.3 Robust control tuning

Now, in this section, the uncertain parameters given in Section 10.1 are taken into account, guarantying the properties achieved above, stability as well as disturbance rejection for the time-delay Vdd-hopping system. That means, to obtain a robust saturated control under

parameter uncertainties, satisfying those properties. For this, Theorem 10.5 is extended in the case of polytopic uncertainties.

Denote

$$\Omega \triangleq [A \quad BK \quad B_w \quad \alpha \quad u_{k-h_1} \quad u_{k-1-h_1}]$$

and assume that $\Omega \in \mathscr{C}o\{\Omega_j, \quad j = 1, ..., 128\}$, namely

$$\Omega = \sum_{j=1}^{n} \lambda_j \Omega_j, \quad \text{for} \quad \text{some}, \quad 0 \leq \lambda_j \leq 1, \quad \sum_{j=1}^{n} \lambda_j = 1$$

and being the vertices of the polytope described by $\Omega_j = [A^{(j)} \quad B^{(j)}K \quad B_w^{(j)} \quad \alpha^{(j)} \quad u_{k-h_1}^{(j)} \; u_{k-1-h_1}^{(j)}]$ for $j = 1, 2, ..., 128$.

Pre and post-multiplying LMI (10.25) by $Q = \text{diag}\{Q_1, Q_1, Q_1, Q_1, I_n\}$ and taking $Q_1 = P_2^{-1} > 0$ and $\bar{P_1} = Q_1 P_1 Q_1$, $\bar{R} = Q_1 R Q_1$, $\bar{S} = Q_1 S Q_1$, the following sufficient condition is achieved:

Theorem 10.6 *Consider system (10.9)–(10.11) with energy-bounded w_k and the control law $u_{k-h} = Kx_{k-h}$ where $h \geq 0 \in \mathscr{R}$ is a known constant delay and $\underline{K}, \underline{G} \in \mathscr{R}^{1\times n}$. If there exist $T, Y \in \mathscr{R}^{n\times 1}$ and $Q_1 \in \mathscr{R}^{n\times n}$ with $K = TQ_1^{-1}$, $G = YQ_1^{-1}$ and $\bar{R}, \bar{P_1}, \bar{S} > 0 \in \mathscr{R}^{n\times n}$ for $j = 1, ..., 128$ such that the LMIs* (10.19) *and*

$$\bar{\Gamma}^{(j)} \triangleq \begin{bmatrix} \bar{\Gamma}_1^{(j)} & \bar{\Gamma}_2^{(j)} & -\alpha^{(j)}B^{(j)}T - (1-\alpha^{(j)})B^{(j)}Y + \bar{S} & B_w Q_1 \\ * & \bar{P_1} - 2Q_1 + h\bar{R} & -\alpha^{(j)}B^{(j)}T - (1-\alpha^{(j)})B^{(j)}Y & B_w Q_1 \\ * & * & -\frac{\bar{R}}{h} - \bar{S}^{(j)} & 0 \\ * & * & * & -\gamma^2 Q_1 \end{bmatrix} < 0, \quad (10.26)$$

$$j = 1, ..., 128.$$

where

$$\begin{aligned} \bar{\Gamma}_1^{(j)} &\triangleq Q_1 {A^{(j)}}^T + A^{(j)} Q_1 - 2Q_1 + \alpha^{(j)} T^T {B^{(j)}}^T + (1-\alpha^{(j)}) Y^T {B^{(j)}}^T + \alpha B^{(j)} T \\ &\quad + (1-\alpha) B^{(j)} Y + I_n \\ \bar{\Gamma}_2^{(j)} &\triangleq \bar{P_1} + Q_1 {A^{(j)}}^T - 2Q_1 + \alpha^{(j)} {B^{(j)}}^T + (1-\alpha^{(j)}) Y^T {B^{(j)}}^T, \end{aligned}$$

are satisfied. Then, in the vertices j and i, the equilibrium is asymptotically stable as well as the disturbances are rejected in the entire polytope.

Proof: This is an extension of Theorem 10.5 for a polytopic uncertainties with some mathematical manipulations. Therefore, this theorem follows Theorem 10.5 proof. ■

Remark 10.7 *This robust control tuning method is conservative due to the definition of the matrix P, as well as, the attraction domain,* $\mathfrak{X}$.

Corollary 10.8 *Gain K, obtained from* T *and* Q_1 *in Theorem 10.6, fulfills Theorem 10.5 and consequently guaranties both robust stability and robust disturbance rejection for a fixed delay.*

The extension of this approach considering the saturation mechanism of the ENARC controller is open for future work.

10.4 Sub-optimal control result

In this section, the previous sub-optimal control tuning is applied with the data reported in Section 7.2. Now, the clock frequency is taken $f_{clk} = 200MHz$. This frequency introduces an one-sample-period delay ($h_1 = 1$) in the control block output due to a power-performance trade-off. Likewise $h_2 = 2$, thus $h = 3$.

The uncertain parameters take the following ranges:

- transistor characteristic, R_0, from 25Ω to 38Ω,
- load dynamic resistance, R_L, from 55.53Ω to 72.46Ω,
- load capacitance, C, from $1pF$ to $1nF$ and
- clock frequency, ω_n, from $125MHz$ to $600MHz$.

Then, LMIs (10.6) are resolved, obtaining

$$\bar{K_1} = -7179 \tag{10.27}$$

$$\bar{K_2} = 12114. \tag{10.28}$$

This was obtained for $c = 7.56$, $P_1 = \begin{bmatrix} 0.0004 & 0.0008 \\ 0.0008 & 1.931 \end{bmatrix} \cdot 10^{11}$ and $G = \begin{bmatrix} -35.09 & 736.45 \end{bmatrix}$.

In this computation, any perturbation was not taken into account. However, this method can be applied for any $\mathscr{L}_2$ exogenous disturbance.

Note that even if the control constant tuning is conservative, there is a feasible solution.

10.5 Simulation Results

In this section some simulations are performed in order to show the properties that the closed-loop system can achieve when the sub-optimal control gains are used in the ENARC controller. Likewise, a comparison between the performance achieved with respect to the control gains obtained by the previous control tuning given in Section 7.2 ($\bar{K_1} = -19.3$ and $\bar{K_2} = 39.27$), and the gains got by the sub-optimal control tuning ($\bar{K_1} = -7179$ and $\bar{K_2} = 12114$) is made.

For these simulations, the parameters values given in Section 7.2 and the data given above are taken. We want to remark that in the following simulations, the delay is $h = 3$ and the load dynamic resistance, R_L, will be time-varying, r_L.

10.5.1 Uncertain clock frequency.

In this kind of systems, clock frequency can be changes. The closed-loop system robustness (with $\bar{K_1} = -7179$ and $\bar{K_2} = 12114$) is displayed when the sampling frequency is $\omega_n = 200MHz$ in Fig. 10.2 and $\omega_n = 400MHz$ in Fig. 10.3. Observe that the effect of the delay is shown in system response. Note that the equilibrium is robust with respect to parameter uncertainties and delay.

10.5.2 Uncertain PMOS resistance

In this first evaluation, it is assumed that the electrical characteristic of the PMOS can suffer changes. For this, $0.8R_0\%$ and $1.2R_0\%$ is changed. This is shown in Fig. 10.4 and 10.5, respectively.

Note that the system in the low voltage level converges to $0.677V$ and 0.797, which are inside the interval given by (10.3), $\mathscr{I}_l = [0.675V, \quad 0.799V]$. Likewise, the high voltage level converges to $1.133V$, which is inside the interval given by (10.4), $\mathscr{I}_h = [1.132V, \quad 1.155V]$. Therefore, system converges to the uncertain intervals. These tests show once again the system robustness.

10.5.3 Uncertain load parameter

Finally, an example shows that system performance is sensitive to $\bar{K_1}$ and $\bar{K_2}$.

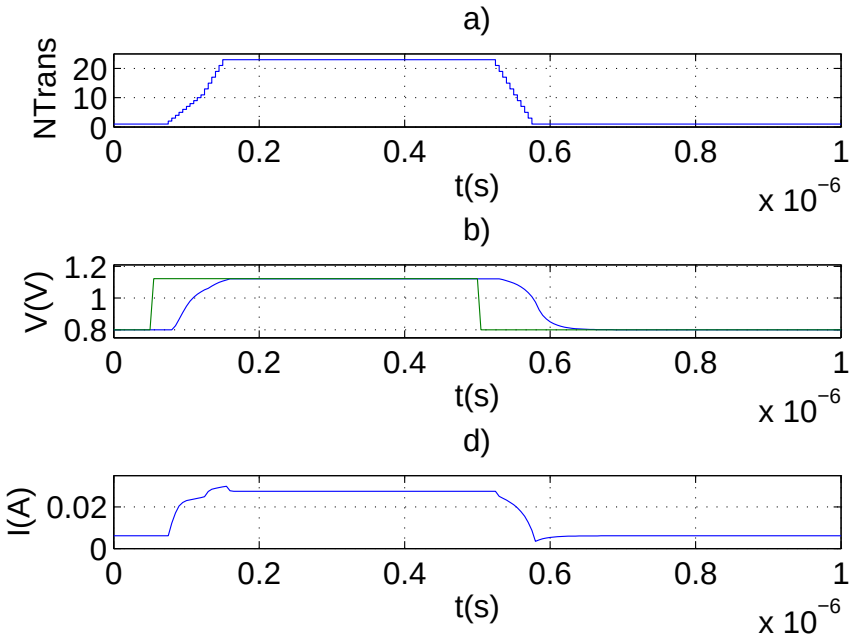


Figure 10.2: $\omega_n = 200MHz$ and $\bar{K_1} = -7179$ and $\bar{K_2} = 12114$. Evolution of the: a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid), c) current I_l.

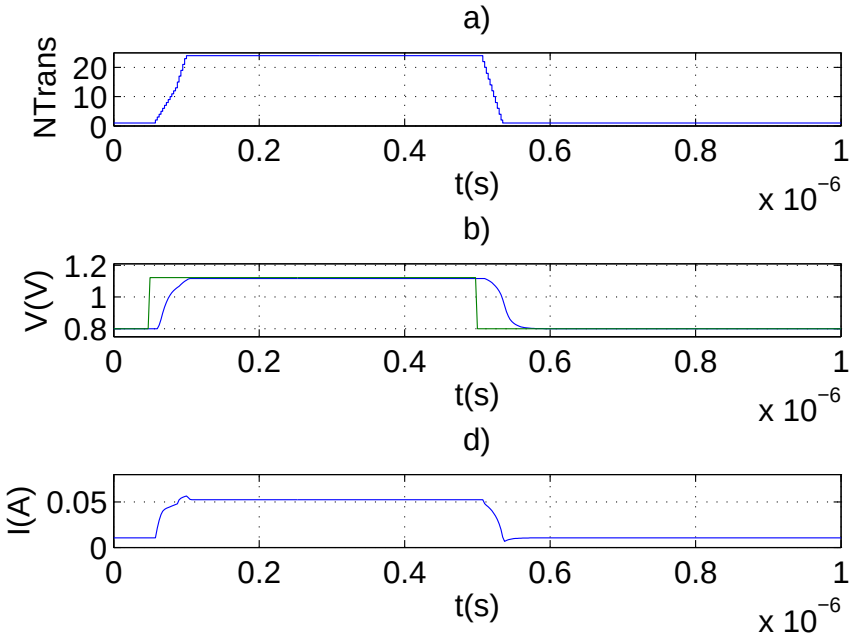


Figure 10.3: $\omega_n = 400MHz$ and $\bar{K_1} = -7179$ and $\bar{K_2} = 12114$. Evolution of the: a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid), c) current I_l.

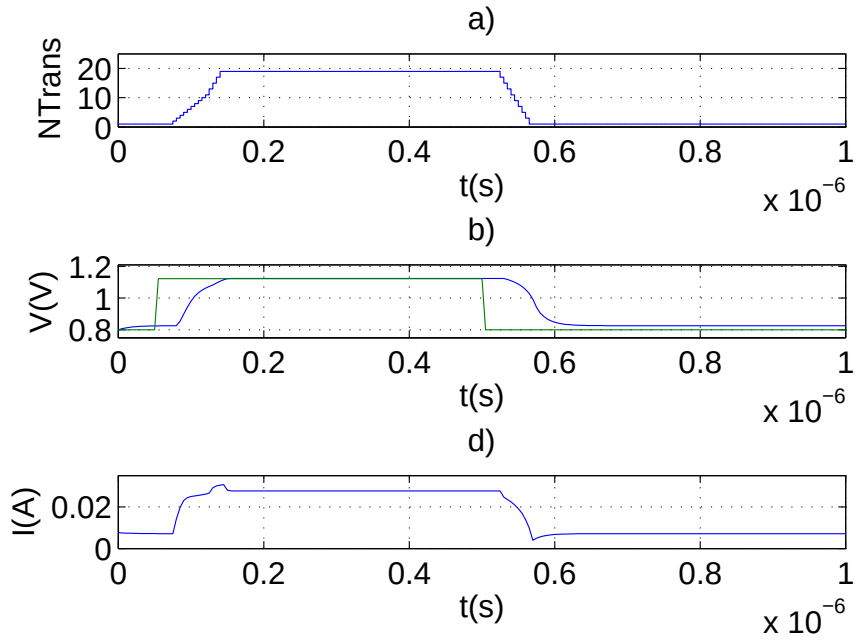


Figure 10.4: $0.8R_0\%$ and $\bar{K_1} = -7179$ and $\bar{K_2} = 12114$. Evolution of the: a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid), c) current I_l.

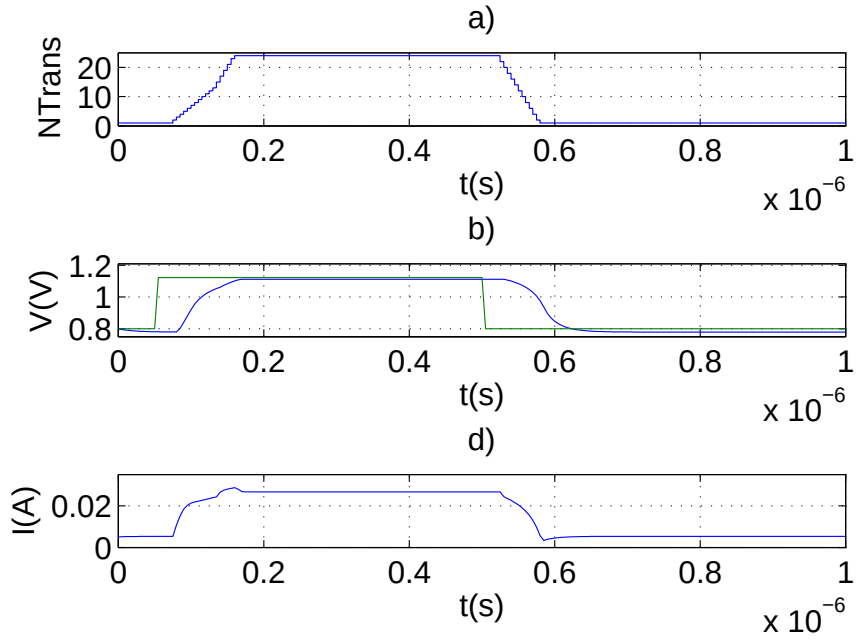


Figure 10.5: $1.2R_0\%$ and $\bar{K_1} = -7179$ and $\bar{K_2} = 12114$. Evolution of the: a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid), c) current I_l.

The capacitance employed in the previous simulations have been $C = 1nF$. In the following, it is desired to validate the system robustness when $C = 1pF$, i.e., 1000 times smaller. The lack of knowledge of the load in the real applications of these systems may achieve this change of three order of magnitude. Some simulations using both the original and sub-optimal control tuning are made.

In Fig. 10.6, it can be seen a wrong behavior of the controller when the previous control tuning given in Section 7.2 $\bar{K}_1 = -19.3$ and $\bar{K}_2 = 39.27$ are used. Nevertheless, Fig. 10.7 shows the simulation employing the sub-optimal control tuning, $\bar{K}_1 = -19.3$ and $\bar{K}_2 = 39.27$. Note that in Fig 10.6, the system does not respond to voltage variation. However, in Fig. 10.7 the system performance is satisfactory.

This example shows the great robustness of the system when the sub-optimal control tuning is employed.

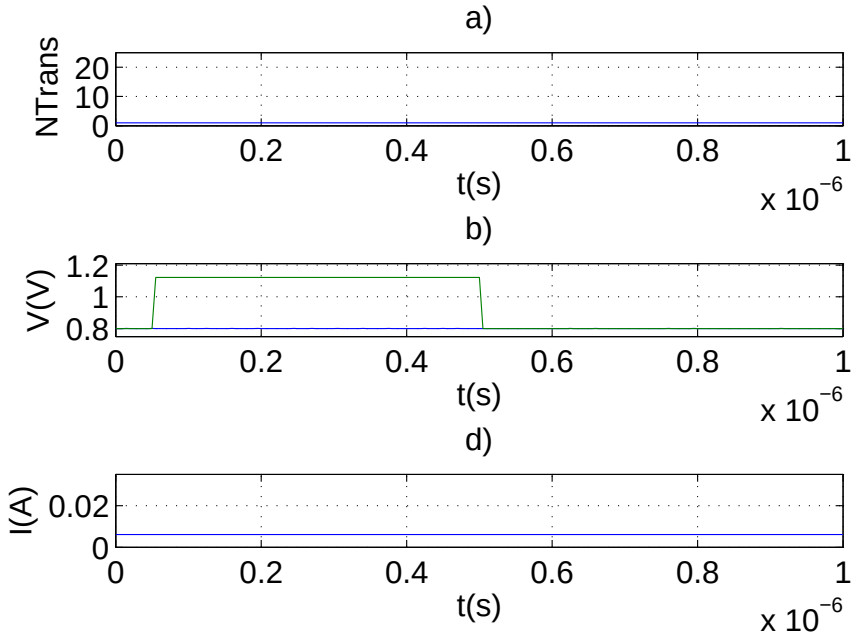


Figure 10.6: $C = 1pF$ and $\bar{K}_1 = -19.3$ and $\bar{K}_2 = 39.27$. Evolution of the: a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid), c) current I_l.

10.6 Evaluation of the tuning methods

In this section, we want to perform an evaluation of the two control tuning approaches presented in this part of the thesis.

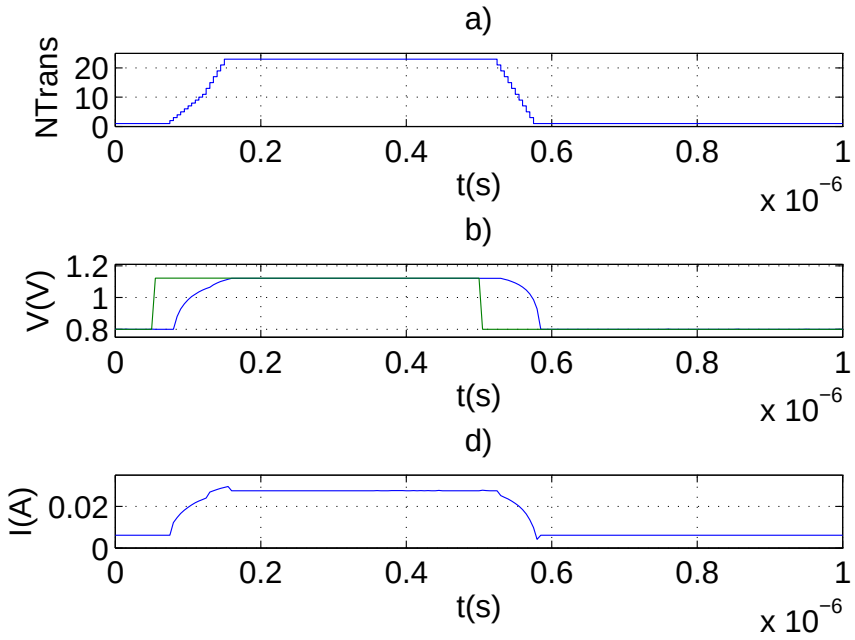


Figure 10.7: $C = 1pF$ and $\bar{K_1} = -7179$ and $\bar{K_2} = 12114$. Evolution of the: a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid), c) current I_l.

The first tuning method for the ENARC controller was presented in Chapter 7. It was developed focussed on ensuring the equilibrium convergence around of a set point for the linearized closed-loop system. Later, in Chapter 9, an approximate stability analysis for the nonlinear system and the approximate continuous-time ENARC controller with this first tuning approach was performed. Consequently, this tuning mechanism takes into account the management of the current peaks and the fast transient periods in such a way that a high energy efficiency is achieved. However, the saturation of the total number of PMOS transistors, system delays and parameter uncertainties have not been studied .

The second tuning method was developed in this chapter. It was developed taking into account the saturation of the total number of transistors, fast transient periods, delays, perturbation rejection and uncertain parameter as well as stability issues. Moreover, the closed-loop system with this method also offers a high energy efficiency. For this, it was called sub-optimal control mechanism. Nevertheless, in this approach was not considered the management of the current peaks. An estimation of an attraction domain, that ensures a maximum variation of the switched transistors in every sampling time, could guarantee that these current peaks are small. As future work, it is desired to extend this result regarding the saturation mechanism that manages the current peaks.

This last control tuning takes into account more control objectives, and thus, it consideres a closed-loop system closer of the real one. In order to test the achieved properties, some

simulations are done employing the ENARC controller (i.e., the controller with the current peak management) with this sub-optimal tuning approach. It can be seen, the right system behavior.

10.7 Conclusions

An energy-aware control has been developed for the Vdd-Hopping system. This controller achieves almost of the control requirements for SoCs technology. Nevertheless, parameter uncertainties and delays have been disregarded. Generally, this kind of systems have delays due to synchronization issues and performance constraints. Furthermore, parameters can change due to task requirements or can be varying on time.

In this chapter, these important issues have been dealt with. An sub-optimal 'conservative' control tuning approach has been developed for the ENARC controller in order to achieve a robust closed-loop system with respect to the parameter uncertainties and delays. For this, the system is rewritten in a state-space form. The control has been based on H_∞ theory applied to time-delay systems [26, 53, 101]. For this, some LMIs have been developed following Lyapunov-Krasovskii method. Conservativeness of the method for the Vdd-Hopping system has been discussed. This kind of method to tune a linear controller are employed in industrial applications [14, 129]. System robustness has been showed by means of some simulations.

An evaluation of the two tunning methods presented in this part of the thesis have been performed taking into account the approximations employed in both approaches.

A future research will be performed, in order to extend this result considering the current peak management in the control signal.

Therefore, with this development, all control requirements specified in Chapter 6 have been achieved. A controller, pending patent under the name ENARC, was designed for the Vdd-Hopping system with the aim of reducing the dissipated energy. This controller has an energy-aware management of current-peaks in the set of PMOS transistors. In addition, a step reference is used, thus, it only needs to know the two set-points. This result comes from the possibility to control more than one transistor at once, i.e., to switch more than one transistor in a same sampling time. As a side effect the transient-periods are diminished. These improvements make that system is more energetically efficient. In a comparison performed with an 'intuitive' controller published in [99], it has been showed that energy-consumption is reduced a 96%. Furthermore, it presents a relative low number of computational blocks, what makes this controller feasible for industry applications. Finally, the closed-loop system has a robust equilibrium stability with respect to parameter uncertainties and delays.

In summary, in this work a controller for the Vdd-Hopping system has been obtained. This controller has the next properties:

- high energy efficiency,
- system stability,
- small current peaks,
- fast transient periods,
- robustness with respect to parameter uncertainty,
- robustness with respect to delays and
- easy implementation.

Hence, it achieves an interesting relevance for SoCs applications and, thus, in ARAVIS project implementation. An implementation of the ENARC controller in VHDL-AMS will be performed in the project context, in order to validate its performed.

Chapter 12

Conclusions and future work

12.1 Conclusions and contribution summary

This thesis contributes to provide nonlinear control problem solutions to several classes of power converters. Specifically, this thesis deals with a DC-AC converter for applications of medium or high power, and a DC-DC converter for low-power applications. The first problem was developed in the 'Departamento de Ingeniería de Sistemas y Automática' at the 'Universidad de Sevilla' (Spain). And the second electronic application was raised in a project of the French government, sponsored by the international competitiveness pole Minalogic, called ARAVIS. The control problem was tackled in the 'Département d'Automatique de GIPSA-Lab' at the 'Institut Polytechnique de Grenoble' and at the 'Institut National de Recherche en Informatique et en Automatique de Grenoble' (France). Both converters are regarded with respect to their work contexts, and thus, the associated control objectives are different.

Due to the dissimilar natures of both applications mentioned before, the thesis is composed of two parts. The first part is focused on the control problem of the DC-AC converter. Its structure is based on a double DC-DC boost converter, obtaining a boost inverter. It is no-minimum phase 4^{th} order nonlinear system. Its main objective is to achieve the desired voltage with a suitable control law, that does not require any reference signal. Furthermore, other problems, as no purely resistive and known loads, and the proposition of an estimated attraction region have been coped with. The second part of the thesis is devoted to a discrete DC-DC converter for low-voltage application in SoC. Its structure is the result of employing DC-DC converters in this kind of technology. It is based on the Vdd-Hopping technic in order to fulfill Dynamic Voltage Scaling, hence, it is called 'Vdd-Hopping converter'. This system is a 1^{st} order nonlinear system. Although, its simple model may not be attractive for control applications, it has relevant interest in this field due to the project context, where

it is dealt with. The control objectives come from the ARAVIS project. In this context, the relevant aim for this DC-DC converter is to achieve a high-efficiency, while the current peaks and the transient periods are minimized. This must be reached with a controller that ensures the convergence to the desired equilibrium points, global stability and robust behaviour with respect to delays and parameter uncertainties.

Next up, the most important contributions of this thesis are highlighted.

For the first part, i.e., controlling the boost inverter circuit, the most important contributions have been:

1. A control law for the boost inverter has been designed based on an energy shaping approach for oscillation generation. This method provides a relevant property, the system is autonomous, and hence, its analysis and implementation are easier, since the system needs no reference signal. Furthermore, the energy shaping approach employed to obtain the control structure ensures global stability.

2. A phase controller inspired by a phase-lock loop is presented in order to synchronize the two output voltages of both parts of the system. This idea is extended to synchronize the circuit with an external signal, as for example, with the electrical grid.

3. By means of developing a control adaptive for the unknown or/and slowing varying load connected to the boost inverter, the desired output voltage is always achieved. This control adaptive needs of a state observer for some variables, although all variables are measured. Global stability of the full system is proved by using singular perturbation method, for this, the system is rewritten in the suitable form by using time-scale separation.

4. The previous problems dealt with before have been extended to a load that is not purely resistive but also has an inductive component. These developed works, have been not considered in this thesis to make a simple reading, since they are just an extension. However, as the inverter control law as the adaptive controller developed for the boost inverter with an inductive load were published in [10] and in [12], respectively.

5. The last issue considered has been the estimation of an attraction region for the boost inverter. It provides a set of initial conditions corresponding to trajectories that converge towards the desired system behavior. This problem comes from the real nature of the boost inverter, which has several constraints, including saturations. This makes that the system has not global stability with the Lyapunov function obtained from energy shaping approach.

   Inspired by this estimation problem of an attraction region for the boost inverter, a general estimation method for this class of problem has been proposed. It takes advantage of certain defined Lyapunov function, that ensures global stability, raising a

simple optimization problem. This fact makes that the estimation is 'conservative'. This problem is resolved rewriting it as a sum of squares optimization.

This method is applied to the boost inverter. For this, the previous Lyapunov function, has been employed. The method provides a good 'conservative' estimation for the inverter.

The second part of the thesis is focused on the control problem of the DC-DC Vdd-Hopping converter. Here, the provided contributions have been:

1. A set of high-performance controllers has been proposed. These controllers have been developed by applying several control theories focused on reaching the desired equilibrium point by the closed-loop system. From the set of controllers, the one that provides a best performance is selected. In order to satisfy the objectives, some developments have been made to this controller, applying optimal and adaptive control theory. This control solution in spite of providing nice properties to the Vdd-Hopping converter behaviour, has a relevant drawback: its computational cost is very large. Therefore, it is not a suitable solution for the ARAVIS project.

2. An innovative controller for the DC-DC Vdd-Hopping converter has been developed based on the control structure with the smallest computational cost from the set of control solutions proposed before. This controller has been designed based on energy-aware concept. Its originality is due to its current-peak managing through saturations with dynamic limits depending on the state of the system. It achieves the desired equilibrium points increasing the energy saving, reducing the current peaks and diminishing the transient periods. It covers almost all requirements in low-power technology. In addition, its simple structure is remarkable for industrial applications.

3. A global stability analysis of the nonlinear model of the Vdd-Hopping converter with the nonlinear controller presented before has been developed. The stability analysis of the closed-loop system has been involved due mainly to the saturation limits depending on the system state. The global analysis is ensured by LaSalle's invariance principle. For simplicity, this analysis has been performed in continuous-time. It is assumed that the stability properties in discrete-time are conserved, as is common in control.

4. The last contribution is performed with respect to delays in parameter uncertainties. On the one hand, some delays can be presented due to the regarded work context of the Vdd-Hopping converter. They may be caused by synchronization issues, as well as, by providing an energy-performance trade-off. These delays can be considered as one only constant delay. On the other hand, depending on the specific application, the system parameters can be diverse and time-varying during the transient periods, as well. Consequently, the problem is to find the optimal gains for the controller. For this, an optimal tuning mechanism for these control gains based on H_∞ theory is proposed. They are obtained resolving some Linear Matrix Inequalities (LMIs),

which have been developed by Lyapunov Krasovskii method. These LMIs ensure the equilibrium robustness with respect to delays and parameter uncertainties.

Finally, it can be concluded that nonlinear control theories can be powerful tools to provide solutions of several natures in industrial applications, in such a way that global stability of these systems is guaranteed.

12.2 Future work

Following the investigations described in this thesis, the next future work will be taken up:

In the boost inverter:

1. A physic implementation of the boost inverter will be made in order to test the performance of the control law proposed from applying energy shaping. In addition, this will allow to compare this control law with other controllers that have been already published for the same inverter.
2. An extension of the proposed adaptive control can be performed considering that not all the states are measured.
3. In the case of the global stability analysis to the system with the adaptive controller, to extend this analysis (which has been performed employing singular perturbation analysis) for a infinite time.
4. To find a less conservative solution to estimate the attraction region by employing another advanced tool to solve the sum of squares optimization problem.
5. .

In the Vdd-Hopping converter:

1. An implementation of the controller proposed in this thesis will be performed in VHDL-AMS, in order to test its real approximate behaviour before to implement it in SoCs.
2. A better numerical solution to obtain an optimal voltage reference for the Lyapunov controller will be performed with another advanced mathematical tool.
3. Extension of the stability analysis of the closed-loop system in discrete-time.

4. Extension of the sub-optimal tuning approach for the control gains considering the saturation of the current peak management.

List of Publications

In conferences:

1. C. Albea, C. Canudas-de-wit. and F. Gordillo, Control and Stability Analysis for the Vdd-hopping Mechanism, *3rd IEEE Multi-conference on Systems and Control (MSC'09)*, Saint Petersburg, Russia. 8-10 July 2009.

2. C. Albea, C. Canudas-de-wit. and F. Gordillo, Advanced Control Design for Voltage Scaling Converters, *34th IEEE Conference of the IEEE Industrial Electronics Society (IECON'08)*, Orlando, Florida, LA, USA.10-13 Nov. 2008

3. C. Albea, F. Gordillo and C. Canudas De Wit, Adaptive Control of the Boost Inverter with Load RL, *17th IFAC World Conference*, Korea Republic. 6-11 July 2008.

4. C. Albea, C. Canudas-de-wit. and F. Gordillo, Diseo de Controladores para Convertidores con Escalado de Tensin, *XXIX Jornadas de Automtica*, Tarragona, Spain. 3-5 Sept. 2008.

5. C. Albea and F. Gordillo., Control of the boost DC-AC converter with RL load by energy shaping, *46th IEEE Conference on Decision and Control (CDC'07)*, New Orleans, LA, USA. 12-14 Dec. 2007.

6. M. Fiacchini, T. Alamo, C. Albea and E. Fernandez Camacho, "Control Applications, Adaptive model predictive control of the hybrid dynamics of a fuel cell system, *1er IEEE Multi-conference on Systems and Control (MSC'07)*, Singapore. 1-3 Oct. 2007.

7. C. Albea, C. Canudas De Wit and F. Gordillo, Adaptive Control of the Boost DC-AC Converter, *1er IEEE Multi-conference on Systems and Control (MSC'07)*, Singapore. 1-3 Oct. 2007

8. C. Albea and F. Gordillo, C. Canudas De Wit, Control Adaptativo del Inversor Boost, *XXVIII Jornadas de Automtica*, 5-8 Huelva, Spain. 5-8 Sept. 2007.

9. C. Albea and F. Gordillo, Estimation of the Region of Attraction for a Boost DC-AC Converter Control Law, *7th IFAC Symposium on Nonlinear Control Systems (Nolcos'07)*, Pretoria, South Africa. 22-24 August 2007.

10. C. Albea C, F. Gordillo and J. Aracil Santoja, Control of the boost DC-AC converter, *32th IEEE Conference of the IEEE Industrial Electronics Society (IECON'06)*, Paris, France. 6-10 Nov. 2006

11. C. Albea C., M. G. Ortega, F. Salas and F. R. Rubio, Aplicacion del control Hinf al PPCAR, *XXVII Jornadas de Automtica*, Almeria, Spain. 6-9 Sept. 2006.

12. C. Albea and F. Gordillo, Control del Convertidor Boost DC-AC por moldeo de Energa, *XXVII Jornadas de Automtica*, Almeria, Spain. 6-9 Sept. 2006

In journals:

1. C. Albea, F. Gordillo and C. Canudas De Wit., Adaptive Control Design for a Boost Inverter, in *Engineering Control Technology*, submitted 2009, accepted August 2010, published September 2010.

2. C. Albea and F. Gordillo, On the estimation of attraction domains for polynomial systems with constraints. Application to electronic converters" (submitted).

3. C. Albea, C. Canudas De Wit. and F. Gordillo, High Performance Control Design for Dynamic Voltage Scaling Devices, (under preparation).

4. C. Albea, F. Gordillo and C. Canudas De Wit. , Robust Control for Low-Power Converters (under preparation).

Patent:

1. C. Albea and C. Canudas de Wit, Dispositif de commande numrique pour un tableau de transistors PMOS en parallele Patent No: 08/07342. Filing date: 22 Dec. 2008 Publ. date: 22 January 2009.

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