Resource-aware Video Processing on Tightly-Coupled Processor Arrays

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To meet the ever increasing computational needs, there is a strong trend towards research in many-core architectures. They offer a high degree of parallelism and achieve a better energy efficiency compared with traditional single processor solutions. Consequently, existing centralized resource management approaches may not scale and thus may become a major system performance bottleneck. Therefore, Teich and others [4] proposed a novel resource-aware computing paradigm for dynamic exploitation of the available level of parallelism, called *invasive computing*. Here an application may dynamically claim and reserve resources (invade), employ them for parallel execution (infect), and finally release them (retreat).

We present a class of highly parameterizable and programmable processor array architectures [1], which we recently augmented by dedicated units for hardware-accelerated decentralized resource management [2]. Such a tightly-coupled processor array (TCPA) consists of an array of processor elements (PE). Each PE consists of a processing unit (PU), having a very long instruction word (VLIW) structure, limited instruction memory, small register file, and minimal control overhead, as well as a so-called invasion controller (iCtrl), which takes care of resource management. Both instruction-level (VLIW architecture) and loop-level parallelism (multiple PEs working concurrently) can be realized efficiently on TCPAs, which makes them suitable as an accelerator for computationally intensive loop programs like image or video processing applications.

More specific, in this demonstration, a TCPA prototype for performing 2-D filtering on an input video stream [3] is presented. A sketch of the architecture is depicted in Fig. 1 and its individual components are described in the following briefly.

Prototyping Platform: For prototyping invasive TCPAs, we used *Synopsys CHIPit prototyping platform*, it is scalable up to 18 FPGAs and has a claimed design capacity of up to 36 million gate equivalents. Data transfer between the host and hardware happens via UMR-bus communication system provided by the CHIPit infrastructure.

Invasive TCPA: For the current demo, a TCPA array of size 5×5, a datapath width of 16 bits, and each VLIW PE is configured for one instance of the ADD, MUL, logical and shift functional units.

Video Input/Output Devices: The input video stream in DVI format, generated from a PC or a video camera, is fed to the TCPA through a *DVI extension board*.

Video Application: The targeted applications on invasive TCPA prototype are several real-time 1-D and 2-D image filters (e. g., FIR filtering, 2-D convolutions, edge and feature detection) on a streaming input video, Here, based on the number of PEs available on the TCPA, a suitable 2D Edge detection or Gaussian filtering kernel is loaded.

We show three scenarios emulating varying workload and competing applications on the TCPA:

Scenario 1: A parasitic application pre-occupies 20 PEs, leaving only 5 PEs for the target application, the target application realizes a 1×3 Sobel filter for edge detection using 3 PEs.

Scenario 2: A parasitic application pre-occupies 10 PEs, leaving 15 PEs for the target application, the target application realizes a 3×3 Laplace filter for edge detection.

Scenario 3: No parasitic application on TCPA, leaving all 25 PEs for the target application, the target application realizes a 5×5 Laplace filter for edge detection.

The quality of output improves from Scenario 1 through Scenario 2 to Scenario 3 because of the increase in number of invaded PEs by the target application.

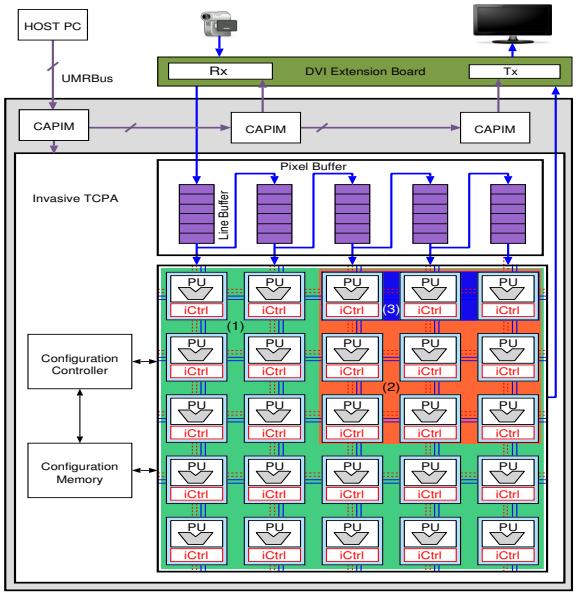

Fig. 1. TCPA prototype performing 2-D image filtering on a video stream.

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