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Photonic Packet Switching: An Overview*

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SUMMARY The application of photonic technologies to packet switching offers the potential of very large switch capacity in the terabit per second range. The merging of packet switching with photonic technologies opens up the possibility of packet switching in transparent photonic media, in which packets remain in optical form without undergoing optoelectronic conversion. This paper reviews recent work on photonic packet switching. Different approaches to photonic packet switching and key design issues are discussed.

key words: *photonic packet switching, photonic packet buffer, wavelength routing, wavelength conversion*

1. Introduction

There is growing motivation for the development of ultra broadband photonic networking technologies. This move to photonic networks arises from the increasing demand for broadband communications and the capability of optical components and devices to provide tremendous bandwidth to satisfy this demand [1], [2]. Asynchronous transfer mode (ATM) switching and other forms of packet switching such as IP routing are emerging as key to the implementation of future high-capacity and multi-function telecommunications networks. Electronic ATM switching techniques, combined with transmission systems using the SDH/SONET standard, provide a platform for flexible transmission and management of broadband traffic from a variety of sources, including video, data, and voice. Meanwhile, IP routing and switching is emerging as a key to future expansion of data and other internet-related services. Electronic packet switching offers great potential, but is ultimately limited in data rate and throughput by the processing capacity of electronic devices [3]–[8]. The ultimate solution is to replace electronic packet switches with optical packet switches in which signals remain in optical form.

The merging of packet switching with photonic technologies opens up the possibility of packet switching in transparent photonic media. Thus, the wide bandwidth of photonic components, combined with the flexibility of wavelength-division multiplexing and wavelength routing techniques [1], [2], and the high-speed capabilities of optical devices such as optical gates and switches [9], [10], optical wavelength converters [11]–[13], and fast multiwavelength lasers [12], [14], provides the potential of packet-switched networks with throughput in the terabit per second range [3]–[8], [15]–[20].

The application of photonic technologies to packet switching have been motivated by a number of driving forces. One of these forces is the anticipated need for high-capacity nodes [3]–[8]. Some studies have shown that the ultimate capacity of photonic-based switching nodes will exceed the capacity of electronic systems [3], [4], [15]–[20]. Thus, high-capacity photonic nodes will be attractive as alternatives to very large electronic switch nodes, even when the individual channels operate at data rates that are compatible with electronic capabilities. Another motivation is the prospect offered by optically transparent self-routing networks [3]–[8], in which optical packets pass through photonic packet switches in a transparent fashion, without undergoing any optical to electrical or electrical to optical conversions. The obvious attraction of such a network is that there is no electronic processing in the data path and the data can ideally pass through the switch without any limitation on bit rate. Also, wavelength-division multiplexing (WDM) can be readily exploited. Thus very large throughput becomes feasible. A third application is in the development of photonic local area and metropolitan networks with a vastly improved throughput [21]–[25].

The purpose of this paper is to give an overview of recent work on photonic packet switching. We will discuss key design issues and different approaches to photonic packet switching. The discussion will focus on photonic approaches to packet routing and buffering, switch fabric architectures, packet header replacement and packet synchronization.

2. Photonic Packet Switches

There have been a number of recent proposals and experimental demonstrations of photonic packet switching in university and industrial laboratories [3]–[8], [15]–[20], [26]–[33]. The switching and/or routing fabric in these demonstrations has generally been opti-

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cal, in order to capitalize on the optical transparency and large bandwidth. However, electronic and opto-electronic components remain attractive alternatives to photonic devices in functions such as address processing, switching and buffing controls [3]–[8]. Large photonic packet switches will probably rely on electronics for control functions, with the packet routing and buffering being carried out by photonic means. This approach provides very large capacity through the transparency of the photonic devices, combined with the functionality and processing power of electronic control circuits.

Figure 1 shows the schematic diagram of a general photonic packet switch. As shown in this diagram, key functions affecting the operation and implementation of photonic packet switches include (a) packet routing, (b) packet buffering, (c) packet header replacement, and (d) packet synchronization and timing recovery. Truly photonic switches require photonic implementations of all of these functions. Packets generally have a fixed duration and consists of a header and a payload. The header contains routing information and other control information. As the header has to be processed at each switch node, it is desirable that the header has a relatively low fixed bit rate suitable for electronic processing (say, less than 10 Gb/s); while the payload could have a variety of bit rates ranging from 10 Gb/s to 100's of Gb/s [3], [4], [7]. The use of fixed length packets can significantly simplify the implementation of packet contention resolution and buffering, packet routing, as well as packet synchronization [3], [4], [7].

Packet header replacement is an important function in ATM-like connection-oriented networks, where it is necessary to change the contents of the packet header as it passes through each switch node. In optically transparent packet switching, it is necessary that the header replacement is carried out photonically [34]. Advances in photonic devices and components such as high-speed optical space switches, semiconductor optical amplifier (SOA) gate switches [9], [10], wavelength routing devices [35], [36], fast tunable lasers and filters [4], [12], [14], and wavelength converters [11], [12], [13], [16] have made it possible to construct photonic packet switch fabrics with a throughput in excess of their electronic counterparts [3]–[8]. Possible routing schemes for photonic packet switch fabrics include wavelength routing, broadcast-and-select routing, space-switch-based routing, and a combination of them. We will discuss the options in detail in Sect. 4.

As shown in Fig. 1, buffering of photonic packets somewhere within the switch fabric is essential to prevent packet contention. The difficulty in implementing fully-functional photonic equivalents to the electronic random access memory (RAM) makes clocked optical buffering and synchronization difficult. One possible approach to the photonic buffering problem is to use fibre delay lines either in recirculating or travelling configurations [4], [5], [37]. Deflection routing may offer an attractive approach to circumvent packet contention in distributed systems, but this approach provides an effective "connectionless" system, in which the order of packet arrivals cannot be guaranteed [6], [25], [27], [63].

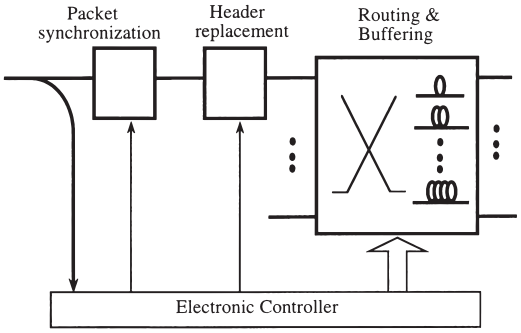

Fig. 1 Schematic of a general photonic packet swith.

We now consider more details of different approaches to photonic buffering and routing, architectures for switch fabrics, and techniques for photonic packet header replacement and packet synchronization.

3. Buffering

In principle, advanced electronic RAMs can be used for packet buffering. Earlier proposed photonic packet switching systems have used electronic RAMs for packet buffering [23], [38]–[40]. However, electronic RAMs have a limited access speed, which will eventually constrain the speed and capacity of photonic packet switching systems. In addition, this electronic approach requires optical-to-electronic (O/E) and electronic-to-optical (E/O) conversions when packets are written into and read out of electronic RAMs and hence adds to the complexity. An all-optical RAM would avoid the speed bottleneck and O/E and E/O conversions. There has been much effort to investigate and develop optical RAMs [41], [42]. Unfortunately, useful optical RAM suitable for photonic packet switching has not yet been found. The alternative is to use optical fibre-delay-lines incorporating other components such as optical gate switches, optical couplers, optical amplifiers, and wavelength converters to realize photonic buffering.

A number of photonic packet buffers based on optical fibre delay-lines have been proposed and demonstrated [4]–[6], [37]. In general, these optical fibre delay-line based buffers can be classified into two basic categories: travelling-type and recirculating type. A travelling-type buffer generally consists of multiple optical fibre delay-lines whose lengths are equivalent to multiples of a packet duration T, and optical space switches to select delay lines [37], as shown in Fig. 2. Travelling-type buffers can be arranged in serial or parallel structures [20], [37], [43], [44]. In such travelling-type buffers, the storage time of a packet is simply

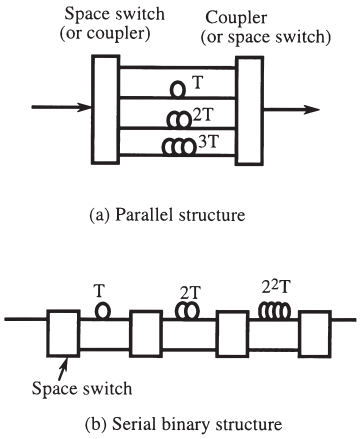

Fig. 2 Travelling-typy packet buffer.

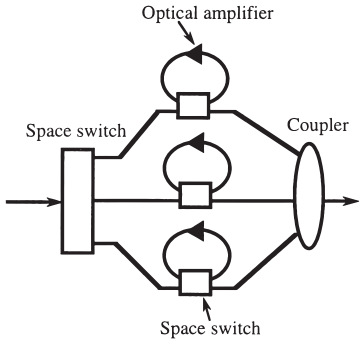

Fig. 3 Recirulating-type packet buffer with a parallel structure.

determined by the duration of a packet propagating through a length of optical fibre. For the parallel configuration, the number of delay-lines and the size of optical space switch is increased as the number of programmable delay amounts is increased. Figure 3 schematically shows a recirculating-type buffer with a parallel configuration [37]. It consists of multiple optical fibre delay-lines each forming a loop with one circulation time equal to one packet duration. The storage time of a packet in such a recirculating-type buffer is determined by the circulating number times the packet duration T. Both of the packet buffers shown in Figs. 2 and 3 are able to store multiple packets with the constraint that only one packet enters and leaves the buffer at a time. This constraint can be removed if WDM is invoked [15], [29], [33], [45].

The recirculating-type buffer is more flexible than the travelling-type buffer in that the packet storage time is adjustable by changing the circulation number [27], [46]. In principle, a recirculating-type buffer offers the capability of random access with storage time depending on the number of recirculations. On the other hand, the storage time of a travelling-type buffer is predetermined by the length of the optical fibre delay-lines. A problem with the recirculating-type buffer is that the signal has to be amplified during each circulation to compensate for the power loss [27], [46]–[48]. This results in accumulated spontaneous emission (ASE) noise from the optical amplifier and signal-level fluctuation, which eventually limits the maximum buffering time [46], [47], [49]. In addition, the gain from the optical amplifier has to be carefully controlled so that the product of gain and the loss in one circulation is slightly less than unity to prevent optical signal lasing.

In packet-switched networks, it is extremely important to ensure a low packet loss probability, while achieving a relatively high throughput [50]. This requires a large buffering capacity, depending on switch architecture. For example, an output-buffered packet switch requires a buffering capacity of more than 50 packets at each output to achieve a packet loss probability less than 10^{-6} at a traffic load of 90% [50]. In the context of photonic packet switching, WDM has been considered to increase the buffering capacity. Based on the principle of travelling-type or recirculating-type buffers, a number of WDM photonic buffers have been reported and demonstrated. These include random wavelength accessible recirculating loop buffers [29], [45], cascaded recirculating loop buffers [18], [49], and wavelength-routed buffers [33], [51]. More details are given in the next section.

4. Switch Architectures

Many different photonic packet switch architectures have been proposed and demonstrated (see [3], [4], [8], [15], [17]–[20], [27]–[33], for example). All of these use photonic means to perform packet buffering and routing; while electronics plays the important role in such functions as address processing, routing and buffering controls. Possible approaches to packet routing within these photonic packet switches include wavelength routing, broadcast-and-select routing, and space-switch based routing.

4.1 Wavelength-Routed Photonic Packet Switch

The first wavelength-routed packet switch discussed here is the photonic matrix switch proposed by Gabriagues and Jacob [30], [52]. This packet switch uses wavelength coding for packet routing and buffering. As shown in Fig. 4, it consists of three functional blocks: a packet encoding block, a buffering block and a packet demultiplexing block. The packet encoding block is composed of N optical tunable wavelength converters (TWCs) which each convert a packet to a new wavelength corresponding to its desired output, i.e. a packet addressed to the i-th output is assigned a wavelength λ_i. The buffering block consists of a N×K SOA-gate switch matrix followed by a set of K optical delay-lines whose lengths range from 0 to (K−1)-packet time. The SOA-gate switch matrix provides wavelength-encoded packets access to appropriate

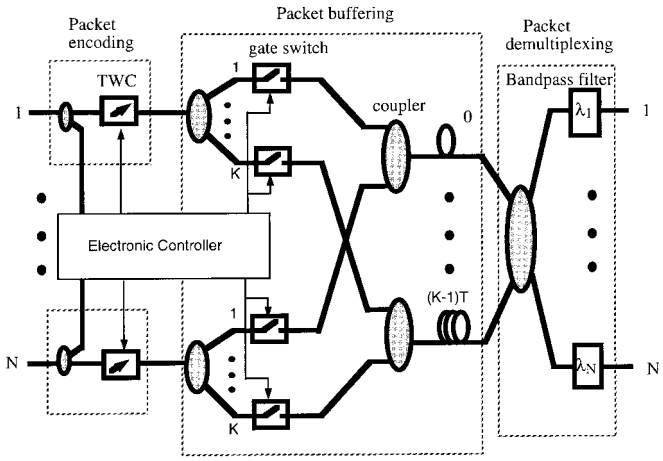

Fig. 4 Wavelength-routed photonic matrix switch [30].

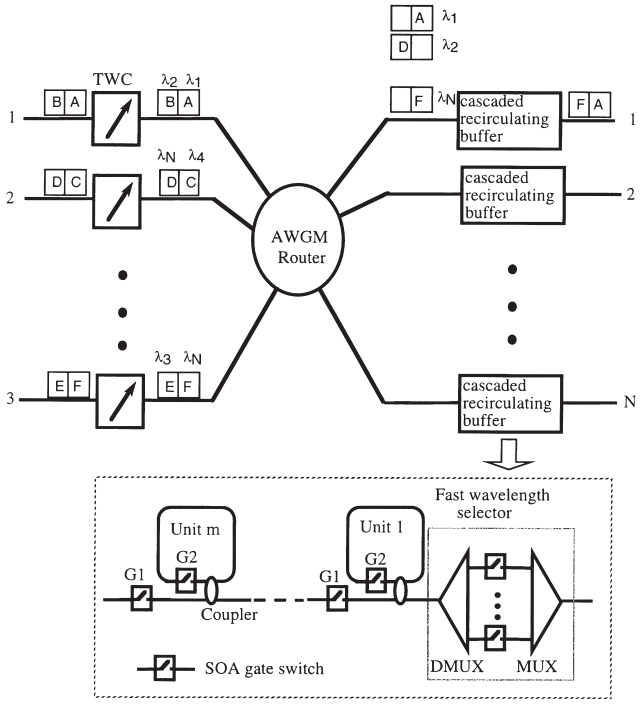

Fig. 5 Frontiernet photonic packet switch[18].

delay-lines in a way that packets that are destined for a given output leave the switch in a first-in first-out (FIFO) manner. The demultiplexing block consists of a K×N star coupler followed by a set of N bandpass filters, one at each output to select packets whose wavelengths are matched with its passband. In addition, there is an electronic controller to control the TWCs and space switches. It is interesting to note that, because packets are wavelength encoded from λ_1 to λ_N, the K delay-lines function as N FIFO buffers, each corresponding to one output and capable of storing up to K packets. One difficulty with this architecture is that the number of SOA gates required in the buffering block increases in proportion to the product of N and K, i.e., the switch size and the buffer size. Also, the optical power loss of a packet is proportional to NK^2 for N<K or N^2K for N>K. The value of K depends on the required packet loss probability and the traffic load.

K. Sasayama, et al., proposed another wavelength-routed packet switch, known as the Frontiernet packet switch [18], [28]. The architecture, as shown in Fig. 5, uses an arrayed-waveguide grating multiplexer (AWGM) [35], [36] in conjunction with wavelength conversion to perform packet routing. For a N×N packet switch, it only requires N wavelengths to fully interconnect N inputs with N outputs. The relationship between the inputs, the outputs and the wavelengths within an 4×4 AWGM is shown in Table 1. With reference to Table 1, this AWGM is capable of simultaneously routing up to N packets of different wavelengths to a given output. This is illustrated in Fig. 5, in which packets A and F from inputs 1 and N are simultaneously routed to output 1 at wavelengths λ_1 and λ_N. The function of the buffer at each output is to regulate packets such that only one packet leave the output at any time slot.

The buffer in the Frontiernet is shown at the bottom of Fig. 5. It consists of multiple recirculating loop units connected in a serial configuration, and followed by a fast wavelength selector (or tunable filter). Each recirculating unit consists of a length of optical fibre forming a loop, and two SOA gate switches and a 3-dB coupler. By appropriately turning on or off the two gate switches G1 and G2 at each loop unit, packets can be either coupled into or cleared from any fibre loop. For example, assuming all loop units are empty and three packets are entering the buffer at the start of time slot 1, these packets are fed into the loop unit 1 by turning on all gate switches G1, and switching off all gate switches G2 except for the gate switch G2 at the loop unit 1. At the same time, one packet is selected out by the fast wavelength selector. In time slot 2, new packets are fed into loop unit 2 only, and so on. The packets in the i-th loop unit are forwarded to the (i−1)-th loop unit if and only if no packet exists in the (i−1)-th loop unit.

Table 1 Relationship between inputs, outputs and wavelengths within a 4×4 AWGM.

		Output			
		1	2	3	4
Input	1	λ_1	λ_2	λ_3	λ_4
	2	λ_2	λ_3	λ_4	λ_1
	3	λ_3	λ_4	λ_1	λ_2
	4	λ_4	λ_1	λ_2	λ_3

Simulation has shown that each buffer requires at

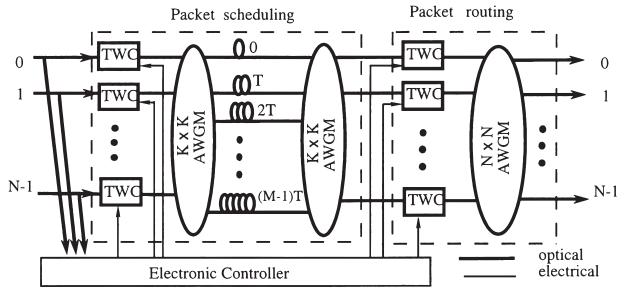

Fig. 6 Input-buffered wavelength-routed packet switch [33].

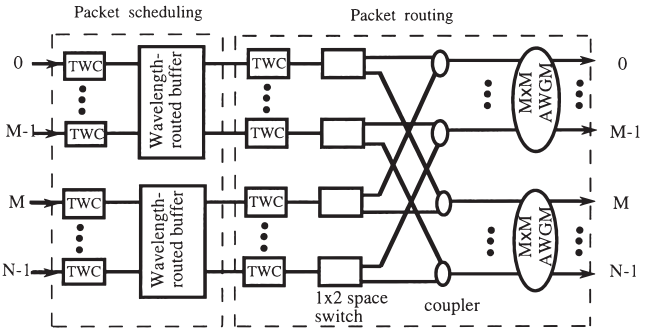

Fig. 7 Modified input-buffered wavelength-routed packet switch [33].

least 18 loop units to achieve a packet loss probability less than 10^{-6} for an 80% traffic load [18]. The complexity of this buffer structure is that an electronic controller (not shown in the figure) has to trace the number of packets in each loop unit, and to carry out forwarding of packets from one loop unit to the next loop unit, which could make the implementation complicated. Forwarding of packets could be avoided if the loop units are arranged in a parallel configuration.

In the above two switch architectures, switching of packets to its desired outputs is carried out before packet buffering. They effectively operate as an output buffered switch and hence achieve the best delay-throughput performance [50]. We have recently proposed a wavelength-routed input-buffered packet switch in which packet buffering is performed before packets are routed to their desired outputs [33], [51]. As a consequence, this packet switch has less complexity, which is in proportion to the switch size N, not N^2 or $N\log_2 N$, in comparison to other photonic packet switches [33]. This is achieved by using a new wavelength-routed packet buffer. The structure is shown in Fig. 6. The switch consists of two blocks: packet scheduling and packet routing. Similar to the Frontiernet packet switch, packet routing is performed by an AWGM in conjunction with a set of N tunable wavelength converters (TWCs), but no more than one packet will be directed to a given output of the AWGM at the routing block. Packet contention is prevented by packet scheduling in a way that each packet is allocated a minimum time delay subject to two conditions in any time slot: (i) no more than one packet is addressed to a given output of the routing block, (ii) only one packet can appear at any input of the routing block.

The packet scheduling block in Fig. 6 contains N TWCs and a wavelength-routed packet buffer. This wavelength-routed packet buffer consists of a pair of AWGMs connected by a set of fibre delay-lines of lengths ranging from 0 to (K−1)T. According to the routing principle of the AWGM (Table 1), a packet entering the buffer at the i-th input port will leave the buffer from the i-th output port after receiving a certain time delay determined by the packet wavelength. In an extreme case, a maximum of N packets from all the inputs can simultaneously access any single delay line without collision. Therefore, this wavelength-routed buffer is equivalent to N single-input single-output packet buffers, which share a common pool of fibre delay-lines through wavelength division multiplexing. Because no couplers or space switches are used, this packet switch has a potentially low power loss, independent of switch size. Simulation has shown that this wavelength-routed input-buffered packet switch can achieve a delay-throughput performance almost as good as the output-buffered packet switch and a very low packet loss probability [33], [51]. It has been shown that a set of 35 delay lines will be sufficient to obtain a packet loss probability less than 10^{-7} at a traffic load of 80%. Figure 7 shows how this architecture can be modified to double its switch capacity by adding additional blocks and 1×2 space switches, but without an increase in the number of wavelengths [33].

4.2 Broadcast-and-Select Packet Switches

The broadcast-and-select approach has been widely employed in photonic networks. With this approach, all the information from signal sources is multiplexed by a star coupler and distributed to all the receivers. Each receiver selects the desired packets. Both time-division multiplexing (TDM) and wavelength-division multiplexing (WDM) can be applied in this broadcast-and-select approach.

Shimatsu and Tsukada [32] have reported an ultrafast photonic ATM switch, known as the ULPHA switch, where an ultra high-speed optical TDM channel was used to broadcast ATM data cells. The architecture of this switch is shown in Fig. 8. The bit pattern of the electronic ATM cells is used to modulate the sequence of ultrashort optical pulses. Shrinking the interval between two consecutive pulses allows data cells from the different inputs to be time-multiplexed on a cell-by-cell basis and broadcast to all the outputs. The corresponding address data of cells are also time-multiplexed and broadcast to all the outputs, but at a different wavelength. Since an address data is much shorter than an ATM cell, the address data need not

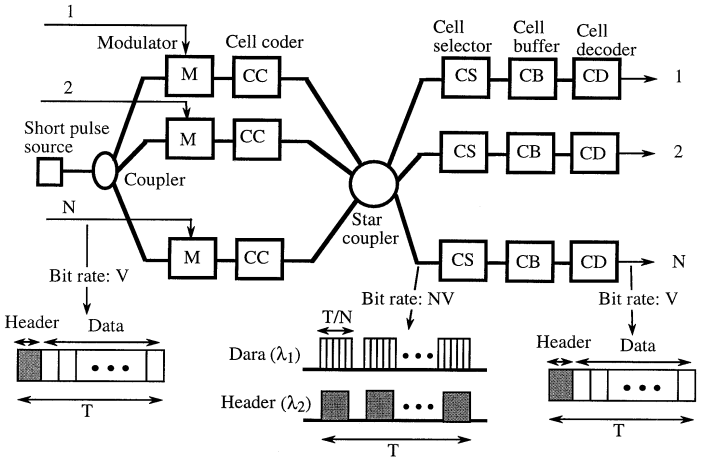

Fig. 8 ULPHA switch [32].

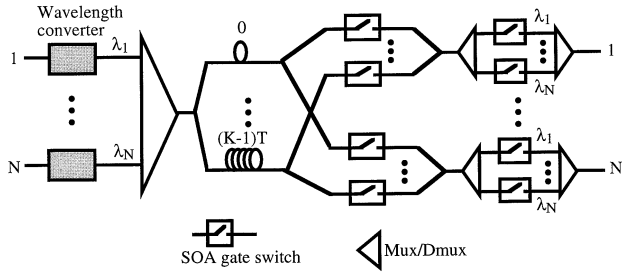

Fig. 9 Broadcast-and-select photonic packet switch [31].

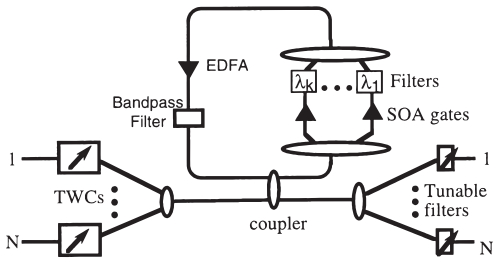

Fig. 10 Fibre loop memory switch [45].

to be time-compressed. This facilitates the detection of address data at each output of the switch. The difficulty with this packet switch is that a high-speed cell coder is required to compress cells at each input, and a cell decoder to decompress cells back into their original form at each output. To overcome this problem, an optical bit-interleaved multiplexing ATM switch was proposed in [53], in which bit-interleaved multiplexing was invoked, rather than cell-interleaved multiplexing. As a result, optical cell compression and decompression are not necessary. It is reported in [17] that by using both ultra high-speed TDM and WDM, the broadcast-and-select architecture can offer a very large switching throughput in the terabit per second range.

Chiaroni, et al. [31], have proposed and demonstrated another broadcast-and-select photonic packet switch, using multiple wavelengths to distinguish packets arriving at different inputs. The switch is shown in Fig. 9. Packets from different inputs are encoded on a different wavelength before they are combined at a star coupler, and then the combined WDM packets are broadcast and fed to a set of K optical delay-lines. Similar to the wavelength-routed packet switches (Figs. 4 and 6), this set of delay-lines is shared by all the packets. After propagating through the set of K delay-lines, each packet can receive any amount of delay ranging from 0 to (K−1) packet-times. Packets emerging at each delay-line are further broadcast to all of the output ports, where two sets of optical gate switches are used for packet selection. That is, at each output, the first set of gate switches selects a particular delay-line through which a desired packet arrives; the second set of gate switches in conjunction with a WDM demultiplexer-multiplexer pair chooses a wavelength at which the desired packet is encoded. In comparison to the above wavelength-routed packet switches, the advantage of this architecture is that it does not require any tunable components. But it has an optical power loss which is proportional to NK^2 and requires $N(N+K)$ gate switches to perform packet selection.

In [45], Bendelli, et al., proposed a simple broadcast-and-select photonic packet switch using a random wavelength accessible recirculating loop buffer. This switch is shown in Fig. 10. It consists of N tunable wavelength converters, one at each input, a random wavelength accessible recirculating loop buffer, and N tunable filters, one at each output. The random wavelength accessible recirculating loop buffer is shared by all the packets from all the inputs. Before entering the buffer, each packet is assigned a wavelength not being used by the packets within the buffer. All the packets in the buffer are broadcast to all the outputs. The tunable filter at each output selects appropriate packets by tuning its wavelength. The packets which are selected by the tunable filters are cleared out of the buffer by turn-

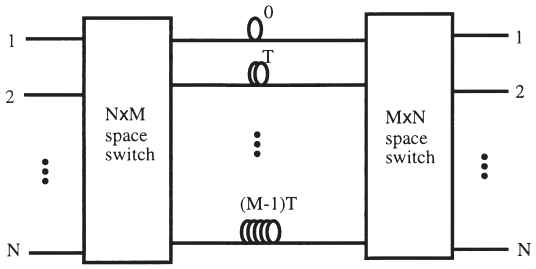

Fig. 11 Staggering switch [20].

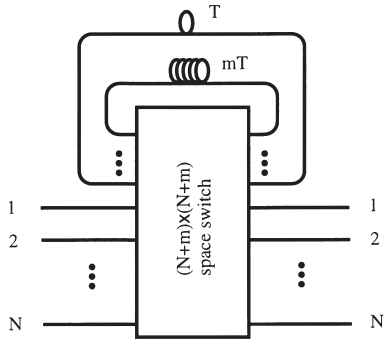

Fig. 12 Shared memory packet switch with recirculating loops [54].

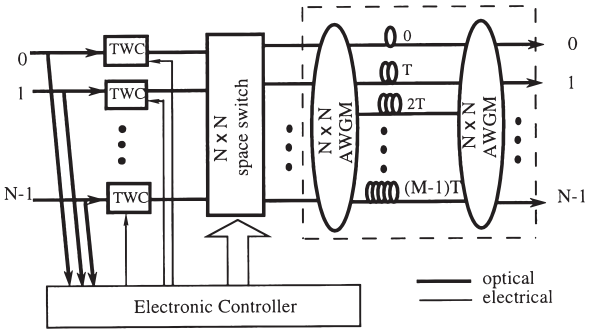

Fig. 13 Output-buffered photonic packet switch using a wavelength-routed packet buffer [33].

ing off the corresponding gate switches contained in the buffer. An electronic controller (not shown in the figure) maintains N packet queues each corresponding to one output of the switch. The capacity of this switch is limited by the tuning range of tunable lasers and filters, and the EDFA bandwidth. The solution is to use multiple loop buffers with a combination of optical space switches [4].

4.3 Space-Switch Based Photonic Packet Switches

Optical space-switches are key components in photonic packet switching systems. With either the wavelength-routed architecture or the broadcast-and-select architecture, optical space-switches are inevitable. A variety of optical space switches have been developed, including $LiNbO_3$ optical switches, InGaAsP/InP-based SOA gate switches, and silicon-silica based waveguide switches. In the context of photonic packet switching, they are required to have a switching speed in a range of several nanoseconds, low crosstalk, and low power loss. Generally, the switching time has to be less than 10% of a packet time to achieve a high utilization in transmission. Another important requirement is that they should be able to be monolithically integrated to reduce the cost and to increase the capacity. It is for these reasons that optical space switches made of SOA gates are most promising [9], [10]. We here describe several photonic packet switch architectures where optical space-switches play the major role in packet routing and buffering.

The Staggering switch [20] uses space switches to perform packet routing and buffering. The architecture of this switch is shown in Fig. 11. It consists of two nonblocking space switches that are interconnected by a set of optical delay-lines of different delay times. The first N×M space switch provides packets with access to the delay lines in a way that, at any time slot, no two packets arrive at the second space switch destined for the same output port, and hence packet contention is resolved. The second space switch routes the packets to their desired outputs. The delay-lines can also be arranged in a recirculating configuration [54], as shown in Fig. 12. A drawback with both of the above architectures is that packets arriving on the same input may leave the switch in the reverse order on the same output [20], [54].

Another space-switch based photonic packet switch, as described in [33], is shown in Fig. 13. Packet routing is performed by an N×N nonblocking space switch capable of broadcasting, while packet buffering is carried out by a wavelength-routed buffer in conjunction with a set of N tunable wavelength converters preceding the space switch. This is an output-buffered packet switch. There may be more than one packet destined for the same output in a time slot, resulting packet contention. However, this packet contention is resolved by wavelength conversion and wavelength-routing based buffering. More specifically, in each time slot, packets that are destined for the same output will be shifted to different wavelengths before they can be routed to the desired output by the optical space switch. Since these packets have been given different wavelengths by the wavelength converters at the input of the switch, they will receive different packet delays at the succeeding wavelength-routed buffer, so that only one packet will emerge at a given output of the switch in any time slot and hence packet contention is resolved. One difficulty with the space-switch based architecture is that the number of crosspoints (or SOA gates) required increases dramatically as the switch size grows.

In order to reduce the complexity of large buffers, a number of photonic packet networks and switches em-

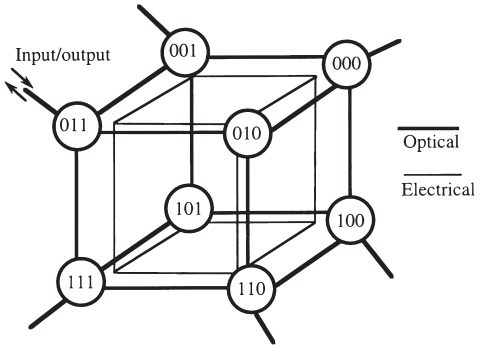

Fig. 14 HiPower photonic ATM switch [55].

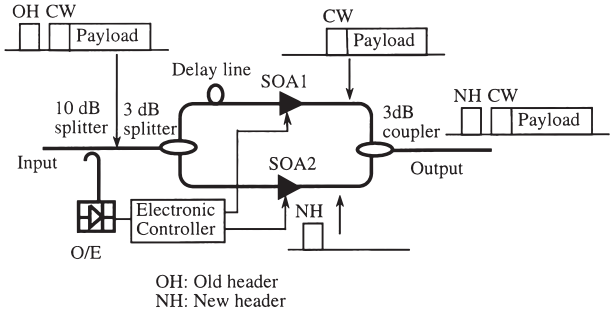

Fig. 15 Packet header replacement module [34].

ploy multihop and deflection routing approaches [23], [39], [63]. Here deflection routing means if more than one packet competes for a given output, only one packet is selected for the desired output, and the remaining packets are routed to other idle outputs, but they will eventually be routed to their desired outputs. Generally these packet networks and switches consist of small packet switch nodes, in which packets may have to traverse multiple nodes before they reach their destination. They can be configured with different topologies such as perfect shuffle or hypercube topologies [23], [39]. The advantage of such packet switches is that they can be implemented by using small space switches and only a small packet buffer is required if deflection routing is used. Figure 14 shows a multihop packet switch architecture reported in [55], using a hypercube topology. For an n-dimensional hypercube packet switch, it consists of $N=2^n$ nodes, each being a small $(n+1)\times(n+1)$ packet switch. Each node is allocated an n-bit binary address. The addresses of adjacent nodes differ by only one bit, which simplifies packet routing control [55]. A link between two adjacent nodes has a length of exactly one or multiple packet times, acting as a packet buffer. There is an electronic layer which has exactly the same topology as the optical layer to control packet routing. Because deflection routing is invoked, only a small packet buffer is required at each local input and output port [55], [56].

5. Packet Header Replacement and Synchronization

With connection-oriented packet-switched networks such as ATM-like networks, the routing information contained in the packet header is known as the virtual circuit number (VCI) and virtual path number (VPI). When packets transverse a switch node, the VCI and VPI are used to identify the output port of the switch by looking up a local routing table. To make the routing table as small as possible and to make the packet header as short as possible, the VCI and VPI contained in the packet header only have a local meaning. This means that the packet header has to be replaced by a new one before the packet is delivered to the next node. In the context of photonic packet switching, optical replacement of packet header is necessary [34]. So far two different methods have been proposed to optically implement the packet header replacement.

In 1993, Spring, et al. proposed and demonstrated a novel technique for optical packet header replacement. The technique introduces a continuous wave (CW) portion between the header and payload when a packet is generated at the source node. As a packet traverses through a switch node, the old packet header is removed from the packet. A copy of the CW portion is modulated by the new header data and is then affixed in the place of the old packet header. Figure 15 shows an implementation of this packet header replacement. It mainly consists of two SOA gates: SOA1 and SOA2. During the packet header period, SOA1 is turned off so as to remove the old packet header, while SOA2 is used to modulate a copy of the CW portion with the new header data and to block the other portions of the packet. An optical delay line of a length equal to the packet header time is inserted before SOA1 to adjust the timing so that the new packet header exiting SOA2 is exactly in the place of the old packet header.

An alternative technique is to use wavelength conversion [60]. With this technique, the payload of the original optical packet is used to optically modulate a CW light at a different wavelength, and while the new header data electronically modulates the same CW light within the place of the old header. Figure 16 shows an example of this technique, where cross-gain compression in SOAs is assumed to perform wavelength conversion. The architecture contains two SOA gates: SOA1 and SOA2. During the packet header period, SOA1 is turned off to block the old header. At the same time, the new header data electrically modulates the CW light at SOA2. The payload of the packet passes through SOA1 and then optically modulates the CW light at SOA2. This wavelength conversion approach does not require an additional CW portion inserted between the packet header and the payload, and hence can more effectively use the transmission bandwidth.

As discussed in Sect. 4, wavelength conversion can play an important role in routing and buffering. By in-

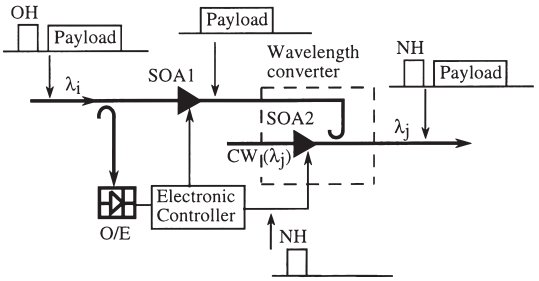

Fig. 16 Packet header replacement using wavelength conversion.

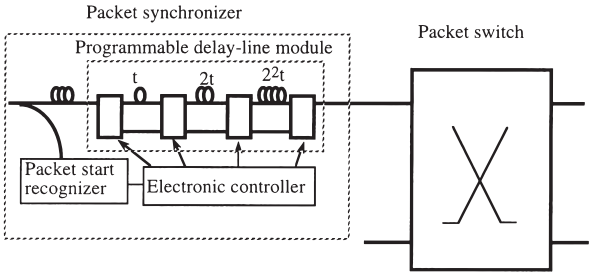

Fig. 17 Schematic of packet synchronization.

tegration of the packet header replacement with wavelength routing or buffering, an exclusive wavelength converter for use in the packet header replacement is not necessary. More importantly, some studies have also shown that optical wavelength conversion capable of regenerating optical pulse signals can significantly remove accumulated noise and crosstalk [58]–[60], and hence improve the cascadability of optically transparent packet switching nodes [57], [60].

Most of the proposed photonic packet switches assume that packets are synchronized at the switch inputs. This is because synchronous operation can simplify the implementation of packet contention resolution, and subsequent buffering and routing. However, all fibre spans interconnecting nodes cannot be designed as integer numbers of the packet duration T. In addition, a slow temperature change would induce variation in path length. Therefore, packet synchronization is necessary for large photonic packet switches. A general implementation of packet synchronization is shown in Fig. 17, which consists of a packet start recognizer and a programmable delay line module [61], [62]. The function of the packet start recognizer is to identify the packet start [61]. Once the packet start is detected, the arrival time of packets can be adjusted by setting the appropriate path within the programmable delay line module [61], [62]. The programmable delay line module can be implemented by a sequence of delay lines and optical space switches, as shown in Fig. 17. The resolution of tunable time is restricted by the number of stages used in the delay line module. If the maximum delay is D and the number of stages is n, the resolution of tunable time is given by $D/2^n$. A fine tuning of delay time can be realized by a tunable wavelength converter and a length of high dispersion fibre [62].

Packet synchronization may substantially increase the hardware complexity. For photonic packet networks that use small switch nodes and multihop routing approaches, asynchronous operation would be useful. This has been demonstrated in a 2×2 input-buffered photonic packet switch [27].

6. Conclusion

Recent advances in photonic technologies and the anticipation of multi-functional telecommunication networks with a very large switch capacity in the terabit per second range have been the driving force in research and development of photonic packet-switched networks. We have reviewed various approaches and techniques to photonic packet switching. It has been shown that the lack of optical equivalents to electronic random access memories and electronic processing capabilities has resulted in the hybrid optoelectronic implementation of photonic packet switching systems. The switching and routing fabric has generally been implemented optically, in order to capitalize on the optical transparency and large bandwidth; while electronic and optoelectronic components remain the important role in such functions as address processing, switching and buffering controls. To achieve satisfactory performance, significant efforts are required in developing key devices and components such as semiconductor optical amplifiers, optical gates and space switches, wavelength converters, fast tunable lasers and filters, and wavelength routers. Along with the developments, new approaches to buffering are needed. Photonic implementation of packet header replacement and synchronization is another key in the implementation of truly optically transparent packet switching systems.

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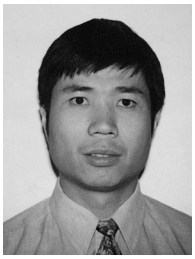

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