

# All-Optical Signal Processing and Applications Within the Esprit Project DO\_ALL

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**Abstract**—This paper reviews the work performed under the European ESPRIT project DO\_ALL (Digital Optical Logic modules) spanning from advanced devices (semiconductor optical amplifiers) to all-optical modules (laser sources and gates) and from optical signal processing subsystems (packet clock recovery, optical write/store memory, and linear feedback shift register) to their integration in the application level for the demonstration of nontrivial logic functionality (all-optical bit-error-rate tester and a  $2 \times 2$  exchange-bypass switch). The successful accomplishment of the project's goals has opened the road for the implementation of more complex ultra-high-speed all-optical signal processing circuits that are key elements for the realization of all-optical packet switching networks.

**Index Terms**—All-optical packet switching, all-optical signal processing, semiconductor optical amplifiers (SOAs), ultrafast nonlinear interferometer.

## I. INTRODUCTION

**I**N recent years, the remarkable advance, maturity, and cost reduction of optical devices and components has intensified research for the realization and exploitation of all-optical signal

processing techniques and systems [1]–[7]. One of the research areas in which all-optical signal processing systems are likely to provide a cost/performance benefit over their electronic counterparts is optical packet switching, which is considered as the means toward the construction of efficient, ultrahigh capacity, global data networks [8]–[14]. Internet-related services and Internet protocol (IP) traffic have been growing, and this is creating the need for the development of intelligent optical networks that avoid intermediate layers, such as synchronous digital hierarchy (SDH) and asynchronous transfer mode (ATM), in an affordable way [15]–[19]. For efficient resource utilization in optical packet switching, the optical layer must possess the ability of changing the connectivity between nodes during the time scale of a packet and possibly to allow for some limited processing at the bit level.

The purpose of the DO\_ALL project has been to research and further in an organized way the state-of-the-art in high-speed all-optical logic and to develop novel signal processing concepts and technologies. In this respect, DO\_ALL has defined, designed, and developed the necessary set of devices and modules required for the construction of optical logic circuits and has applied them into application experiments of nontrivial functionality to qualify their performance and limitations. Within this frame, the applications that have been explored in depth are 1) the demonstration of all-optical bit-error-rate (BER) measurements capability and 2) the demonstration of an optically addressable exchange-bypass switch using all-optical techniques. The first application was selected so as to investigate whether it is possible to build a complex optical circuit consisting of several optical logic modules that would challenge in performance the corresponding electronic designs. The second application was chosen so as to demonstrate that the logical functionality of optical circuits is advantageous since in this instance one optical gate can replace several electronic gates.

In order to achieve its goals, the DO\_ALL project has demonstrated concepts and technologies across the chain spanning from advanced devices, modules, and subsystems and their integration to the application level. More specifically, contributions have been made in key areas of optical signal processing, including the demonstration of the following:

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- 1) improved optical semiconductor devices, consisting of high-gain optical amplifiers and high-speed distributed feedback (DFB) lasers;
- 2) a variety of fiber laser sources operating up to 40 GHz;
- 3) Boolean logic capability of optical gates up to 40 Gb/s;
- 4) clock-recovery schemes that are compatible with optical gates and can be used for their synchronization;
- 5) addressable optical memories/buffers directly applicable to optical packet storage;
- 6) the logical functionality of optical gates that may be used to replace the equivalent of several electronic gates;
- 7) optical logic circuit designs with feedback, such as optical linear feedback shift registers (LFSRs).

Furthermore, the outcome of the project has allowed to extract useful guidelines concerning the conditions under which the semiconductor optical amplifiers (SOAs) and gates must be ideally operated for optimum performance and to exploit them in the demonstration of enhanced nontrivial logic functionality through the development of more complex all-optical circuits. In this sense, DO\_ALL has played the crucial role of the technological precursor for a number of research activities that have followed its conclusion.

The partners that contributed to the DO\_ALL project were the Photonics Communications Research Laboratory (PCRL) of the National Technical University of Athens, Athens, Greece; the Swiss Federal Institute of Technology Zurich (ETHZ), Zurich, Switzerland; the Femtosecond Optics Group at Imperial College, London, U.K.; Acterna GmbH, Eningen, Germany; Optospeed Switzerland; Opto Speed Deutschland, Darmstadt, Germany; and Deutsche Telekom.

This paper aims at presenting the main results obtained within the frame of the project. The remainder of the paper is organized as follows. Section II presents the high-performance semiconductor devices and laser sources that were developed within the project, with characteristics that make them applicable to all-optical signal processing systems. Section III addresses the all-optical logic modules implemented with the SOA-based ultrafast nonlinear interferometer (UNI) and focuses on their exploitation as basic building blocks to demonstrate AND and XOR Boolean gates, a packet all-optical clock-recovery circuit, an all-optical write/store memory, and an all-optical LFSR. Section IV analyzes the design issues related to the realization of an optical bit-error-rate tester (BERT). Finally, Section V summarizes the results from the demonstration of an optically addressable  $2 \times 2$  exchange-bypass switch that may be used in optical packet switch fabrics.

## II. HIGH-PERFORMANCE SEMICONDUCTOR DEVICES AND LASER SOURCES

### A. Semiconductor Optical Amplifiers

The significance of the design and development of high-performance SOAs lies on the fact that their amplification characteristics are not used only to amplify optical signals but are also combined with their dynamic behavior in gain and phase to perform switching functions [20], [21]. The objective was to fabricate SOAs that are fast enough to be used in all-optical

TABLE I  
TYPICAL VALUES OF THE MAIN PARAMETERS OF A 1500- $\mu\text{m}$ -LONG SOA

Parameter	Value	Unit
ASE output power	10.4	mW
ASE peak wavelength	1565	nm
ASE ripple	< 0.7	dB
Small signal gain (fiber-to-fiber)	32	dB
Output saturation power	11.5	dBm
Polarisation dependence	6	dB
10-90% gain recovery time	50	ps

gates operating at 40 Gb/s and to integrate them into fully packaged modules. During the DO\_ALL project, improved SOAs, in terms of gain and speed operation, were designed and developed, and their dynamical behavior was studied experimentally and theoretically.

The SOAs had a bulk InGaAsP-/InP ridge waveguide structure. Amplifiers with active region lengths between 250 and 2000  $\mu\text{m}$  were manufactured. For the reduction of the facet reflectivity, the waveguide was  $10^\circ$  tilted with respect to the output facets and a two-layer antireflection (AR) coating ( $\text{SiO}-\text{Al}_2\text{O}_3$ ) was evaporated on each facet. The DO\_ALL SOA chips were pigtailed with lensed fibers using an active alignment technique. Typical coupling losses were approximately 3 dB per facet. The amplifiers were fully packaged into temperature-stabilized modules.

The performance of the fabricated SOAs was characterized, and Table I summarizes typical parameters of a 1500- $\mu\text{m}$ -long SOA. All values shown in this table were recorded at  $20^\circ\text{C}$ , with a bias current of 750 mA. The amplifier had a maximum chip gain of 38 dB, resulting in a fiber-to-fiber gain of 32 dB. The gain ripples were lower than 0.7 dB, corresponding to an overall reflectivity of less than  $6 \cdot 10^{-6}$ .

A useful insight into the nonlinear capabilities of an SOA can be obtained from the investigation of the temporal evolution of the gain recovery time of the amplifier. This parameter represents a good estimate of the speed of the SOA. In [22], measurements and calculations of the gain recovery time have been presented, and it has been shown that it can be shortened by exploiting the holding beam technique [23] to deplete the carrier density of the amplifier. It has been also demonstrated that longer SOAs have shorter recovery times, and a 10%-90% gain recovery time of 50 ps has been achieved in a 1500- $\mu\text{m}$ -long SOA. These findings have been confirmed by pump-probe measurements of the gain dynamics at 10 and 40 GHz. The pump signal was provided at 1550 nm with a pulse energy of 170 fJ, and the amplifier gain was measured with 5.37-fJ probe pulses at 1540 nm. Fig. 1 depicts the normalized probe transmission at 10 and 40 GHz for a 500- and 1500- $\mu\text{m}$  bulk SOAs biased at 250 and 750 mA, respectively, in a copropagating fashion for the pump and probe signals. In the 1500- $\mu\text{m}$  device, the gain recovered almost back to the unsaturated level at 10 GHz, as opposed to the 500 one. Thus, the recovery time decreased with the increase of the SOA length. Fig. 1 also indicates that the 1500 SOA recovers faster than the 500 amplifier at 40 GHz.

Based on the feedback that experiments give to theory, a new optimized frequency-domain model of the SOA gain dynamics

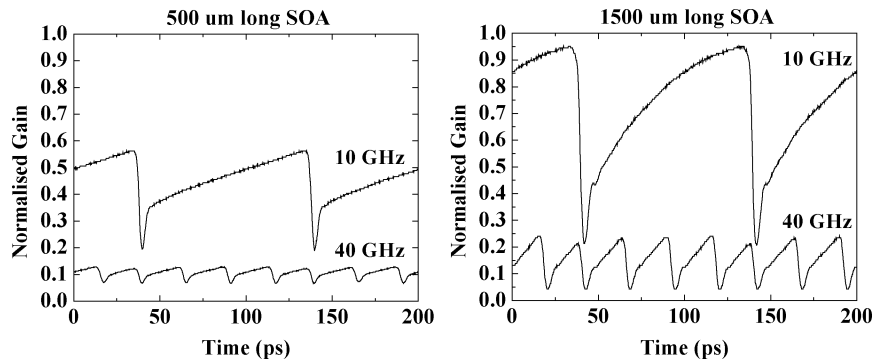


Fig. 1. Normalized probe transmission at 10 and 40 GHz for 500 and 1500 SOAs.

was developed [22], which includes a position- and time-dependent carrier lifetime and the effect of amplified spontaneous emission (ASE). Compared with a constant lifetime model, it allows more accurate simulation of the recovery dynamics in SOAs of various lengths. This model has been very helpful in exploring the possibility of using the SOA intraband effects for ultrafast all-optical signal processing applications.

The gain-recovery dynamics in Fig. 1 exhibit two time constants. The slower recovery described previously is governed by carrier density pulsations as a result of electrical pumping. The fast compression, on the other hand, results from intraband effects, mainly carrier heating and spectral hole burning. This intraband recovery time is of the order of 1 ps and thus considerably shorter than the interband recovery time. The intraband gain-recovery time and the gain compression induced by subpicosecond pulses in various SOAs have been experimentally and numerically investigated, and it has been shown that these effects depend on the operational conditions of the SOAs [24].

The performance of all-optical gates based on the cross-phase modulation (XPM) mechanism can be evaluated knowing the phase-shift magnitude that is obtained using an SOA as the nonlinear medium [25]. The phase is often deduced from the gain using the gain-phase coupling coefficient (also called the alpha factor). We define the effective alpha factor as  $a_{\text{eff}} = -0.5 \cdot \Delta\Phi / \ln(G_{\text{max}}/G_{\text{min}})$ , where  $\Delta\Phi$  is the phase shift and  $G_{\text{max}}$  and  $G_{\text{min}}$  are the maximum and minimum gain values associated with the (slow) gain recovery, respectively. In [26], experimental and theoretical results on the variation of the effective alpha factor for different amplifier lengths and average current density have been presented. Fig. 2 shows qualitative agreement between theory and experiment, indicating that  $a_{\text{eff}}$  increases with bias current and amplifier length.

The results obtained from the detailed studies of the SOA dynamics have indicated that for all-optical switching applications in interferometric gates, at speeds of 40 Gb/s and beyond, long SOAs driven at high current densities must be employed. Furthermore, the theoretical and experimental investigation of the SOA's ultrafast saturation properties have revealed that they have the potential for exploitation in various all-optical signal-processing tasks depending on their degree of saturation. More specifically, they can find application in the development of all-optical gates, if they are biased to operate in the low-gain saturation regime, and as laser sources and clock recovery circuits if they are biased to operate in the heavy-gain saturation

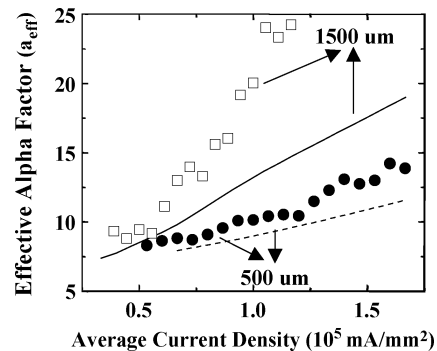


Fig. 2. Measured data and simulation results of effective alpha factor versus current density of 500  $\mu\text{m}$ -long (black circles and dashed line, respectively) and 1500  $\mu\text{m}$ -long (white squares and solid line, respectively) SOAs.

regime, as it will be described in the following subsection as well as in Section III.

### B. Laser Sources

High-repetition-rate, short-pulse laser sources are key elements for the realization of all-optical, signal processing circuits, as they provide the clocks of the optical gates. Within DO\_ALL, significant effort has been invested in the development of appropriate clock and pattern sources, including pulse compression and bit interleaving techniques, but here we will restrict the discussion to the laser sources only.

Several techniques have been investigated, and these have included high-speed gain-switched and mode-locked DFB laser diode sources [27], a variety of short-pulse fiber mode-locked ring laser sources operating up to 40 GHz [28]–[32] and DFB and electroabsorption modulators with a nonlinear compression source [33]. More recently, a novel method for multiplying the repetition rate of a local-clock laser oscillator by optical means from 10 to 40 GHz with less than 0.25-dB and 650-fs amplitude modulation and timing jitter, respectively, has been demonstrated using a Fabry–Pérot filter (FPF) followed by an SOA [34]. The FPF is chosen so as to have a free spectral range (FSR) that is a multiple of the laser repetition frequency and equals the desired repetition rate of the transmitter. The method relies on the property of an FPF that its time-domain impulse response is an exponentially decaying sequence of pulses at a repetition frequency equal to its FSR and whose decay constant is determined by the filter finesse ( $F$ ). As a result, the pulse train at the output of the FPF displays an amplitude modulation, which can

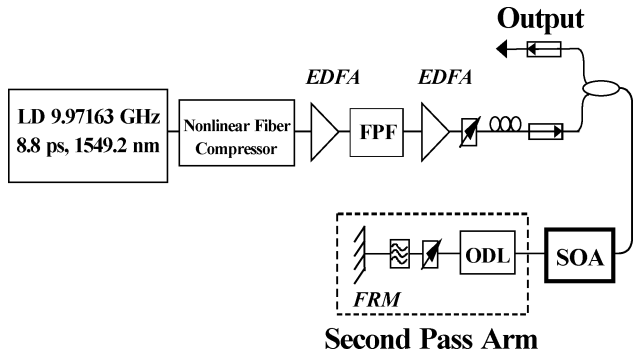


Fig. 3. Experimental setup of 10–40-GHz-rate multiplier. ODL: Optical delay line; FRM: Faraday rotator mirror.

be reduced by the SOA provided that it is operated under heavy saturation, well into its nonlinear regime. In this manner, pulses with higher energy at its input receive less gain than pulses with lower energy, resulting thus in a reduced amplitude modulation. Furthermore, the experimental observations revealed that if the amplitude equalizing property of the SOA is used successively, and especially twice, the output pulse train can exhibit nearly zero amplitude modulation. This is due to the fact that the second pass through the SOA is particularly effective at equating the amplitudes of the pulse train, since it can be used in conjunction with the gain recovery of the SOA by appropriate temporal synchronization of the two pulse trains. The proposed scheme is relatively simple to implement and can be easily upgraded to higher repetition rates without the need to change optical sources or laser driver electronics.

The experimental setup is shown in Fig. 3. The initial pulse train was produced by a gain-switched DFB laser, operating at 1549.2 nm. The laser yielded 8.8-ps pulses at a repetition rate of 9.971 63 GHz, after linear compression through dispersion-compensating fiber (DCF) with a total negative dispersion of 54.27 ps/nm. The laser output pulses were then amplified in an erbium-doped fiber amplifier (EDFA) and had their temporal width reduced in a two-stage nonlinear fiber compressor comprising of alternating sections of dispersion-shifted fiber (DSF) and single-mode fiber (SMF). By filtering the compressor output with a 2-nm filter, 3.2-ps nearly transform-limited hyperbolic secant pulses were obtained. The pulse train was further amplified and fed into the Fabry–Pérot filter. The FPF was an AR-coated fused quartz substrate with an FSR equal to 39.886 52 GHz and a finesse of 50. After exiting from the FPF, the signal was reamplified and inserted in a 3-dB coupler used for monitoring and to provide the output of the source on its return path from the SOA amplitude equalization stage. Following the 3-dB coupler, the signal was introduced into a commercially available 1.5-mm-long SOA (Optospeed S.A.). This had small signal gain of 24 dB at 1549.2 nm, 3-dB polarization gain dependence, a 10%–90% gain-recovery time of 80 ps, and 10-fJ saturation energy, when driven with 700-mA dc current. After passing once through the SOA, the pulse train entered the second-pass arm. Here, it was filtered in a 2.8-nm bandpass filter and was reflected back again into the SOA by a Faraday rotator mirror (FRM). An optical delay line (ODL) was used in the second-pass arm to provide adjustment of the

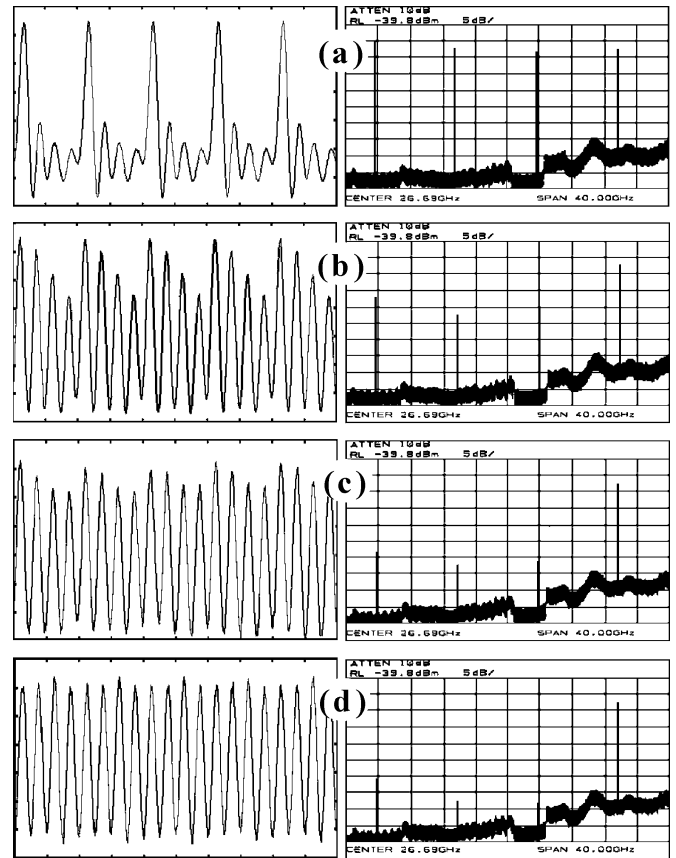


Fig. 4. Oscilloscope traces and corresponding radio-frequency (RF) spectra at (a) compressor output, (b) FPF output, (c) output after first SOA pass, and (d) output after second SOA pass. The oscilloscope trace time base is 50 ps/div. The RF spectra amplitude scale is 5 dB/div, and the frequency scale is 4 GHz/div.

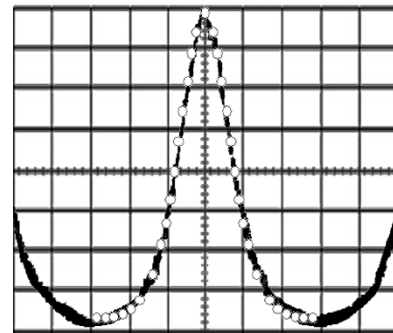


Fig. 5. Second harmonic autocorrelation trace. The white dots indicate the fitted hyperbolic secant autocorrelation profile. The time base is 3.66 ps/div.

temporal synchronization between the counter-propagating pulses. Variable optical attenuators were used before the SOA inputs to adjust the power level of the first- and second-pass signals.

Fig. 4 shows the experimental results at different points of the setup monitored on a sampling oscilloscope and a microwave spectrum analyzer. Fig. 4(a) illustrates the oscilloscope trace and the corresponding microwave spectrum of the initial 10-GHz clock signal. Fig. 4(b) displays the signal at the output of the FPF, showing a 40-GHz clock pulse train with 1.65-dB amplitude modulation (highest to lowest pulse power ratio). Fig. 4(c) shows the pulse train after its first pass

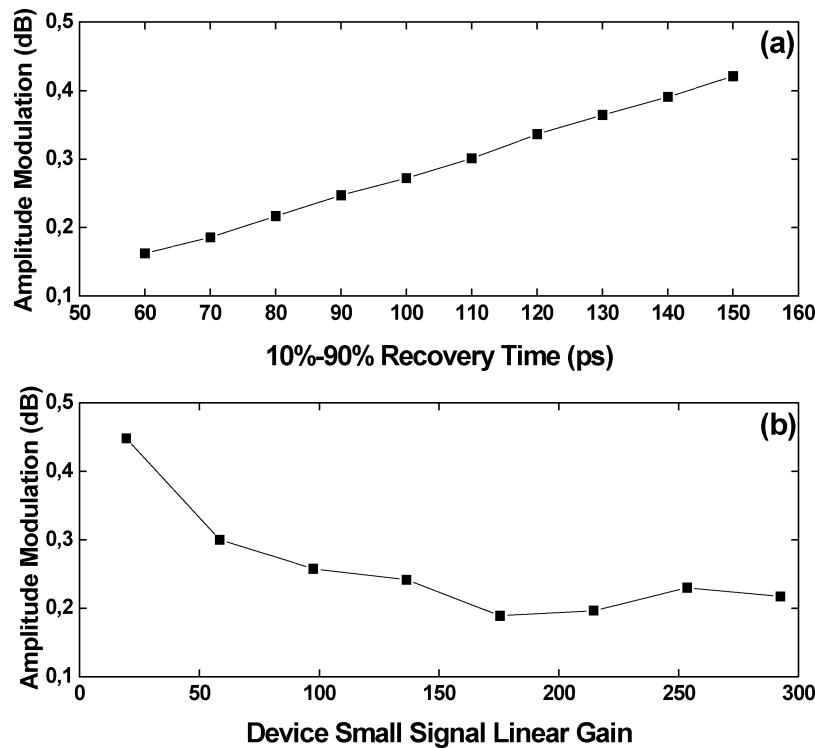


Fig. 6. (a) Amplitude modulation versus SOA recovery time and (b) amplitude modulation versus device small-signal gain.

through the SOA, with its amplitude modulation reduced to 0.8 dB. Finally, Fig. 4(d) shows the signal after its second pass through the SOA. This time the amplitude modulation recorded on the sampling oscilloscope was reduced to 0.15 dB. The corresponding microwave spectrum reveals that the combination of the FPF with the double pass through the SOA has resulted in effective suppression in excess of 26 dB of the 10-GHz component, while the 20- and 30-GHz frequency components are suppressed by approximately 35 dB. Analysis of the spectrum at the output of the source using the inverse Fourier series indicates that the amplitude modulation of the signal is below 0.25 dB, which is in close agreement to the measurements made with the sampling oscilloscope. Spectral analysis also showed that the timing jitter was less than 650 fs. The temporal width of the output 40-GHz pulses was measured using an second harmonic generation (SHG) autocorrelator, and Fig. 5 shows the resulting autocorrelation trace. Assuming a hyperbolic secant profile, the output pulses have a full-width at half-maximum (FWHM) of 3.8 ps. This is marginally increased from 3.5 ps at the input of the SOA primarily due to modal gain difference and birefringence in the SOA. The output power of the source was 680  $\mu\text{W}$ .

In order to obtain the results shown in Fig. 4(d), the optical power and relative timing of the signals for the two passes in the SOA must be appropriately adjusted. The input powers of the pulse trains before entering the SOA were 850  $\mu\text{W}$  for the first and 80  $\mu\text{W}$  for second pass, respectively. These input powers correspond to a mean energies/pulse of 25 fJ for the first pass and 2 fJ for the second pass. With these input powers, the SOA operated in a deeply saturated regime, but the degree of saturation and recovery is primarily determined by the first-pass pulse train. In contrast, the second-pass signal has low energy value

and accesses the saturated amplifier gain. Arranging the temporal adjustment of the second-pass signal with respect to the first pass using the ODL, it is possible to use the gain recovery of the SOA as an additional parameter to enhance the amplitude equalization of the SOA for the second-pass pulse train. It was found that optimized performance is obtained when the second-pass pulses enter the SOA just after their equivalents from the first-pass exit and that is with a delay of approximately 5 ps.

In principle, rate multiplication with approximate amplitude equalization could also be achieved with a single FPF of high finesse [35]. For example, to achieve amplitude modulation of 0.25 dB in the rate-multiplied pulse train with a single FPF, simulations have shown that its finesse must be equal to 325, and this figure grows more if the amplitude modulation must be further reduced. In this case, the filter has very sharp resonance peaks so that it may be harder to construct and less practical as it will display no tolerance on variations of the input line rate.

A simulation tool was developed in order to provide insight on how the gain and recovery time of the SOA affect the resulting amplitude modulation and assess whether this technique can be used for higher rates or for simultaneous multiplication of several different wavelength sources. The simulation tool was based on the equations for gain saturation and recovery derived in [36], modified to take into consideration the presence of the double-pass signal in the amplifier and was used with the parameters of the experimental setup. Fig. 6(a) shows the amplitude modulation with respect to the SOA recovery time and displays an almost linear increase of the amplitude modulation with the recovery time. This is to be expected, since in faster SOAs, the gain excursions will be larger during amplification, reducing the amplitude modulation. However, this result is important because

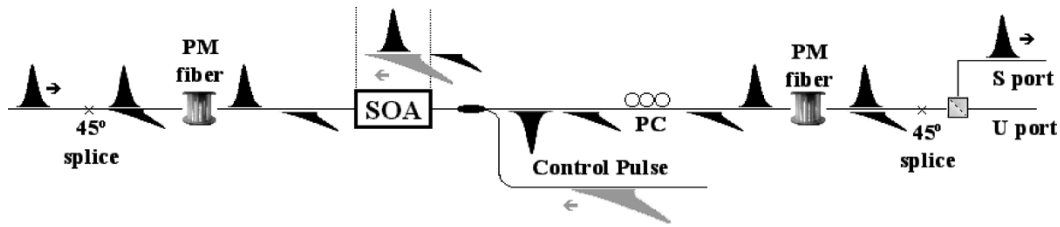


Fig. 7. Principle of operation of UNI switch.

it shows that at least in principle this rate multiplication and gain equalization technique should be extendable to achieve higher multiplication factors to higher rates. Fig. 6(b) shows the resulting minimum amplitude modulation of an input pulse train of 1.65-dB modulation, after a double pass through an SOA with a saturation energy of 10 fJ and optimized synchronization of the two pulse trains. Low amplitude modulation can be achieved for a gain region between 21 and 25 dB, in close agreement with the experimental results. For small variations of the gain parameter within this regime, no significant changes on the amplitude modulation take place. This shows that a single SOA can in principle be used to simultaneously multiply the repetition frequency of several laser sources at different wavelengths with the same FPF and SOA, provided that the small-signal gain varies within a certain range, and that they are temporally synchronized in the SOA.

### III. DIGITAL FIBER LOGIC MODULES

Within the frame of the DO-ALL project, two types of SOA-assisted optical logic modules were designed, developed, and evaluated using either polarization or wavelength for signal input discrimination in order to perform single control, dual control, and feedback experiments. The SOA-assisted Sagnac interferometer architecture (dual branch, counterpropagating signal, and control pulses) was initially investigated [37]–[40], while the effort concentrated later on the ultrafast nonlinear interferometer (UNI) architecture (single branch, counterpropagating signal, and control pulses) [41]–[44]. Both configurations exploit the optically induced fast nonlinearities in the gain and refractive index of an SOA due to carrier changes [44]. In this section, we report on results obtained with the UNI configuration.

The concept of operation of the UNI switch relies on the polarization rotation of an incoming clock signal to be switched in the presence of a switching/control signal in an SOA [42]. The incoming clock pulse is split into two orthogonal polarization components, which are relatively delayed in a length of birefringent fiber before entering into the SOA. For single logic rail operations, one of these two components (black-colored pulse on the left-hand side) is temporally synchronized with the control pulse (gray-colored pulse), as shown in Fig. 7. This causes a local, time-dependent refractive-index change in the SOA, which in turn imparts a phase change only on the synchronized polarization component. On exiting the SOA, the relative delay between the two polarization components is removed with a polarization-maintaining fiber (PMF) of equal birefringence, and they interfere on a polarization beam splitter (PBS). In the presence of the control signal, the clock signal exits through the

so-called switched port (S) of the interferometer, while in its absence it exits from the other port of the PBS, which is called the unswitched port (U). One advantage of this switch geometry is that long-lived nonlinearities (i.e., those that recover on time scales longer than the temporal pulsewidth) in amplitude and phase are balanced out to first order, as they are equally perceived by the two orthogonal polarization components of the clock signal. On the other hand, short-lived nonlinearities, such as carrier heating and instantaneous virtual electronic processes, are induced only on the clock component that overlaps with the control signal inside the SOA so that ultrafast differential phase modulation between the two orthogonal clock components can be achieved.

From an application perspective, the UNI switch possesses the practical advantages of multiterminal operation, which is important for the demonstration of ultra-high-speed all-optical Boolean functions, and interferometric stability since all signals travel along the same optical path. Moreover, when the UNI is used with signal and control inputs that have identical wavelength, it may be cascaded without the need for wavelength conversion. The UNI switch has been shown to have the potential for speeds beyond 100 Gb/s in a copropagating configuration [45], [46] and 40 Gb/s in a counterpropagating configuration [47], at least for single rail logic operations.

Within the frame of DO-ALL, the UNI switch was exploited in the SOA low- and heavy-gain saturation regime to demonstrate all-optical Boolean AND and XOR operations and an optical clock-recovery circuit, respectively, as well as in a feedback configuration to demonstrate an optical write/store memory and an optical LFSR, according to the description in the following subsections.

#### A. AND Gate

If the SOA in the previously described UNI configuration is biased to operate in the low-gain saturation regime, then the AND gate can be implemented. More specifically, the output signal at the S-port of the switch is the logic AND operation between the two data signals (input and control). Alternatively, the input signal can be a full duty-cycle signal (clock) so that the control or data signal is imprinted on the clock signal at the S-port of the switch and its complementary at the U-port. Within the frame of DO-ALL, the UNI switch has been evaluated for an AND operation with clock and control signals at a 10-, 20-, and 40-GHz repetition rate.

Fig. 8 shows the block diagram of the UNI switch configured as an AND gate. The clock (input signal) and data (control) signals were produced from a 10-GHz gain-switched DFB laser diode operating at 1554.3 nm and producing 8-ps pulses

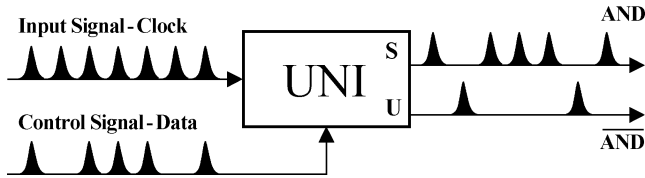


Fig. 8. Block diagram of the UNI switch operating as an AND gate.

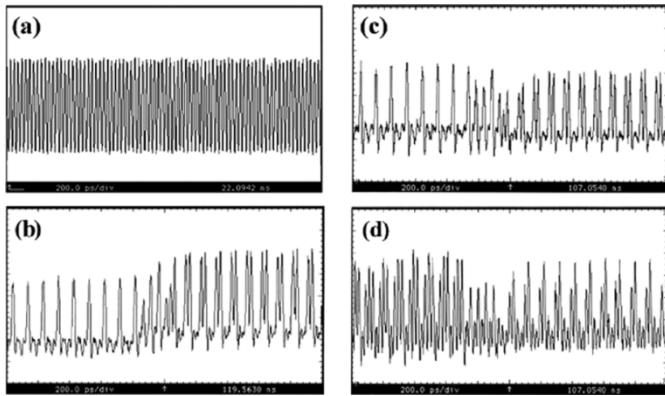


Fig. 9. Oscilloscope trace of (a) the 40-GHz clock signal, (b) the 40-Gb/s control pattern, (c) the result of the AND operation at the S-port, and (d) the corresponding result at the U-port. The time base is 200 ps/div.

after linear compression. The 40-GHz clock and 40-Gb/s pattern signals were generated by rate multiplication with bit interleaving. The active switching element in the UNI was a 1500-long bulk InGaAsP-InP ridge waveguide-type SOA with 30-dB small-signal gain at 1561-nm (29-dB gain at 1554.3 nm) and 80-ps recovery time when driven with a 700-mA dc current. The two PMFs of the switch had identical lengths and introduced 12.5-ps relative delay between the orthogonal polarization components of the clock signal.

Successful Boolean AND operation between the clock and control is accomplished when the switched port of the gate records a logical “1”, if the corresponding bit of control is logical “1”, and a logical “0” if the corresponding bit of control is logical “0”. Fig. 9 shows the signals through the switch monitored with a 40-GHz photodiode and sampling oscilloscope and in particular (a) the 40-GHz clock signal, (b) the 40-Gb/s control pattern, (c) the result of the AND operation between the clock and control pulses at the S-port, and (d) the corresponding result of the AND operation at the U-port. The contrast ratio between logical “1” and logical “0” was 10:1 and 4:1 at the S- and U-ports, respectively. This essentially implies that the S-port of the gate must be preferably used in switching applications. In this configuration, the optimum pulse energies for the clock and control signals were 3 and 16 fJ, respectively.

The BER performance of the UNI configured as an AND gate was also analyzed with a SDH/STM-64 Network Analyzer. The switched port of the gate was detected at the receiver of the network analyzer, and the BER was statistically estimated to be  $10^{-11}$ . Fig. 10 shows the recorded eye diagrams. More specifically, Fig. 10(a) and (b) depicts the eye diagrams of the data (input signal) and clock (control signal) signals respectively, while Fig. 10(c) and (d) displays the S-port (upper graph) and the U-port (lower graph) of the switch in the presence and in the

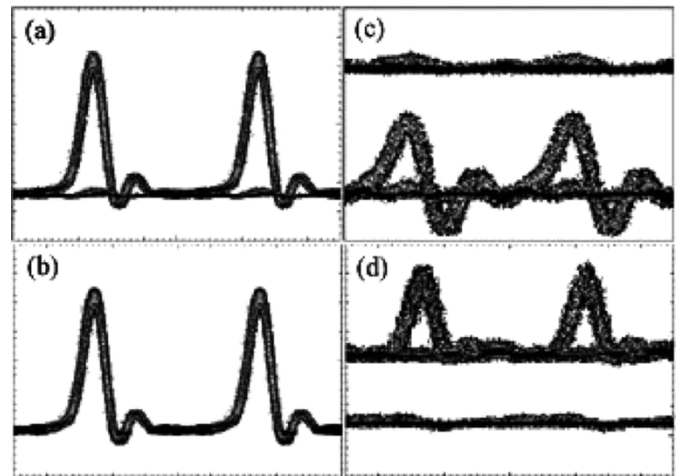


Fig. 10. Eye diagrams of (a) the input signal (SDH data), (b) the control signal (clock) and the output at the S-port (upper graph) and U-port (lower graph), (c) in the absence and (d) in the presence (AND operation) of the control signal. The time base is 20 ps/div.

absence of the control signal, respectively. The eyes at the S- and U-ports of the UNI were recorded simultaneously with two different 40-GHz photodiodes, thus exhibiting different eye forms. For these experiments, the optimum pulse energies for the clock and data signals were 2 and 8 fJ, respectively.

## B. XOR Gate

The UNI switch may also be configured for dual rail logic, such as the XOR operation. In order to achieve this, each of the orthogonal polarization states of the incoming signal shown in Fig. 7 must be accessed in the SOA with a control pulse. Each controlling pulse is arranged so as to impart a phase modulation on the equivalent signal polarization component to which it is synchronized. In this configuration, the input signal of the switch is a full duty-cycle signal (clock) on which the logic operation between the two control data patterns is written. More specifically, the output at the S-port of the UNI gate is the logic XOR operation between the two control signals A and B, while the output at the U-port appears the result of the complementary XOR logic operation. Within the frame of DO\_ALL, the XOR operation with the UNI switch was demonstrated and evaluated at 20- and 40-GHz repetition rates [48], [49].

Fig. 11 shows the block diagram of the UNI switch configured as a XOR gate. The clock and the two control signals were produced from two 10-GHz gain-switched DFB lasers operating at 1545.2 and 1554.6 nm generating 9-ps pulses after linear compression. The first DFB provided the 20-GHz clock and control signal A by pulse-train bit interleaving. The second DFB provided the 20-Gb/s control signal B by modulation followed by bit interleaving. The active switching device in this experiment was the same SOA used in the switch discussed previously and configured as an AND gate. The two PMFs at the input and output ports of the SOA were arranged to introduce 25-ps relative delay between the two orthogonal polarization clock components.

Successful Boolean XOR operation between A and B is accomplished when the S-port of the gate records a logical “1” if either A or B is “1” and a logical “0” if both A and B are “1” or “0”. Fig. 12 shows the output at the S-port of the gate for

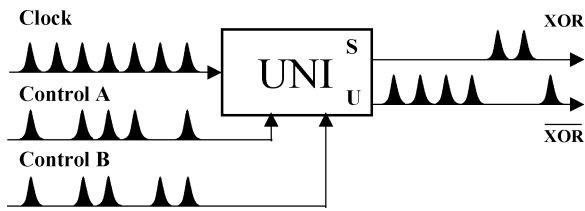


Fig. 11. Block diagram of the UNI switch operating as an XOR gate.

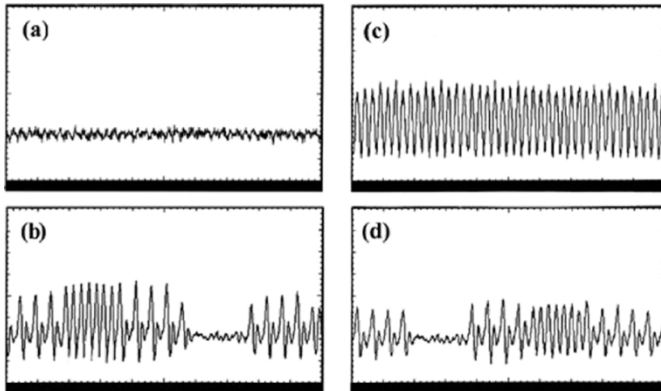


Fig. 12. Oscilloscope trace of the S-port (a) in the absence of control signals, (b) in the presence of control signal B, (c) in the presence of control signal A, and (d) in the presence of both control signals (XOR operation). The time base is 200 ps/div.

the four logical combinations of control data A and B. In particular, Fig. 12(a) shows the output in the absence of the control signals, (b) and (c) show the output with either one of the two controls present, and (d) shows the result of the XOR operation between the control signals A and B. The contrast ratio between the ON–OFF states of the switch was up to 6:1, and the switched signal showed low pattern dependence. The energy of the clock, control A, and control B pulses for optimum performance were 2.5, 15, and 4 fJ, respectively. These switching energy values are indeed low, and the gate may operate in a loss-optimized logic circuit, even without an amplifier.

### C. Packet Clock Recovery

The ability to recover the optical clock is a requirement in ultra-high-capacity transmission and all-optical processing systems [50]. It is particularly necessary in the design and development of high-functionality multigate systems, as it is the way to synchronize the optical signals between remote processing units [51]. For example, in order for a BERT to operate, its transmitter and receiver units must be precisely synchronized, and this is performed with a clock-recovery circuit.

Several techniques have been proposed for all-optical clock recovery, including synchronized mode-locked ring lasers [52], electronic phase-locked loops [53], and self-pulsating DFBs [54], [55]. Ring lasers and phase-locked loops require a long time for synchronization to the data streams and are not suitable for asynchronous short optical packet traffic. Self-pulsating DFBs require significantly less overhead for clock acquisition and have been demonstrated to operate successfully with asynchronous data packets comprising of a few thousands of bits and guard bands of a few hundreds of bits [54], at rates up to 40 Gb/s [55]. Here, we describe an all-optical clock-recovery

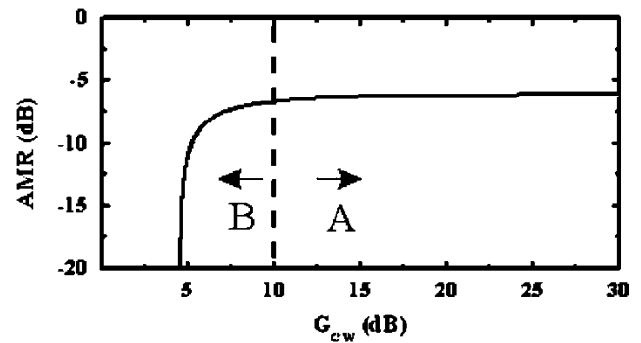


Fig. 13. Theoretically calculated amplitude modulation reduction at the output of the Mach–Zehnder interferometer (MZI) gate for various  $G_{CW}$  values.

circuit consisting of a low-finesse FPF and the SOA-based UNI switch configured as an AND gate (see Section III-A), which is capable of recovering short asynchronous 10-Gb/s data packets, arriving at time intervals of only 1.5 ns between them, irrespective of their precise phase relation [56]. The scheme is self-synchronizing and requires no high-speed electronics.

The operational principle of this circuit relies on the FPF, which is used to partially fill the “0”s in the incoming data stream from the preceding “1”s and to create a signal that resembles the packet clock but that is amplitude modulated, and on the UNI gate, which is used to provide improved pulse amplitude equalization under strong SOA saturation conditions caused by a continuous-wave (CW) input signal. More specifically, the theoretical and experimental analysis of saturated SOA-based interferometric switching arrangements has revealed that the presence of a strong CW signal can transform the regular sinusoidal transfer function of the interferometric switch into an almost flat, strongly nonlinear curve and result in an amplitude modulation suppression of the incoming pulse train of more than 10 dB at the output. In this manner, the operation of an SOA-based switch can be discriminated in two regions, as shown in Fig. 13, which depicts the amplitude modulation reduction (AMR) for different CW gain values. Region A covers a broad SOA operational range, corresponds to the low or moderate saturation regime of the SOA, and is usually employed in switching schemes such as the ones configured for Boolean AND and XOR operations (see Sections III-A and B). In contrast, region B is narrower, corresponds to the heavy saturation regime of the SOA, and offers enhanced amplitude modulation suppression at the output of the all-optical gate.

Fig. 14 shows the experimental configuration that consists of two main subsystems: the asynchronous packet flow generator and the packet clock-recovery circuit. A gain-switched DFB laser (LD1) at 1.290 75 GHz, provided 9-ps pulses at 1549.2 nm after linear compression. This pulse train was modulated with a  $2^7 - 1$  pseudorandom binary sequence (PRBS) signal from a pattern generator and a LiNbO<sub>3</sub> modulator (MOD1) and was three-times bit-interleaved to generate a 10.326-Gb/s pseudo-data stream. Data packets of variable length and period were formed using a second modulator (MOD2) driven from a programmable pulse generator. The packet stream was amplified in EDFA1 and split into two different optical paths via a 3-dB fiber coupler. The two paths were made so as to provide a maximum of 17.9-ns relative delay between the split signals. Polarization



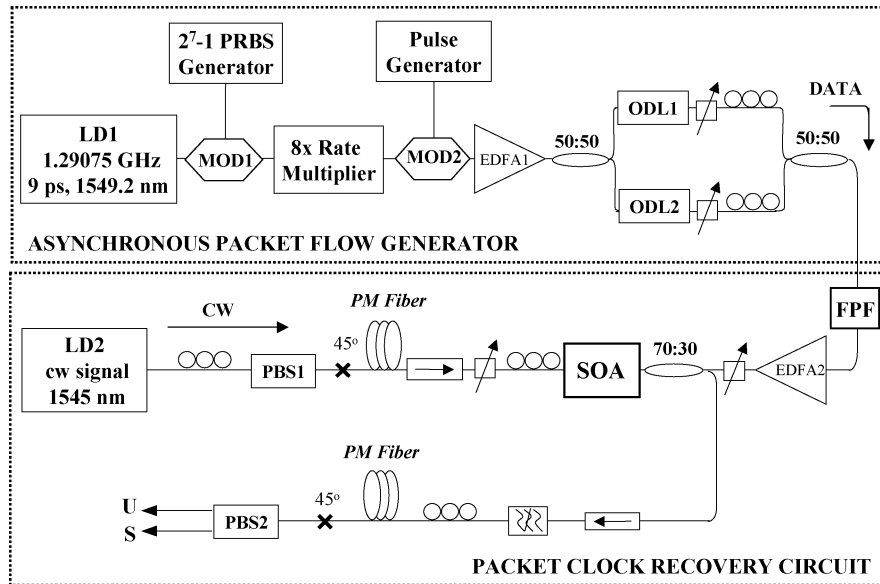


Fig. 14. Packet clock-recovery experimental setup.

controllers and attenuators were used to independently adjust the polarization state and power in the two branches. Variable ODLs ODL1 and ODL2 were also used to independently control the relative arrival time of the packets at the clock-recovery circuit so as to investigate the minimum acceptable delay between successive packets and to assess the circuit ability to operate with successive packets that are asynchronous at the bit level. The asynchronous packet stream was then launched into the packet clock-recovery circuit, which consists of an FPF and a UNI gate, powered by a CW signal at 1545 nm (LD2). The FPF had an FSR equal to the line rate and a finesse of 20.7, corresponding to a  $1/e$  lifetime of roughly 7 b. The output of the filter was amplified in EDFA2 and inserted into the UNI gate as the control signal. The UNI gate was optimized for operation at 10 Gb/s and used PMF at the input and output ports of the SOA to induce 50 ps of differential delay between the two orthogonal polarization components of the CW signal. The active element was a 1.5-mm bulk InGaAsP–InP ridge waveguide SOA with 27-dB small-signal gain at 1550 nm, 24 dB at 1545 nm, 3-dB polarization gain dependence, and a recovery time of 80 ps, when driven with 700-mA dc current. After exiting the SOA, the polarization components of the CW signal were filtered in a 2-nm filter, had their relative delay removed, and were made to interfere in PBS2. The interferometer was biased so that, in the absence of the control signal, the CW signal appeared at its unswitched port U, while in the presence of the control, it appeared at its switched port S.

Data packets of different length, period, and content were used to evaluate the performance of this clock-recovery scheme for an asynchronous packet stream at 10 Gb/s. Fig. 15(a) shows a typical data stream, obtained from the asynchronous packet flow generator. More specifically, a sequence of four data packets is illustrated, each packet containing 41 b (approximately 4-ns duration). Packets 1 and 3 are traveling through the upper, and packets 2 and 4 are traveling through the lower branch of the packet generator. The coarse relative delay between packets 1

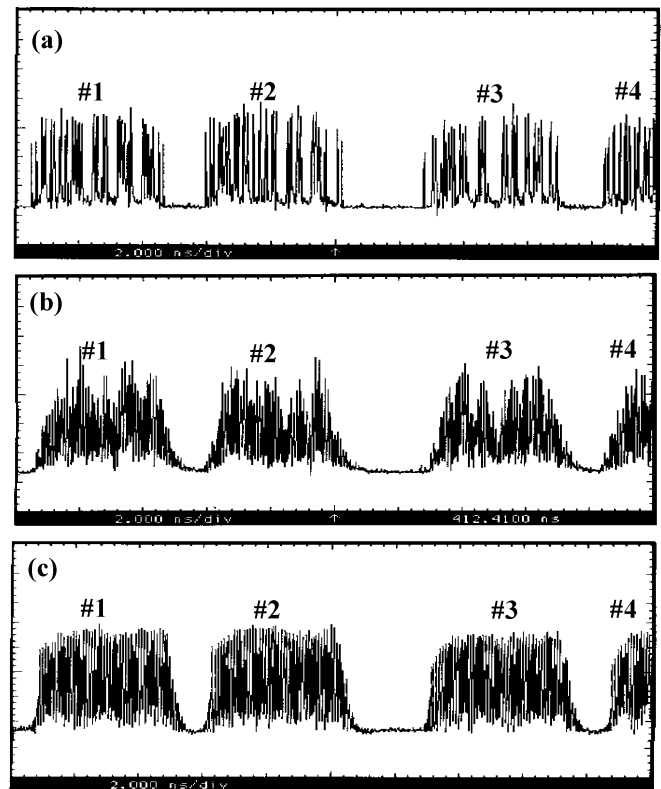


Fig. 15. (a) Incoming asynchronous data stream of four packets and corresponding (b) FPF output and (c) recovered packet clocks. The time base is 2 ns/div.

and 2 was 1.5 ns and between packets 2 and 3 was 2.9 ns. Packets 2 and 3 are shown in more detail in Fig. 16(a) and (b), respectively.

At the FPF, the asynchronous packet stream is convolved with the exponentially decaying response function of the filter so that an amplitude modulated, but clock resembling signal is obtained. Fig. 15(b) shows the corresponding output of the FPF

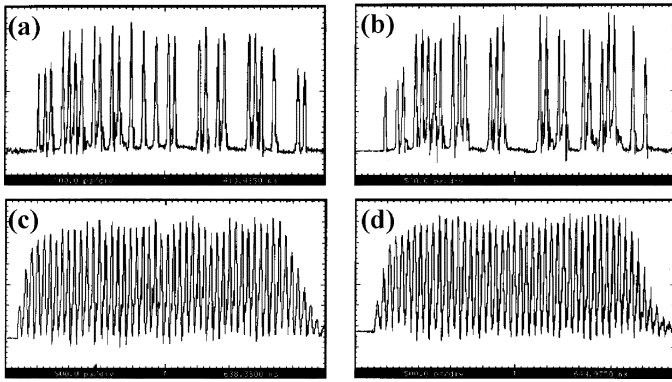


Fig. 16. (a) and (b) Detailed representation of two incoming data packets and (c) and (d) corresponding recovered packet clocks. The time base is 500 ps/div.

for packets 1 to 4. This is used as the control signal into the UNI gate to induce an almost  $\pi$ -phase shift between the orthogonal polarization components of the CW signal. This results in a packet clock signal of nearly equal amplitude “1”s and very short rise and fall times. Fig. 15(c) shows the acquired packet clock signal. A more detailed representation of the recovered packet clocks for packets 2 and 3 is illustrated in Fig. 16(c) and (d).

The packet clocks display rise and fall times of 2 and 8 b, respectively, and amplitude modulation of less than 1.5 dB (highest to lowest pulse ratio), within the span of the original 41-b data packet. The circuit required 1 mW of optical power from the CW signal and 110 fJ/pulse from the data signal, corresponding to 0.9-mW average power for the packets shown here. Packet clocks of the same quality were obtained irrespective of the precise relative phase adjustment between the packets as set by the delay lines ODL1 and ODL2.

The quality of the asynchronously extracted clock signal was also examined using a 50-GHz microwave spectrum analyzer. Fig. 17(a) and (b) depicts the RF spectrum of the packet signal from dc to 11.2 GHz and within a 810-MHz band centered around the 10.326-GHz component, respectively. The asynchronous operation is confirmed by the suppressed clock component at 10.326 GHz with respect to the adjacent 80-MHz-spaced packet subharmonics. Fig. 17(c) and (d) shows the corresponding output of the FPF. The effect of the filter is primarily to suppress all data modes outside a 500-MHz band around the baseline rate. Data-mode suppression within this 500-MHz band is achieved by taking advantage of the nonlinear transfer function of the deeply saturated SOA-based interferometric gate [57]. Fig. 17(e) and (f) shows the RF spectrum of the extracted packet clock at the output of the UNI gate for asynchronous traffic revealing data-mode suppression in excess of 35 dB with respect to the 80-MHz-spaced packet subharmonics. Finally, the root-mean-square (rms) timing jitter of the extracted clock was also calculated using the microwave spectrum analyzer for a total span of 3 KHz around the packet clock components and resolution bandwidth of 10 Hz and was found to be less than 1 ps.

It should also be noted that the amplitude ratio between the 10.326-GHz clock component and the packet subharmonics has the same value in Fig. 17(b), (d), and (f), showing that the ex-

tracted clock retains the phase alignment of the initial asynchronous data stream. This amplitude ratio varies between a maximum value and zero, depending on whether the packets are perfectly phase-aligned or misaligned by  $\pi$ , and this adjustment is provided by the setting of ODL1 or ODL2 within a bit-period time interval of approximately 100 ps.

#### D. All-Optical Write/Store Memory

One of the most important fiber logic modules that was developed within the frame of the DO\_ALL project is the optical-shift register circuit or the optical write/store memory. This formed the technological platform for the development of an optical LFSR and an error counter circuit. The optical LFSR is the basic building block of the PRBS generator in a BERT, and the error counter follows the bit comparator circuit in the receiver of the BERT. Moreover, regenerative optical memories are useful network units because they can store data packets and at the same time reshape and retime the data bits so as to minimize the effects of accumulated timing jitter [58]. The first regenerative optical buffers were built with fiber-based optical switches [59], [60], but they were not suitable for single-packet storage because of the long length of fiber that they require to achieve switching. On the other hand, regenerative buffers using compact semiconductor interferometric switches are characterized by low latency and are more appropriate for data packet storage [61]–[63]. Within the DO\_ALL project, the UNI switch was used in a feedback configuration for the implementation of optical write/store memories that were operated with 10- and 20-Gb/s packets [61].

Fig. 18 shows the logical electronic equivalent of the regenerative optical write/store memories, and Fig. 19 shows the block diagram of the experimental configuration to demonstrate such optical memory unit with the UNI switch. The UNI gate is utilized in a counterpropagating configuration and is powered from a 20-GHz clock signal at 1545.2 nm. The signal for the data packet used to load up and to be stored in the memory was provided by a second diode at 1554.6 nm and was a 20-Gb/s, 32-b-long periodic data sequence of 1.56-ns duration. The pulsewidth of both signals was 9 ps after linear compression. For the memory loop or the shift register to be realized, the S-port of the UNI gate is fed back into the gate as control signal. Data are loaded up once at start-up and are let to perform several recirculations  $N$  after which they exit the memory circuit. In this manner, if the amount of time that data need to travel once the feedback loop is  $T$ , then buffering times longer than  $T$  can be achieved as multiples of this fundamental time by performing  $N$  recirculations so that the total storage time is  $(N + 1) \times T$ . Since  $T = (n_{\text{eff}}/c) \times L$ , where  $n_{\text{eff}}$  is the fiber's effective index of refraction and  $c$  the velocity of light in vacuum, it can be deduced that the primary factor that affects the ultimate storage time is the length of the feedback loop, which in turn is the sum of the physical length and the pigtails of the active and passive components it consists of and can be several tens of meters long. This essentially means that the storage time can be altered at will by simply adding or removing fiber without significant cost in power dissipation or energy loss [59], [60], which is clearly an advantage for

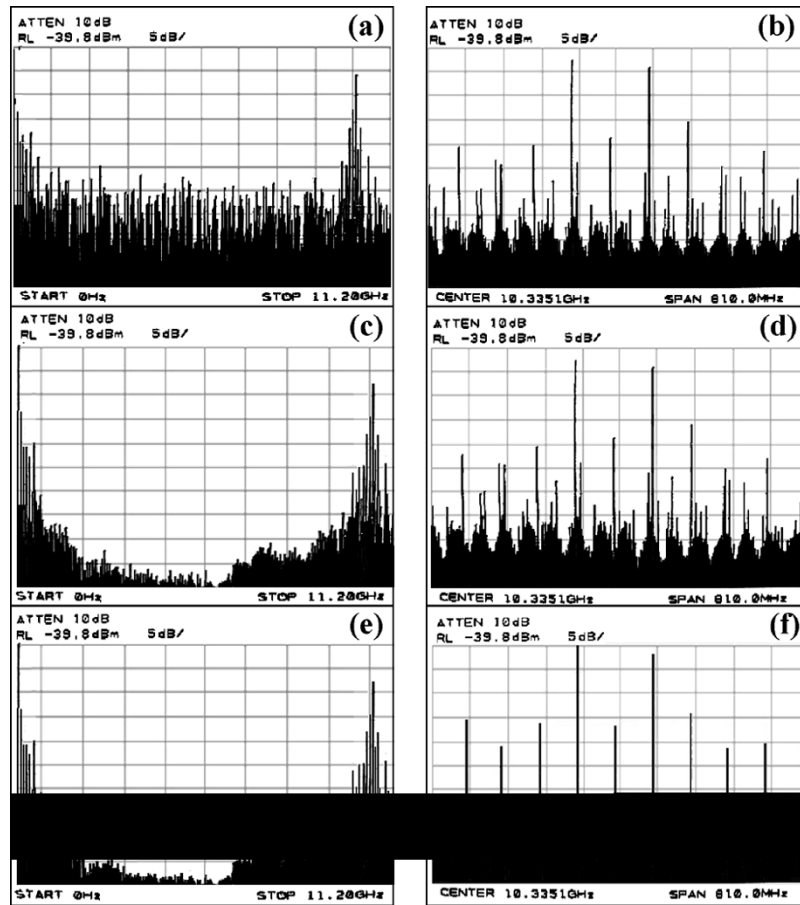


Fig. 17. (a) and (b) RF spectrum of incoming asynchronous data packets from dc to 11.2 GHz and within a 810-MHz band centered around 10.326 GHz, respectively, (c) and (d) corresponding FPF output, and (e) and (f) RF spectrum of the extracted packet clock at the output of the UNI gate. The amplitude scale is 5 dB/div.

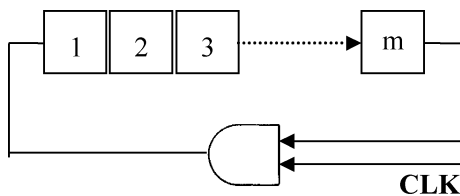


Fig. 18. Electronic equivalent of a regenerative buffer.

this SOA-based interferometric type of memory. However, the introduced latency must be kept at the same time to acceptable values for ultra-high-speed all-optical applications, namely to the order of few tens of nanoseconds so that real-time data processing is feasible. Thus, provided that the total width of the load-up frame, which is determined by the duration of the individual data packets it consists of, or equivalently the number of bits and their period in the data sequence of each packet, as well as the time delay (guard band) between them, is appropriately adjusted so as to correspond to the single circulation time through the shift register, then it can be stored if its period satisfies  $(N + 1) \times T$  for a certain  $N$ . It must be noted that since this is a regenerative memory and pulses are replaced in each circulation without performance degradation, there is actually no inherent limitation in the number of recirculations  $N$  and hence in the storage time so that a frame of arbitrary length can be essentially buffered, and only triggering in the diagnostic

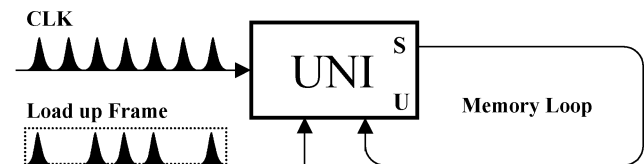


Fig. 19. Block diagram of an optical regenerative memory.

instruments imposes detection and monitoring restrictions. The active switching device in the UNI was the same SOA that was used in the switch configured as an AND gate, and each of the two PMFs was arranged to introduce 25-ps relative delay between the two orthogonal polarization clock components. The length of the feedback circuit was 143.2 m, corresponding to 14.320 electronic equivalent memory units in the shift register. The shift register recirculation time was 716 ns. Variable delay lines were used for precise time synchronization between the three optical signals. In the absence of the control signal, the output appears in the U-port of the UNI gate; otherwise, it appears in the S-port. It should be noted that if there is no circuit available to load up a data sequence, only the U-port may be used to provide the feedback or else the memory will never start to operate.

Successful write, store, and read operations were achieved with different frame formats over many circulations through the memory. Fig. 20(a) and (b) shows typical load-up and stored

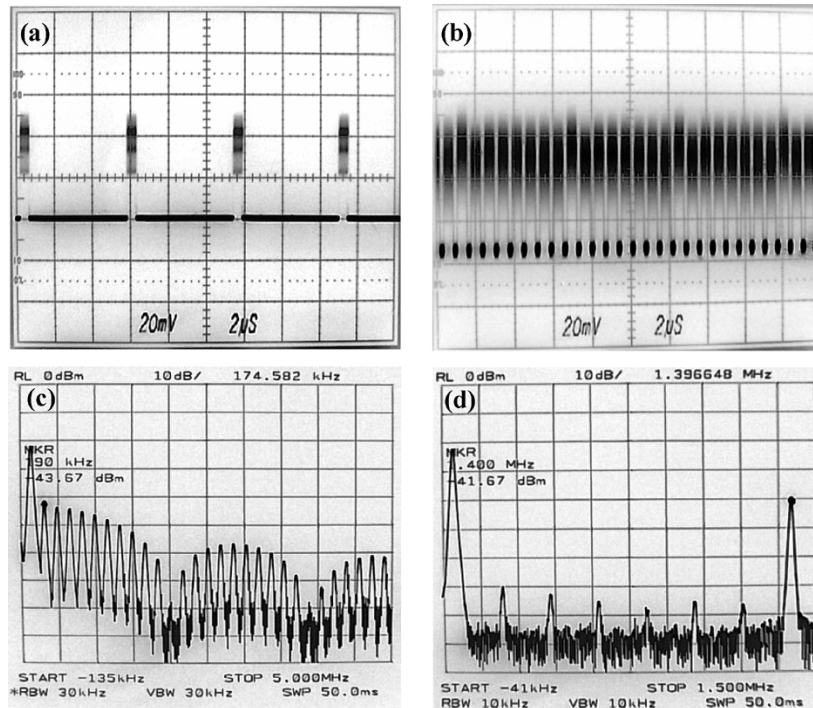


Fig. 20. Oscilloscope trace of (a) the load-up signal and (b) the content of the memory after seven circulations (the time base is  $2 \mu\text{s}/\text{div}$ ), and the corresponding microwave spectrums (c) and (d).

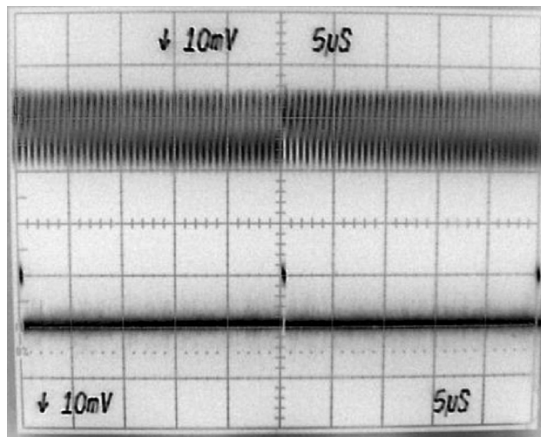


Fig. 21. Memory content with the S-port of the UNI used in the feedback circuit after 40 circulations (upper row) and the corresponding load-up signal (lower row).

frames using the S-port of the UNI for feedback of the memory loop, while Figs. 20(c) and (d) shows the corresponding electrical spectrums. In this case, the frame consists of a 516-ns data packet, which contains 322.5 consecutive 32-b-long data sequences at 20 Gb/s. The period of the load-up signal was adjusted to be  $5.728 \mu\text{s}$  ( $\sim 174.581 \text{ kHz}$ ) so that each frame can be stored for seven recirculations after it has been loaded up (total storage time  $5.728 \mu\text{s}$ ). It is worth noting that the first harmonic of the recirculating signal, which occurs at 1.396 648 MHz (1/716 ns), is 30 dB higher than the first harmonic of the load-up signal that occurs at 174.581 kHz.

Fig. 21 depicts the content of the memory after 40 recirculations in the upper row and the loading-up pattern in the lower one, which consists of one data packet with a total duration of

352 ns. The two signals were monitored with an analogue oscilloscope using two photodiodes and the chop vertical mode. Setting the time base at  $5 \mu\text{s}/\text{div}$ , it has been possible to monitor two successive ON-OFF states of the loading-up signal and the consequent write and store capability of the circuit. It was also possible to monitor the stored pattern through more than 80 successive circulations, corresponding to more than  $57 \mu\text{s}$  of storage time, and the stored pattern still presented no deterioration.

The memory loop can use for feedback either the S- or U-port of the UNI, which can be selected at will with the use of polarization controllers before the SOA and before the PBS at the output of the UNI switch. Fig. 22 shows the output of a typical stored pattern, after seven recirculations, with (a) the S-port and (b) the U-port of the UNI feeding the memory loop. The data frame consists of four data packets, while each data packet is made out of 32 32-b-long sequences. As it can be seen, the use of the U-port causes, according to the description of the UNI's operation, data inversion after each recirculation, which is clearly undesirable in terms of complexity because it would require further signal processing for reading out the packets. On the other hand, the data frames appearing in the S-port are not inverted and have higher quality with respect to extinction ratio, compared with the ones in the U-port that cannot be monitored for more than 20 recirculations. Consequently, the performance of the circuit at the bit level is expected to be better when the S-port of the UNI is feeding the memory loop. Figs. 23(a)–(c) shows the loading-up pattern before storage and the stored pattern with the S- and U-ports, respectively, after seven circulations on a 40-GHz sampling scope and indicate indeed far superior performance of the memory when the S-port is used in feedback. The slow modulation that appears on the patterns is due to the

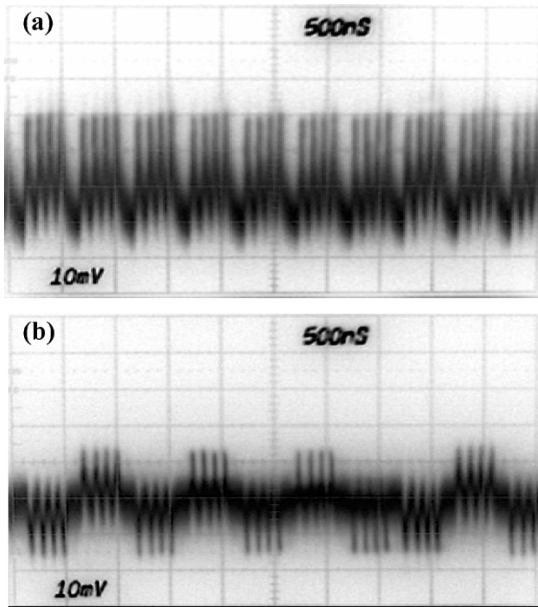


Fig. 22. Memory content with (a) the S-port and (b) the U-port of the UNI used in the feedback circuit.

electrical pulse driving the modulator. The pulse energies of the clock, loading-up, and recirculating signals were 3, 23, and 33 fJ, respectively, making this memory a low-energy-consumption circuit.

### E. All-Optical Linear Feedback Shift Register

One of the simplest and most effective devices for generating PRBSs is the LFSR [64], [65]. A LFSR of degree  $m$  is a device consisting of  $m$  consecutive two-state memory units, which are regulated simultaneously by a clock. All the memory units change state together in synchronization with the input clock pulses, and in every clock pulse the content of each memory unit is shifted to the next one. If no signal is introduced into the first delay element during this process, then at the end of  $m$  shifts all the memory units will have no content. To convert the shift register from a delay line unit to a sequence generator, a feedback loop is needed. The feedback loop feeds the content of certain memory units, which are called taps, into a modulus 2 adder (XOR operation) and then back to the first memory unit. In that way, a new term is computed for the first stage based on some of the previous  $m$  terms. Fig. 24 illustrates an LFSR of degree  $m$  with two taps; the last memory unit or  $m$ -tap and the  $k$ th memory unit or  $k$ -tap. All-optical LFSRs are useful in applications such as BER measurements and encryption/decryption, offering the advantage of speed. The optical shift registers, and the SOA-based interferometric XOR gates discussed so far can be used for the implementation of an all-optical LFSR. However, the huge size of the optical shift register restricts the applicability of all-optical LFSRs, because they cannot be easily programmed to produce controllable PRBSs. Despite this fact, a design algorithm has been constructed to allow for easy programming of the all-optical LFSRs, irrespective of the shift register size.

Fig. 25 illustrates the block diagram of an all-optical LFSR implemented with the UNI. Following the classic electronic de-

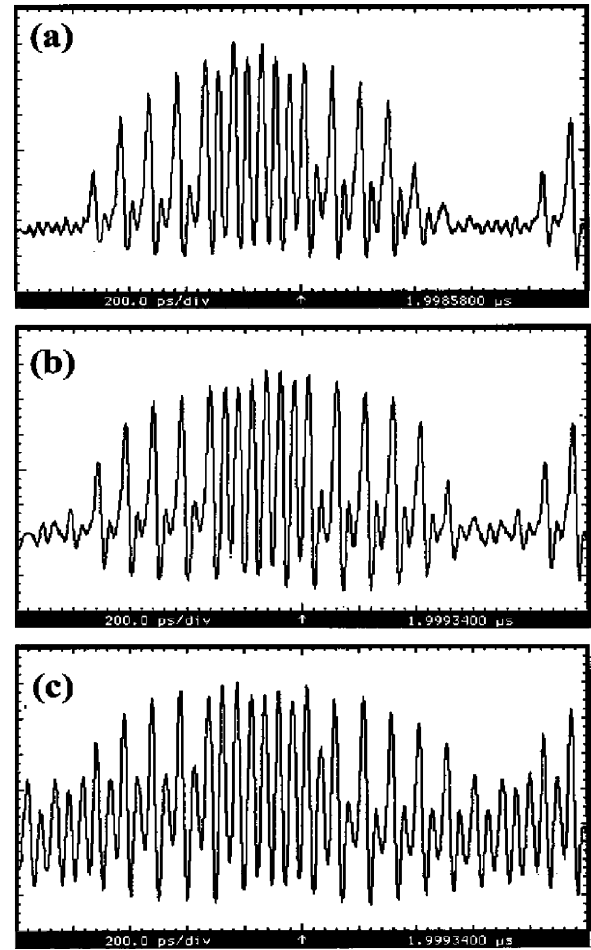


Fig. 23. Oscilloscope trace of (a) the load-up signal, (b) the memory content with the S-port of the UNI used in the feedback circuit, and (c) the memory content with the U-port of the UNI used in the feedback circuit.

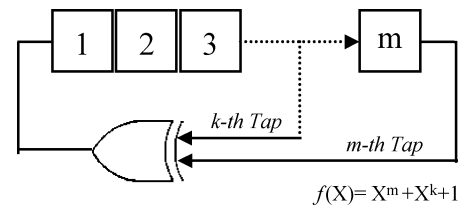


Fig. 24. Block diagram of an electrical LFSR.

sign, it comprises an optical XOR gate and an all-optical shift register with two taps. In order for the circuit to start producing binary sequences, an initial condition (IC) must be loaded up into the shift register once at the beginning. The fused fiber coupler with 50:50 splitting ratio forms two optical loops with lengths  $L_1$  and  $L_2$  ( $L_1 > L_2$ ) so that the IC signal is split in two delayed replicas, which are launched as control signals into the gate (ports 1 and 2). After the XOR operation, the produced bits are switched at port 3 (S-port of the UNI switch) and fed into the loop so that the process can repeat itself. The longest optical path can be considered as the entire shift register or the first feedback, while the shortest one is the second feedback of the LFSR. In this configuration, two taps are selected: the last one and one intermediate. The optical shift register is constructed from fiber-pigtailed optical components, and thus its length is

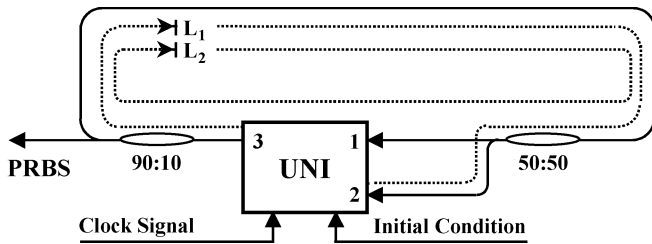


Fig. 25. Block diagram of an all-optical LFSR.

in practice several tens of meters long (see Section III-D). The number of memory units or flip-flops (FFs) associated with the optical shift register length is given by

$$N_{\text{FF}} = \frac{n_{\text{eff}}}{c} \times L \times F \quad (1)$$

where  $N_{\text{FF}}$  is the number of FFs,  $n_{\text{eff}}$  is the fiber's effective index of refraction,  $c$  is the velocity of light in vacuum,  $L$  is the effective length of the shift register, including optical components and fiber, and  $F$  is the repetition frequency of the clock signal driving the circuit. It should be noted that the FFs of an all-optical LFSR are not discrete memory units, as in an electronic LFSR, but fiber sections that contain only one bit. Equation (1) shows that for a 50-m-long fiber shift register operated at 40 GHz,  $N_{\text{FF}}$  is 10 000. This means that the produced maximal-length sequence has period  $2^{10\,000} - 1$ , while submaximal sequences with shorter periods can also be generated with the appropriate tap selection. This selection determines the equivalent characteristic polynomial that describes the LFSR and hence the exact form of the generated PRBS. Only primitive characteristic polynomials "produce" maximal-length sequences, while nonprimitive but irreducible polynomials "produce" submaximal sequences. Alternatively, the LFSR can be designed to have a reducible characteristic polynomial, which in association with the IC, defines the period and the structure of the produced PRBS.

The aforementioned considerations underline the need for a robust design principle that will lead to controllable all-optical PRBS generators and that must take into account the fact that all-optical LFSRs are thousands of FFs long. If, for example, the desired sequence is a  $2^{31} - 1$  maximal-length PRBS, only 31 FFs are needed, and yet this must be produced from an all-optical LFSR that contains thousands of them. The study of trinomials with degree of tens of thousands is a difficult task even for very powerful computers, and the determination of primitive, irreducible, or even reducible trinomials that "produce" the desired PRBS is practically impossible. A design algorithm for the implementation of an all-optical LFSR capable of operating at ultrahigh data rates and that uses large shift registers is described in detail in the Appendix.

#### IV. ALL-OPTICAL BERT

The first major objective of the DO\_ALL project was to explore the feasibility of all-optical BER measurements at 40 Gb/s or beyond based on the technological platform of the developed

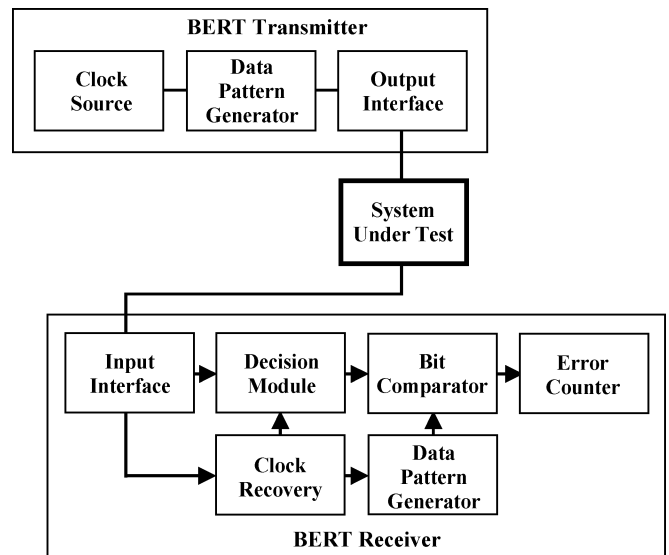


Fig. 26. Generic block diagram of BERT equipment.

fiber logic modules. The design and demonstration of the all-optical BERT relies not only on the maturity of these modules but on their functional integration as well. Two subsystems are required for the application to be performed: the transmitter and the receiver unit. The former is responsible for the all-optical generation of a test signal, while the latter for the appropriate all-optical signal processing.

The requirements for BER measurements were investigated and analyzed in terms of the existing photonic technology in order to properly design the transmitter and receiver units. The transmitter unit requires the all-optical implementation of an LFSR and a XOR gate, while the receiver a XOR gate, a clock-recovery circuit, and an error counter. Fig. 26 illustrates the principle of the BER measurement technique. The clock source generates a clock signal at a specific line rate, which drives the optical LFSR (data pattern generator) so that the pseudorandom signal or test signal is generated. The output interface module, which may be an optical booster amplifier, prepares the signal for the system under test. The system under test can be an optical fiber link with or without optical amplifier or any other transmission system component. At the output of the system under test, the signal is received by the input interface module and may be an optical preamplifier. A clock-recovery circuit extracts the clock from the data signal. The clock signal retimes the data signal in the decision module, and the received bit pattern is compared bit by bit with the same bit pattern that was generated in the transmitter part. Any difference in the bit pattern is counted as a bit error, and the total number of errors is recorded and evaluated accordingly.

The implementation of the all-optical BERT can be achieved with the fiber logic modules that were developed during the DO\_ALL project. Specifically, depending on the operation rate of the BERT, the clock source can be realized using the repetition 40-GHz upgrading technique described in Section II-B. The clock can be recovered using the circuit of Section III-C that consists of an FPF and a nonlinear UNI gate. The functionalities of the decision module and the bit comparator can be performed by a single XOR logic gate module (see Section III-B). The data

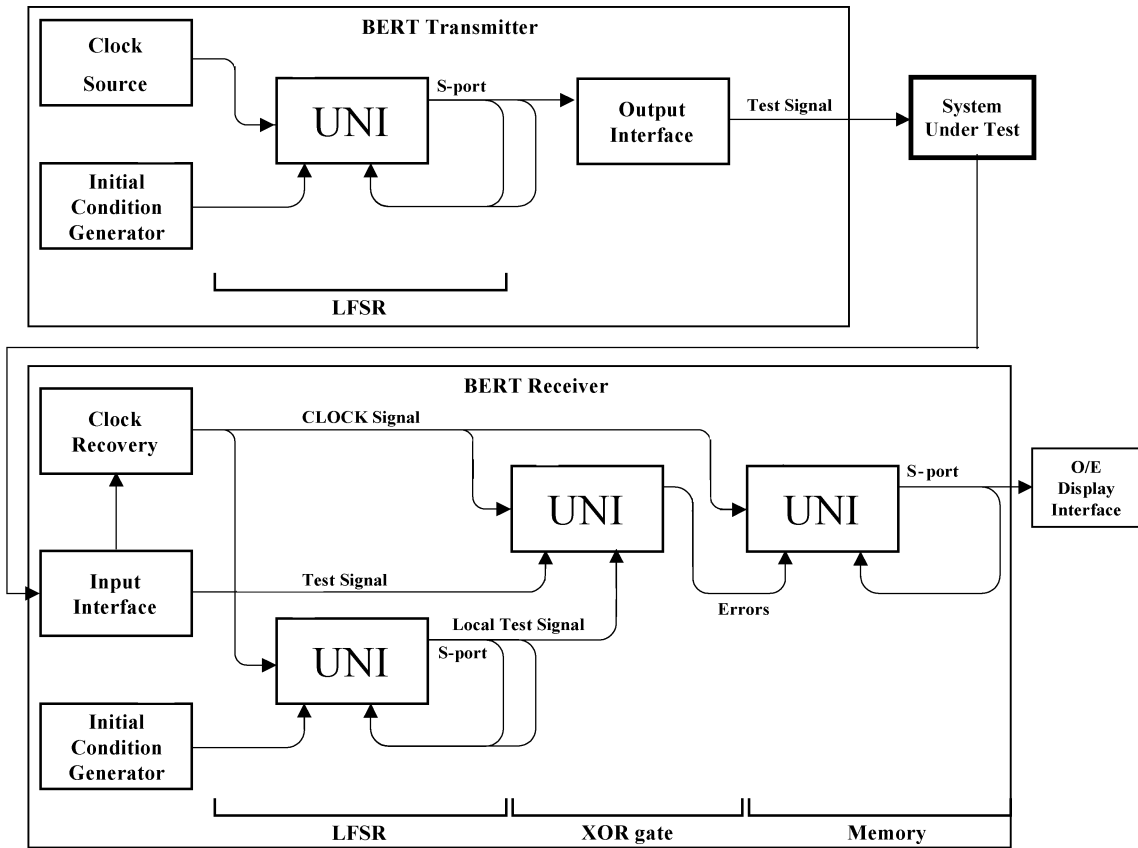


Fig. 27. Generic block diagram of BERT equipment using the UNI.

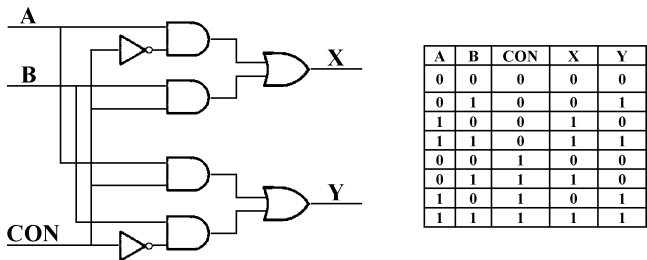


Fig. 28. Electronic implementation of a  $2 \times 2$  exchange-bypass switch and the corresponding truth table.

pattern generator is an optical LFSR properly designed (see Section III-E), and the error counter circuit is an optical memory (see Section III-D) combined with a low frequency optoelectronic display module. Fig. 27 shows the design of the all-optical BERT, which uses the UNI switch as the basic building block.

V.  $2 \times 2$  ALL-OPTICAL EXCHANGE-BYPASS SWITCH

The second major objective of the DO\_ALL project was the demonstration of an all-optical exchange-bypass switch. The  $2 \times 2$  exchange-bypass switch is the basic unit of the switching fabric in telecommunications switch architectures [66], [67]. The speed at which these switches may operate depends on the speed of each individual exchange-bypass switch. Electronic exchange-bypass switches may require the implementation of up to eight gates, as shown in Fig. 28.

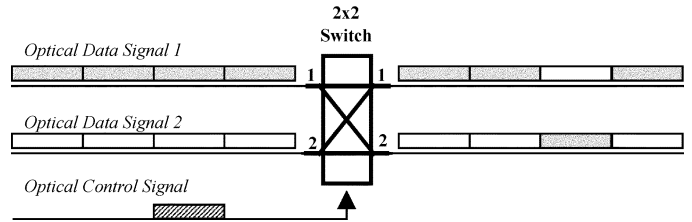


Fig. 29. Principle of operation of the  $2 \times 2$  exchange-bypass switch.

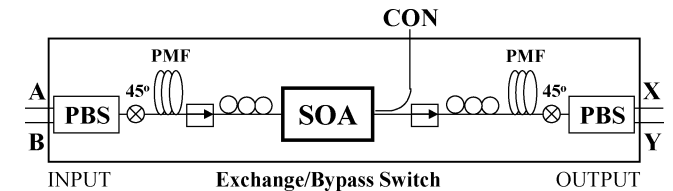


Fig. 30. UNI-based  $2 \times 2$  exchange-bypass switch in counterpropagating configuration.

As the switch speed requirements increase, it becomes increasingly difficult to implement large switch matrices with large numbers of fast exchange-bypass switches. In this application demonstration of the digital logic modules, the intention is to show that it is possible to build an ultrafast exchange-bypass switching unit and, more important, to perform a logic function with a single SOA-assisted gate compared with the multiple gates that are required in conventional electronic designs.

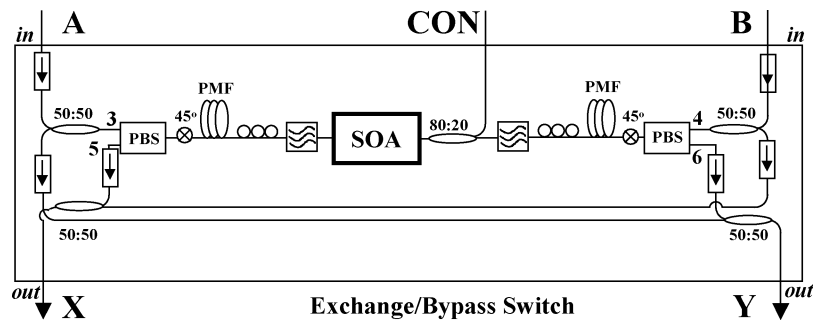


Fig. 31. UNI-based  $2 \times 2$  exchange-bypass switch in hybrid counter and copropagating configuration.

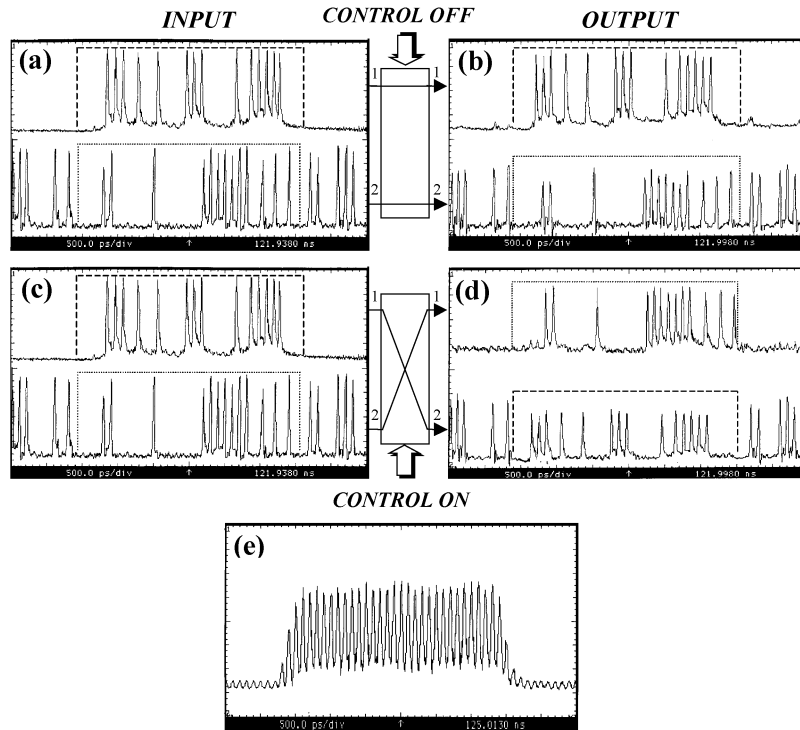


Fig. 32. BAR and CROSS state: (a) and (c) input signals, (b) output data streams with the control signal off, (d) output data streams with the control signal on, and (e) control signal. The time base is 500 ps/div.

For the operation of an optically addressable  $2 \times 2$  exchange-bypass switch, three optical signals are needed, specifically two data signals and one control signal, as shown in Fig. 29. Data signals enter the switch from input ports 1 and 2. If there is no control signal, the switch is in the BAR state and both data signals pass straight through to output ports 1 and 2. If the control signal is present, the switch is in the CROSS state, and the two data streams are interchanged at its output. The length of the bit sequence that is interchanged through the switch is determined by the length of the control signal and may be arbitrarily long or short depending on the length of the incoming packet.

The optical exchange-bypass switch was constructed using a single UNI gate, operated either in a counterpropagating configuration [68], as shown in Fig. 30, or in a hybrid counter and copropagating configuration [69], as shown in Fig. 31. Data signals 1 and 2 enter through input ports A and B, while the control signal enters through port CON. If there is no control signal, then data signal 1 exits through port X, while data signal 2 exits through port Y. In the presence of a control pulse, the phase of the two synchronized polarization components is changed si-

multaneously so that when the components of each data signal recombine at the PBSs, their polarization states rotate by  $90^\circ$ . In this way, data signal 1 exits through port Y, while data signal 2 exits through port X. In both implementations, the nonlinear element in the UNI gate was the same SOA as the one used in the other fiber logic modules (see Section III).

The performance of the switch in both configurations was investigated in two experiments. In the first experiment, the performance was evaluated at data packet level, including different packet lengths. In this instance, the switch was used as a data packet exchanger, and the input data signals emulated sequences of packets. In the second experiment, the error performance of the switch was evaluated in a static configuration with SDH/STM-64 data.

In the first experiment, data signal 1 consisted of packets containing  $2^7 - 1$  PRBS at 10 GHz and data signal 2 of the full PRBS. The data pulsewidth was 8.1 ps at 1549.2 nm. The control signal consisted of packets containing 10-GHz clock pulses with 8.4-ps temporal width at 1554 nm. Fig. 32 shows the two output ports of the switch monitored simultaneously with a sampling oscilloscope. Specifically, Fig. 32(a) and (c) shows the input



data signals 1 and 2 into the switch. Fig. 32(b) and (d) shows the corresponding output signals for the BAR and CROSS states, and Fig. 32(e) shows the control signal. In the BAR state, the data packets from signals 1 and 2 depicted by the thick dashed and thin dotted lines, respectively, cross the switch unchanged. When the optical control signal is present, the switch is in the CROSS state, and the packets are interchanged in the output ports. The pulse energies for data 1, data 2 and control pulses were 2, 2, and 8 fJ, respectively. The crosstalk of the switch in the BAR state was  $-12$  dB and in the CROSS state  $-10$  dB, in the worst case. In the presence of the control signal, there was also a 1-dB drop in the switched signals due to additional SOA gain saturation, which can be mitigated using a gain-transparent interferometric switch arrangement [70].

It is important to note that if this exchange-bypass unit is used in an optical packet switch matrix, it relaxes the requirement for guard bands between the packets, since the switch changes state within the bit period. By avoiding guard bands, the improvement in throughput becomes more pronounced as the packet length decreases.

In the second experiment, the data signals that powered the switch were generated by using the SDH/STM-64 Network Analyzer provided by Acterna, which generated SDH packets containing a  $2^{31} - 1$  maximal-length PRBS at 9.953 28 Gb/s and consisting of 10-ps pulses at 1549.2 nm. The control signal was a continuous clock at the same rate consisting of 10-ps pulses at 1554 nm. The data input streams were decorrelated in the switch by using different optical delays between them, while the control stream could be turned on or off to assess the switch states.

Fig. 33 shows the eye measurements for the input and output signals from the switch. In particular, Fig. 33(a) and (b) shows the eyes of the two input data streams, which are identical. Fig. 33(c) and (d) shows the two output streams for the BAR state and the CROSS state, respectively. The degradation of the eye diagrams at the output of the switch is due to crosstalk and incomplete polarization extinction in the switch. The error rate was statistically calculated from the network analyzer by checking the appropriate control bits at each SDH/STM-64 packet and was less than  $10^{-11}$  for both data signals in both switching states. The switch was polarization sensitive due to the polarization gain dependence of the SOA as well as to the PMF arrangement in the UNI so that the error rate gradually increased as the polarization states of the interacting signals drifted. However, simple adjustment of the polarization controllers was sufficient to revert to the initial error-free operation. This means that the switch may be error-free-operated with a closed-loop electrical polarization controller.

## VI. CONCLUSION

All-optical switching technologies have become very mature over the past few years, and development has reached the point that the first all-optical switches are now commercially available. At the same time, application domains for which all-optical processing techniques possess significant cost and performance advantages compared with the electronic ones are starting to emerge. In this context, the ESPRIT DO\_ALL project has significantly contributed to the demonstration

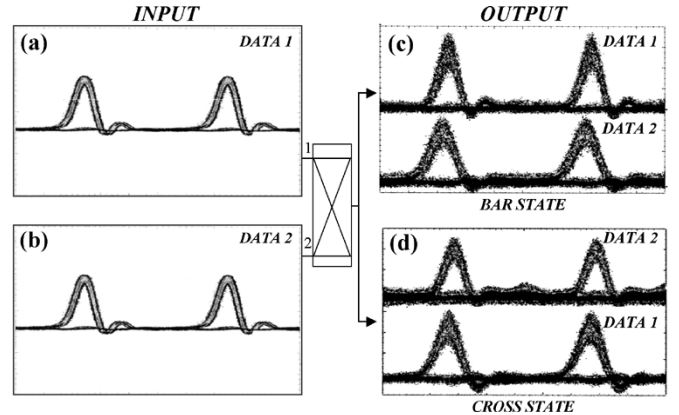


Fig. 33. Eye measurements with (a) and (b) STM-64 input frames, (c) BAR state, and (d) CROSS state. The time base is 20 ps/div.

TABLE II  
REPRESENTATIVE SAMPLES OF ICs AND THE PERIODS OF THE  
GENERATED BINARY SEQUENCES

IC	Period of the generated PRBS	T <sub>BS</sub>
001101001110	0111001011001011100101011110	28
001001101111	11110110010010	14
001011100101	1010011	7

of a complete set of logic modules and to the construction of the technological platform required to perform all-optical signal processing tasks. It has also investigated the subsystem integration capability to perform error-rate measurements in the optical domain, and it has proved, through the demonstration of an optically addressable exchange-bypass switch that advanced functionalities can be obtained from single optical gates. Moreover, the theoretical and experimental work performed within its frame on the operation of the SOA devices and all-optical gates has enabled the development of useful operational guidelines, which, in turn, have led to the demonstration of several novel functional subsystems for all-optical packet switching applications, such as packet address and payload separation for short 10-Gb/s packets [71], a 10-Gb/s all-optical half-adder [72], and a clock- and data-recovery circuit for 10-Gb/s asynchronous optical packets [73]. However, further efforts are still needed to provide integrated solutions for the demonstration of true all-optical packet switching. The outcome of these efforts, combined with the direction that the telecommunications business will take from now on and for the next few years, will influence the verdict on the commercial applicability of all-optical circuits and all-optical processing techniques.

## APPENDIX DESIGN ALGORITHM OF ALL-OPTICAL LFSR

It is well known that in the Galois field of order 2 (GF(2)) for every integer  $q$ , each polynomial  $f(X)$  of degree  $m$  is given by [74]

$$[f(X)]^{2^q} = \sum_{i=0}^{m-1} f_i(X^i)^{2^q}. \quad (2)$$

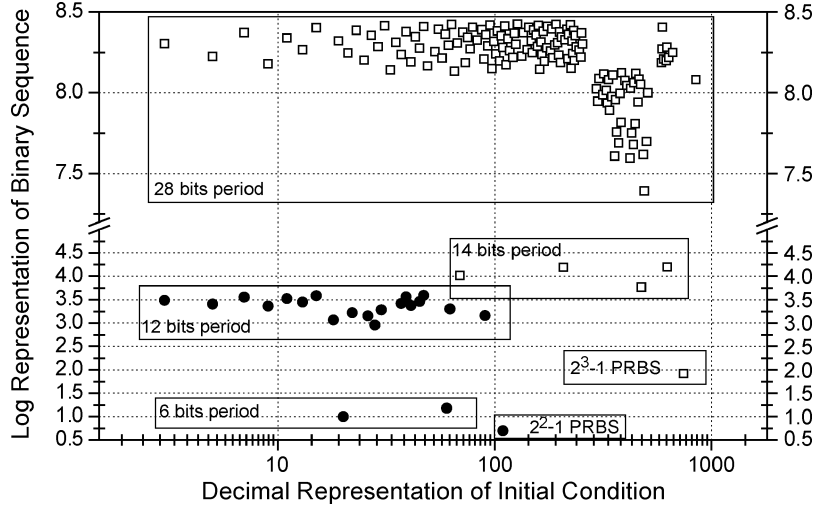


Fig. 34. Logarithm of decimal representation of ICs versus the logarithm of the decimal representation of the binary sequence for the characteristic polynomial  $X^{12} + X^4 + 1$  (white squares) and  $X^8 + X^4 + 1$  (black circles).

The generating function  $G(X)$  of a linear feedback shift register (LFSR) with a characteristic polynomial that satisfies (2) is given by [75]

$$G(X) = \frac{\sum_{i=1}^m c_i X^i [\alpha_{-i} X^{-i} + \dots + \alpha_{-1} X^{-1}]}{1 + \sum_{i=1}^m c_i X^i} = \frac{g(X)}{[f(X)]^{2^q}} \quad (3)$$

where  $c_i$  are the binary feedback coefficients ( $c_i = 1$  if the  $c_i$ th tap is selected as feedback, else  $c_i = 0$ ) and  $\alpha_{-1}, \alpha_{-2}, \dots, \alpha_{-m}$  are the bits of the initial condition (IC). The polynomial  $g(X)$  is determined from the feedback function of the LFSR and the IC. The latter can always be selected so that

$$g(X) = [f(X)]^{2^q - 1}. \quad (4)$$

Equations (3) and (4) indicate that if an LFSR has a characteristic polynomial given by (2) and is initialized according to (4), then it is equivalent in terms of the PRBS that it produces to the LFSR whose characteristic polynomial is the primitive polynomial  $f(X)$ . The generating function of the former LFSR is indeed given by

$$G(X) = \frac{[f(X)]^{2^q - 1}}{[f(X)]^{2^q}} = \frac{1}{f(X)}. \quad (5)$$

Equation (5) shows that the initial LFSR of degree  $(m \times 2^q)$  can be “shrunk” to a new one of lower degree  $m$ , if it is initialized with a binary sequence that is the reciprocal primitive polynomial  $f^{-1}(X)$ . The PRBS produced is then a maximal-length PRBS with period  $2^m - 1$ .

According to this analysis, the design algorithm of an all-optical LFSR is as follows.

- Step 1) Determine the primitive polynomial  $f(X) = X^m + X^k + 1$  that produces the desired  $2^m - 1$  maximal-length PRBS.
- Step 2) Determine experimentally the number of FFs of the longest feedback or the shift register ( $N_{\text{FF}}$ ) and the

number of FFs of the shortest feedback or intermediate tap ( $N_{\text{Tap}}$ ).

- Step 3) If  $N_{\text{FF}} = m \times 2^q$  and  $N_{\text{Tap}} = k \times 2^q$ , where  $q$  is an integer, then the circuit is ready, else the number of FFs of the LFSR ( $N_{\text{FF}}$ ) and the number of FFs of the intermediate tap ( $N_{\text{Tap}}$ ) must be set experimentally by adjusting the frequency of the radio-frequency (RF) driving generator, according to the aforementioned conditions.

- Step 4) Initialize the LFSR with  $N_{\text{FF}}$  bits of the  $2^m - 1$  maximal-length PRBS that is produced from the reciprocal primitive polynomial  $f^{-1}(X) = X^m + X^{m-k} + 1$ .

A simulation tool was developed to verify the validity of this algorithm. As an example, we consider the case that the desired PRBS is the  $2^3 - 1$  maximal-length PRBS “produced” from the primitive characteristic polynomial  $X^3 + X + 1$ . We assume that the experimentally adjusted lengths of the two feedbacks (shift register and intermediate tap) of the LFSR correspond to the characteristic polynomial  $X^{12} + X^4 + 1$  ( $X^{12} + X^4 + 1 = X^{3 \cdot 2^2} + X^{2^2} + 1 = [X^3 + X + 1]^{2^2}$ ) according to the algorithm. The algorithm stipulates that if the LFSR is initialized with the  $2^3 - 1$  maximal-length PRBS “produced” from the primitive characteristic polynomial  $X^3 + X + 1$  (modulated so that the shift register is fully filled), the characteristic polynomial of the equivalent LFSR is  $X^3 + X + 1$ , and the PRBS produced has period  $2^3 - 1$ , instead of the normally expected maximal- or submaximal-length PRBS with period  $2^{12} - 1$ . The LFSR with characteristic polynomial  $X^{12} + X^4 + 1$  was simulated, and it was found that it generates binary sequences that can be categorized in three families in terms of their period. Specifically, the LFSR generates 144 different binary sequences with 28-b-long periods, four different binary sequences with 14-b-long periods, and finally one binary sequence with a 7-b-long period. This last binary sequence is the  $2^3 - 1$  maximal-length PRBS, which is produced from the primitive polynomial  $X^3 + X + 1$ . The corresponding IC consists of one period, and the five first bits of the second period

of the  $2^3 - 1$  maximal-length PRBS. Specifically, the IC is  $\{001011100101\}$ , and the bold bits represent the period of the  $2^3 - 1$  maximal-length PRBS, produced from the primitive polynomial  $X^3 + X^2 + 1$ . Table II shows representative samples of the ICs and the period of the produced binary sequence ( $T_{BS}$ ) of the three aforementioned families.

Fig. 34 depicts the results of the algorithm. As examples, we consider the binary sequences produced from the LFSRs with characteristic polynomials  $X^{12} + X^4 + 1$  (white squares) and  $X^8 + X^4 + 1$  (black circles). The graph shows the logarithm of the decimal representation of the ICs versus the logarithm of the decimal representation of the binary sequences produced. Binary sequences with longer period have binary digits of higher order and consequently appear with higher corresponding decimal values. As a result, the three groups of the produced binary sequences are distinct, as it can be seen in Fig. 34. Furthermore, there is only one IC that “shrinks” the characteristic polynomial of the LFSR from  $X^{12} + X^4 + 1$  to  $X^3 + X + 1$  and from  $X^8 + X^4 + 1$  to  $X^2 + X + 1$  so that the produced PRBSs are the  $2^3 - 1$  and  $2^2 - 1$  maximal-length sequences, respectively. We were able to simulate LFSRs with characteristic trinomials of degrees up to 25 with a computational time of a few minutes, and in all cases the algorithm was verified.

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