Metrology for the Electrical Characterization of Semiconductor Nanowires

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(Invited Paper)

***Abstract*—Nanoelectronic devices based upon self-assembled semiconductor nanowires are excellent research tools for investigating the behavior of structures with sublithographic features as well as a promising basis for future information processing technologies. New test structures and associated electrical measurement methods are the primary metrology needs necessary to enable the development, assessment, and adoption of emerging nanowire electronics. We describe two unique approaches to successfully fabricate nanowire devices: one based upon harvesting and positioning nanowires and one based upon the direct growth of nanowires in predefined locations. Test structures are fabricated and electronically characterized to probe the fundamental properties of chemical-vapor-deposition-grown silicon nanowires. Important information about current transport and fluctuations in materials and devices can be derived from noise measurements, and low-frequency $1/f$ noise has traditionally been utilized as a quality and reliability indicator for semiconductor devices. Both low-frequency $1/f$ noise and random telegraph signals are shown here to be powerful methods for probing trapping defects in nanoelectronic devices.**

***Index Terms*—Nanoelectronics, semiconductor nanowires, test structures, $1/f$ noise.**

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I. Introduction

A CRITICAL barrier to the development of novel semiconductor nanowire devices with enhanced performance or new functionality is the development of the basic measurement science infrastructure for these structures. There are two approaches typically used to fabricate electronic devices based upon semiconductor nanowires: "bottom–up" approaches based on the growth [usually via chemical vapor processes (CVDs)] of semiconductor nanowires [1]–[5] and "top–down" methods based on defining nanowire devices by advanced lithography and etching [6]–[10]. Self-assembled or furnace-grown semiconductor nanowires have emerged as powerful building blocks for the assembly of nanoscale devices by the bottom–up paradigm (see, for example, [1]). Such "bottom–up" nanowire devices hold the promise to overcome some of the fabrication challenges associated with making devices with sub-30-nm feature sizes. Liquid-vapor-phase growth catalyzed by metal nanoparticles can control the nucleation and subsequent growth of semiconductor nanowires [2]–[4]. By using this process, nanowires can be readily grown with lengths that are tens of micrometers long and diameters ranging from the sublithographic (as small as 3 nm [5]) to hundreds of nanometers. In addition to single-crystal structures with a homogeneous composition, axial and radial heterostructures can be grown [1]. Furthermore, since they are grown directly from catalyst, nanowires can be grown with smooth (nominally atomically smooth) sidewalls. Thus, there are none of the artifacts and processing difficulties associated with line-edge roughness that would be associated with top–down wires formed by using conventional lithography and etching techniques. While top–down methods leverage the extensive fabrication infrastructure developed for the Si complementary metal–oxide–semiconductor (CMOS) industry, fabrication of Si nanowire (SiNW) devices by this approach requires advanced (and costly) lithography and etching processes. Many bottom–up nanowire-based devices can be made without extensive and expensive fabrication facilities, enabling a wider range of research scientists to investigate and make advances in this technology.

New test structures and associated measurement methods are the primary metrology needs necessary to enable the development, assessment, and adoption of emerging nanoelectronic device technologies such as those based upon semiconductor

nanowires to enhance and extend the capabilities of CMOS. In particular, test structures that enable electrical contacts to nanowires with sublithographic diameters and advanced electrical characterization of these devices are required to develop SiNW field-effect transistors (FETs) into a commercially viable technology.

While it is relatively straightforward to grow small diameter nanowires, it is a challenge to reliably contact the nanowires to form test structures and demonstrate prototypical devices. We present two fabrication approaches that can be used to form semiconductor nanowire devices: one based upon harvesting and positioning nanowires [11] and one based upon the direct growth of nanowires in predefined locations [12]. These approaches can be applied generically to nanowires of nominally any material, and they do not rely on deep submicrometer electron beam or projection lithography. Because of the pervasive nature of silicon in today's integrated circuit technology, we demonstrate these fabrication methods by fabricating nanoelectronic test structures for SiNWs.

Because of the large surface-to-volume ratio of nanowire FETs and subsequently enhanced scattering from surface states, the low-frequency current noise fluctuations can be pronounced in such devices. Therefore, a thorough understanding of the noise properties is critical to reduce the noise and fluctuations in nanowire devices and for the eventual design and integration of semiconducting nanowire functional units in nanoelectronics. Noise contains important information about current transport and fluctuations in materials and devices, and low-frequency $1/f$ noise has traditionally been utilized as a quality and reliability indicator for semiconductor devices [13]–[16]. Because noise is more sensitive to traps and defects as the size of devices is reduced, the use of noise as a defect characterization method has become more popular in recent years due to device scaling (unlike capacitance–voltage and charge-pumping measurement methods which become less accurate as the device size decreases and require a substrate contact). The noise properties of individual SiNW FETs (formed by using directed assembly) were measured and are reported here. The Hooge's parameter is determined from the gate dependence of the noise amplitude. A direct correlation between $1/f$ noise and interface state density is observed by characterizing devices before and after annealing to passivate many of the scattering sites.

Discrete switching events in the drain current measured as a function of time or random telegraph signals (RTSs) arise from the fluctuating occupancy of individual electron traps near the conduction channel of nanowire FETs [17]. The study of RTS can provide a novel technique to probe a single trap and allows one to understand the fundamental physics behind the carrier transport and current fluctuations in nanoscale devices [14], [19], [20]. In this paper, two- and three-level RTSs are observed at low temperatures in n-type ZnO nanowire FETs. The physical nature of the traps responsible for this switching is analyzed.

II. Test Structure Fabrication Approaches

A. Single Nanowire Manipulation System (SNMS)

We have developed a SNMS to precisely maneuver and align individual nanowires to form prototypical nanowire devices and test structures [11]. With this SNMS, individual nanowires can be picked up and transferred to a predefined location by electrostatic force. Fabrication processes based on one level of photolithography have been developed to simultaneously pattern multiple aligned nanowires. After growth, the SiNWs are harvested into a suspension of deionized (DI) water by sonication (1 min) [Fig. 1(b)]. The SiNW solution is dispersed onto a template substrate (which has been previously patterned into a series of mesas to reduce the electrostatic attraction between the nanowires and the substrate) and dried for 4 h under vacuum at 100 mtorr [Fig. 1(c)]. As shown schematically in Fig. 1(c) and (d), the SNMS is then used to pick up selected nanowires and transfer them to predefined locations on a device substrate that has been photolithographically patterned. If needed, the nanowires are further aligned to the device substrate more precisely. Finally, top metal contacts were patterned via conventional photolithography [Fig. 1(e)] to complete the nanowire devices and test structures.

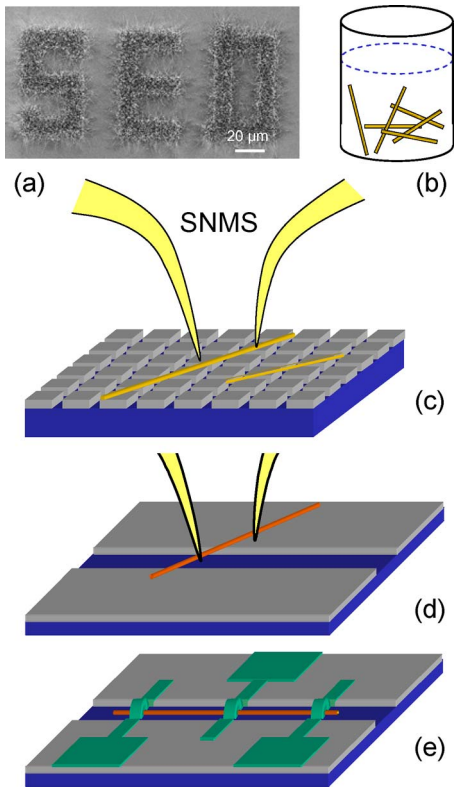

Fig. 1. SNMS fabrication approach. (a) Scanning electron beam micrograph of SiNWs grown from patterned Au catalyst on a Si wafer. (b) Nanowires harvested into a suspension of DI water. A drop of the nanowire solution was dispersed on a template substrate and evaporated under a vacuum of 100 mtorr for 4 h. (c) Schematic of manipulator tips picking up a nanowire from a template substrate. (d) Placing a single nanowire on a device substrate containing an alignment trench. (e) Device after formation of metal contacts.

The SiNWs used in this paper [Fig. 1(a)] were formed by using low-pressure chemical vapor deposition under 350 mtorr SiH_4, at 450 °C, with thin Au films (≈2–4 nm) as the catalyst via a vapor–liquid–solid mechanism [1]–[3]. The nanowires obtained by this approach are 20–300 nm in diameter and 2–150 μm in length. An example of SiNWs on a patterned catalyst substrate is shown in Fig. 1(a). Several nanowires ranging from ≈40 to ≈100 nm in diameter were characterized

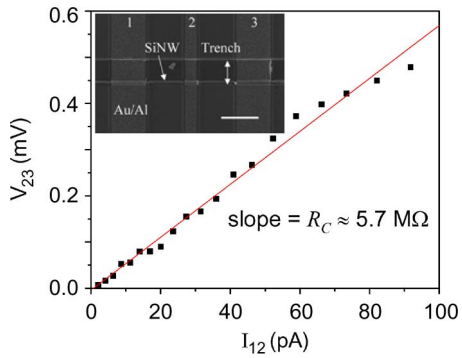

Fig. 2. Kelvin test structure to extract metal/nanowire contact resistance. Inset: Scanning electron beam micrograph of Kelvin test structure (scale bar: 5 μm). This structure, fabricated by using the SNMS, has three electrodes: 1, 2, and 3. Plot of the voltage between metal/SiNW contacts 2 and 3 (V_{23}) as a function of the current through electrodes 1 and 2 (I_{12}). The slope is the contact resistance ($\approx$5:7 MΩ) of this SiNW (78 nm in diameter).

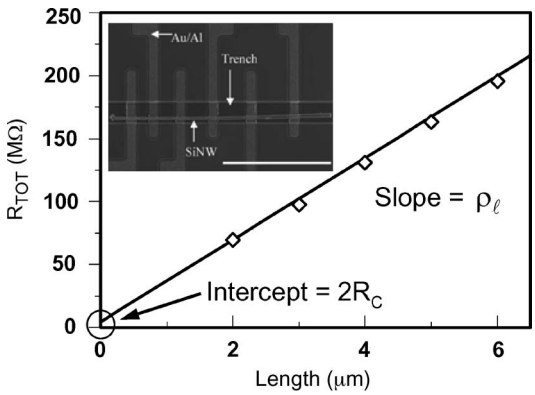

Fig. 3. Plot of total resistance (R_{TOT}) as a function of contact spacing length (2–6 μm) obtained at 1.0 nA. The intercept is $2R_C$, where R_C is the contact resistance (R_C is 2.4 MΩ on average). The slope is the resistance per micrometer ρ_ℓ (32.5 MΩ on average for this undoped SiNW; 150 nm in diameter). Inset: SEM image of a TLM test structure for the characterization of metal/SiNW contact resistance fabricated by using the SNMS. (Scale bar: 20 μm).

by transmission electron microscopy (data not shown). These SiNWs were observed to have a hexagonal cross section and growth along the expected [111] direction [4] with a spacing between the (111) planes, which are oriented perpendicular to the SiNW growth direction $\approx$0.31 nm.

The SNMS is an excellent approach for fabricating test structures to probe the fundamental properties of semiconductor nanowires. For example, it can be used to fabricate Kelvin test structures and transfer length method (TLM) structures which rely on multiple contacts to a single nanowire to separate the contact resistance from the nanowire resistance.

The Kelvin test structure is a conventional semiconductor characterization technique widely used to measure contact resistance [24]. As shown in the inset of Fig. 2, a nanowire-based Kelvin test structure with Al contacts to the SiNW was fabricated by using the SNMS. This three-contact structure was annealed in nitrogen at 420 °C for 60 s to improve the electrical contacts. The contact resistance R_C is

$$R_C = \frac{V_{23}}{I_{12}} \tag{1}$$

where the current I_{12} flows from contacts 1 to 2 and V_{23} is the voltage drop measured between contacts 2 and 3. The contact resistance ($\approx$5.7 MΩ for this device) is determined from the slope of the plot of I_{12} as a function of V_{23} (as shown in Fig. 2) by using a linear least square fit (LLSF).

The TLM test structure has been widely used as a precise technique for extracting both the contact resistance and the resistance of the nanowire itself [24], [25]. A SiNW-based TLM test structure with Al contacts is shown in the inset of Fig. 3. This device was fabricated by using the SNMS followed by annealing with N_2 at 420 °C for 60 s to improve the Al/Si contact. In a TLM test structure, the total resistance (R_{TOT}) of any two contacts is

$$R_{\mathrm{TOT}} = 2R_C + p_\ell L \tag{2}$$

where R_C is the contact resistance, ρ_ℓ is the resistance per unit length of this relatively large SiNW (165 nm in diameter), and L is the contact spacing. The plot of total resistance R_{TOT} as a function of contact spacing is shown in Fig. 3. For this particular intrinsic SiNW, the intercept $2R_C = (4.85 \pm 0.24)$ MΩ, and the slope is $\rho_\ell = (32.5 \pm 0.3)$ MΩ/μm as determined from the average (and standard deviation) of the slope and intercept of LLSFs for seven experimental total resistance curves obtained under currents of 0.8–1.4 nA (in 0.1-nA steps). The contact resistivity $\rho_c = (R_c) \cdot$ area can be estimated by approximating the area of the nanowire/metal contacts as the nanowire circumference times the length of the metal/nanowire contact. For these examples, it is found that ρ_c is approximately $2 \times 10^{-2}\ \Omega \cdot \mathrm{cm}^2$ from the TLM measurements and $3 \times 10^{-2}\ \Omega \cdot \mathrm{cm}^2$ from the Kelvin structures.

In addition to fabricating FETs and electronic test structures, the SNMS fabrication approach has been shown to be effective for fabricating nanowire electromechanical (NEM) switches [26]. These NEM devices—consisting of CVD-grown silicon nanowires suspended over metal electrodes—are operated by applying a voltage which creates an electromechanical force and bends the suspended part of the nanowire to touch a metal electrode. In addition to performing as excellent nanometer-scale electrical switches, such structures can also be used to extract material properties such as Young's modulus which can be challenging to determine in nanometer-sized device components.

B. Directed Self-Assembly

While most research on self-assembled nanowire devices involves forming a nanowire solution by harvesting nanowires from the preparation substrate and suspending them in liquid, these approaches are likely to introduce contaminants on the surface of the nanowires. Such a contaminated surface could increase the device interface states (D_{it}) and seriously deteriorate the device performance. Growing semiconductor nanowires in place from predefined catalyst locations is an approach that both enables the simultaneous batch fabrication of large numbers of nanowire devices and reduces the number of processing steps that may contaminate the nanowire surfaces.

To illustrate the self-aligned nanowire growth approach, we have fabricated SiNW FETs with HfO_2 as the gate dielectric. In this directed assembly approach [12], devices are fabricated

from SiNWs that are grown in place from Au catalyst (~1 nm thick) patterned in predefined locations on 50-nm thermal SiO_2. In the simplest structures, the p-type silicon substrate can be used as a bottom gate electrode. The SiNWs were grown in a low-temperature CVD furnace, at 420 °C, under 500-mtorr SiH_4 via a vapor–liquid–solid mechanism. Under these conditions, SiNWs are nominally 20 nm in diameter and regularly ≈20–30 μm in length after a growth time of 2 h. The SiNWs are thermally oxidized at 700 °C for 30 min to grow a thin oxide (estimated to be 3.5 nm thick [27]) that will be the basis of the dielectric interfacial layer. Because of the high diffusion constant of Au, it is a well-known problem in Si CMOS; therefore, there is always great concern about the use of Au as a catalyst to grow SiNWs. While Au atoms have been detected in SiNWs grown by using Au catalyst in the VLS process, direct measurements of the minority carrier diffusion length versus nanowire diameter observed that the influence of Au is minimal, and surface recombination controls minority carrier transport [28]. In the directed assembly process, the Au catalyst that remains on the end of the wire is not removed before the devices are processed. We presume that the additional chemical processing to remove the Au is more likely to be detrimental to the overall performance of the devices than the remaining gold which is covered by the source/drain metals in these SiNW FET structures and located several micrometers away from the conducting channel.

After oxide growth and before HfO_2 deposition, source/drain contact openings were formed by a 60-s etch in 2% HF. Ni was then thermally evaporated followed by metal liftoff to form the source/drain contacts. A layer of HfO_2 was then deposited as the top gate dielectric of the SiNW FET by atomic layer deposition at 250 °C. The top gate electrode (Al) is formed by using liftoff processes similar to those used in forming the source and drain electrodes. A schematic of the resulting devices is shown in Fig. 4(a) and (b) along with a scanning electron micrograph of a top-gated FET device in Fig. 4(c). The transfer curves for a typical top-gated SiNW FET (with a nominal diameter of 20 nm and a nominal length of 6 μm) formed by directed self-assembly are shown in Fig. 5(a) to illustrate the effectiveness of this fabrication approach. It is observed that, in some device fabrication runs, the use of Ni contacts leads to ambipolar device behavior; however, in certain device fabrication runs, little or no "reverse" current is observed for positive gate biases. Data are obtained for a device both before and after a forming-gas rapid-thermal anneal for 300 s at 300 °C. After annealing, the hysteresis observed in the I_d–V_g characteristics that swept from −3 V to +3 V and back to −3 V is typically 25–35 mV at the threshold voltage. Before annealing, the hysteresis is slightly (tens of millivolts) larger but is still relatively small. The increase in the saturation current [Fig. 5(a)] and the dramatic decrease in the subthreshold slope [Fig. 5(b)] after annealing indicate the importance of this final processing step. The change in the subthreshold slope indicates that a large number of interface defects are passivated by the forming gas anneal. This decrease in defects also contributes to the increased saturation current. In addition, it is likely that the Ni contact will react with the Si in the nanowire during the anneal to form a silicide [29], [30] which could extend into

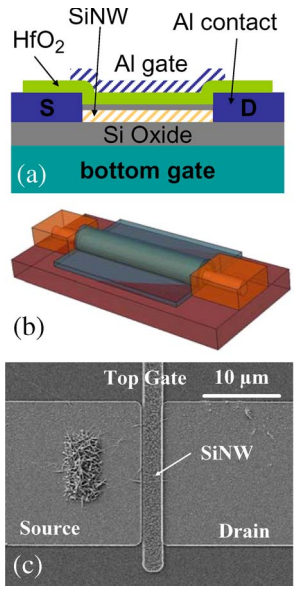

Fig. 4. SiNW FET formed by directed self-assembly. (a) Schematic drawing of device cross section along the length of the SiNW. (b) Three-dimensional schematic of top-gated SiNW FET. (c) Scanning electron beam micrograph of a typical top-gated SiNW FET with no gate-to-source/drain overlap. This example device appears to have two SiNWs: Note the patterned catalyst region in the source from which the SiNWs were grown.

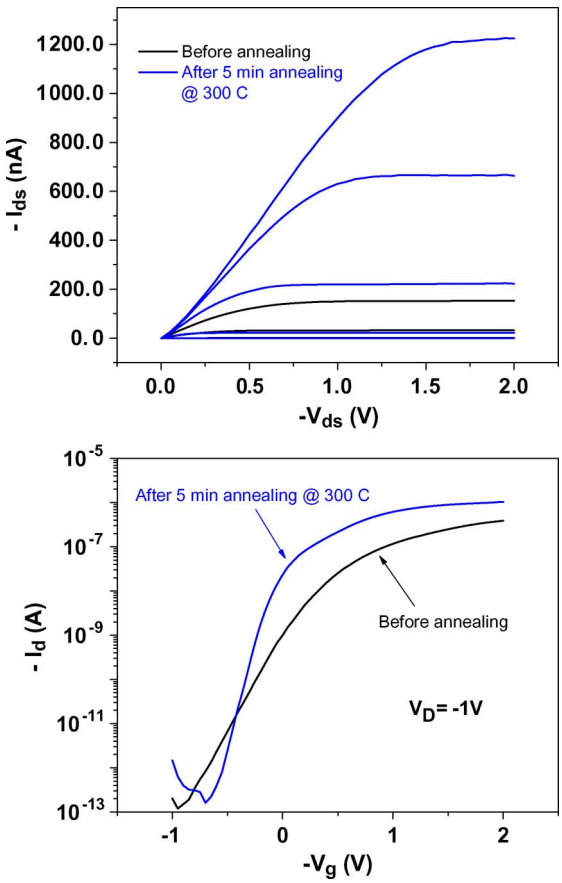

Fig. 5. Electrical characterization of a typical top-gated SiNW FET (with a nominal diameter of 20 nm and a nominal length of 6 μm) formed by directed self-assembly before annealing and after forming gas rapid thermal annealing for 300 s at 300 °C. (a) I_{DS}–V_{DS} curves at $V_g = +0.5$ to -1.5 V in -0.5-V steps. I_{ds} and V_{ds} are negative and shown in the positive quadrant for convenience sake. (b) I_{ds} as a function of V_g (before and after annealing) for $V_{ds} = -1$ V.

the channel region, effectively shorten the channel region, and further increase the saturation current.

This directed self-assembly fabrication approach has been shown to be effective for batch fabrication of a range of electronic devices such as large area (multiwire) thin-film transistors and charge storage devices for memory applications based on SiNWs with *in situ* grown oxide/nitride/oxide charge trap dielectrics [12]. Furthermore, high-performance Si NW FETs with a HfO_2 gate dielectric have been fabricated by using this technology which exhibited excellent electrical performance with large $I_{\rm on}/I_{\rm off}$ ratios $\sim 10^6$ and sharp subthreshold slopes $S < \approx 62$ mV/dec, approaching the limitations of conventional bulk Si FETs [31].

III. Noise Measurements

A thorough understanding of the noise properties of emerging nanoelectronic devices such as those based on semiconductor nanowires is critical because the signal-to-noise ratio is a fundamental factor limiting their performance. Noise measurements can also give great insights into defects and scattering mechanisms in nanowire devices. Because semiconductor nanowire devices have a very small total area (by definition), the capacitance associated with such devices is extremely difficult to measure accurately. This capacitance measurement challenge makes it impossible to use traditional capacitance–voltage/conductance–voltage techniques [24], [32]–[36] to determine the interface trap capacitance and, subsequently, information about the properties of the interface traps themselves. In addition, semiconductor nanowire devices have no body contact; therefore, charge-pumping techniques [24], [34], [37] cannot be used to investigate charge trapping centers. However, the trapping and detrapping of charge carriers from the nanowire conduction channel lead to low-frequency noise [16], [38], [39]. Under some conditions (such as at low temperatures or in extremely small nanowire devices), the trapping and emission of carriers by discrete interface or border traps lead to experimentally observed RTSs. Thus, noise measurements are the most experimentally accessible method to probe trap-induced scattering in semiconductor nanowire devices.

Typical normalized drain–current noise spectra $S_{\rm Ids}/I_{\rm ds}^2$ for a SiNW device fabricated by using directed self-assembly are shown in Fig. 6 with the device biased with a source–drain voltage, $V_{\rm ds} = -1$ V and the gate bias (V_g) varying from -1.5 to -2.4 V. The frequency range is from 1 Hz to 1.6 kHz. For consistency's sake, this is the same device from which the results in Fig. 5 are obtained. The low-frequency noise spectra are predominantly $1/f^{\alpha}$, with the frequency exponent α close to one (α ranges from 0.93 to 1.16 before annealing and from 1.10 to 1.13 afterward.)

Hooge introduced an empirical relationship relating the noise amplitude A (which is the product of the normalized drain–current noise spectra and f^{α}) to the total carrier number in the system N to describe the $1/f$ noise in homogenous bulk materials [40]

$$A = \frac{\alpha_H}{N} \tag{3}$$

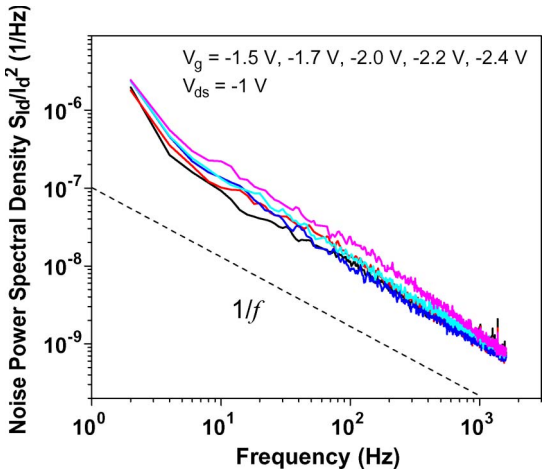

Fig. 6. Typical normalized drain–current noise spectra for a SiNW device fabricated by using directed self-assembly. $V_{\rm ds} = -1$ V, and the gate bias varies from -1.5 to -2.4 V. The frequency range is from 1 Hz to 1.6 kHz. (Note that data are from the same device as in Fig. 5).

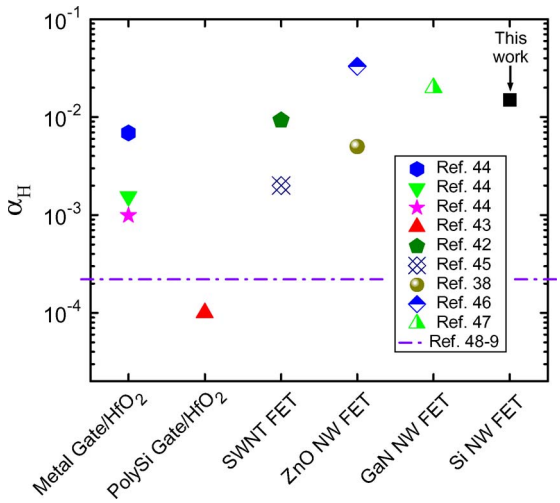

Fig. 7. Summary plot of the Hooge's constant obtained in this paper (black square) with previously published data for planar Si FETs with a poly-silicon gate/HfO_2 gate stack, a metal gate/HfO_2 gate stack, single-wall nanotube FETs, ZnO nanowire FETs, and GaN nanowire FET devices. Different values of the same type of device are from different reports. The dash-dotted line shows the ITRS requirement on α_H for the 45-nm technology node.

where α_H is the Hooge's constant. The Hooge's constant can be used to compare $1/f$ noise in different systems regardless of the specific device parameters and measurement conditions [40], [41]. α_H is typically on the order of 10^{-3} for bulk materials. By using (3) and writing N in terms of the device capacitance $C_{\rm dev}$, the inverse of A can be expressed as [38], [42]

$$\frac{1}{A} = \frac{C_{\rm dev}}{e\alpha_H}|V_g - V_{\rm th}|. \tag{4}$$

Thus, α_H can be determined from the relationship $1/A$ versus $(V_g - V_{\rm th})$ which can be calculated from the gate dependence of the noise amplitude. For these $\approx$20-nm SiNWs with a top gate and an interface oxide/HfO_2 dielectric, α_H is estimated to be 1.5×10^{-2} (after annealing). Fig. 7 shows the Hooge's constant of these unoptimized SiNW FETs, compared with previously published data for other advanced and emerging

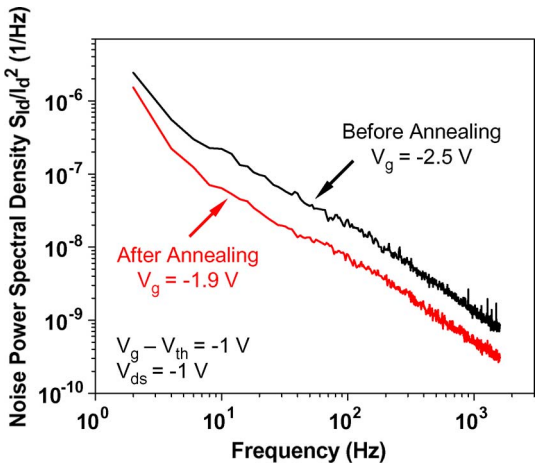

Fig. 8. Normalized drain–current noise spectra for a SiNW device (black) before and (red) after a 300-s forming gas anneal at 300 C. $V_g = -2.5$ and -1.9 V, respectively, so that $(V_g - V_{\rm th}) = -1$ V. $V_{\rm ds} = -1$ V.

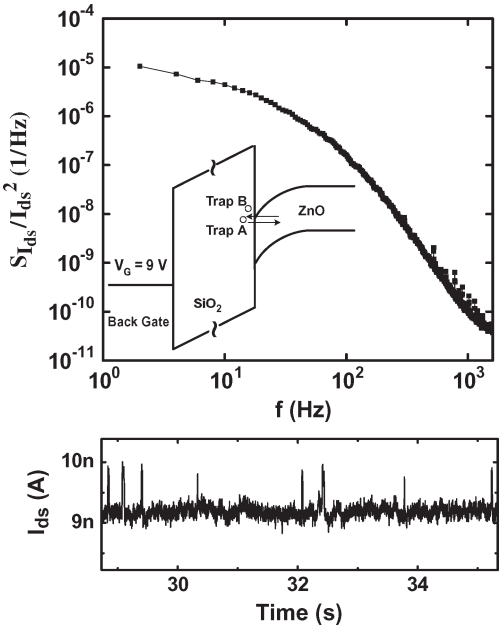

Fig. 9. ZnO nanowire FET noise properties at 4.2 K. (a) Typical Lorentzian spectrum when the device is biased at $V_g = 8$ V and $V_{\rm ds} = 2$ V. Inset: Band diagram for back gate voltage at 9 V with two near interface oxide (border) traps. (b) Time domain RTSs. Typical segment of a full 300-s $I_{\rm ds}$ versus time trace at $V_g = 8$ V and $V_{\rm ds} = 2$ V.

field-effect technologies: planar Si FETs with a poly-silicon gate/HfO_2 gate stack [43], Si FETs with a metal gate/HfO_2 gate stack [44], single-wall nanotube FET devices [42], [45], ZnO nanowire FETs [38], [46], and GaN nanowire FETs [47]. The dash-dotted line shows the ITRS requirement on α_H for the 45-nm technology node [48], [49]. Due to the high surface-to-volume ratio of nanowires, it is expected that noise may be larger in such devices compared with similar structures based on bulk substrates. However, low Hooge's constants $(\approx 1 \times 10^{-5})$ have been calculated for SiNW resistors where the noise of the reported devices with the lowest resistivity was analyzed by using a simple model in terms of the bulk and contact resistances [39]. While the Hooge's constant determined for the SiNW FETs reported here is not as dramatically small as this previous report, as shown in Fig. 7, the Hooge's constant of our SiNW FETs is similar to the values reported recently for other emerging nanowire FET technologies. In addition, it is anticipated that by optimizing the processing—particularly for the Si/dielectric interface formation and ALD HfO_2 deposition—the noise level of these research-grade devices will be greatly reduced.

As was shown in Fig. 5, a forming gas anneal (300 s at 300 °C) greatly improves the performance of the SiNW FETs. Fig. 8 shows that a decrease in the normalized drain–current noise power spectrum density is also observed after annealing. From the dramatic change in the slope of the $I_{\rm ds}$–V_g subthreshold curves [Fig. 5(b)], it can be qualitatively seen that a substantial number of interface traps were passivated during the anneal. By comparing the threshold voltage before and after annealing and making a simple estimate for the gate dielectric capacitance, the reduction in the number of interface traps $\Delta {\rm D_{it}}$ can be estimated [24], and it was found to be $\approx 5 \times 10^{12}/{\rm cm}^2$. This decrease in trap density is directly observable as a reduction in the noise power spectrum illustrating that $1/f$ noise can be used to probe interface traps in nanowire devices.

As just discussed, at room temperature, the noise power spectra of semiconductor nanowire FETs typically have a classic $1/f$ dependence. When the temperature is lowered significantly, the low-frequency noise sometimes changes from $1/f$ to a Lorentzian spectrum, and the current traces as a function of time show RTSs [17]. By carefully measuring and analyzing RTS, the sources of scattering in semiconductor nanowire devices can be understood in greater detail. We illustrate such an RTS behavior here for single nanowire FETs fabricated from ZnO nanowires that were synthesized by thermally vaporizing a mixed source of commercially available ZnO powder (99.995%) and graphite powder (99%) with a ratio of 1 : 1 in a tube furnace [38]. In these ZnO nanowire FETs, the low-frequency noise in the same device changes from $1/f$ at room temperature to a Lorentzian spectrum when the temperature is lowered to 4.2 K [17]. We have observed that discrete switching events in the drain current are more reliably observed in these ZnO FETs than in our SiNW FETs where we seldom observe RTS, even at cryogenic temperatures. Fig. 9(a) shows the typical Lorentzian noise spectrum of a ZnO nanowire FET biased at $V_{\rm ds} = 2$ V and $V_g = 8$ V at 4.2 K. Such a Lorentzian spectrum can be associated with the trapping and detrapping of a single defect in the dielectric around the nanowire and can be described by

$$\frac{S_{I_{\rm ds}}}{I_{\rm ds}^2} = \frac{K}{(1 + f/f_c)^2} \tag{5}$$

where K is a constant independent of frequency and f_c is the corner frequency of the Lorentzian. Such a single trap state signature is illustrated by RTS in the drain–current time trace (for $V_{\rm ds} = 2$ V and $V_g = 8$ V) segment in Fig. 9(b), where the channel current switches between two discrete values. Due to the shrinking of the activated energy window ($\approx 4k_BT$, where k_B is the Boltzmann constant and T is the temperature) in the dielectric band gap that occurs with the temperature reduced to 4.2 K, the number of defects energetically accessible to the

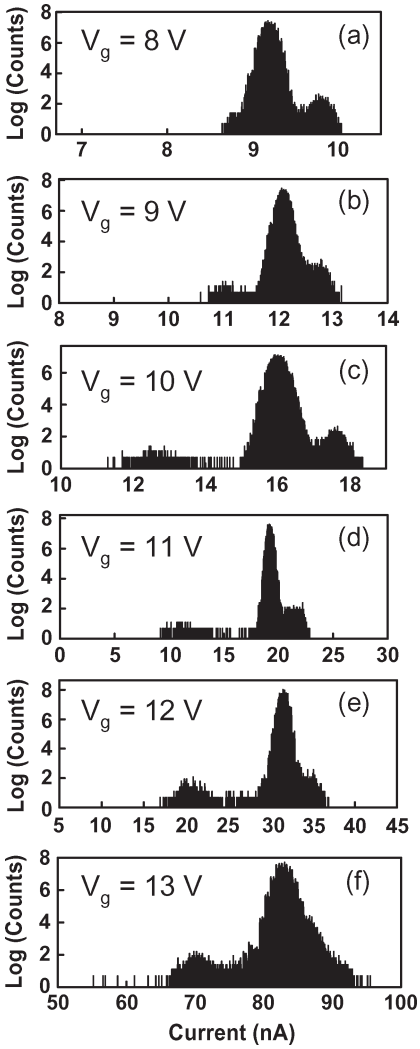

Fig. 10. Histograms formed from 300-s $I_{\rm ds}$ versus time trace at $V_{\rm ds} = 2$ V and $V_g = 8$–13 V in 1-V steps. $T = 4.2$ K.

carriers in the wire and responsible for the fluctuations is decreased to a few individual traps. In addition to the reduction in thermal energy broadening, in these ZnO nanowire FETs, there are three orders of magnitude decrease of current at 4.2 K compared with room temperature. As a result, the trapping/detrapping of carriers from the traps causes more dramatic fluctuations of the channel current.

RTS data with two discrete levels [such as in the segment of the $V_g = 8$ V trace shown in Fig. 9(b) and the accompanying histogram obtained from ≈300 s of such switching data shown in Fig. 10(a)] can be qualitatively described by a physical model in which there is only one near interface oxide (border) trap, i.e., A, interacting with the carriers through tunneling. This trap in the dielectric (or at the dielectric/semiconductor interface) resides in the band gap within $\approx 2k_BT$ of the Fermi level of the channel and is physically close enough to the channel to be able to be electrically active and take part in reversible capture and emission processes with the channel carriers. In this description, the state where one electron is captured by trap A is associated with the low current level, whereas the high current level corresponds to the empty state. Experimentally, as V_g is increased, negative peaks appear starting at $V_g = 9$ V, and the current trace shows three levels, as shown by three distinctive peaks in the histograms for $V_g = 9$–12 V [Fig. 10(b)–(e)]. While it has been reported that such a three-level switching could be due to multiple electron trapping at one defect site [14], we consider this an unlikely situation due to the repulsive force between an electron and a negatively charged trapping center. In a more likely scenario—shown by the schematic band structure in the inset of Fig. 9(a)—there is a second border trap [50], i.e., B, with a slightly different energy than trap A. Trap B comes within $\approx 2k_BT$ of the Fermi level in the ZnO nanowire at slightly higher gate biases. In this description, the high current value corresponds to the state where both traps are unoccupied, the middle current level is observed when trap A is charged while trap B is empty, and the low current level likely corresponds to the state where both traps are filled. At the highest gate voltages shown (13 V), only trap B aligns with the Fermi level, and trap A no longer participates in reversible capture and emission processes. In this case, a simple two-level RTS is again observed.

By applying signal processing techniques to time-dependent current traces, such data can be quantitatively analyzed. We have applied a method in which a hidden Markov model is estimated based on a Gaussian mixture and quantified by using a Viterbi decoder to measure the discrete current switching events [51]. Such an analysis enables the estimation of parameters such as event lifetime and event amplitudes. For example, by decoding the $V_g = 8$ V data, the mean time in the low current (≈9.2 nA) state is $\langle \tau_{\rm off} \rangle \approx 2.2$ s, whereas the mean time in the high current (≈9.8 nA) state is $\langle \tau_{\rm on} \rangle \approx 16$ ms. The frequency associated with these dwell times $f_c = 1/(2\pi\tau_0) \approx 10$ Hz, where $1/\tau_0 = 1/\tau_{\rm on} + 1/\tau_{\rm off}$, is consistent with the corner frequency f_c estimated by locating the peak in the $S_{I_{\rm ds}} \cdot f$ versus f plot (not shown). A full quantitative analysis of large statistically relevant data sets – particularly temperature-dependent data – will enable models to be understood in greater detail and the experimental determination of scattering parameters such as trap cross sections and energy barrier heights.

IV. Conclusion

While bottom–up semiconductor nanowire devices are a promising nanoelectronic technology of the future, they are already an important research tool nowadays. We have shown here two methods for fabricating nanoelectronic devices based on nanowires. Because these simple fabrication approaches do not rely on extremely expensive processing and lithography equipment, they should enable a large range of scientists to use them to advance nanowire research and technology. The batch processing aspect of the directed assembly approach allows the fabrication of statistically meaningful ensembles of similar SiNW devices. This feature enables the characterization of the reliability properties and failure mechanisms in nanowire devices. We have used noise measurements, an underutilized experimental approach, to characterize the low-frequency $1/f$ noise and RTS properties of nanowire FETs. The examples described here illustrate that noise measurements are the most experimentally accessible method for probing trapping defects in nanoelectronic devices.

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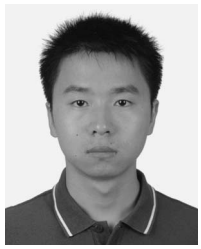

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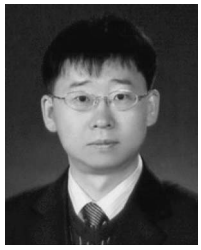

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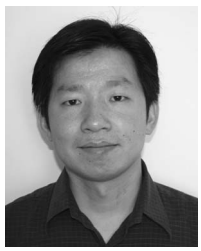

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