A 900-MHz 2.5-mA CMOS Frequency Synthesizer with an Automatic SC Tuning Loop

Tsung-Hsien Lin and William J. Kaiser, *Senior Member, IEEE*

***Abstract*—A 900-MHz phase-locked loop frequency synthesizer implemented in a 0.6-μm CMOS technology is developed for the Wireless Integrated Network Sensors applications. It incorporates an automatic switched-capacitor (SC) discrete-tuning loop to extend the overall frequency tuning range to 20%, while the VCO gain ($K_{\rm VCO}$) resulting from the CMOS varactor continuous-tuning is kept low at only 20 MHz/V in order to improve the reference spurs and noise performance. This frequency synthesizer achieves a phase noise of −102 dBc/Hz at 100 kHz offset frequency and reference spurs below −55 dBc. The synthesizer, including an on-chip VCO, dissipates only 2.5 mA from a 3-V supply.**

***Index Terms*—Frequency synthesizer, phase-locked loop, VCO.**

I. Introduction

WIRELESS Integrated Network Sensors (WINS) is a low-power, distributed, wireless micro-sensor network [1]. It combines sensing, signal processing, decision capability, and wireless networking capability in a compact system. Compact geometry and low cost allows WINS to be embedded and distributed at a small fraction of the cost of conventional wire-line sensor and actuator systems.

WINS can be deployed to collect physical data through densely distributed nodes. These collected data are processed locally among nodes. The processed sensor information will then be conveyed to the users at low bit rate with low-power transceivers. Typical WINS applications include condition-based maintenance, home automation, industrial controls, and biomedical instrumentation. These applications are usually characterized by the requirements for efficient wireless communication at a low data rate (<100 kbps) and short range (<30 m). Short range represents low path loss between nodes and low-data-rate communication requires only a low SNR at the receiving path. These range and data bandwidth reduction yield a significant advantage (60–80 dB) in the link budget in comparison with conventional long-range wireless communication systems. This link budget advantage can be properly factored into system design and translates into lower transmitting power and relaxed receiver requirements, thus achieving optimum system performance with low-power operation.

Manuscript received July 28, 2000; revised October 18, 2000. This work was supported by the Defense Advanced Research Project Agency, Electronics Technology Office, DARPA/ETO.

The authors are with the Department of Electrical Engineering, University of California, Los Angeles, CA 90095 USA (e-mail: tsunghsi@ee.ucla.edu; kaiser@ee.ucla.edu).

Publisher Item Identifier S 0018-9200(01)01475-5.

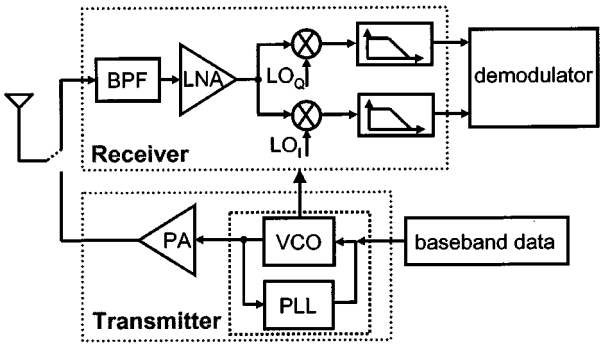

Fig. 1. Simplified WINS transceiver schematic.

The proposed transceiver operates at the 902–928-MHz ISM band with binary FSK signaling. The simplified transceiver schematic is shown in Fig. 1. A direct-conversion architecture is chosen to implement the receiver; the processed data are transmitted infrequently by directly modulating the VCO. Owing to the node-to-node link budget advantage resulting from range and data bandwidth reduction, a very low power receiver is feasible. Furthermore, since the transmitter only turns on infrequently, this leaves the frequency synthesizer (including the VCO) to determine the average power consumption of the whole transceiver.

The WINS remote sensing nodes are designed to operate with long life while powered by Li cells. This stringent power limitation along with the unique WINS system characteristics call for a new design methodology for a micro-power CMOS transceiver. One key component, a frequency synthesizer, is reported here.

II. Frequency Synthesizer Design Approaches

The primary design goal of the WINS communication system is to facilitate practical low-power radio implementation. A wide channel spacing of 250 kHz is chosen such that the FSK tone frequency can be placed away from dc (high modulation index). This arrangement effectively minimizes the impact of direct-conversion receiver noise (especially the overwhelming MOS devices $1/f$ noise) and ultimately saves power. Furthermore, most sensor applications are latency-tolerant and require only a slow hopping rate (<100 hops/s). A channel switching time of 2 ms is therefore adequate.

Until now, the only practical low-power frequency synthesis technique operating at the gigahertz range is the phase-locked loop (PLL). The limited available battery power mandates the simple integer-N PLL architecture. Although the relaxed

channel spacing and switching time requirements permit this PLL architecture, several design approaches are developed for this system to achieve low power.

In an integrated CMOS VCO design, large output voltage swings are usually favorable to improve the oscillator phase noise and mixer noise figure (NF). However, the poor Q-factor of CMOS on-chip inductors results in an inefficient usage of power [2]. In this work, high-Q off-chip inductors are employed to implement a high-performance low-power VCO. Ultimately, the high-Q passive components will be embedded in an LTCC substrate for an integrated radio [1]. Owing to the relaxed link budget, the WINS receiver can tolerate an NF of 25 dB. It is a waste of power to increase VCO output swings just for a minor improvement of mixer NF. Therefore, our VCO incorporating high-Q off-chip inductors optimizes for low phase noise with minimum currents, and it only produces necessary voltage swings for driving the mixer.

In evaluating the PLL noise performance, in addition to the oscillator phase noise, one also needs to consider other noise sources, especially the noise from the VCO tuning nodes. Any small amount of tuning noise will translate into frequency fluctuations and spurs. The magnitude of the reference spurs can be approximated by narrow-band FM and is determined by the VCO gain [$K_{\rm VCO}$ (Hz/V)], the amplitude of tuning noise (V_m), and the reference frequency ($f_{\rm ref}$), as demonstrated by the following relation between spur amplitude $A_{\rm spur}$ and carrier amplitude $A_{\rm carrier}$:

$$\frac{A_{\rm spur}}{A_{\rm carrier}} = \frac{1}{2}\,\frac{K_{\rm VCO}\times V_m}{2\pi f_{\rm ref}}. \tag{1}$$

From the equation above, it is evident that reducing both V_m and $K_{\rm VCO}$ can minimize the spurs. While increasing $f_{\rm ref}$ is helpful, this is not a normal practice. $f_{\rm ref}$ is usually not a design variable since it is determined by system specifications and PLL architecture.

Typically, a CMOS VCO with 20% of frequency tuning range is desirable in order to compensate for process and temperature variations. This results in a large $K_{\rm VCO}$ (it may be more than 100 MHz/V for a 3-V, 1-GHz VCO), which is more prone to higher spurs and phase noise. One approach to achieve a large tuning range and a small $K_{\rm VCO}$ simultaneously is by breaking a single wide-range tuning curve into several narrower-range sections with sufficient frequency overlap. This is accomplished by employing both discrete and continuous tunings, as illustrated in Fig. 2. CMOS on-chip continuous tuning can be implemented as reverse-biased PN junctions or MOS capacitors (either in the inversion-depletion or accumulation-depletion mode). The discrete tuning scheme has been exploited previously in [3]. It can be realized in the form of switched-inductor (SL) or switched-capacitor (SC) networks. In this work, the SC tuning topology is chosen over SL for its simplicity in design and maturity in standard CMOS technologies.

For a 900-MHz frequency synthesizer with this dual-loop topology, the ideal design is to have each VCO curve spanning twice the desired frequency range (2 $\times$ 26 MHz, 6% of 900 MHz) with 26 MHz ($\sim$3%) of overlap between two adjacent curves. This will guarantee that at least one curve can

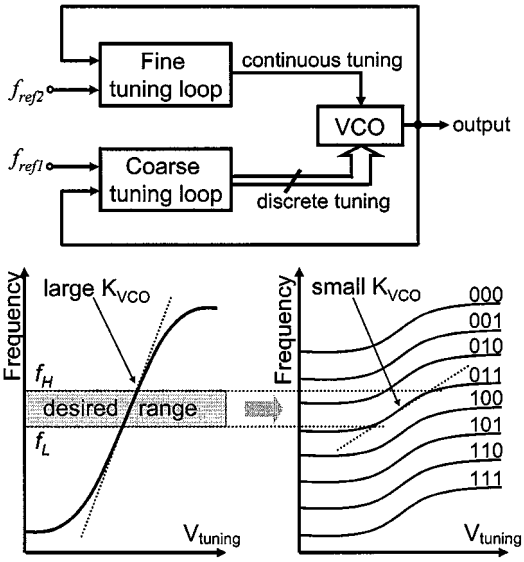

Fig. 2. Method of achieving a wide frequency tuning range with small VCO gain.

cover the whole ISM band. In practical implementation, the frequency tuning range is narrower at the low-frequency end due to increased capacitance. Therefore, each curve is nominally designed with a slightly larger tuning range. Even so, compared with a single tuning curve that covers the whole 20% frequency range, this technique still provides roughly 10-dB improvement in spur performance.

Low VCO gain design is also beneficial in improving power supply rejection. Supply noise manifests itself by modulating the transistor junction capacitance, thus creating sidebands near the oscillation frequency. By applying the same analysis technique as in analyzing the reference spurs (VCO control line noise), a result similar to that of (1) is obtained for the supply noise. This indicates that the low $K_{\rm VCO}$ design is less sensitive to the supply noise than is a VCO with high tuning gain.

Another design feature made to further reduce power is by operating the power-hungry dual-modulus divider at a lower frequency. For a high-speed dual-modulus divider, with additional logic operation to toggle between two moduli (7 and 8 in this work), it requires sharp-transition, high-frequency clocks, i.e., a VCO with large voltage swings. This is undesirable in a low-power system. Furthermore, the divider itself will drain large currents just by operating at 1 GHz. By inserting a divide-by-2 prescaler between the VCO and the dual-modulus divider, the requirement on the VCO output swing is relaxed, and the dual-modulus divider now operates at a lower 500 MHz. However, this modification requires the reduction of the reference frequency to 125 kHz to maintain a channel spacing of 250 kHz; thus, it trades low power for higher spurs [see (1)]. To address this issue, a third-order passive loop filter topology is chosen with the additional pole to improve the spur suppression.

This dual-loop PLL frequency synthesizer works as follows. The SC coarse tuning loop first searches for the proper frequency curve that covers the entire ISM band. Once found, the CMOS varactor is tuned to synthesize the desired channel in the main loop. To fully utilize this SC tuning approach, an automatic

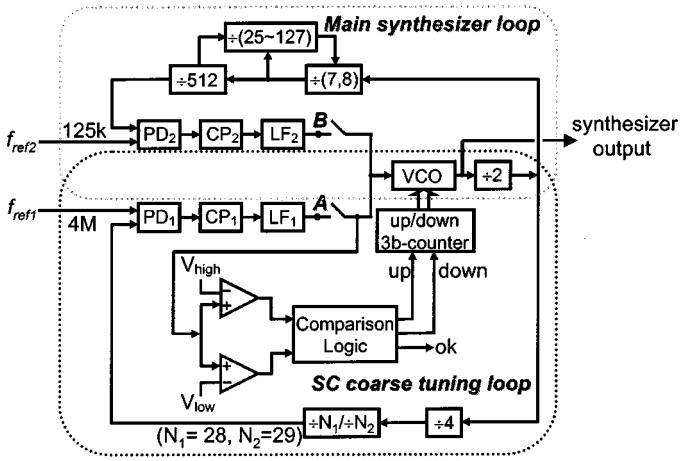

Fig. 3. Complete PLL frequency synthesizer schematic.

searching scheme has been developed and is detailed in the next section.

III. Frequency Synthesizer Operation

The complete PLL frequency synthesizer schematic is shown in Fig. 3. All the design parameters and the added divide-by-2 stage are shown. The SC coarse tuning loop is first enabled when the synthesizer is powered on. An up/down counter, which is controlled by some comparison logic, determines the switch positions of the SC network in the VCO. The search for the proper SC state (that represents the right frequency curve) is based on frequency comparison/locking. The VCO frequencies are compared to the lower (f_L) and upper (f_H) threshold frequencies to determine how to update the counter. These two frequencies are determined based on the following rules: $f_H \geq 928$ MHz and $f_L \leq 902$ MHz. In this work, f_H is set to 928 MHz (4 MHz $\times$ 8 $\times$ N_2) and f_L to 896 MHz (4 MHz $\times$ 8 $\times$ N_1). Here, N_1 is 28 and N_2 is 29.

The choice of these two threshold frequencies f_H and f_L entails some tradeoffs. To minimize the VCO gain ($K_{\rm VCO}$), one would set f_H and f_L to just the upper and lower edge of the ISM band to keep the required frequency range of each curve minimum. On the other hand, extending f_H and f_L outside of the ISM band can reduce the nonuniformity of $K_{\rm VCO}$. The tuning curves tend to flatten out when approaching the upper and lower ends of the frequency range. Therefore, $K_{\rm VCO}$ diminishes accordingly and the loop performance will depart from the desired one and sometimes even becomes unpredictable. This is a more serious concern for the main synthesizer loop since this loop is responsible for generating accurate channel frequencies for communication. Extending f_H and f_L further outside of the ISM band effectively places the desired 902–928-MHz range in the portion where the tuning curve is more linear and $K_{\rm VCO}$ is more constant. The nonuniformity of $K_{\rm VCO}$ is less a concern for the SC loop as long as this loop remains under stable operation. For demonstration purposes here, f_H and f_L are chosen so as to simplify the counter design.

A reference frequency of 4 MHz is chosen for the SC loop to enable a wide loop bandwidth and speed up the searching process. The searching process is detailed in the next section.

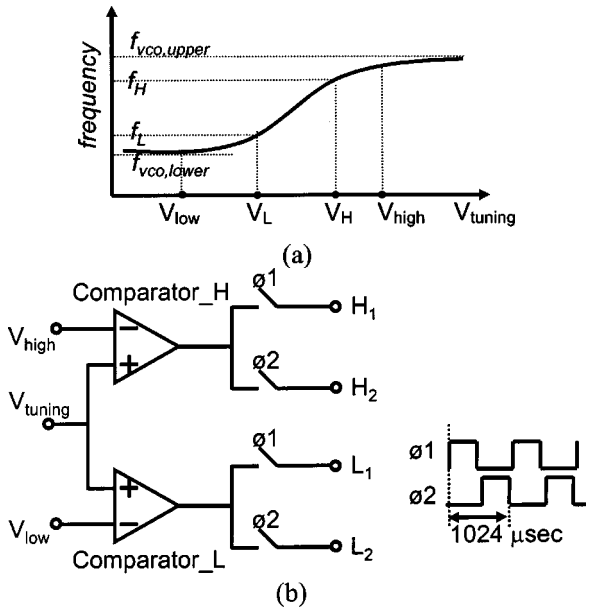

Fig. 4. (a) Frequency versus voltage at the 'ok' state. (b) Comparison stage schematic.

The SC loop is guaranteed to converge at the proper state by sufficient frequency overlap between adjacent VCO curves. Once the proper SC state is reached, the synthesizer will activate the main loop. The SC loop can then be shut down to save power or part of the loop (the comparison stage) can remain active to monitor the channel frequency. This SC searching process is required when the synthesizer is first turned on (initial calibration) or when the monitoring circuitry indicates that the frequency range is off (recalibration). Some applications may require periodic recalibration before transmitting or receiving.

IV. Circuit Implementation

A. Comparison Stage

The frequency comparison/locking during the searching of the right SC state is accomplished by comparing voltage quantities. Two comparators compare the loop filter (LF) outputs with two predefined voltages $V_{\rm high}$ and $V_{\rm low}$. Fig. 4(a) illustrates the relationships between frequencies and tuning voltages at the 'ok' state. At this state, the SC loop can lock the VCO frequencies to both f_H and f_L, with corresponding tuning voltages $V_H < V_{\rm high}$, and $V_L > V_{\rm low}$. Since typical MOS varactors have predictable tuning patterns, it is trivial to define these values. Here, $V_{\rm high}$ and $V_{\rm low}$ are set to 2.75 and 0.25 V, respectively, where the tuning curves are flatter (lower VCO gain). The schematic of the comparison stage is shown in Fig. 4(b).

A pair of nonoverlapping clocks ϕ_1 and ϕ_2 are generated by dividing 125 kHz (from the reference signal of the main loop) by 128. Each clock phase provides 512 μs for a comparison operation. During $\phi 1$, the SC loop tries to lock the VCO to 896 MHz, and to 928 MHz during $\phi 2$. The comparison begins at $\phi 1$, and the results are stored at H_1 and L_1; the comparison results are stored at H_2 and L_2 during $\phi 2$. After both comparisons are completed, the up/down counter updates its 3-bit output based on these stored results. Table I lists all combinations of the comparison results and the corresponding up/down/ok actions.

TABLE I
COMPARISON RESULTS

H_1	H_2	L_1	L_2	Frequency range	Action
1	1	1	1	$f_{vco,lower} < f_L$, $f_{vco,upper} < f_L$	down
0	1	1	1	$f_{vco,lower} < f_L$, $f_L < f_{vco,upper} < f_H$	down
0	0	1	1	$f_{vco,lower} < f_L$, $f_{vco,upper} > f_H$	lock
0	0	0	1	$f_L < f_{vco,lower} < f_H$, $f_{vco,upper} > f_H$	up
0	0	0	0	$f_{vco,lower} > f_H$, $f_{vco,upper} > f_H$	up

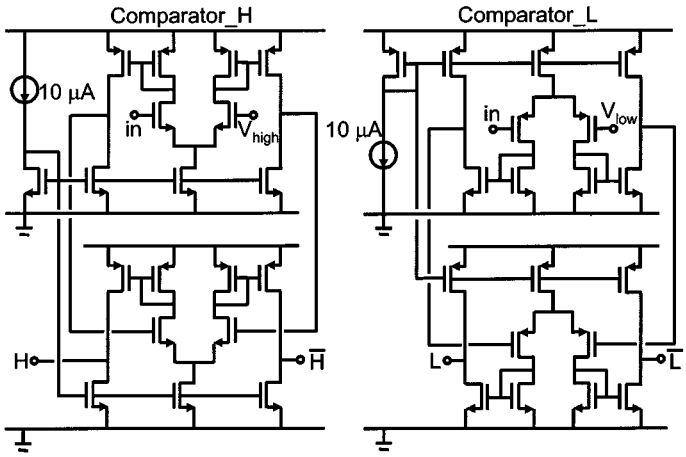

Fig. 5. Comparator circuits.

Two comparators are designed differently with comparator_H to sense voltages near V_{DD} and comparator_L to sense voltages near V_{SS}. For broad ranges of $V_{\rm high}$ and $V_{\rm low}$, the designs of both comparators are rather relaxed, since fine voltage comparisons are not required. A cascaded two-stage design, with the second stage sized to be 1/3 of the first stage for low power, provides a high open-loop gain to ensure binary outputs to interface with the following digital circuitry. Fig. 5 shows both comparators. Each comparator draws 40 μA.

B. VCO

The VCO schematic is shown in Fig. 6. Only one inductor is employed in this design in order to reduce external component counts. A pair of pMOS transistors instead of an nMOS pair is used to generate negative g_m to overcome the loss of the LC tank, for two reasons. First, in this fabrication process, pMOS has lower device flicker noise than that of the nMOS. Fig. 7 shows the measured MOS gate-referred noise at 100 kHz (both pMOS and nMOS have same geometry). While the discussion of this measured behavior is beyond the scope of this paper, it did indicate that pMOS has lower $1/f$ noise ($3 \sim 11$ dB) compared with nMOS in the interested biasing region. This can result in lower up-converted phase noise. Furthermore, the pMOS resides inside an N-well and is well isolated from the noisy Si substrate. Despite its lower mobility, pMOS is favored in this design due to low noise considerations.

The CMOS varactor in Fig. 6 is implemented as an accumulation-depletion mode MOS capacitor, for it has a better Q-factor [4]. An off-chip high-Q ($Q \sim 30$) chip-inductor is used in this VCO implementation. This inductor will be embedded in the low-temperature co-fired ceramic (LTCC) [5] substrate in future

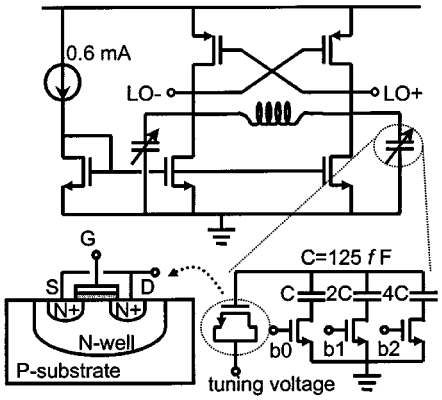

Fig. 6. VCO schematic.

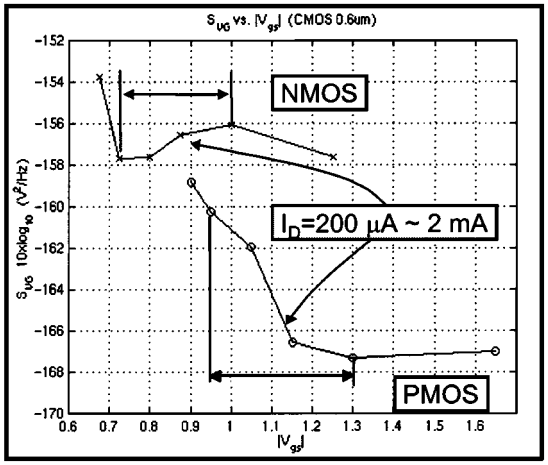

Fig. 7. Measured device flicker noise.

integration. LTCC offers a low-loss substrate and high-quality conductor which makes it attractive for high-Q, low-power applications. In one fabrication process that is currently under evaluation, the measured LTCC inductor quality factor is around 20–30. This is roughly one order of magnitude better than those of CMOS on-chip inductors. Higher Q can be achieved in LTCC with process modification.

In Fig. 6, two nMOS transistors mirror the biasing currents into the VCO core. With proper choice of transistor sizes and biasing current, the output dc voltage sits near half V_{DD}. This dc level effectively places the tuning curve in the middle of the power supply range, so that the whole tuning range of the accumulation-depletion mode MOS varactors can be fully applied. Furthermore, this circuit topology allows VCO to drive the prescaler (and the mixers of the receiving path) directly without the need of level shifting or ac coupling.

The design of the MOS switches in the SC network entails some tradeoffs. Wide transistors reduce the switch on-resistance, therefore improving the quality factor of the overall LC tank. However, this also increases parasitic capacitance at the drain nodes of the switches and limits the ratio of capacitance variation, consequently limiting the frequency tuning range. The choice of switch sizes must balance the requirements of low on-resistance and large ratio of capacitance variation.

The off-chip induced parasitic capacitance from bond pads, packages, and PCB traces can severely limit the tuning range.

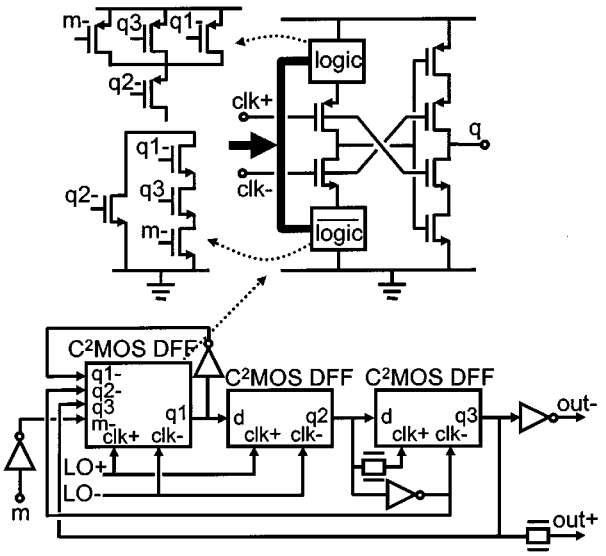

Fig. 8. The schematic of the dual-modulus divider.

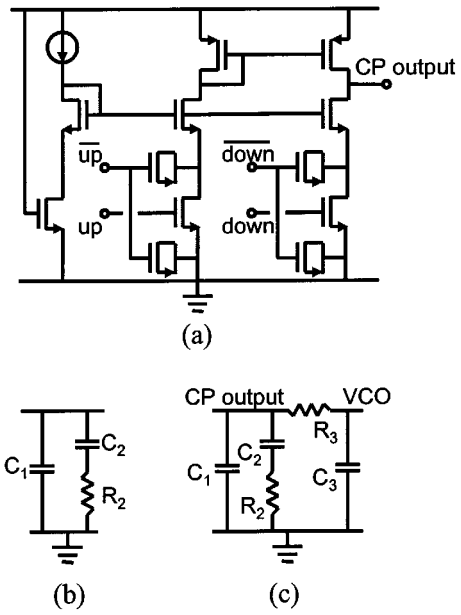

Fig. 9. (a) Charge pump circuit. (b) Second-order loop filter for the SC loop (on-chip). (c) Third-order loop filter for the main loop (off-chip).

Therefore, the ring-shaped transistor layout technique is used extensively to minimize parasitic capacitance at critical devices/nodes [3], [6]. These include the VCO output nodes, MOS switches, and in high-speed dividers.

C. Dividers

The 1-GHz divide-by-2 prescaler is implemented in C^{2}MOS logic [7] because it has few transistors and it utilizes differential signals from VCO, balancing the VCO's output loads. The rail-to-rail output of a C^{2}MOS DFF can easily interface with following divider stages. The divide-by-2 consumes 590 μA at 1 GHz. The following 500-MHz divide-by-4 and dual-modulus divider are also built in C^{2}MOS DFFs, and dissipate 130 and 190 μA, respectively. Fig. 8 shows the schematic of the dual-modulus divider. The modulus control logic has been absorbed into the first C^{2}MOS DFF to reduce current. The dividing ratio is controlled by signal "m."

To avoid large clock buffers and prevent strong switching noise, the programmable dividers (in both the SC loop and the main loop) use asynchronous circuits. These dividers use standard static DFFs implemented in NOR gates with minimum transistor sizes to reduce both peak and average currents. Before reaching the PFD, the programmable divider output feeds through a DFF which is clocked by the divide-by-2 output to reduce the jitter accumulated during asynchronous operation.

D. PFD, CP, and Loop Filter

The PFD employed in this work is a typical dual-DFF structure. It is based on an asynchronous race-free design and is adopted from [8]. The idea is to minimize the simultaneous activation of "up" and "down" signals to reduce the perturbation on the loop filter. The charge pump, shown in Fig. 9(a), uses current mirrors with switches to control the charging and discharging currents. The switches include dummy devices to cancel the charge injection [8] and to provide equal loading for both phases of up and down signals.

The SC loop incorporates an on-chip second-order passive RC filter. Since frequency accuracy and spur and noise performance are not a main concern during the SC loop operation, a stable second-order loop filter is adequate [Fig. 9(b)]. The SC-loop bandwidth is set to around 120 kHz. With an interval of 512 μs during each clock phase ($\phi 1$ and $\phi 2$), the SC loop has sufficient time to settle for the following comparators to sample the final values.

The filter in the main synthesizer loop is a third-order off-chip passive RC filter [Fig. 9(c)]. It is designed to balance the requirements of spur suppression and switching time. The main-loop bandwidth is set to 2 kHz. With the narrow-loop bandwidth, this leaves the VCO to determine the output phase noise around the FSK tone frequency ($\gg$ 2 kHz). Another source that may contribute to the output phase noise is the thermal noise associated with the resistors in the loop filter [9]. However, thanks again to the low $K_{\rm VCO}$ design, this noise contribution is much smaller than the VCO's intrinsic phase noise and is not important.

V. Measurement Results

This PLL frequency synthesizer has been fabricated in a 0.6-μm CMOS technology. Fig. 10 shows the die photo. The active area is estimated to be around 1 mm by 0.7 mm. The circuit is tested from a 3-V supply voltage at room temperature. Including an on-chip VCO, this synthesizer dissipates 2.5 mA, and it drains only 2.2 mA when the SC loop is powered down after reaching the "ok' state. The VCO core consumes roughly 1.2 mA, higher than designed. This higher current is attributed to the SC networks where the actual loss associated with the switches is greater than simulated, thus degrading the quality factor of the VCO tank circuit. An experiment was done by sweeping the SC state manually and observing the oscillator start-up condition. The required minimum current to initiate the VCO oscillation is increasing as the SC state sweeping from

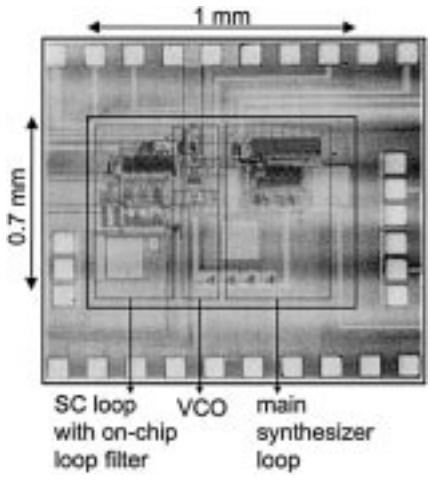

Fig. 10. Chip photo.

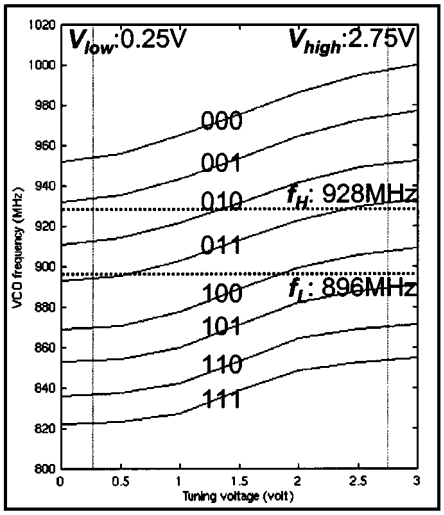

Fig. 11. Measured VCO tuning characteristics.

000 to 111, indicating that the switch on-resistance of the SC networks degrade the Q.

The measured VCO tuning characteristics are shown in Fig. 11. The overall frequency tuning range is around 20% (821 MHz $\sim$ 1 GHz), and the VCO gain is low at only 20 MHz/V. For testing purposes, a 36-pin QFP leaded chip carrier is used. The extra parasitics from the package reduce the tuning range at the low frequency end and the amount of frequency overlap between adjacent VCO curves is also limited. However, as mentioned previously [1], the complete WINS transceiver will be embedded in an LTCC substrate, thus removing the need for such packages. Each individual tuning curve is expected to cover at least 6.5% with sufficient frequency overlap after removing the package. Of course, the VCO gain will also increase slightly. This estimated VCO gain is still considerably smaller than that of the conventional single-curve tuning topology.

Fig. 12 demonstrates the synthesizer operation. When the "enable" signal goes high, the SC loop begins searching for the proper VCO frequency curve. (This corresponds to the SC state of 011 in this measurement.) Once reached, the "ok" (SC-OK) signal goes high and the main loop takes over to tune the VCO to the predefined channel. Fig. 12(a) and (b) shows the cases where the SC state (counter output) starts at 000/111. In both cases, they successfully reach 011 and lock to the predefined channel

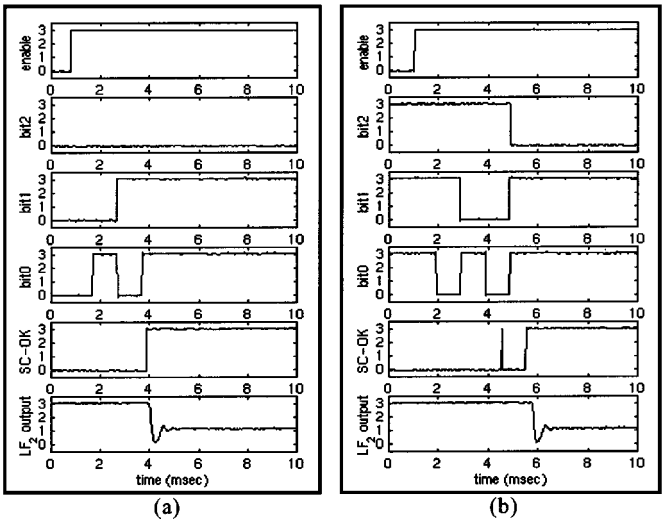

Fig. 12. Frequency synthesizer operation with the SC state starting at (a) 000 and (b) 111.

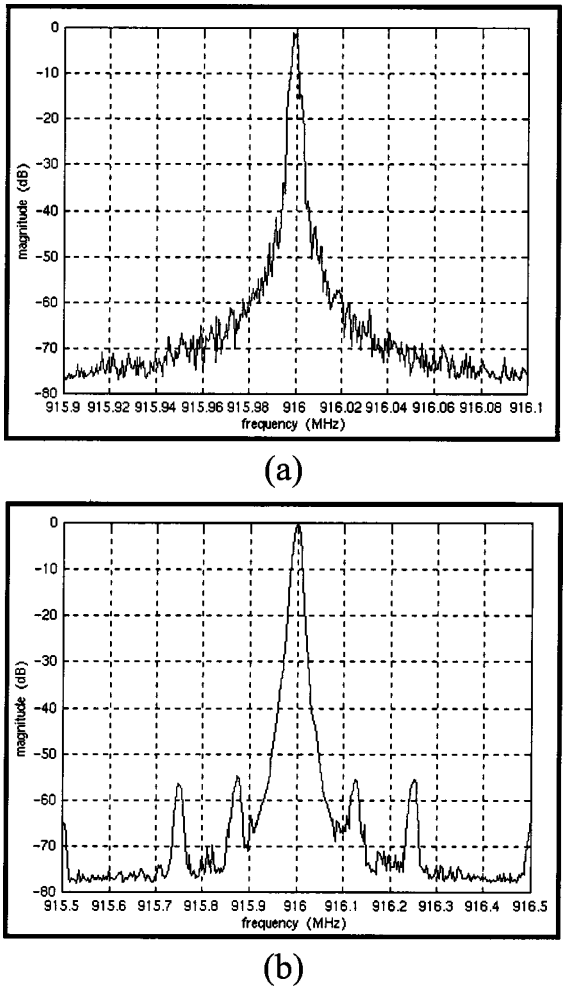

Fig. 13. Measured frequency synthesizer output spectrum at 916 MHz: (a) 200-kHz span (RBW: 1 kHz); (b) 1-MHz span.

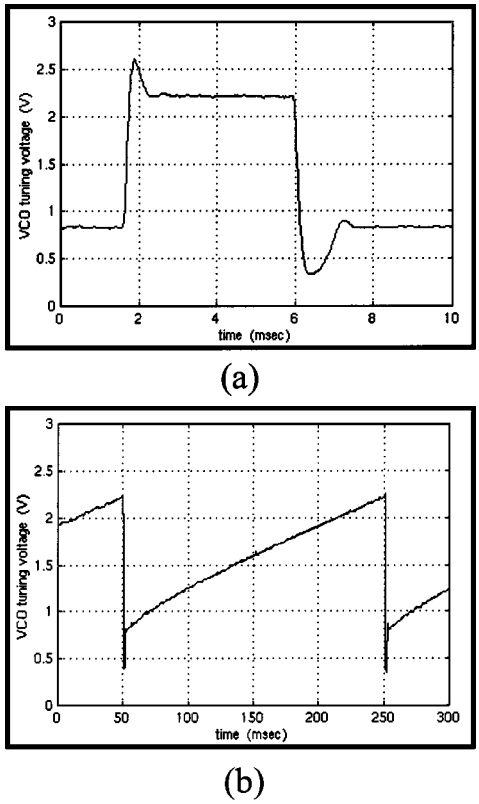

Fig. 14. Channel switching behaviors. (a) Channel switches from end to end. (b) Channel frequency hops across the entire ISM band.

TABLE II
PLL PERFORMANCE SUMMARY

Supply voltage	3 V
Current consumption	2.5 mA
Frequency tuning range	821 MHz ~ 1 GHz (~ 20%)
K_{VCO}	20 MHz/V
Switching time	< 2 msec
Operating frequency	ISM band (902 - 928 MHz)
Reference spurs	< -55 dBc
Phase noise @ 100 kHz	-102 dBc/Hz

frequency afterwards. Note that, in Fig. 12, "LF_2 output" represents the main loop filter output (node B) of Fig. 3.

The spectrum of the synthesized output at 916 MHz is shown in Fig. 13. The phase noise extracted from the spectrum analyzer is -102 dBc/Hz at 100-kHz offset frequency and the spurs are lower than -55 dBc. The synthesizer switching behaviors are illustrated in Fig. 14. Fig. 14(a) shows the transient of the VCO tuning voltage waveform with channel jumping between the lowest and highest frequencies. The switching time is less than 2 ms. Fig. 14(b) demonstrates the frequency hopping capability. All designated channels within the ISM band are synthesized, and hopping from channel 1 (902.25 MHz) to channel 103 (927.75 MHz) occurs in sequence, and then repeats. Finally, Table II shows the performance summary of this low-power PLL frequency synthesizer.

VI. CONCLUSION

A 900-MHz, low-power PLL frequency synthesizer is developed for the WINS transceiver in a standard CMOS technology. This PLL exhibits high performance by efforts in every design level, from system specifications, PLL architecture and circuit designs to choices of passive components (on-chip or off-chip) and layout techniques.

In the system design stage, careful frequency planning and reasonable system requirements enable the low-power integer-N architecture. In the PLL architecture design stage, by incorporating both discrete- and continuous-tuning loops, low-noise and low-spur performance is attained without the penalty of excess power dissipation or sacrificing the overall frequency tuning range. In the circuit implementation stage, building appropriate circuits, especially VCO, high-speed dividers, PFD, and CP, is essential in achieving high performance. The employment of off-chip high-Q inductors in VCO is advantageous in low-power and low phase noise design. Here, VCO phase noise is important since the PLL loop bandwidth is small and it is the oscillator that dominants the output phase noise spectrum. Others, such as the ring-shaped layout technique, also prove important in minimizing parasitics and improving the overall performance.

With the advance of CMOS technology, this 0.6-μm PLL is expected to achieve better performance with less power when migrating to 0.35- or even 0.18-μm technologies. This PLL is intended to be integrated into the WINS transceiver and embedded in the LTCC substrate in a compact form. This frequency synthesizer paves the way to a true micro-power, frequency-hopped WINS CMOS radio.

ACKNOWLEDGMENT

The authors would like to acknowledge valuable discussions with Prof. B. Razavi, Dr. T. Y.-C. Tseng, and Dr. D. C.-K. Wei.

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Tsung-Hsien Lin received the B.S. degree in electronic engineering from the National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. in 1991 and the M.S. and Ph.D. degrees from the University of California, Los Angeles, in 1997 and 2001, respectively.

He is currently with Broadcom Corporation, in El Segundo, CA. His research interests include analog and RF IC design for wireless applications.

William J. Kaiser (M'95–A'96–SM'96) received the Ph.D. degree in solid-state physics from Wayne State University, Detroit, MI, in 1984.

During his graduate program, he was a member of the Research Staff of Ford Motor Company where his research included the development of automotive sensor technology from measurement methods, through circuits, structures, materials, and deposition methods, resulting in large volume commercial sensor production. In 1986, he joined the staff of the Jet Propulsion Laboratory (JPL) where he initiated the NASA microinstrument program. His research is concentrated on the development of distributed, networked, embedded systems. Specific current focus is on Wireless Integrated Network Sensors (WINS). His research focuses on low-power analog and digital electronics, distributed sensor networks, and information technology for distributed embedded systems. In 1994, he joined the faculty of the Electrical Engineering Department of the University of California at Los Angeles, where he served as Chair from 1996 through 1999. He has authored over 100 publications and 100 invited presentations and holds 21 patents. He cofounded the new company, Sensoria Corporation, with Prof. Greg Pottie, that is commercializing the first complete, Internetworked WINS platform.

Prof. Kaiser has received the Allied Signal Faculty Research Award, the Peter Mark Award of the American Vacuum Society, the NASA Medal for Exceptional Scientific Achievement, the Arch Colwell Best Paper Award of the Society of Automotive Engineers, and two R&D 100 Awards.