Photonic Crystal Waveguide Based Y-Junction Splitter Through Finite Difference Time Domain (FDTD) Simulation Method

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Abstract: In the present analysis we have investigated the photonic crystal waveguide (PCW) based Y-junction splitter through three dimensional finite difference time domain simulation methods to overcome some of the difficulties like mode mismatch, bandwidth and bending region transmission and challenges. The structure can be applied to communication systems and also be integrated with other photonic crystal (PC) based devices.

Keywords: Photonic crystal, waveguide, Y-junction, finite difference time domain, simulation, bandwidth, transmission, communication.

1 Introduction

Since the implementation of photonic crystal there have been increasing attention paid to develop the nanostructure in micro scale device in various applications (John, 1987; Yablonovitch, 1987). PCs have the potential to provide ultra compact photonic component that will enable the miniaturization of optical circuits and promise to revolutionize integrated optics. These photonic components are based on the planar photonic crystal (PC) structure and operate in the photonic band gap (PBG) of the periodic dielectric structures which allow control of the light propagation on the wavelength scale. Photonic crystal waveguides (PCWs) are formed by line defects in PC. Thereby light is confined horizontally by an in-plane PBG and vertically by TIR. Because of the PBG effect in a PCW, light can be routed around sharp corners with bending radii of the order of the wavelength. Due to the sharp bend higher-order modes are generated that affect the single mode operation in the PCW (Chutinan and Noda, 2000). Researchers have theoretically investigated photonic crystal with array of dielectric rods in air. Based on this concept the T-junction, Y-junction and MMI effects have already been extensively studied (Fan and Johnson, 2001; Yu et al., 2008; Yang et al., 2010). Unfortunately, the 'rod in air' approach does not provide sufficient vertical confinement and is difficult to implement for most practically useful device implementations in the 55 optical regime. A slab waveguide structure consists of air holes etched into a dielectric medium such as silicon (Soltani et al., 2003), GaAs/AlGaAs hetrostructure (Krauss et al., 1996) or a semiconductor membrane (Loncar et al., 2000; Chowm et al., 2000; Notomi et al., 2001) which remedies this problem and allows waveguides with tolerable losses. The problem encountered for the 'holes in dielectric' approach is that the single-defect PCW becomes multi-moded, which makes it difficult to get light to flow efficiently around the circuit because higherorder modes are easily excited at discontinuities (Notomi et al., 2001; Joannopoulos, 2001; Zhen et al., 2005). This multimode leads to mode-mixing problem at intersection of the PCW which creates a mismatch between input and output fields and introduces large reflections at the interface. Whereas straight waveguides and bends have been studied by many groups, the very important problem of junctions based complex circuits operation has only recently received attention (Wilson et al., 2003; Frandsenet al., 2004; Borel et al., 2005; Dekkiche and Naoum, 2006). The most straightforward Y-splitter design consists of three single-defect ('W1') waveguides joined together at 120^0 which leads to strong reflections and narrow- bandwidth operation. Due to strong reflection only 20% of the input power is transmitted at the output ports (Koshiba et al., 2000). After that Frandsen et al. in 2004 proposed an alternate design which was based on a triple line defect waveguide. In their design the bandwidth and power transmission were improved by 25nm and 45% of input power by adding an additional hole at 120^0 junction and modified 60^0 bend. FDTD is a time domain simulation method for solving Maxwell's equations in arbitrary materials and geometrics. The basic principle is to substitute the curl equations and partial time differential with finite central differences in spatial domain and time domain respectively (Taflove and Hagness, 2000). The computational domain is meshed as shown in fig. 1 where different field components are located at different computational nodes. This typical configuration is referred to Yee's cell.

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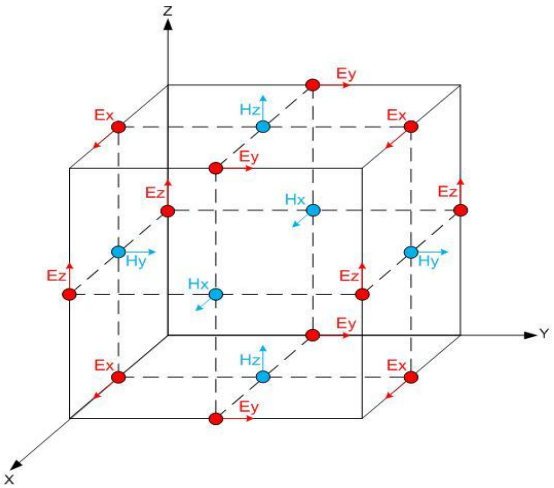

Fig.1 Yee's cell

$$\nabla.\vec{H}(\vec{r}) = 0 \qquad (1)$$

$$\nabla.\left[\varepsilon(\vec{r})\vec{E}(\vec{r})\right] = 0 \qquad (2)$$

$$\nabla \times \vec{H}(\vec{r}) = -j\,\omega\,\varepsilon(\vec{r})\,\varepsilon\vec{0}\,\vec{E}(\vec{r}) \qquad (3)$$

$$\nabla \times \vec{E}(\vec{r}) = j\omega\,\mu\,\vec{0}\,\vec{H}(\vec{r}) \qquad (4)$$

By substituting partial differentials in Maxwell's equations (1)-(4) with central finite difference, the electromagnetic field at each time step is calculated by iteration of algebraic equation. FDTD simulation can provide complete information on the propagation of electromagnetic waves in dielectric structures with any arbitrary geometry. In order to obtain convergent simulation results and to reduce the numerical dispersion, a fine mesh is critical. In our study, the grid size *d* is chosen such that *d<λ/20n*, where λ is the minimum wavelength of the source spectrum and *n* is the refractive index of the slab. This mesh configuration ensures the convergence and high accuracy of the simulations. The stability factor *S* is defined as $S = c\,\Delta t$, where *c* is the speed of light in *d* vacuum and *_t* is the time step. In Y-junction base splitter simulation file *S* is set to 0.99 for satisfying the stability condition of 3-D FDTD simulations.

2 Simulation boundaries in 3-D FDTD

Since any computational resource can only deal with finite size of the matrix, the simulation region has to be terminated boundaries, which must have very low reflection otherwise the waves will be reflected back from the boundaries into the simulation region to affect the results. In Y-junction based structure analysis, perfect matched layer (PML) is used in the 3-D FDTD simulations. Instead of PML boundary other two types of boundaries are also frequently used in 3- D FDTD. These are symmetric/anti-symmetric boundaries and Bloch boundaries.

3 Description of Y-Junction Structure

The planar PC Y-junction based structure is defined by an array of air holes in a 300nm thick dielectric substrate with refractive index of 3.47 (silicon). The regular holes are placed in a triangular lattice and have a radius r =0.25a, where lattice constant a = 400nm. The PC Y-junction base structure is formed by the intersection of three PCWs at 1200 as shown in fig. 2.

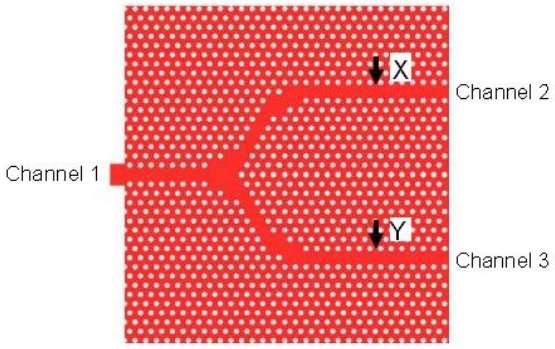

Fig. 2 Preliminary Y branch structure

The output channels of Y splitter are parallel to the input channel and have a 60^0 bend and seven periods spaced from the Y junction. The 120^0 junction and 60^0 bend represent severe discontinuities in the PCWs and are potential regions in which the single mode operation might suffer from large transmission losses. Therefore the discontinuities in these regions are carefully designed.

4 Characterization of Y-Junction in 3-D FDTD

From 3-D FDTD simulation time domain electromagnetic field is obtained. The Y- junction structure is simulated by a mode source located on the conventional waveguide which is attached with the Y-junction structure. This technique is very powerful and versatile and is useful for this type of waveguide (Mekis et al., 1996; Koshiba et al., 2000).

5 Simulation setup

The 3-D FDTD simulation for the designed of Y-junction in slab is shown in fig. 3. The design of Y-junction in silicon slab is created in the simulation region. In order to excite the mode, PML boundary is used. This boundary absorbs the outgoing wave. A 3- D profile monitor is located on the Y-junction structure to record the electric field distribution at 120^0 junction, 60^0 bend and output channels. Two power monitors are placed at the output channel in order to record the power transmission from input to output. The output power is calculated at each port by integrating the Poynting vector over the cells of the output ports. The spectrum of the power transmission is calculated by using FDTD method over a time period of 800fs. The FDTD mesh size and time step are 0.0142μm×0.0142μm×0.0349μm and $\Delta t = \Delta x * S/c$ (c is speed of light in free space, Δx is distance between two mesh point, S is stability factor and Δt is time interval of the time step) respectively.

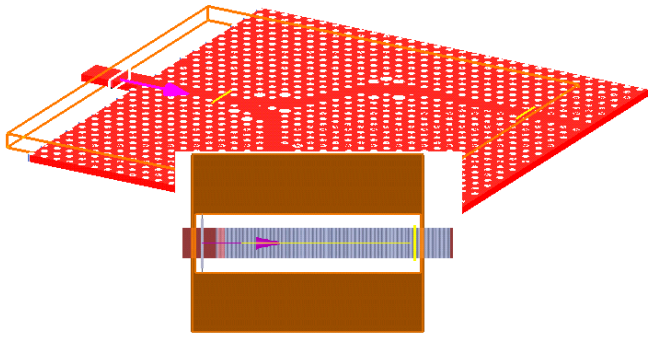

Fig. 2 Three dimensional FDTD simulation setup for designes Y-junction Power transmission of unmodified structure

Fig. 2 shows the basic structure of Y junction base splitter. First we have investigated the transmission of this structure using 3D FDTD method with perfectly matched layer (PML) boundary condition. The output transmitted power is monitored at two points on the 600 bend output waveguides; one at the output of channel 1and the other at the output of channel 2 as indicated in fig. 2. The optical pulses are injected on the waveguide and each pulse covers the same range of wavelength which is 1.5μm-1.588μm. The numerical transmission spectrum of unission unmodified Y-junction structured is shown in fig. 4.

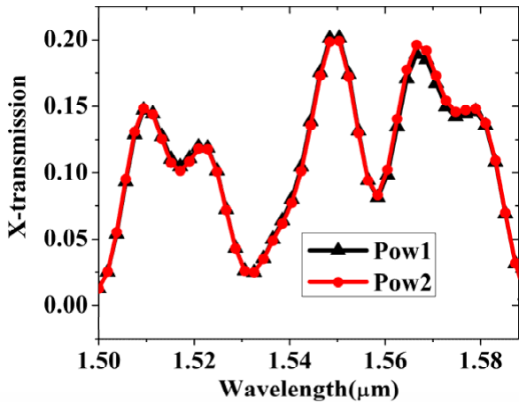

Figure 4 3-D FDTD calculation of normalized output power transmission of an unmodified Y-junction structure

The spectrum indicates that a maximum of 20% of the input power is transmitted through each channel that is quite low. The discontinuities at the Y- junction and the subsequent 60^0 bend are said to be responsible for this lowsible transmission.

6 Modification of the design

In order to maintain the single mode operation and acieve the better transmission we modified the Y-branch structure. The 60^0 bends are modified by displacing one hole and removing two holes in the bend. Moreover, four border holes (denoted by 'A', 'F', 'G'; as shown in Figure 3.5) and one top corner holes (denoted by 'D') are placed with larger holes with radius 'A'= 160nm, 'F'= 180 nm, 'G'=150 nm and 'D'= 170 nm respectively. However, one border hole (denoted by 'E') in the 60^0 bending region and displaced hole also in the 60^0 bending region (denoted by 'C') are replaced with smaller holes with radius 50nm and 80nm respectively. The Y junction is altered in a similar way by removing three holes on both sides of the junction and replacing five border holes with larger holes. However, this could transform the Y junction into a multimode optical cavity which could decrease the performance of the splitter because the cavity modes might not be supported by the PCWs. Therefore two additional holes are added in the splitting region, whereby the size of the junction cavity is reduced.

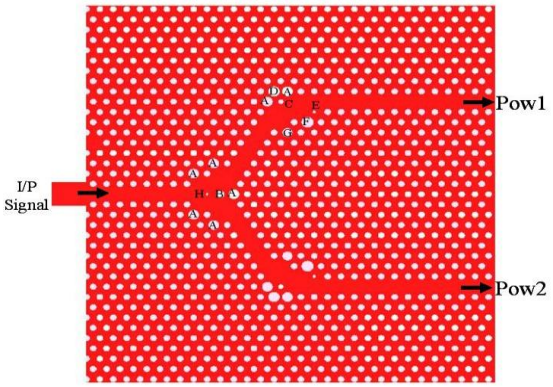

Fig. 5 Modified Y branch structure

In the splitting region i.e. at 120^0 junction the smaller hole followed by a line of holes gradually increasing in size which minimizes the mode mismatch problem between the 120^0 junction and 60^0 bending waveguide. The radius of the initial hole is designed to be 40nm and the second to be 120 nm. The design of the modified Y-junction based power splitter is shown in fig. 5.

7 Analysis of modified Y-junction

To improve the power transmission at the output channels we have modified the Y-junction and adjacent 60^0 bend. While doing so we have changed the radius of the holes at Y-junction (denoted by 'A') and 600 bend (denoted by 'A', 'C', 'D', 'E', 'F' and 'G') which is depicted at fig. 5. Fig. 6 displays the improved power transmission of modified Y-junction based power splitter based on these modifications. Due to this modification the single mode operation is not disrupted. Therefore more power is transmitted from input to output channels. The performance of the transmitted power is improved by 18% at each output channel which means 38% power is transmitted at both of the output channels. The improved transmission which has been received by optimizing of Y junction based power splitter structure is still lower than the existing Y-junction based design (Wilson et al., 2003). As a result, a better improvement is inevitable. So we have introduced additional two holes at the 120^0 junction denoted by 'H' and 'B'. Due to this modification the performance of transmitted output power of Y-junction splitter is improved.

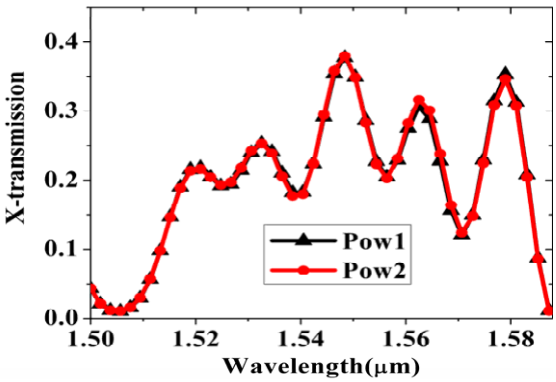

Fig. 6 Normalized transmission of output power spectrum of modified Y-junction based power splitter

Fig. 7 shows the improved version of transmitted output power of the second set of modification of the Y- junction based power splitter. In this modified version of the structure the higher transmitted power is achieved which is 84.4% with each channel equally transmits 42.2% of input power. Whereas more than 22% power is achieved at each output channel in the frequency range of 1540nm-1567nm (with bandwidth about 27nm) and 20% power is achieved at each output channel in the frequency range of 1526nm-1568nm (with bandwidth about 42nm), indicated by blue dash line with highest pick value of 42.2% power for channel 1 and 2. This maximized transmitted power is well comparable with the existing results (Wilson et al., 2003; Frandsen et al., 2004).The unmodified structure of the Y-junction which is shown in fig. 2, transmits only 20% of input power to each channel. This is due to mode mismatch of input PCW and 60^0 bend output PCWs. To overcome this large transmission loss holes are resized at the splitting region i.e. the 120^0 junction and the 60^0 bending regions. As a subsequent result of resizing the holes size, the bending loss gets minimized and it has an impact on the transmitted output power. For further improvement two additional holes are placed at the junction. The effect of introducing additional holes at the junction is the decrease in volume of the intersection which prevents the expansion of the higher-order mode. Boscolo et al. (2002) showed that poor transmission can originate from modal mismatch at the junction.

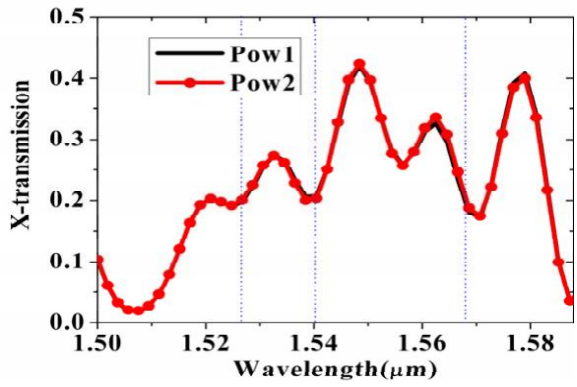

Fig. 7 Normalized maximum transmitted output power of Y-junction based power splitter

If the incoming mode has space to expand in the junction area, it excites the higher order modes which are either lossy or cannot able to propagate through 60^0 bend output waveguides. So, most of the incoming light is reflected and the transmission is poor.

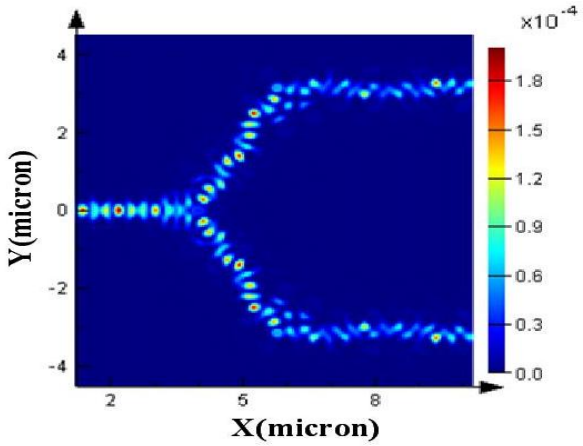

Fig. 8 FDTD simulation of the electric field distribution in the optimized Y-junction base power splitter when the incident wave arrives at the level of the additional holes

By placing the two additional holes at the junction, the incident wave is divided into two parts and propagated through the each output channels. Here, the dimension of the additional holes play an important role which distributes the single mode incident wave in two single mode waves crossing the two output channels as illustrated in fig. 8. According to modification, the Y-junction based power splitter transmits 84.4% of input power on both output channels. Due to the higher transmission of power at each channel, the 1×2 splitting topology is divided into 1×4.

8 Design of 1×4 power splitter based on Y junction

Based on the FDTD analyzed result of unmodified and modified Y-junction in previous section we want to investigate 1×4 power splitter which is based on Y-junction. The schematic diagram of 1×4 power splitter is shown in fig. 9. Basically the whole structure is divided into two stages. First stage consists of one Y- junction and second stage consists of two Y-junctions. The two stages cascade each other. The configurations of holes size of 2nd and 3rd Y-junction are same as 1st Y- junction. The entire structure is surrounded by twelve PML layers to absorb the outgoing waves. A continuous optical pulse is injected into the first Y-junction PCW (fig. 9) and then after propagation of the certain distance this pulses are divided into two channel and coupled into the next stage i.e. stage 2.

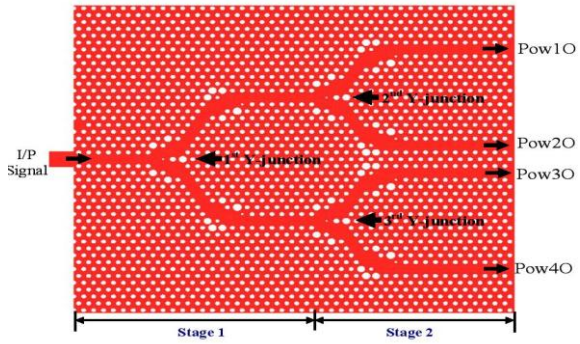

Fig. 9 Architecture of 1 to 4 power splitter using Y-junction

In the second stage the signal is divided into four channels which are shown in fig. 9. The whole structure is partially optimized and 58.3% of input power is achieved at four channels as shown in fig. 10. The output transmitted power is quite low and is not equally distributed. In order to maintain single mode operation at each channel the design should be further modified to transmit equal and maximum power at each output channel. Modification of smaller Y-junction which in turn increase spacing between channel 2 and 3 at the output, which may improve the equal power distribution and also maximize the power at each output channel.

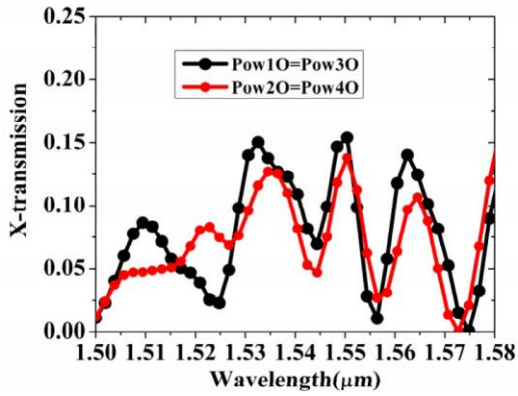

Fig. 10 Normalized transmitted output power of Y-junction based 1×4 power splitter

The high power transmission and broad bandwidth of Y-junction based 1×2 power splitter is achieved through 3-D FDTD simulation analysis. This simulation is well comparable with the published result (Wilson et al., 2003; Frandsen et al., 2004). So, we have decided to fabricate the Y-junction 1×2 structure in silicon on insulator (SOI) platform. In order to do that 250nm SOI substrate is available so we have configured our structure on the basis of 250nm slab thickness.

9 Improve transmission by changing slab thickness

In order to fabricate Y-junction structure for 1×2 power splitter application, the entire structure is simulated with 250nm slab height. The simulation parameter and hole size are similar as before but slab height is changed only. The whole structure is investigated with 3-D FDTD simulation method. Fig. 11 shows the each channel transmits 43.9% of input power which is higher than the 300nm slab height of Y-junction structure. As a result overall power transmission is also improved. The power transmission of the new Y-junction based power splitter is 87.5%. At each output channel more than 30% power is achieved in the frequency range of 1546nm-1577nm (with bandwidth about 31nm) and 34% power is achieved at each output channel in the frequency range of 1547nm-1576nm (with bandwidth about 29nm), indicated by blue dash line (fig. 11) with highest pick value of 43.9% power for channel1 and 2. This maximized transmitted power is well comparable with the published results (Wilson et al., 2003; Frandsen et al., 2004). The output transmitted power is maximized due to less amount of vertical loss. In 2-D slab PC the vertical loss is depend on the slab thickness. If the slab thickness is more than the vertical loss will be more and vice versa.

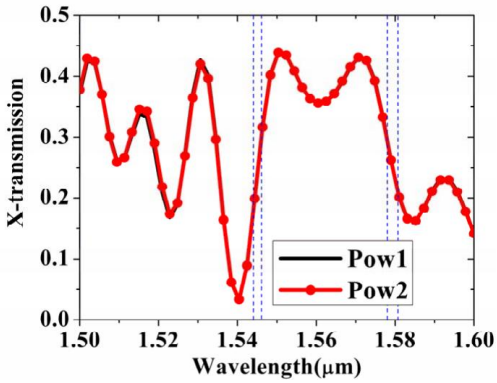

Fig. 11 Normalized transmission of output power spectrum of modified Y-junction with 250nm slab thickness

In order to achieve a high transmission at 1×2 Y-junction structure, we have also partially investigated 1×4 splitter based on Y-junction structure. In this investigation the power transmission is improved by only 1.6% which is not a considerable increment. The output transmission of 1×4 power splitter is shown in fig. 12.

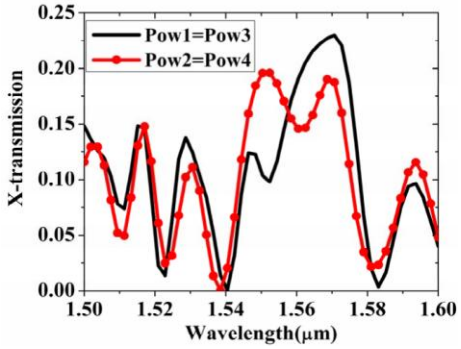

Fig. 12 Transmitted output power of Y-junction base 1×4 power splitter with 250nm slab thickness

This power transmission is not high enough and also it is not equally distributed into each channel which is shown in fig. 12. 10.3% of the input power is transmitted through

channel 1 and channel 3 and the 19.5% of input power is transmitted through channel 1 and channel 4. From the simulated result it is quite clear that Y-junction is better for 1×2 splitting technique not for 1×4. Based on 1×2 Y-junction power splitter simulation result, we have fabricated this structure on 250nm thick SOI platform. In the next section we will discuss the fabrication step of 1×2 Y-junction base power splitter.

10 Fabrication of 2-D Slab 1×2 Y-Junction Base Power Splitter

This section deals with nanofabrication steps of 1×2 Y-junction base power splitter. Electron beam lithography (EBL) is used to transfer the pattern and etched on the top silicon layer. Bosch process is used to develop the pattern. Proper steps have been developed to make a Y-junction base 1×2 power splitter. The parameter of the fabricated device are lattice constant (a) of 400nm and radius of dielectric hole with 100nm. The device is fabricated on 4" SOI wafer purchased from SOITEC. The wafer consists of 500μm thick silicon handle with a layer of buried oxide followed by a device layer of crystalline silicon. The thickness of the buried oxide is 1μm and thickness of device layer is 0.25μm. The 1μm silicon oxide is selected to prevent the substrate from affecting the transmission characteristics of the PC waveguide. PC Y- junction structure with air above and 1 micron oxide below is fabricated on SOI wafer. For good coupling, the PC Y-unction structure is connected with a 0.8μm dielectric waveguide. The recipe developed for conventional waveguide and alignment mark is presented in Appendix A and Appendix B. The process flow of PC Y-junction structure is shown in fig. 13. For electron-beam (e-beam) lithography, the sample is coated with Zep photoresist which is an electron-beam sensitive resist. The resist has to be thin to allow for the fine features of the photonic crystal. The detail process is in Appendix C. It is worth mentioning that when an electron beam is incident on a material, the electrons are not destroyed but are scattered both elastically (with an angle changes but without energy loss) and inelastically (with energy loss). Back-scattered electrons often cause features written by e-beam lithography to be wider in densely patterned areas. Due this proximity effect, the hole size on the PC is not exactly the same as what is written on the sample. For good accuracy, a dose test helps to determine the proper hole diameter written and beam current so that the developed hole radius equals the expected value. To pattern the PC Y-junction base splitter, e-beam lithography is employed. After exposure of e-beam, the sample is subject to develope in Zep developer then the pattern is ready to be etched into the silicon. Dry etching method selectively removes away the exposed part which is not protected by photoresist. There are two leading technique of dry etching for etching deep into silicon which are "Bosch" process and a cryogenically cooled process.

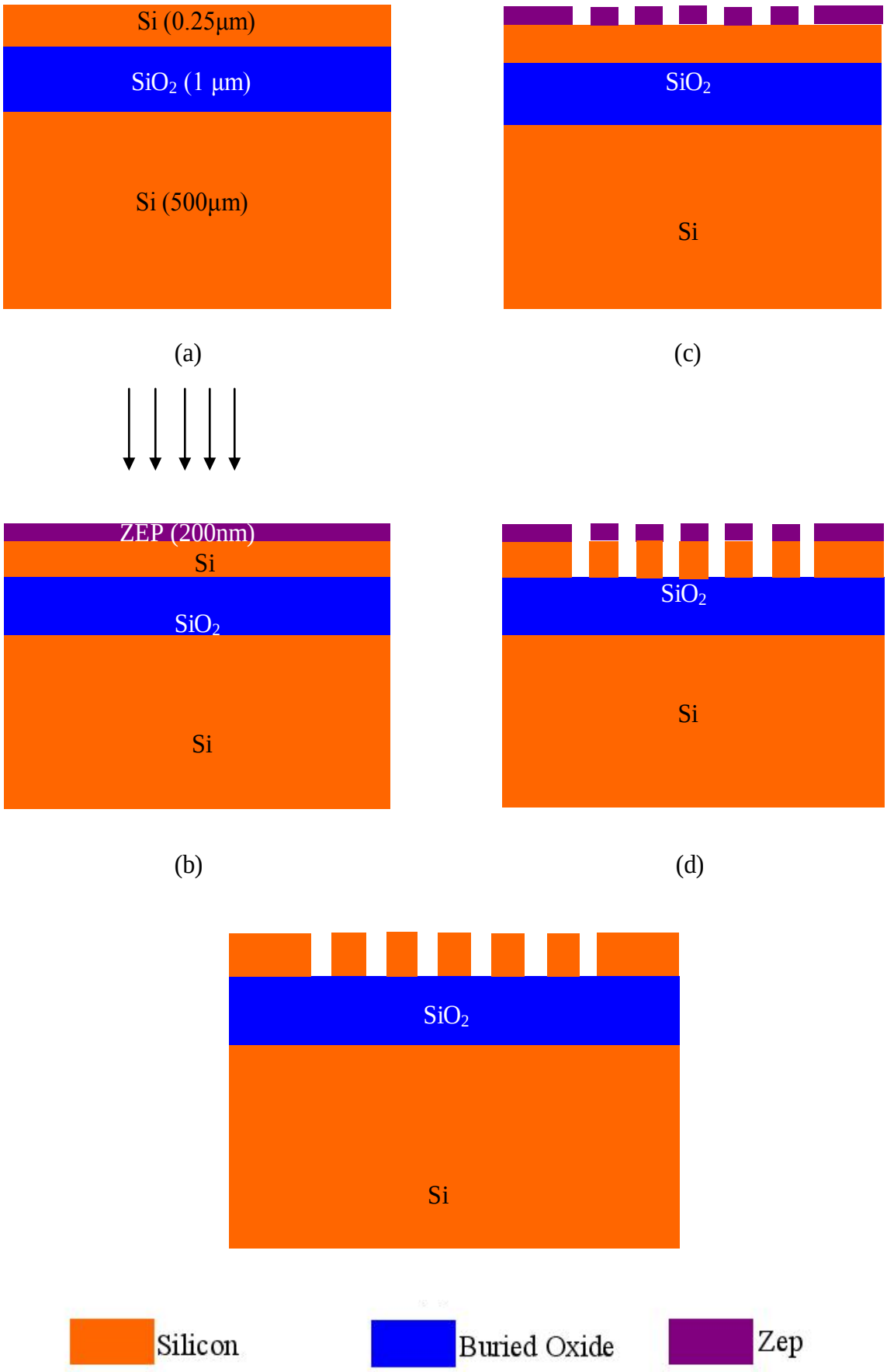

Fig. 13 Schematic diagram of a PC base 1×2 Y-junction power splitter fabrication on SOI platform

After the e-beam exposure, the silicon etch process is accomplished with an Inductive Coupled Plasma set up (Alcatel 601E). Anisotropic etching in SF_6 inductively coupled plasma has become standard for silicon etching. The PC base Y-junction design, written by using e-beam lithography, is transferred to 250nm thick device layer silicon by inductively coupled plasma (ICP) etched in the Alcatel operating at 2.45GHz.with He (Helium) gas flowing at the back of the substrate for temperature control. The substrate is RF (Radio Frequency) driven for independent ion energy control towards the sample.

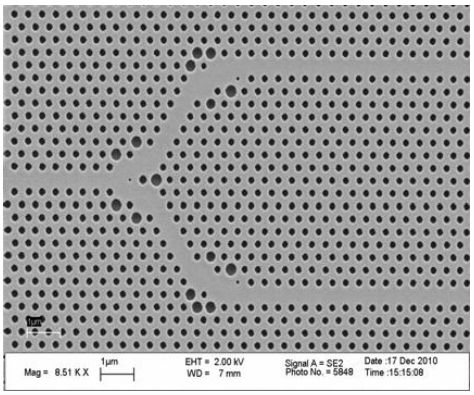

Fig. 14. SEM image of Y-junction structure

Bosch process is used to achieve vertical deep plasma etching. Thin fluro-carbon polymer film is used for side wall protection. After dry etch the Zep layer is stripped by using Deep UV (ultraviolet) exposure and sample is cleaned in PG remover. The cleaning process terminated by using Acetone followed by Iso-Propyl-Alcohol (IPA) and blow drying. The result of this process is a planar PC Y-junction base splitter made of a perforated silicon membrane lying on the buried oxide as shown in fig.14. The SEM (Scanning Electron Microscope) image of fabricated Y-junction is shown in fig. 14.

11 Conclusions

We have discussed here the photonic crystal waveguide (PCW) based Y-junction splitter through three dimensional finite difference time domain simulation method to overcome some of the difficulties like mode mismatch, bandwidth and bending region transmission and challenges. The structure can be applied to communication systems and also be integrated with other photonic crystal (PC) based devices. Y-junction is convenient for 1×2 power splitter application. It has less mode miss match and bending loss problems. It is also the most compact design. On the other hand, cascaded Y-junction based 1×4 power splitter is not suitable for equal power splitting, as it has problem of junction and bending loss. Tuning the entire device would be very challenging. Therefore we have chosen a different design technique which does not contain junction and bending waveguide.

12 References

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