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Study on Data Acquisition and Storage Based on FPGA in Carrier-based Photoelectric Warning System*

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ABSTRACT

In order to capture and storage video data real-time for carrier-based photoelectric warning system, an acquisition and storage system based on FPGA is designed. To complete the asynchronous interface timing of the camera and the storage system, the video data which come from infrared camera and visible light camera is stored to FIFO by FPGA, and then four SDRAM as cache and ping-pong operation cache-data storage to the CF card, this structure not only takes advantage of high-speed reading and writing skills of CF card, but also to ensure the integrity of the video data. In the final experiment proved that the system can be effectively applied to ships the photoelectric warning scanning system, its performance fully meet the needs of practical application.

Keywords: FPGA; Ping-Pong Operation; CF Card; Carrier-based Photoelectric Warning System

1. Introduction

When the ship is at sea, a variety of objects around within a certain distance including other vessels, offshore reefs can cause some potentially dangerous. Especially in some of dangerous waters, there are a lot of pirates, which is a larger threat to commercial vessels. Therefore, in order to be able to detect dangerous and warning need to install photoelectric tracking and monitoring system, to facilitate carry out maritime search, monitoring, law enforcement evidence, fault diagnosis, and could serve as military target positioning, tracking [1-3]. Because it is very important of data storage, especially incidents of data storage, an acquisition and storage system based on FPGA and CF card is designed, which takes advantage of the high-speed flexible configuration characteristics of the FPGA, as well as the unique advantages of the CF card.

CF card (compact flash card) is a large capacity, small size, high speed memory card which is easy to carry, it is first proposed by SanDisk Corporation in 1994, and compatible with PCMCIA-ATA, it is a kind of solid products, whose safety and reliability is much higher than traditional hard drives and other portable storage devices. Its storage speed is the biggest advantage; usually can reach 40MByte/s when read or write[4-6].

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2. Structure of System

2.1. The Structure of the Overall System

Carrier-based photoelectric warning system is mainly used for targets detection, tracking, monitoring and recording in the distance of the river and sea. The system uses an embedded system design, includes high-performance optical lens, CCD cameras, infrared cameras and infrared lenses. Computer automatic control technology, image processing and pattern recognition techniques (real-time video enhancement, abnormal target detection and identification automatic target acquisition and tracking), real-time electronic image stabilization technology and real-time early warning technology are also applied in the system. The system overall structure is shown in **Figure 1.**

In order to achieve real-time processing of video images, the system uses a linear pipelining array structure based on the DSP + FPGA.

The system requires two DSP for tracking process of long-wave infrared and visible light images respectively, and the FPGA is responsible for transferring the video to the DSP cache for processing, and while transfers the processed data to a CF card for data storage.

2.2. The Structure of Data Acquisition and Storage

In the system, FPGA not only to control the timing of capturing video, also needs to transfers the collected

video data to the DSP for processing, and save the emergency(such as suspicious-target or collision, accident, etc.) original video to the CF card by the DSP commands. Since the transmission of the video clock is 27 MHz, and SDRAM read and write clock is 100 MHz, and DSP to read and write clock is 150MHz, and CF card reader clock is 54 MHz, how to manage the FPGA asynchronous timing is the key to ensure system normal operation, Therefore, we have adopted the asynchronous FIFO structure [7], and the system structure shown in **Figure 2**.

3. Interface between CF Card and FPGA

There are three basic modes supported by CF card: PC Card Memory mode, PC Card I / O mode and True IDE mode. This system uses the PC Card Memory mode, and takes advantages of the feature of hot-swappable. The main communication interface between FPGA and CF Card as follows:

1) REG for ordinary operating CF card memory or the configuration memory, active low;

2) OE, WE are reader strobe pin of the CF card, active low;

3) CE1, CE2 pins are used to select the CF card work in 8-bit mode or 16-bit mode, active low;

4) CFADR0 ~ CFADR10 are CF card address bus;

5) CFDAT0 ~ CFDAT15 are CF card data bus;

The hardware interface between FPGA and CF card is shown in **Figure 3**.

4. Design of System Software

4.1. System Workflow

The system works as follows:

1) First, two camera's video data is collected through the decoder chip and stored in the SDRAM by FPGA. There should be four SDRAM chips for ping-pong operation, of which two are used to do video capture and storage, the other two as output cache [8].

2) Assuming that the current video data is being written to the B SDRAM by FPGA, and an image data has been stored in the A SDRAM, then FPGA should simultaneously transmitted data in the A SDRAM through the FIFO to the DSP for corresponding processing.

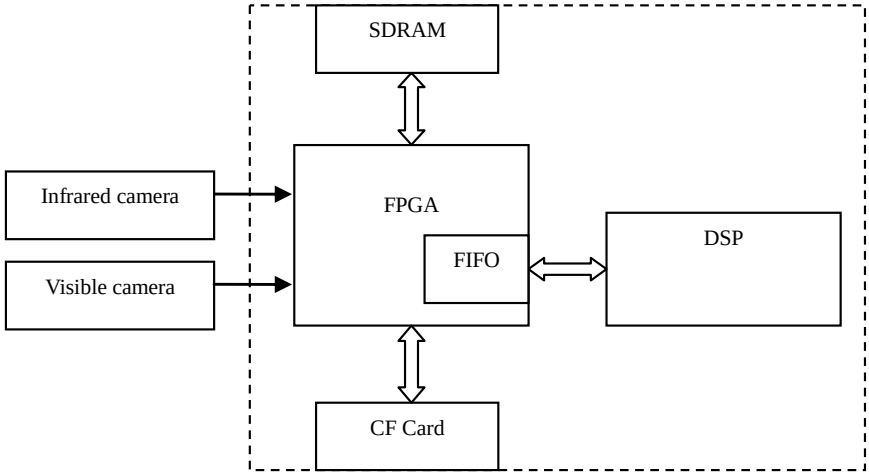

Figure 1. Embedded image processing system based on DSP + FPGA.

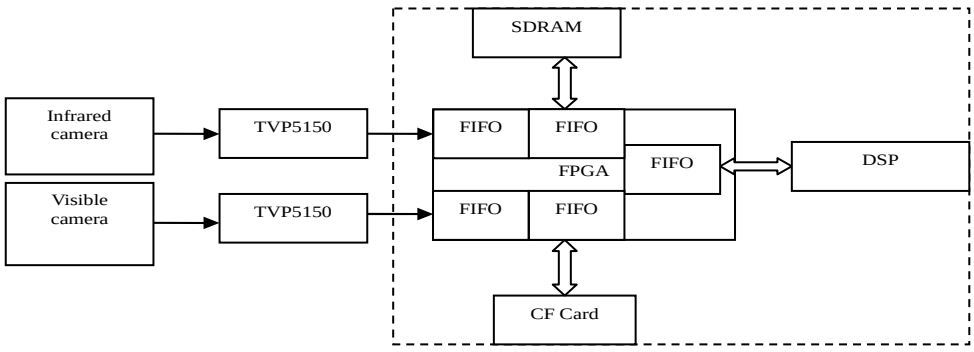

Figure 2. The structure diagram of video data acquisition and storage.

3) The data should be transferred to SDRAM by FPGA through the FIFO after being processed by DSP.

4) If the current data from DSP is stored to the D SDRAM cache, and the C SDRAM has a data stored, then the FPGA required data in the C SDRAM output via the encoder chip, and if DSP judges that the current video needs to be saved, then it will be saved to the CF card by FPGA.

The two cameras are all analog signals, so the infrared camera should be synchronized on the basis of the visible light camera. Two camera data will be captured and stored to an SDRAM at the same time, and since the video data needs to be cached before processing and outputting, there will be three frame delays of outputs.

4.2. The Design of Ping-pong Operation in FPGA

According to the above description, in this article, the most important ping-pong operation in the system is studied, shown in **Figure 4**.

In the ping-pong operation, SDRAM write module simply sustained write video data in the FIFO to the SDRAM bus while SDRAM read module turns the video data on the SDRAM bus to the input FIFO. Which SDRAM read or written is decided by SDRAM bus arbitration module. **Figure 5** is the module code.

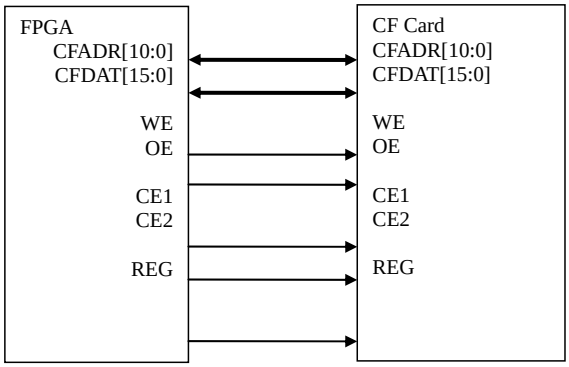

Figure 3. The hardware interface between FPGA and CF card.

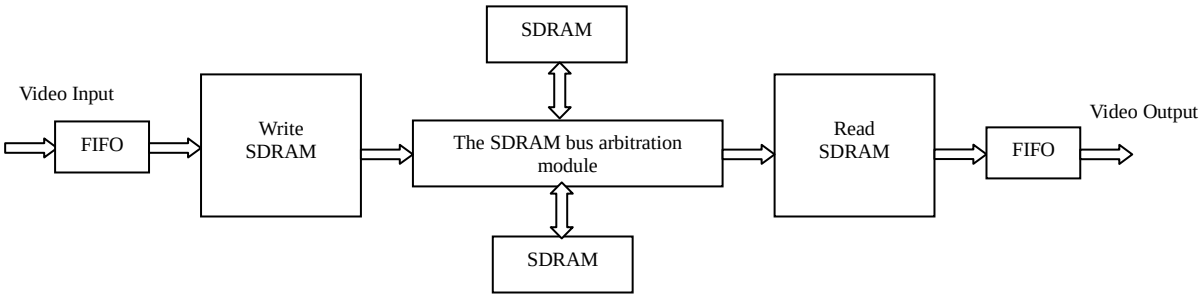

Figure 4. Pong operation procedures schematic.

```
//******************Bus Arbitration**********

// The assignment of output pin
assign D31_sdram_wr_req     =  write_d31_sdram_release ? sdram_wr_req : 1'b0;
assign D31_sdram_rd_req     = !write_d31_sdram_release ? sdram_rd_req  : 1'b0;
assign D31_sys_addr             =  write_d31_sdram_release ? write_sys_addr : read_sys_addr;
assign D31_sys_data_in      =  write_d31_sdram_release ? sys_data_in        : 16'd0;

assign D32_sdram_wr_req     =  write_d32_sdram_release ? sdram_wr_req : 1'b0;
assign D32_sdram_rd_req     = !write_d32_sdram_release ? sdram_rd_req  : 1'b0;
assign D32_sys_addr             =  write_d32_sdram_release ? write_sys_addr : read_sys_addr;
assign D32_sys_data_in      =  write_d32_sdram_release ? sys_data_in        : 16'd0;

assign sdram_rd_ack = write_d31_sdram_release ? D32_sdram_rd_ack : D31_sdram_rd_ack;
assign sys_data_out   = write_d31_sdram_release ? D32_sys_data_out : D31_sys_data_out;

assign sdram_wr_ack = write_d31_sdram_release ? D31_sdram_wr_ack : D32_sdram_wr_ack;
```

Figure 5. SDRAM bus arbitration procedure code.

5. Conclusions

In order to meet the need to capture and store video in real-time in the ship photoelectric warning system, a high-capacity acquisition and storage system is designed based on FPGA. Using the FPGA speed features and flexible configuration to capture the video data of the infrared camera and the visible camera, and using the FIFO method to guarantee asynchronous timing communication, also use of the advantages of SDRAM capacity fast cache to save video data to CF card in real-time by ping-pong operation. The tests at sea show that the system can effectively store the emergencies video integrity, and play a crucial role as the ship photoelectric warning system.

6. Acknowledgements

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