# DESIGN AND IMPLEMENTATION OF AREA AND POWER OPTIMISED NOVEL SCANFLOP

R.Jayagowri[1] and K.S.Gurumurthy[2]

[1]Research Scholar, Department of Electronics and Communication Engineering, Jawaharlal Nehru Technological University, Hyderabad, India
rjgowri@rediffmail.com
[2]Professor, Department of Electronics and Communication Engineering, University Visveswaraya College of Engineering, Bangalore, India
drksgurumurthy@gmail.com

**ABSTRACT**

*The power consumption of IC during test mode is higher than its normal mode. This brings the power as one of the major design constraints for today's low power design technologies. In normal scan based test circuits most of the power consumed due to the switching activity of scanflops during shift and capture cycles. In this paper a novel scanflop is presented which reduces the switching activity of the scanflop for clock and it reduces the power consumption of the circuit and it also reduces area and test time too. The proposed Dual Mode One Latch Double Edge Triggered (DMOL-DET) scanflop which shift the two bits of test vector in a clock cycle, during its test mode and captures the single data in a clock cycle during its data mode. The design and functionality of the proposed scanflop is discussed and compared with the different flipflops which shows that the proposed scan flop reduces the test time and clock switching activity by 50%, area by 30% and static power by 25%.*

**Keywords**

*Scanflop, Double edge triggered flipflop, test time, low power, Latch, Testing, Scan chain.*

## 1. INTRODUCTION

Testing of a chip is a mandatory to ensure its quality after manufacturing process. Scan based testing is one among the popular testing techniques. The scan chains are introduced into the VLSI circuit design to improve the testability of the circuit. After the logic synthesis of any design all the flipflops in the circuit are replaced by the Scanflops and are connected as a shift register to form the scanchain, through which the vectors are applied into the design for test [1]. The conceptual example of scan chain is shown in Figure 1. The logic diagram of scanflop used in scan chain is as shown in Figure 2. Usually the scanflop is the combination of multiplexer and a D-flipflop. Scan based testing happens with the help of scan flop in three different cycles. During the shift-in cycle of testing the scanflop allows the test vectors to enter into the design and during the capture cycle, the data from combo cloud is captured into flops. Finally during the shift-out cycle the captured vectors are shifted out of the design to compare the current output with the expected output to ensure the quality of the chip.

Every chip has to work in both in normal mode and in test mode. Zorian [2] showed that the power consumed by the chip in test mode is twice that of the normal mode. The test power [3] can be calculated using the equ (1 – 3).

The energy of the circuit during test is

$$E(V_{K-1}, V_K) = 1/2C_0V_{DD}^2 \sum_i S(i,k) F_i \quad \text{--- (1)}$$

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Peak dynamic power during test is

$$\text{Ppeak} = \max_K \left[ E \frac{(V_{(k-1)} - V_{(k)})}{T} \right] \quad \text{--- (2)}$$

The average power is

$$Pave = Etotal / T \times L \quad \text{--- (3)}$$

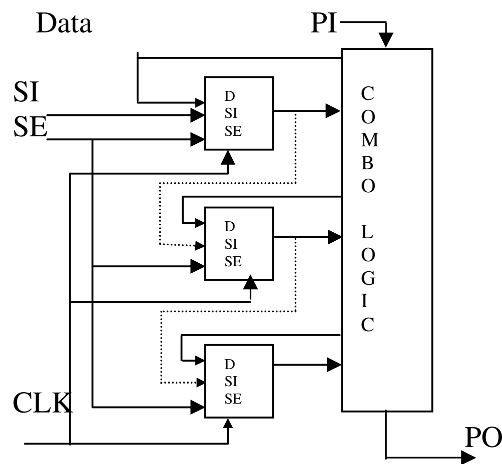


Figure 1. The model of the scan chain

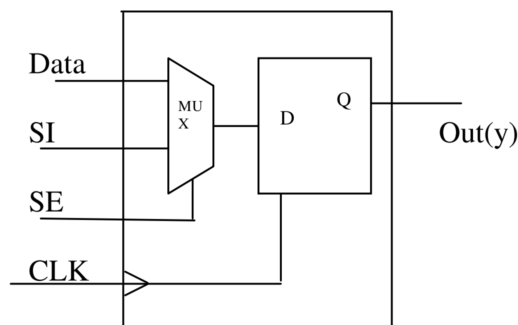


Figure 2. Block diagram of Scan flop

Where in equ (1) the K denotes K$^{th}$ vector, I denotes the i$^{th}$ node of the CUT and in equ (2 ,3) the term T denotes the time period. Where in equ (3) the L is the length of the test which is the number of test patterns applied. There are different test methods [4-5] and techniques proposed in the literature. Scan based test is the very popular technique of testing because of their simple

architecture, repeatability, direct controllability and direct observability [1]. The clock scheme modification is one of the power reduction approach for scan based testing. Pouya and Crouch [6] showed that the clock tree is the major contributor for the test power. Sankaralinkam, Pouya and Touba [7] proposed and proved the technique which uses the multiple scan chain for the full scan circuits. Bonhomme et.al present a technique [8] based on a gated clock scheme for the scan path and clock tree feeding for the scan path. Using such a modified clock scheme during scan operation reduces the clock rate on scan cells and clock transition density in the CUT [5]. In [9] it is explained that even double edge triggered flipflops are also meant for reducing the clock transition in the circuit and the total power consumption too.

In this paper a power reduction technique is presented using a novel double edge triggered flipflop with a clock scheme to reduce the test power. This paper is organized as Section-2 explains the proposed method, Section -3 shows the simulated results and it is compared with other scanflops in terms of its performance, area, static power and Section-4 concludes the work and future work.

## 2. PROPOSED METHOD

In this proposed method the scanflop which is introduced into the design after the logic synthesize is modified to reduce with the number of clock transition. Usually any flipflop is a combination of two latches. The first latch acts as a Master latch and second latch acts as a slave latch. For a positive edge triggered flipflop master latch is a negative latch and followed by a slave latch which is a positive latch to capture the data change in a flipflop during the positive edge of the clock pulse. Similarly the negative edge triggered flipflop has the positive latch as its master and negative latch as its slave to capture the data change only during the negative edge of the clock pulse. In the proposed method the D-flipflop has only one positive latch which itself made to use as a flipflop which can capture the change in data only during the edges of the clock pulse. This is achieved by generating a clock trigger signal from the system clock pulse. The generated clock trigger signal has very narrow ON time which exactly coincide with the edges of the system clock to capture the data either at the positive or negative edges of the system clock. The same flipflop is made to capture the data during both positive and negative edges of clock it works like a double edge triggered flipflop.

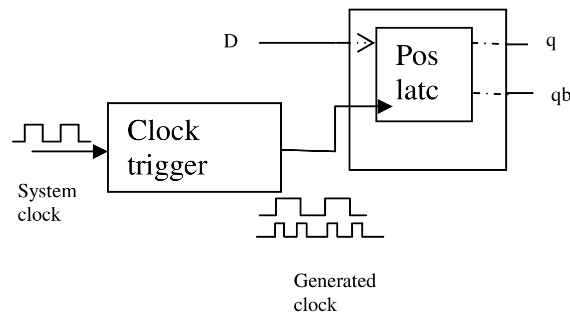


Figure 3. Block diagram of one latch-double edge triggered flipflop.

In the proposed method the onelatch-flipflop is made to work both as a positive edge triggered flipflop in one mode and double edge triggered flipflop in another mode. The block diagram of onelatch-double edge triggered flipflop is shown in Figure 3.

The proposed flipflop can be introduced into testing as a scanflop just by combining it with the multiplexer. The structure of OL-DET scanflop is shown in Figure 4. The proposed OL-DET scanflop is efficient enough to reduce the power during testing because it required only n/2 clock cycles to shift-in or shift-out the n-vectors into the n-number of flipflops in scanchain, because this flop captures two data per clock cycles.

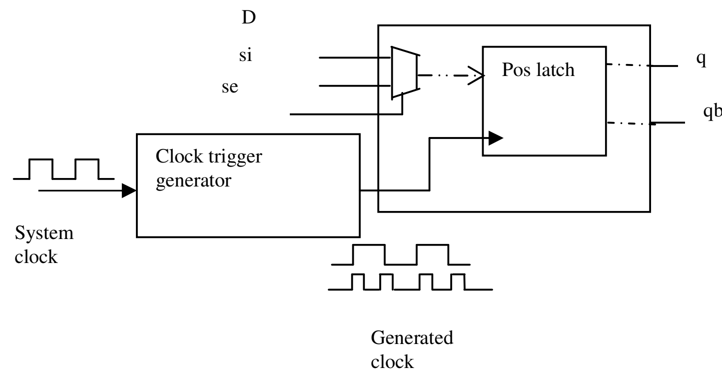


Figure 4. Structure of OL- DET scanflop

During the shift-in and shift-out cycle of testing the circuit works in test mode where the entire scanflop works as a shift register and it is independent of the combo cloud present in the circuit and it can work comfortably with half a clock cycle. But during capture cycle the circuit works in the data mode. It is necessary that the combo cloud should evaluate the vector values from the flop and the output from combo is captured again by the flipflop. The entire evaluation of combo should happen in half a cycle if the flop is a double edge triggered flipflop. It is advantageous in one way as a fast system but another way it may lead for more number of multicycle path constraints. To avoid this problem the same scanflop is modified as dual mode double edge triggered flipflop just by modifying the clock trigger generator circuit. The circuit diagram of clock trigger generator is shown in Figure 5.

The and-gate (A1) is responsible for generating the pulse with a narrow on time as a output of clock generator during the positive edge of the system clock. Similarly Nor-gate (A2) is responsible for the generating pulse with narrow ON time during the negative edge of the system clock. The inverter (A5) in the circuit is a slow gate when compared to other gates which is responsible for a narrow ON time in the generated clock pulse. During the ON time of the generated clock pulse the latch in DFF capture the change in the data. The and-gate(A3) in the circuit which helps the entire flop to work in the dual mode. During the test mode scan enable (se = 1) which allows the clock trigger generator signal to generate narrow positive pulse (ON time) during both positive and negative edges of the system clock pulse. So, the flop works as a double edge triggered flipflop during shift-in and shift-out cycle of testing. During the capture cycle the circuit enters into the data mode with the values of scan enable (se= 0) which stops generating the positive level of the clock trigger pulse during the negative edge of the system clock and allow the circuit to generate the narrow pulse only during the positive edge of the system clock. So, the DMOL-DET works as a single edge ordinary

positive edge triggered flipflop in data mode. This helps in avoiding the multicycle path constraint and unnecessary partitioning of the circuit.

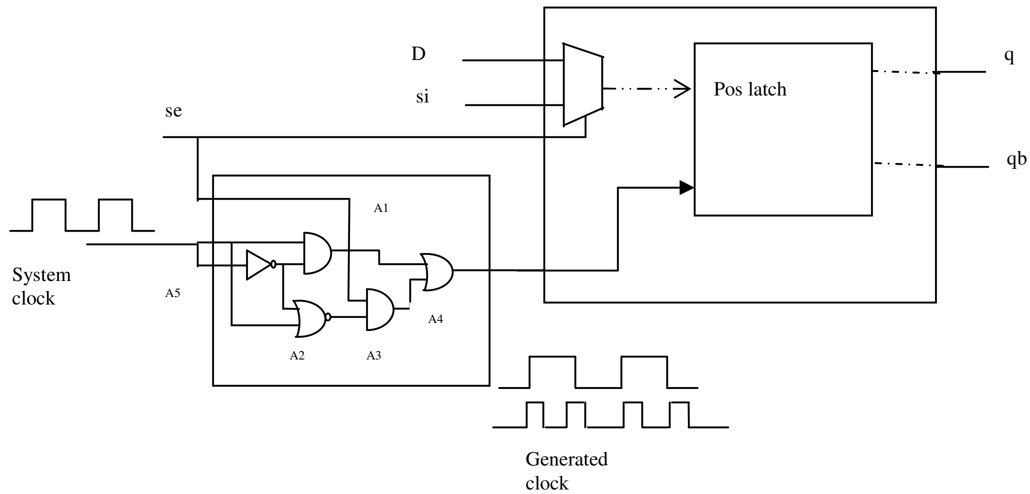


Figure 5. Dual mode one latch Double Edge Triggered flipflop

## 3. RESULTS

In this paper the proposed circuit is implemented and simulated using Cadence NCSIM tool to observe its functionality. The results are shown in Figure 6. It is observed from the simulated output waveform the clock trigger generator circuit is able to generate the narrow positive pulse during the positive and negative edges of system clock when se =1 and only during the positive edge when se = 0. The input data 'si' entered into the flop during se = 1 and during se = 0 the data values of 'd' entered into the flop. The circuited is simulated for 10 MHz .

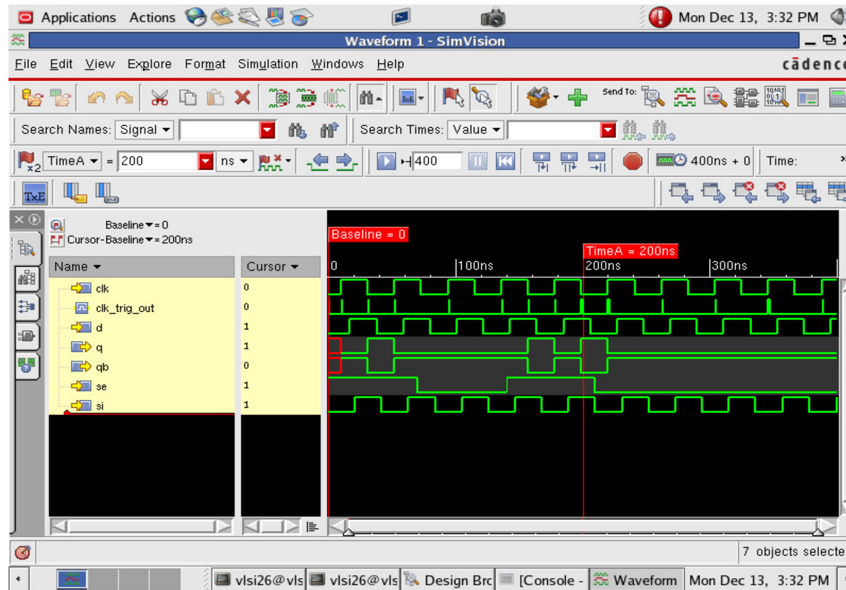


Figure 6. Simulated output of DMOL-DET

It is also observed from the waveform the speed of the flop is increased during the shift cycles. The same circuit is synthesized using the RTL compiler of Cadence tool for 180nm technology to observe the area required for the circuit and static power analysis. The comparison of different scan flops[10] are shown in the Table.1. From the table it is observed that the area required for DMOL-DET is less for DFF with the extra cost of area for clock trigger generator circuit area. If it is compared as a single flop the cost of the clock trigger generator circuit area is explicit but, when scanchain is formed using these flops the appreciable amount of area reduction can be observed in the DMOL-DET flop.

Table 1. Comparison of Different Scanflops.

| Type of flop /parameters | Usual scanflop | Pipelined DET scanflop | DMOL-DET scanflop(Flop + clock generator circuit) |
|---|---|---|---|
| Single scanflop area (in gate counts) | 59.70 | 80.73 | 41.86 + 27.03 = 68.89 |
| Area of 10 flops as a scanchain | 624.06 | 834 | 445.6 + 27.03 = 472.63 |
| Number of cycles to shift 10 bits | 10 | 5 | 5 |
| Static leakage power (nw) | 52.43 | 60.19 | 30.55 + 8.90 = 39.45 |

## 4. CONCLUSIONS

It is observed from the result that DMOL-DET reduces the chip area about 30% when compared to the ordinary scanflop and 43% when compare to the Pipelined DET scanflop.It also reduces the static power about 25% when compared to the usual scanflop, 35% when compared to the pipelined DET scanflop and the speed of testing get increased during shift cycle for about 50% when compared to the usual scanflop. As a conclusion the DMOL-DET can be used in the digital circuit as a good scanflop for testing purpose which helps in reducing the area, power and increasing speed. As a future work the characteristics and its dynamic power analysis of the proposed scanflop can be carried out.

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