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Implementation of Truncated Multiplier for FIR Filter based on FPGA

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Abstract- Multiplication of two bits produces an output which is twice that of the original bit. It is usually needed to truncate the partial product bits to the required precision to reduce area cost. Fixed-width multipliers, a subset of truncated multipliers, compute only n-most significant bits (MSBs) of the 2n-bit product for n × n multiplication and use extra correction/compensation circuits to reduce truncation errors. Truncated multipliers provides significant improvements in area, delay, and power. The proposed method finally reduces the number of full adders and half adders during the tree reduction. The output is in the form of LSB and MSB. Finally the LSB part is compressed by using operations such as deletion, reduction, truncation, rounding and final addition because of which area is reduces.

In the proposed truncated multiplier design, introduces column-by-column reduction. In this design of truncated multiplier, to minimize the half adders in each column because the full adder has high compression rate when compared to HA. FPGAs reprogram ability and high degree of parallelism attracts them for DSP applications. The hardware description language VHDL is used to describe the design. The design is synthesized using Quartus-II software /Xilinx Project Navigator 13.1 software. Simulation is done using Modelsim. The design implementation is done on Altera DE board CYCLON-II family device EP2C35F672C6.

Keywords- Deletion, reduction, truncation, rounding, final addition, truncated multiplier, adaptive filter.

I. INTRODUCTION

The multiplier is an essential element of digital signal processing operations such as filtering and convolution. Most of the digital signal processing operations such as Discrete Cosine Transform (DCT) or Discrete Wavelet Transform (DWT) is accomplished by repetitive multiplication and addition. Hence the speed of these operations exclusively depends upon the speed of the multiplication operation being performed. It has been observed that the multiplier requires the longest delay among the basic operational blocks in a system; hence the critical path is predominantly determined by the multiplier.

Also, the standard multiplier has been observed to consume comparatively more area and power. Therefore a design which will reduce the consumed area or power or speed or any combination of the above three parameters is of research interest.

There is need of standard multiplier for DSP application such as filtering, convolution, and fast Fourier or discrete cosine transform. These operations for DSP application can be performed using truncated multiplier. Standard multiplier produces 2n bit output for n x n bit multiplication, whereas truncated multiplier gives n-bit output. This truncated multiplier follows steps such as delete non require bits, reduce the level, truncation, round up result using correction logic and final addition which offers precision improvement.

II. LITERATURE SURVEY

A faithfully rounded truncated multiplier design is presented where the maximum absolute error is guaranteed to be not more than 1 unit of least position. In there proposed method, they jointly considers the delete non require bits, reduce the level, truncation, round up result using correction logic and final addition of partial product bits in order to minimize the number of full adders and half adders during tree reduction. In this method efficiency of the proposed faithfully truncated multiplier with area saving rates of more than 30%. In addition, the truncated multiplier design also has smaller delay due to the smaller bit width in the final carry-propagate adder. The faithfully truncated multiplier has a total error of no more than 1 ulp and can be used in applications which need accurate result. By using this method we can be easily extended to signed or Booth multiplier design [1].

Low-cost finite impulse response (FIR) designs are presented using the concept of faithfully rounded truncated multipliers. They jointly consider the optimization of bit width and hardware resources without sacrificing the frequency response and output signal

precision. Non uniform coefficient quantization with proper filter order is proposed to minimize total area cost. Multiple constant multiplications-accumulations in a direct FIR Structure is implemented using an improved version of truncated multipliers. Compare to other FIR design approaches show that the proposed designs achieve the best area, delay and power results [2].

III. REDUCTION SCHEMES OF PARALLEL MULTIPLIERS

PP (partial product) generation produces partial product bits from the multiplicand and multiplier. PP reduction is used to compress the partial product bits to two. Finally the partial products bits are added by using carry propagate addition. Two famous reduction methods are available,

1. Dadda tree

2. Wallace tree

Dadda reduction performs the compression operation whenever it required. Wallace tree reduction always compresses the partial product bits.

In this proposed work standard parallel multiplier is design & truncated multiplier design, introduces column-by-column reduction. The result is obtained from standard parallel multiplier and truncated multiplier gives close result. Truncated multiplier minimizes the half adders in each column because the full adder has high compression rate when compared to HA.

A parallel tree multiplier design usually consists of three major steps, i.e PP generation, PP reduction, and final carry propagate addition. PP generation produces PP bits from the multiplicand and the multiplier. The goal of PP reduction is to compress the number of PPs to two, which is to be added for final addition. Wallace tree reduction manages to compress the PPs as early as possible, whereas Dadda reduction only performs compression whenever.

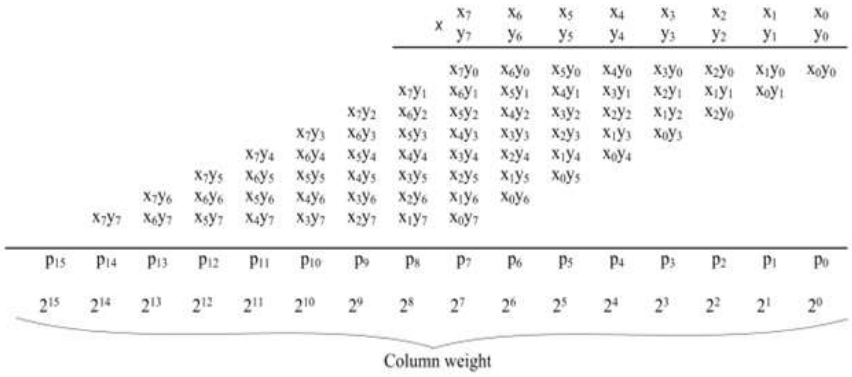


Fig. Standard parallel 8 x 8 bit multiplier

In this proposed work we first design standard parallel 8x8 multiplier which gives following result.

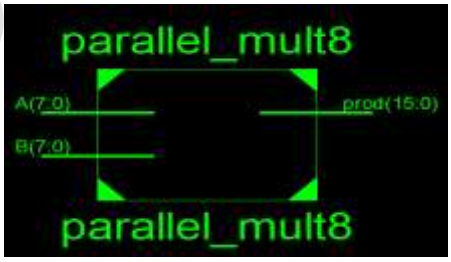


Fig. Block diagram of 8 x 8 parallel multiplier

Simulation result of standard parallel 8 x 8 bit multiplier is shown

/parallel_mult8/a	212	112	111	212
/parallel_mult8/b	140	112	60	140
/parallel_mult8/prod	29680	12544	6660	29680

This standard parallel 8x8 multiplier provides accurate result but requires large number of component to design by virtue of its area requirement is more. Also it requires more power and propagation delay. To reduce this requirement of area, power and delay we proposed truncated multiplier.

IV. PROPOSED TRUNCATED MULTIPLIER DESIGN

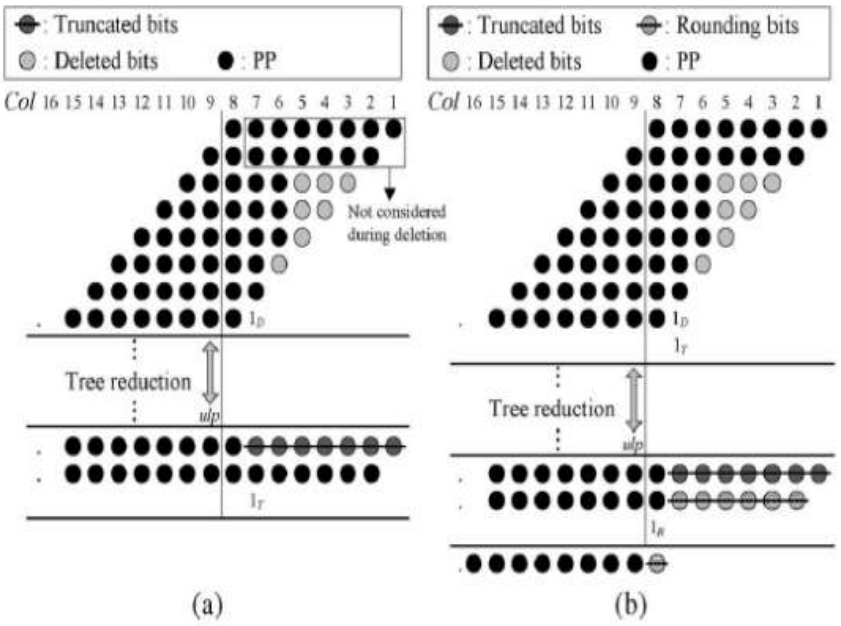


Fig. Proposed truncated multiplier design

For convenience, we assume 8 x 8 unsigned multiplication of two numbers. The objective of a good multiplier is to provide a better result, high speed and low power consuming chip. To save area requirement and power consumption of a VLSI design. In a truncated multiplier, number of the least significant columns of bits in the partial product matrix are not formed. Fig1. Show 8x8 truncated multiplication. (a) Deletion, reduction and truncation. (b) Deletion, reduction, truncation, rounding with correction logic and final addition.

PROPOSED ALGORITHM

In proposed architecture we multiply 8 x 8 bits, and the bits are reduced in step by step manner. Deletion is the first operation performed in Stage 1 to remove the PP bits, as long as the magnitude of the total deletion error is no more than 2^{-P-1}. Then numbers of stages are reduce the final bit width without increasing the error. Fig. shows proposed truncated multiplier. This reduces the area and power consumption of the multiplier [3]. For this we used Half Carry (HC), Full Carry (FC), Half Adder (HA), Full Adder (FA) logic to improve the result. Requirement of component for this truncated multiplier is less as compared to standard parallel multiplier; however it reduces the area required as well as delay and power. Following result is obtained for proposed 8 x 8 bit truncated multiplier which is approximately same as that of standard parallel multiplier with precision improvement.

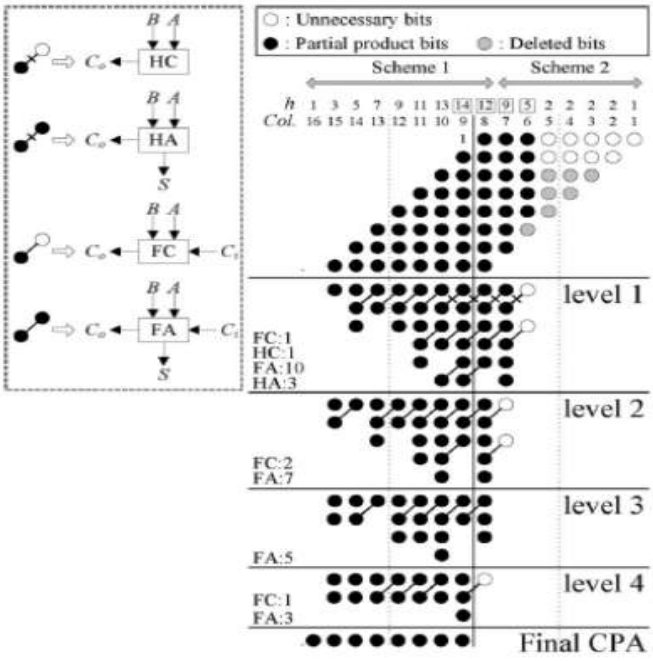


Fig. Proposed 8 x 8 bit truncated multiplier

The truncated multiplier for general M × N unsigned multiplication with a full product of M+N bits truncated to P bits. In other words, there are T = M + N – P bits truncated . First, perform deletion in stage 1 to remove the PP bits, as long as the magnitude of the total deletion error is not more. Bits[Col] represents the number of PP bits of column Col. Note that the first two rows of PP bits from column 1 to column T 1 are kept unchanged during the deletion process. Note that at column T + 1, we add a constant of which is the sum of the three constants (1_D, 1_T, and 1_R) in the aforementioned deletion, truncation, and rounding. In stage 2, for column Col, determine whether an HA is required or not (HA[Col] = true or false) and find the number of carry bits to the next column.

Furthermore, according to this experiments, it is observed that HAs should be used as early as possible in order to reduce the critical path delay because HAs have a smaller pin-to-pin delay compared with FAs. In stage 3, tree reduction is performed along with truncation and rounding. For the final two rows of PP bits from column 1 to column T − 1, there no need to generate these PP bits because they will be removed during the subsequent truncation and rounding processes. For example, in figure the two white dots at level 1 and the two white dots at level 2 are not generated during the compression with FAs or HAs. Thus, in this introduce two simplified versions of the FA and HA cells, i.e., full and half adders without the sum output bits. For column T, only need to generate the carry bit (to column T + 1) for the last FA compression because the sum output bit will be discarded during the rounding process. For example, the FA compression does not need to generate the white dot (the sum output bit) at level 4 of figure. Note that for column T + 1 to M + N, although it is adopted to determine whether an HA is needed or not, we actually do not compress the column height to one because this compression will cause ripple carry. Indeed, at the last level of the reduction process, some column, for example column i, has a height of three, and the remaining columns beyond this specific column, i.e., columns i +1, i + 2….., have a column height of two, as shown in level 4 of figure. Afterward, a final CPA performs the final summation. In the example in figure, the bit width of the final CPA is 7.

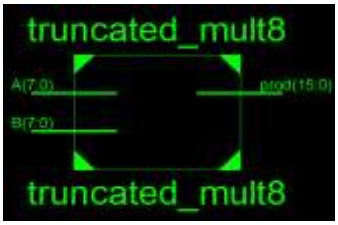


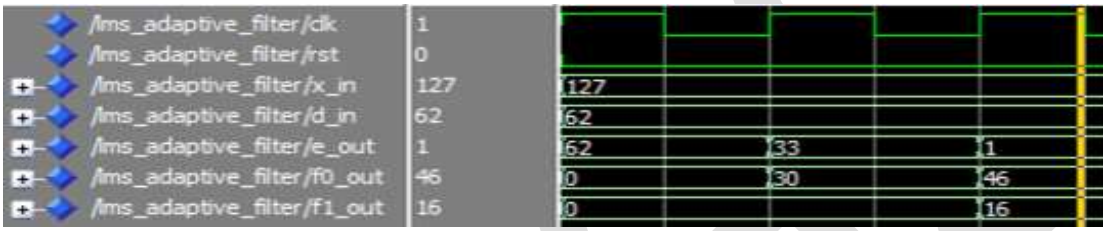
Fig. Block diagram of 8 x 8 bit truncated multiplier

Following simulations shows result of 8 x 8 truncated multiplier

This truncated multiplier is proposed multiplier for DSP applications. For this truncated multiplier there are different logic is applied such as deletion, reduction, truncation, rounding and final addition. It is providing multiplication of 8 × 8 bit which gives approximate result.

For FIR filter with standard 8 × 8 bit parallel multiplier

This simulation is for 2-Tap Adaptive FIR filter with standard parallel multiplier. From this it is clear that error continuously tending towards zero.



For FIR filter with 8 × 8 bit truncated multiplier

V. EXPERIMENTAL ANALYSIS

A) SYNTHESIS RESULT

For synthesis purpose we use Quartus-II software on hardware platform of Altera Cyclon-II family device EP2C35F672C6.

I. For Standard 8 × 8 bit parallel multiplier

For this standard 8 × 8 bit parallel multiplier requires more area as there is requirement of more number of logic elements.

Logic utilization	Used	Available	Utilization
Number of logic elements	189	33216	0.57%
Number of pins	32	475	6.7%

II. For 8 × 8 bit truncated multiplier

For this 8 × 8 bit truncated multiplier requires less area as there is need of less number logic elements which is comparatively less as compare to standard 8 × 8 bit parallel multiplier.

Logic utilization	Used	Available	Utilization

Number of logic elements	109	33216	0.328%
Number of pins	32	475	6.7%

This synthesis result shows the comparison between standard parallel multiplier and truncated multiplier on the basis of logic utilization.

III. For 2-Tap Adaptive FIR Filter with Standard 8 × 8 Bit Parallel Multiplier

Logic utilization	Used	Available	Utilization
Number of logic elements	758	33216	2.28%
Total logic registers	40	33216	----
Total pins	66	475	13.9%

IV. For 2-Tap Adaptive FIR filter with 8 × 8 Bit Truncated Multiplier

Logic utilization	Used	Available	Utilization
Number of logic elements	528	33216	1.58%
Total logic registers	88	33216	----
Total pins	66	475	13.9%

These synthesis result shows numbers of logic elements are required for 2-tap adaptive FIR filter with standard parallel multiplier is more as compared to truncated multiplier. It is concluded form this synthesis result area requirement is more as compare to truncated multiplier.

B) POWER ANALYSIS

In this power analysis result gives details of power dissipation for the different designs.

Power Analysis for Standard 8 × 8 Bit Parallel Multiplier

Core static thermal power dissipation	79.94mW
I/O thermal power dissipation	33.70mW
Total thermal power dissipation	113.64mW

Power Analysis for 8 × 8 Bit Truncated Multiplier

Core static thermal power dissipation	79.94mW
I/O thermal power dissipation	33.67mW
Total thermal power dissipation	113.61mW

Power Analysis for 2-Tap Adaptive Filter with Standard 8 × 8 Bit Parallel Multiplier

Core static thermal power dissipation	79.95mW
I/O thermal power dissipation	37.89mW
Total thermal power dissipation	117.84mW

Power Analysis For 2-Tap Adaptive FIR Filter with 8 × 8 Bit Truncated Multiplier

Core static thermal power dissipation	79.95mW
I/O thermal power dissipation	37.81mW
Total thermal power dissipation	117.76mW

It is concluded from this result power dissipation is more for standard multiplier as compare to truncated multiplier regarding 2-tap adaptive FIR filter.

C) TIMING ANALYSIS

Propagation delay for standard 8 × 8 bit parallel multiplier	22.412ns
Propagation delay for 8 × 8 bit truncated multiplier	19.366ns
Propagation delay for 2-Tap Adaptive FIR filter with standard parallel multiplier	21.56ns
Propagation delay for 2-Tap Adaptive FIR filter with truncated multiplier	9.79ns

D) COMPARATIVE ANALYSIS

There is need of more number of logic elements for implementing the design for standard 8 × 8 bit parallel multiplier as compare to truncated of multiplier. Also there is reduction in power dissipation and propagation delay for truncated multiplier. It is observed from the table, there is reduction in area, power and delay in truncated multiplier as compare to truncated multiplier.

Parameter	Parallel multiplier	Truncated multiplier	Filter with parallel multiplier	Filter with truncated multiplier
Design summary	LE 189/33216	109	758	528
Power analysis	Thermal Pd 113.64mW	113.61mW	117.84mW	117.76mW
Timing analysis	t_{pd}=22.412ns	19.366ns	21.56ns	9.79ns
No of HA, FA, HC, FC	8HA, 48FA	3HA,32FA, 1HC,4FC	more	less

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FUTURE SCOPE

Truncated multiplier can be effectively implemented in FIR filter structure. Conventional FIR filer performs ordinary multiplication of co-efficient and input without considers the length. Thus the structure can be made effective by replacing the existing multiplier with the proposed fixed width truncated multiplier for visible area reduction. It is nowadays used in PI temperature controller. Truncated multiplier is having more no of usages in that applications wherever truncation is possible to get approximate result. This truncated multiplier also applicable to any type of DSP applications where there is a need of multiplication process.

CONCLUSION

In this truncated multiplier, design is implemented by jointly considering the deletion, reduction, truncation, and final addition of PP bits. It is observed that the results of standard parallel multiplier and then compare this result with truncated multiplier which is approximately same. It is analyzed that area required for implementation of truncated multiplier reduces to large extent as compare to standard parallel multiplier. Also there is reduction in power dissipation and propagation delay. In this system final truncated multiplier satisfies the precision requirement.

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