A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator

Gabriel A. Rincon-Mora, *Member, IEEE*, and Phillip E. Allen, *Fellow, IEEE*

***Abstract*— The demand for low-voltage, low drop-out (LDO) regulators is increasing because of the growing demand for portable electronics, i.e., cellular phones, pagers, laptops, etc. LDO's are used coherently with dc-dc converters as well as standalone parts. In power supply systems, they are typically cascaded onto switching regulators to suppress noise and provide a low noise output. The need for low voltage is innate to portable low power devices and corroborated by lower breakdown voltages resulting from reductions in feature size. Low quiescent current in a battery-operated system is an intrinsic performance parameter because it partially determines battery life. This paper discusses some techniques that enable the practical realizations of low quiescent current LDO's at low voltages and in existing technologies. The proposed circuit exploits the frequency response dependence on load-current to minimize quiescent current flow. Moreover, the output current capabilities of MOS power transistors are enhanced and drop-out voltages are decreased for a given device size. Other applications, like dc-dc converters, can also reap the benefits of these enhanced MOS devices. An LDO prototype incorporating the aforementioned techniques was fabricated. The circuit was operable down to input voltages of 1 V with a zero-load quiescent current flow of 23 μA. Moreover, the regulator provided 18 and 50 mA of output current at input voltages of 1 and 1.2 V, respectively.**

***Index Terms*— Low drop-out, low-voltage regulators, power supply circuits, regulators.**

I. Introduction

THE low drop-out nature of the regulator makes it appropriate for use in many applications, namely, automotive, portable, industrial, and medical applications [1]. The automotive industry requires low drop-out (LDO) regulators to power up digital circuits, especially during cold-crank conditions where the battery voltage can be below 6 V. The increasing demand, however, is especially apparent in mobile battery-operated products, such as cellular phones, pagers, camera recorders, and laptops [2]. In a cellular phone, for instance, switching regulators are used to boost up the voltage but LDO's are cascaded in series to suppress the inherent noise associated with switchers. LDO's benefit from working with low input voltages because power consumption is minimized accordingly, $P = I_{\text{Load}} * V_{\text{in}}$. Low voltage and low quiescent current are intrinsic circuit characteristics for increased battery efficiency and longevity [3]. Low voltage operation is also a consequence of process technology. This is because isolation barriers decrease as the component densities per unit area increase, thereby exhibiting lower breakdown voltages [4], [5]. Therefore, low power and finer lithography require regulators to operate at low voltages, produce precise output voltages, and have characteristically lower quiescent current flow [5]. By the year 2004, the power supply voltage is expected to be as low as 0.9 V in 0.14-μm technologies [5], [6]. Drop-out voltages also need to be minimized to maximize dynamic range within a given power supply voltage. This is because the signal-to-noise ratio typically decreases as the power supply voltages decrease while noise remains constant [7]. Lastly, financial considerations also require that these circuits be realized in relatively simple processes, such as standard CMOS, bipolar, and inexpensive BiCMOS technologies [8]. An example of the relatively inexpensive BiCMOS process is the 2-μm MOSIS technology (information is available through the Internet at http://www.isi.edu/mosis). This is a vanilla CMOS process with an added p-base layer to realize vertical NPN transistors. Fig. 1 illustrates the general components of a typical low drop-out regulator, namely, an error amplifier, a pass device, a reference circuit, a feedback network, and some loading elements. The associated gate capacitance of the pass device is depicted as C_{par}.

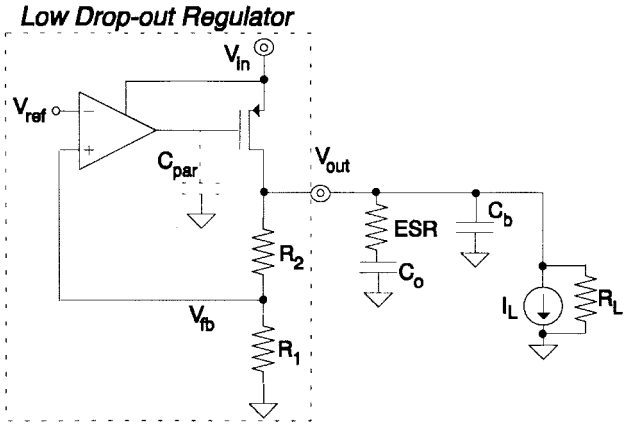

Fig. 1. Typical low drop-out regulator topology.

II. Current Efficient Buffer

A. Current Efficiency

Current efficiency is an important characteristic of battery-powered products. It is defined as the ratio of the load-current to the total battery drain current, which is comprised of load-

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G. A. Rincon-Mora is with the Standard Linear Design Branch, Texas Instruments Incorporated, Dallas, TX 75243 USA.

P. E. Allen is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA.

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current $(I_{\rm Load})$ and the quiescent current (I_q) of the regulator

$$\text{Efficiency}_{\text{current}} = \frac{I_{\rm Load}}{I_{\rm Load} + I_q}. \tag{1}$$

Current efficiency determines how much the lifetime of the battery is degraded by the mere existence of the regulator. Battery life is restricted by the total battery current drain. During conditions where the load-current is much greater than the quiescent current, operation lifetime is essentially determined by the load-current, which is an inevitable characteristic of linear regulators. On the other hand, the effects of quiescent current on battery life are most prevalent during low load-current conditions when current efficiency is low. For many applications, high load-current is usually a temporary condition, whereas the opposite is true for low load-currents. As a result, current efficiency plays a pivotal role in designing battery-powered supplies. The two performance specifications that predominantly limit the current efficiency of low drop-out regulators are maximum load-current and transient output voltage variation requirements. Typically, more quiescent current flow is necessary for improved performance in these areas.

B. Challenges

Output current and input voltage range directly affect the characteristics of the pass element in the regulator, which defines the current requirements of the error amplifier. As the maximum load-current specification increases, the size of the pass device necessarily increases. Consequently, the amplifier's load capacitance, $C_{\rm par}$ in Fig. 1, increases. This affects the circuit's frequency performance by reducing the value of the parasitic pole present at the output of the amplifier [9]. Therefore, phase-margin degrades and stability may be compromised unless the output impedance of the amplifier is reduced accordingly. As a result, more current in the buffer stage of the amplifier is required, be it a voltage follower or a more complicated circuit architecture. In a similar manner, low input voltages require that MOS pass device structures increase in size and thus yield the same negative effects on frequency response and quiescent current as just described. This is because the gate drive decreases as the input voltages decrease, thereby demanding larger MOS pass elements to drive high output currents.

Further limits to low quiescent current arise from the transient requirements of the regulator, namely, the permissible output voltage variation in response to a maximum load-current step swing. The output voltage variation is determined by the response time of the circuit, the specified load-current, and the output capacitor [9]. The worst case response time corresponds to the maximum output voltage variation. This time limitation is determined by the closed-loop bandwidth of the system and the output slew-rate current of the error amplifier [9]. These characteristic requirements become more difficult to realize as the size of the parasitic capacitor at the output of the amplifier $(C_{\rm par})$ increases, which results from low-voltage operation and/or increased output current specifications. Consequently, the quiescent current of the amplifier's gain stage is limited by a bandwidth minimum while the quiescent current of the amplifier's buffer stage is limited by the slew-rate current required to drive $C_{\rm par}$.

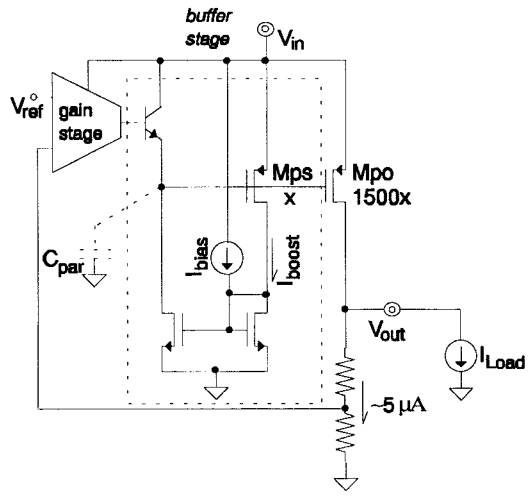

Fig. 2. Current efficient LDO buffer stage.

C. Proposed Circuit Topology

A topology that achieves good current efficiency performance is illustrated in Fig. 2. The operation revolves around sensing the output current of the regulator and feeding back a ratio of the current to the slew-rate limited node of the circuit. Transistor Mps sources a fraction of the current flowing through the output transistor Mpo. During low load-current conditions, the current fed back $(I_{\rm boost})$ is negligible, thereby yielding high overall current efficiency and not aggravating battery life. Consequently, the current through the emitter follower is simply $I_{\rm bias}$ when load-current is low. During high load-current conditions, the current through the emitter follower is increased by $I_{\rm boost}$, which is no longer negligible. The resulting increase in quiescent current has an insignificant impact on current efficiency because the load-current is, at this point, much greater in magnitude. However, the increase in current in the buffer stage aids the circuit by pushing the parasitic pole associated with $C_{\rm par}$ (P_3) to higher frequencies and by increasing the current available for slew-rate conditions. Thus, the biasing conditions for the case of zero load-current can be designed to utilize a minimum amount of current, which yields maximum current efficiency and prolonged battery life.

1) Frequency Response: When the load-current is low, the magnitude of the system's dominant pole (P_1), determined by the output capacitor and the output impedance of the pass device, is also low [10]. This is because the output impedance of the pass device is inversely proportional to the current flowing through it

$$P_1 \approx \frac{1}{2\pi C_o R_{o\text{-pass}}} \approx \frac{\lambda I_{\rm Load}}{2\pi C_o} \tag{2}$$

where C_o is the output capacitance, $R_{o\text{-pass}}$ is the output resistance of Mpo, λ is the channel length modulation parameter, and $I_{\rm Load}$ is the load-current. Consequently, the unity gain frequency (UGF) is at low frequencies when the load-current is low, which relaxes the requirement of the parasitic pole at the

output of the error amplifier (P_3) to be approximately greater than or equal to the minimum unity gain frequency $(\mathrm{UGF}_{\min})$. This corresponds to a phase margin of approximately 45 to 90° with an associated design equation of

$$P_{3_{\text{no-load-current}}} \approx \frac{g_{m_{\text{npn}}}}{2\pi C_{\text{par}}} = \frac{I_{\text{bias}}}{2\pi V_t C_{\text{par}}} \geq \mathrm{UGF}_{\min} \tag{3}$$

where $g_{m_{\text{npn}}}$ is the transconductance of the emitter follower and V_t is the thermal voltage. As load-current increases, however, the dominant pole increases linearly and consequently so does the UGF. The open-loop gain (A_v) is inversely proportional to the square root of the load current

$$A_v \approx A_{\text{amp}} g_{mp} R_{o\text{-pass}} \propto \frac{\sqrt{I_{\text{Load}}}}{I_{\text{Load}}} = \frac{1}{\sqrt{I_{\text{Load}}}} \tag{4}$$

where A_{amp} is the gain of the error amplifier, while g_{mp} and $R_{o\text{-pass}}$ are the transconductance and the output resistance of the pass device, respectively. Since the dominant pole (P_1) increases faster than the gain decreases with load-current, the unity gain frequency increases as the load-current increases [(2) and (4)]. These consequential effects of load-current on frequency response are graphically illustrated in Fig. 3. Zero Z_1 and pole P_2 are defined by the output capacitor (C_o), associated equivalent series resistance (ESR) of C_o, and the bypass capacitors (C_b) shown in Fig. 1 [9]. Therefore, the parasitic pole (P_3) is also required to increase with load-current, which is achieved by the load dependent boost current. This is apparent from the following equation:

$$P_3 \approx \frac{g_{m\text{NPN}}}{2\pi C_{\text{par}}} = \frac{I_{\text{bias}} + I_{\text{boost}}}{2\pi V_t C_{\text{par}}} \approx \frac{I_{\text{bias}} + kI_{\text{Load}}}{2\pi V_t C_{\text{par}}} \tag{5}$$

where k corresponds to a constant mirror ratio, i.e., 1/1500 for Fig. 2. The circuit can be designed such that P_3 increases at a faster rate than the UGF with respect to load-current. This results in the following relation:

$$\begin{aligned} P_{3\text{-rate}} = \frac{\partial P_3}{\partial I_{\text{Load}}} &\approx \frac{k}{2\pi V_t C_{\text{par}}} \geq P_{1\text{-rate}} \\ &\approx \frac{\lambda}{2\pi C_o} > \mathrm{UGF}_{\text{rate}} \end{aligned} \tag{6}$$

or

$$k \geq \frac{\lambda V_t C_{\text{par}}}{C_o} \tag{7}$$

where $P_{3\text{-rate}}$, $P_{1\text{-rate}}$, and $\mathrm{UGF}_{\text{rate}}$ are the rates with respect to load-current of pole P_3, pole P_1, and the unity gain frequency, respectively. Thus, current efficiency can be maximized to accommodate the load dependent requirements of P_3. If the load dependence of P_3 is not incorporated into the circuit, then more current than necessary is used during low load-current conditions. The frequency response behavior was confirmed through simulations.

2) Transient Response: The circuit of Fig. 2 exhibits the transient response illustrated in Fig. 4 depicted as trace "a" where a maximum load-current step swing is applied to the load. One of the parameters that determines the maximum

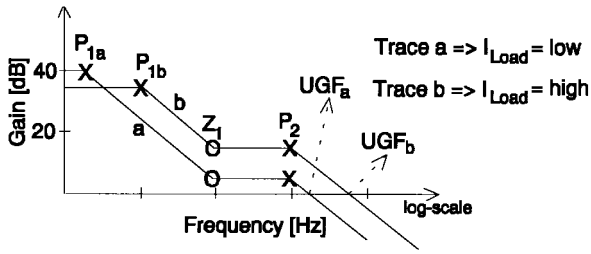

Fig. 3. System frequency response as a function of load-current.

output voltage variation is the response time (Δt_1) required for the system to react and may be expressed as

$$\Delta t_1 \approx \frac{1}{\mathrm{BW}_{\text{cl}}} + t_{\text{sr}} = \frac{1}{\mathrm{BW}_{\text{cl}}} + C_{\text{par}} \frac{\Delta V}{I_{\text{sr}}} \tag{8}$$

where BW_{cl} is the closed-loop bandwidth of the system, ΔV is the voltage change associated with C_{par}, and I_{sr} is the output slew-rate current of the error amplifier [9]. However, the slew-rate current is not constant for the circuit proposed, $I_{\text{sr}} = I_{\text{bias}} + kI_{\text{boost}}$. As a result, a slew-rate condition does not aptly describe the operation of the circuit at hand. During a load-current transition from zero to maximum value, the response time of the circuit is dominated by the bandwidth of the system and the transient response of the buffer stage. In particular, the response time is composed of the time required for the amplifier to respond (t_{amp}), for the sense PMOS transistor (Mps) to start conducting current $(t_{\text{Mps-on}})$, for the positive feedback circuit to latch up $(t_{\text{latch-up}})$, and for the output PMOS device (Mpo) to conduct the load-current (t_{Mpo}). This is represented by the following equation:

$$\begin{aligned} \Delta t_1 &\approx t_{\text{amp}} + t_{\text{Mps-on}} + t_{\text{latch-up}} + t_{\text{Mpo}} \\ &\approx \frac{1}{\mathrm{BW}_{\text{cl}}} + t_{\text{Mps-on}} + t_{\text{latch-up}} \end{aligned} \tag{9}$$

where BW_{cl} is the closed-loop bandwidth of the system (approximately $(t_{\text{amp}} + t_{\text{Mpo}})^{-1}$). The composite buffer stage is essentially a localized positive feedback circuit. The system is stable because the positive feedback gain is less than one. Consequently, the circuit attempts to latch up until the output transistor is fully turned on; at which point, the error amplifier forces the circuit back into the linear region. As a result, the performance tradeoffs between the slew-rate and the quiescent current requirements of typical LDO's are circumvented. For instance, if the parasitic capacitance (C_{par}) is 200 pF, the source-to-gate voltage change required for the output PMOS transistor (ΔV_{sg}) is 0.5 V, the bandwidth of the system is 1 MHz, and the response time is limited to be less than 5 μs, then the slew-rate current $(I_{\text{sr}} = I_{\text{bias}})$ required is approximately 25 μA [(8)]. For the case of the circuit in Fig. 2, a dc current bias (I_{bias}) of only 1 μA can provide the same performance. The dominant factor of the new Δt_1 is the time required for the sense transistor (Mps) to go from being off to subthreshold and finally to strong inversion. Fig. 4 illustrates the simulation results showing the effect of the presence of boost element Mps in the circuit shown in Fig. 2 on the output voltage, for the same biasing conditions. In this case, the load-current is stepped from zero to a maximum of 50 mA in 1 ns.

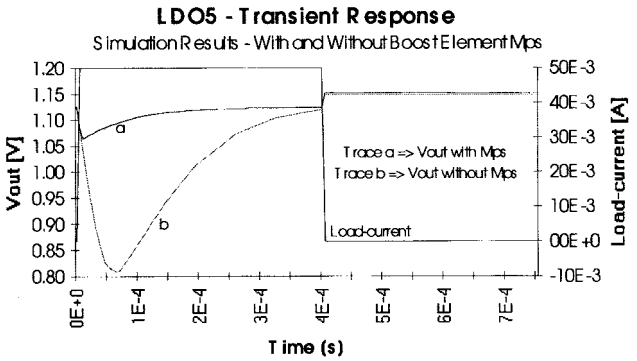

Fig. 4. LDO output voltage variation with and without the boost element Mps in the current efficient buffer stage.

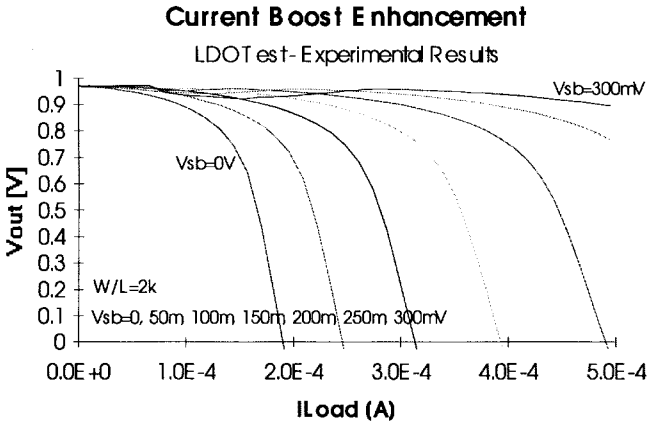

Fig. 5. Maximum load-current performance of the current boost enhancement.

It is observed that the output voltage variation is lower for the circuit implementing the current efficient buffer resulting from a reduction in response time. This does not come at the expense of additional quiescent current flow during zero load-current conditions. Consequently, current efficiency and battery life are maximized.

III. Current Boosting

A. Challenge

As the power supply voltages decrease, the gate drive available for the PMOS pass device decreases. As a result, the aspect ratio of the power transistor needs to be increased to provide acceptable levels of output current. However, the parasitic gate capacitance also increases as the size of the PMOS transistor increases. This constitutes an increase in $C_{\rm par}$ in Fig. 1, which pulls the parasitic pole (P_3) down to lower frequencies. Consequently, the phase margin of the system is degraded and stability may be compromised. This presents a problem when working in a low quiescent current environment.

B. Boosting Technique

One way to improve gate drive without increasing input voltage or device size is by forward biasing the source-to-bulk junction of the PMOS pass device. This results in a reduction of threshold voltage, commonly referred as the bulk effect phenomenon. The threshold voltage $(V_{\rm th})$ is described by

$$|V_{\rm th}| = |V_{\rm to}| + \gamma\left\langle\sqrt{2|\phi_f| - V_{\rm sb}} - \sqrt{2|\phi_f|}\right\rangle \qquad (10)$$

where $|V_{\rm to}|$ is $|V_{\rm th}|$ at a source-to-bulk voltage $(V_{\rm sb})$ of zero, γ is the body bias coefficient, and $|\phi_f|$ is the bulk Fermi potential [11]. Consequently, the threshold voltage decreases as $V_{\rm sb}$ increases, thereby effectively increasing the gate drive of the power PMOS transistor (pass device).

1) Maximum Output Current: For comparative analysis, the maximum current can be observed at the region where the power PMOS device is in saturation, which corresponds to the nondrop-out condition. The corresponding drain current $(I_{\rm sd})$ of the device is

$$I_{\rm sd} \approx \frac{K_p W}{2L}\langle V_{\rm sg} - V_{\rm th}\rangle^2 \approx \frac{K_p W}{2L}\left\langle V_{\rm sg} - |V_{\rm to}| - \gamma\left\langle\sqrt{2|\phi_f| - V_{\rm sb}} - \sqrt{2|\phi_f|}\right\rangle\right\rangle^2 \qquad (11)$$

where K_p is the transconductance parameter of a PMOS transistor. Maximum output current results when the gate drive is at its peak, which occurs when the source-to-gate voltage $(V_{\rm sg})$ is equal to the input voltage $(V_{\rm in})$. Thus, if K_p is 15 μA/V^2, $V_{\rm to}$ is 0.9 V, W/L is 30 kμm/μm, and $V_{\rm in}$ is 1.2 V, then the maximum output current $(I_{0\text{-}\max})$ is 20.2 mA when the source-to-bulk junction is not forward biased. On the other hand, if the source-to-bulk junction is forward biased by 0.3 V, then $I_{0\text{-}\max}$ is 38.5 mA (assuming that γ is 0.5 V$^{1/2}$ and $2|\phi_f|$ is 0.6 V). As a result, the output current capability of a PMOS device can be significantly increased by simply forward biasing the source-to-bulk junction. Fig. 5 illustrates how this technique performs on the prototype circuit of Fig. 2 where the aspect ratio of the power PMOS transistor is 2 kμm/μm. A battery is placed between the source and bulk of the output PMOS device, and the load-current $(I_{\rm Load})$ is swept from 0 to 500 μA. For the same input voltage, the maximum output current capability is increased as $V_{\rm sb}$ is increased, in other words, the circuit stays in regulation for an increased load-current range. At a forward-biased junction voltage of 0.3 V, the output current is more than doubled compared to its nonforward-biased state.

Fig. 6 illustrates a successful implementation of the technique in a low drop-out regulator. This concept could easily be extended to dc-dc converters. The forward-biased junction is defined by the voltage drop across the Schottky diode (Ds). This voltage drop has to be less than a base-emitter voltage to prevent the parasitic vertical PNP transistors of the power PMOS device (Mpo) from turning on and conducting significant ground current through the substrate via the well. The effects of the parasitic bipolar transistors are mitigated by placing a heavily doped buried layer underneath the well of the power PMOS transistor, if this layer is available. Furthermore, the ability to shut off Mpo is not degraded since the forward

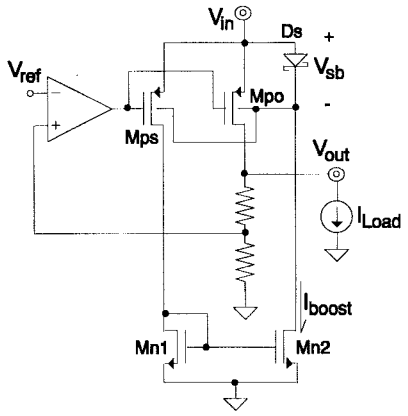

Fig. 6. LDO with current boosting capabilities.

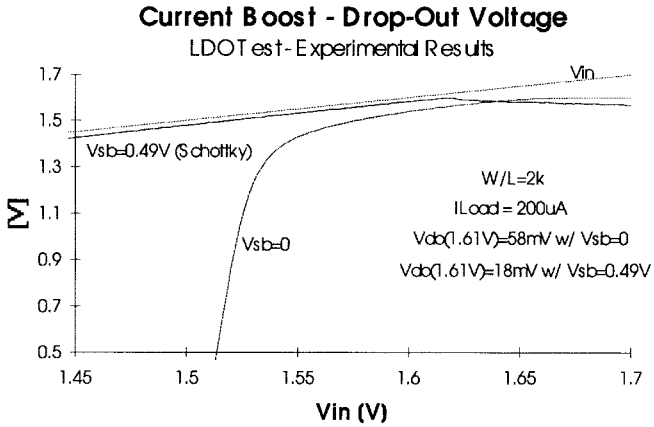

Fig. 7. Drop-out voltage performance of the current boost topology.

bias voltage is a function of load-current. This is similar to the operation of the current efficient circuit of Fig. 2. Thus, $I_{\rm boost}$ is low and $V_{\rm sb}$ is close to zero at low load-currents. At high load-currents, however, $I_{\rm boost}$ and $V_{\rm sb}$ increase, thereby decreasing the threshold voltage and increasing the gate drive of the output PMOS device.

2) Drop-Out Voltage: The method of forward biasing the source-to-bulk junction also yields lower drop-out voltages. In other words, the "on" resistance of the pass device (Mpo) is reduced. When the regulator is in drop-out, Mpo is characteristically in the triode region and exhibits the well-known current relationship of

$$I_{\rm sd} \approx \frac{K_p W}{2L}\left\langle \langle V_{\rm sg} - V_{\rm th}\rangle V_{\rm sd} - V_{\rm sd}^2 \right\rangle \approx \frac{K_p W}{2L}\langle V_{\rm sg} - V_{\rm th}\rangle V_{\rm sd}. \tag{12}$$

The "on" resistance $(R_{\rm on})$ of the PMOS device is approximately

$$R_{\rm on} \approx \frac{V_{\rm sd}}{I_{\rm sd}} \approx \frac{2L}{K_p W}\cdot\frac{1}{\langle V_{\rm sg} - V_{\rm th}\rangle} \approx \frac{2L}{K_p W}\cdot\frac{1}{\left\langle V_{\rm sg} - |V_{\rm to}| - \gamma\left\langle\sqrt{2|\phi_f| - V_{\rm sb}} - \sqrt{2|\phi_f|}\right\rangle\right\rangle} \tag{13}$$

and the drop-out voltage $(V_{\rm do})$ is

$$V_{\rm do} \approx R_{\rm on} I_{\rm Load} \approx \frac{2L}{K_p W}\cdot\frac{I_{\rm Load}}{\left\langle V_{\rm sg} - |V_{\rm to}| - \gamma\left\langle\sqrt{2|\phi_f| - V_{\rm sb}} - \sqrt{2|\phi_f|}\right\rangle\right\rangle}. \tag{14}$$

Thus, if K_p is 15 μA/V^2, $V_{\rm to}$ is 0.9 V, W/L is 30 kμm/μm, $V_{\rm in}$ is 1.2 V, and $I_{\rm Load}$ is 20 mA, then the drop-out voltage is 296 mV (corresponding to 14.8 Ω) when the source-to-bulk junction is not forward biased. However, if the source-to-bulk junction is forward biased by 0.3 V, then $V_{\rm do}$ becomes 216 mV (corresponding to 10.8 Ω) assuming that γ is 0.5 V$^{1/2}$ and $2|\phi_f|$ is 0.6 V. There is a theoretical improvement of approximately 27%. Fig. 7 illustrates the effects of forward biasing the source-to-bulk junction on the drop-out performance of the prototype circuit of Fig. 6 where the aspect ratio of Mpo is 2 kμm/μm. There is an experimental improvement of roughly 67% with a forward bias voltage of 0.49 V.

3) Frequency Response: During low load-current conditions, the current through the sense transistor (Mps) and consequently the current through the Schottky diode (Ds) is negligible. This is because of the high mirror ratio of the output and the sense transistor, Mpo and Mps in Fig. 6. However, Mps and Ds start conducting appreciable current at higher load-currents. Therefore, these elements constitute another ac signal path for the system. The effect of this path manifests itself through the transconductance of the pass device (g_{mp}) in the open-loop gain response. The effective transconductance of the composite pass device of the circuit in Fig. 6 can be described as

$$g_{mp} \approx g_{m\text{-}o} + \frac{g_{mx} r_d g_{mb\text{-}o}}{1 + sC_b r_d} \le g_{m\text{-}o} + g_{mx} r_d g_{mb\text{-}o} \tag{15}$$

where $g_{m\text{-}o}$ is the transconductance of Mpo, r_d is the impedance of the diode Ds, C_b is the total bulk capacitance of Mpo and Mps, $g_{mb\text{-}o}$ is the channel conductance of the bulk of Mpo

$$g_{mb\text{-}o} = \frac{\partial I_{\rm sd}}{\partial V_{\rm sb}} \approx \frac{K_p W}{L}\langle V_{\rm sg} - V_{\rm th}\rangle \frac{\gamma}{2\sqrt{2|\phi_f| - V_{\rm sb}}} = g_{m\text{-}o}\frac{\gamma}{2\sqrt{2|\phi_f| - V_{\rm sb}}} \tag{16}$$

and g_{mx} is

$$g_{mx} = \frac{g_{m\text{-}s} g_{m\text{-}n2}}{g_{m\text{-}n1}} \tag{17}$$

where $g_{m\text{-}s}$, $g_{m\text{-}n1}$, and $g_{m\text{-}n2}$ are the transconductances of Mps, Mn1, and Mn2, respectively. As a result of the high mirror ratio between Mpo and Mps, the effective transconductance of the pass device (g_{mp}) is virtually unaffected by the current boosting technique, i.e., $g_{mp} \approx g_{m\text{-}o}$. This can be illustrated by assuming that W/L_o is 30 kμm/μm, W/L_s

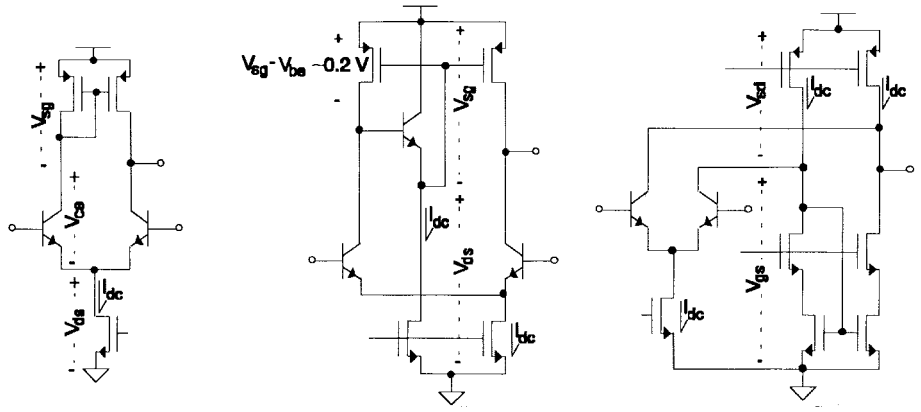

Fig. 8. Amplifier topologies.

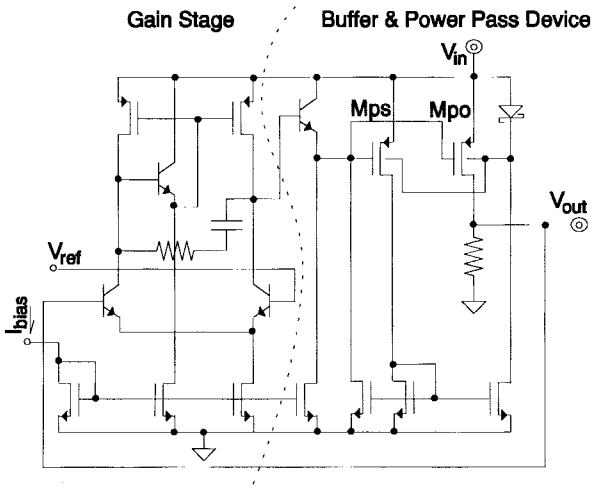

Fig. 9. Low voltage LDO.

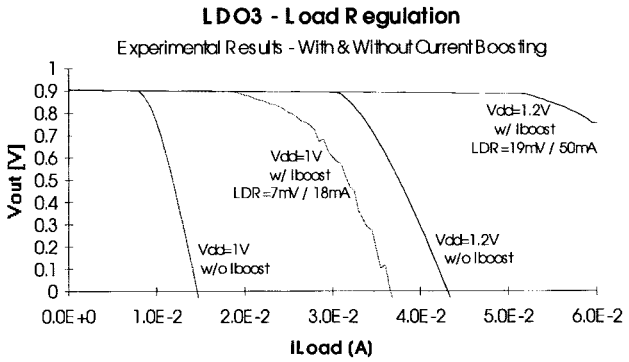

Fig. 10. Load regulation performance.

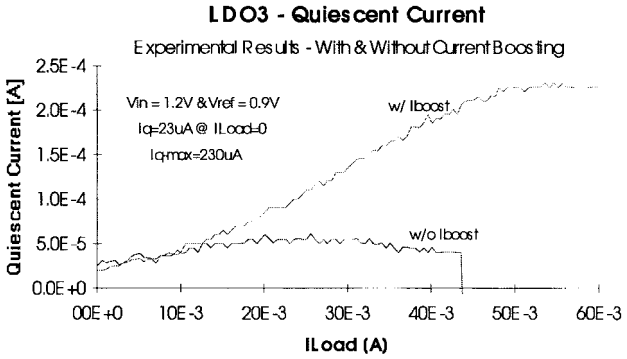

Fig. 11. Quiescent current as a function of load-current.

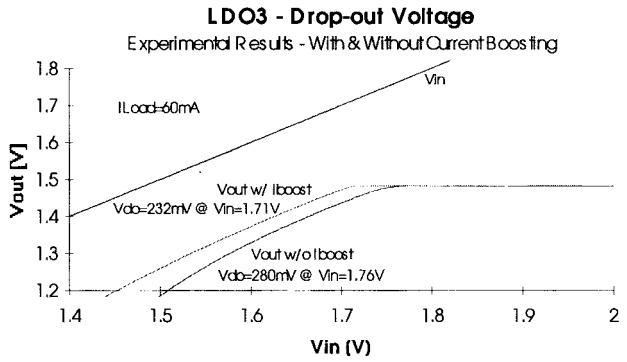

Fig. 12. Drop-out voltage performance at 60 mA of load-current.

is 20 μm/μm, $I_{\rm Load}$ is 50 mA, and Mn1/Mn2 have a 1:1 mirror ratio; the effective transconductance of the composite power PMOS transistor is approximately $g_{m\text{-}o}(1+0.05)$ at dc, where $r_d \approx V_t/I_{\rm diode}$, $K_p = 15$ μA/V^2, $\gamma = 0.5$ V$^{1/2}$, $2|\phi_f| = 0.6$ V, and $V_{\rm sb} = 0.3$ V.

IV. Circuit Design

The problems of low voltage operation emerge in the form of headroom, common-mode range, dynamic range, and voltage swings. Appropriate design techniques must be implemented to approach the practical low voltage limits of a given process technology. Some of the techniques that are generally recommended are complementary input amplifiers and common source [emitter] gain stages. On the other hand, some of the discouraged techniques are unnecessary cascoding, Darlington configurations, and source [emitter] followers [7]. At the end, however, the choice of circuit topology and configuration depends on the specific application and the process technology. The theoretical headroom limit of low voltage operation is a transistor stack of one diode and one nondiode connected device $(V_{\rm gs}[V_{\rm be}] + V_{\rm ds}[V_{\rm ce}])$, which is

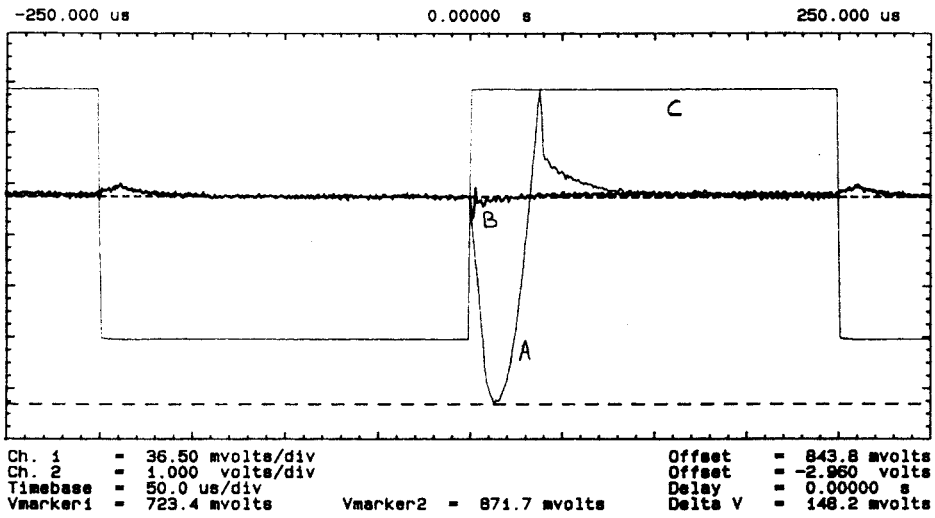

Fig. 13. Output voltage variation (Traces A & B—without and with the transient boost) resulting from a load-current pulse train (Trace C—0 to 50 mA).

TABLE I
PERFORMANCE SUMMARY

	LDO	LDO w/o Current Boost	LDO w/o Trans. Boost
$I_{quiescent}$ @ no-load	23 µA	23 µA	23 µA
$I_{quiescent-max}$	230 µA	50 µA	200 µA
I_{o-max} @ V_{in}=1.2V	50 mA	32 mA	50 mA
@ V_{in}=1V	18 mA	8 mA	18 mA
Line Reg.	4 mV / 3.8 V	3 mV / 3.67 V	4 mV / 3.8 V
Load Reg.	19 mV / 50mA	12 mV / 30 mA	19 mV / 50mA
$V_{drop-out}$ @ 60mA	232 mV	280 mV	232 mV
R_{on}	3.9 Ω	4.7 Ω	3.9 Ω
ΔV_o for I_{Load}=pulse (0 to 50mA)	19 mV	19 mV	148 mV
V_{offset} @ I_{Load}=1mA	4 mV	4 mV	4 mV
Chip area (not including schottky diode)		1103 µm x 1250 µm	

approximately between 0.9 and 1.1 V in most of today's standard technologies.

The theoretical headroom limit of low voltage for the MOSIS 2-μm n-well technology with an added p-base layer is roughly 1–1.1 V (corresponding to $V_{\text{sg-pmos}} + V_{\text{ds-nmos}}$). The threshold voltage of MOS devices is roughly between 0.88 and 0.9 V. The same process technology also offers vertical NPN transistors; however, the respective saturation voltage is large as a consequence of high collector series resistance. The absence of a highly doped buried layer prevents this series resistance from decreasing to more favorable levels. Consequently, NPN saturation voltages are avoided in transistor stacks that define the low voltage headroom limit. The circuit design of the amplifier can be partitioned into the output buffer and the gain stage.

The idea of the buffer is to isolate the large capacitor associated with the gate of the power PMOS transistor from the large resistance of the output of the gain stage. As a result, the buffer needs low input capacitance and low output impedance. Furthermore, the output voltage swing needs to extend from as low as possible to the point where the pass device is shut off ($V_{\text{ds}} \leq V_{o\text{-swing}} \leq V_{\text{in}} - 0.7$ V). The lower limit is defined to provide maximum gate drive for the pass element (PMOS transistor). On the other hand, the upper limit is set by the voltage necessary to shut off the pass device, in other words, extend to just beyond the threshold voltage. This can be accomplished by a class "A" NPN emitter follower stage. This assumes that the output swing of the gain stage includes the positive power supply, approximately $V_{\text{in}} - V_{\text{sd}}$.

The gain stage of the amplifier needs a relatively small common-mode range and an output swing that includes the positive supply voltage. The common-mode range is defined around the reference voltage (V_{ref}), which, in turn, can be designed to be almost any value [12]. The low-voltage, current-mode bandgap reference topology of [13] illustrates how this can be done. As a result, the best device choice for a low-voltage differential pair is the NPN transistor (for the case of MOSIS). This is because its base-emitter voltage drop is roughly 0.6–0.7 V, whereas the gate-to-source voltage of MOS devices is approximately 0.9 V. Thus, a 0.85–0.9 V reference is necessary to accommodate the voltage headroom requirements of the NPN differential pair in a low voltage environment.

The choice of amplifier topology, however, is limited if the theoretical low voltage limit is to be approached ($V_{\text{sg}} + V_{\text{ds}}$). The single-stage, five-transistor amplifier shown in Fig. 8(a) is simple enough to yield good frequency response for a given amount of quiescent current flow. However, a regular current mirror load presents a problem for low-voltage operation. A regular mirror load, as seen in the figure, yields a transistor stack whose associated voltage drop is $V_{\text{sg}} + V_{\text{ce}} + V_{\text{ds}}$, which is limited by approximately 1.4–1.5 V in the MOSIS technology. Therefore, a different low-voltage mirror load that yields the theoretical low-voltage limit for the MOSIS technology is proposed ($V_{\text{sg}} + V_{\text{ds}} \approx$ 1–1.1 V), as illustrated in Fig. 8(b). It is basically a mirror with an emitter follower level shift. The circuit operates properly because

the base-emitter voltage drop of the NPN transistor is less than the source-to-gate voltage of the PMOS device. The current through the NPN transistor is designed such that the parasitic pole at the gate of the PMOS device is at high frequencies. This parasitic pole ($P_{\text{parasitic}}$) is approximated to be

$$P_{\text{parasitic}} \approx \frac{g_{m_{\text{npn}}}}{2\pi} \cdot \frac{1}{2C_{\text{gs}}} \tag{18}$$

where $g_{m_{\text{npn}}}$ is the transconductance of the NPN transistor and C_{gs} is the gate-to-source capacitance of each PMOS transistor in the mirror. Among the amplifiers in Fig. 8, this topology exhibits the best systematic offset performance because the voltages at the collector of both NPN transistors in the differential pair are the same, $V_{\text{in}} - V_{\text{sg}} + V_{\text{be}}$. This results because the voltage at the input of the buffer stage (or output of the gain stage) is defined by a PMOS pass device and an emitter follower, as seen in the current efficient buffer shown in Fig. 2. Another possible circuit topology for the amplifier is that of a folded architecture, Fig. 8(c). This circuit also works properly at the theoretical limit of $V_{\text{gs}} + V_{\text{sd}}$ (equivalent to $V_{\text{sg}} + V_{\text{ds}}$). However, systematic offset performance for this circuit is poor. Furthermore, bandwidth performance per given total quiescent current flow is not as favorable as that of the circuit shown in Fig. 8(b) because there are more current sensitive transistor paths to ground.

V. Experimental Results and Discussion

Fig. 9 illustrates the final integrated circuit design of the low-voltage, LDO regulator. The circuit was fabricated in MOSIS CMOS 2-μm technology with an added p-base layer. The Schottky diode was not included in the layout but instead implemented discretely. The aspect ratio of the power device Mpo is 30 kμm/μm. The LDO produced a maximum output current of 18 and 50 mA at input voltages of 1 and 1.2 V. The circuit achieved approximately a 65% output current improvement over its noncurrent boosted counterpart, as shown in Fig. 10. The quiescent current flow was 23 μA at zero load-current and 230 μA at 50 mA of load-current, illustrated in Fig. 11. The maximum quiescent current at full load was higher than expected by simulations, approximately 180 μA higher. This is because of the effects of the large voltage drop across the Schottky diode on the parasitic vertical PNP transistors inherent in the PMOS structure. This can be improved by increasing the diode's area and/or by placing a heavily doped buried layer (unavailable in MOSIS) underneath the power PMOS transistor. The line regulation performance of the LDO was 4 mV/3.8 V. Moreover, the circuit achieved a load regulation of 19 mV/50 mA. The drop-out voltage at 60 mA of load-current was 232 mV, which corresponds to a 17% improvement over its noncurrent boosted version, Fig. 12. Fig. 13 shows the maximum transient output voltage variation resulting from a sudden load-current pulse (zero to 50 mA), approximately 19 mV (83% improvement over the same circuit but without the aid of Mps in Fig. 9). The settling time of the LDO response without Mps is appreciably longer, illustrated by the large overshoot of trace A. This is attributed to decreased phase margin resulting from the parasitic pole being at low frequencies (consequence of low bias current through the emitter follower of the buffer). Table I gives a summary of the performance parameters of the low voltage LDO.

VI. Conclusion

A low-voltage, low quiescent current, low drop-out regulator has been designed and implemented. Low quiescent current flow is especially important in portable products where the total current drain determines battery life. The regulator worked down to 1 V yielding an output current of 18 mA with 23 μA of quiescent current at zero load-current. At 1.2 V, the circuit was able to provide 50 mA of output current with 230 μA of quiescent current. Two significant contributions, current efficient buffer and current boosted pass device, made the low-voltage design viable for battery powered circuits. Both techniques take advantage of the availability of a sense element that provides a linearly load dependent current. This is intrinsic for low quiescent current flow during low load-current conditions. The resulting circuit takes maximum advantage of the transistors utilized to yield low component count and low overall ground current. Furthermore, the current boosting technique can be readily implemented in applications requiring low switch-on resistors, i.e., dc-dc converters. In conclusion, some techniques have been developed and verified that allow the design of low drop-out regulators under existing technologies to meet today's and tomorrow's low-voltage market demands.

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Gabriel A. Rincon-Mora (S'91–M'97) was born in Caracas, Venezuela. He received the B.S.E.E. degree with high honors from Florida International University, Miami, in 1992 and the M.S.E.E. and Ph.D. degrees (named outstanding Ph.D. graduate) in electrical engineering from Georgia Institute of Technology, Atlanta, in 1994 and 1996, respectively.

He is presently working in the Linear Design Branch with Texas Instruments Incorporated, Dallas, TX. He has been involved in the design of BiCMOS power supply systems, i.e., references, linear and switching regulators, power drivers, and associated control and protection circuitry. His general technical interests include low-power and low-voltage analog and mixed-signal BiCMOS/CMOS circuit and system design. He has several patents as well as publications in the field of integrated circuit design.

Dr. Rincon-Mora is a member of Tau Beta Pi, Eta Kappa Nu, and Phi Kappa Phi.

Phillip E. Allen (M'62–SM'82–F'92) received the Ph.D. degree in electrical engineering from the University of Kansas, Lawrence, in 1970.

He presently is a Professor in the School of Electrical Engineering at Georgia Institute of Technology, Atlanta, and holds the Schlumberger Chair. He has worked for the Lawrence Livermore Laboratory, Pacific Missile Range, Texas Instruments, and consulted with numerous companies. He has taught at the University of Nevada at Reno, the University of Kansas, the University of California at Santa Barbara, and Texas A&M University. His technical interests include analog integrated circuit and systems design with focus on implementing low-voltage and high-frequency circuits and systems in standard CMOS technology. He is also involved in research to improve and enhance the teaching of undergraduate and graduate courses in analog circuits. He has over 40 refereed publications in the area of analog circuits. He has co-authored *Theory and Design of Active Filters* (1980), *Switched Capacitor Filters* (1984), *CMOS Analog Circuit Design* (1987), and *VLSI Design Techniques for Analog and Digital Circuits* (1990).