Design Techniques for Timing Circuits in Wireline and Wireless Communication Systems

DESIGN TECHNIQUES FOR TIMING CIRCUITS IN WIRELINE AND WIRELESS COMMUNICATION SYSTEMS

by

Deping Huang

A Dissertation Submitted to the Faculty of the

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

In Partial Fulfillment of the Requirements

For the Degree of

DOCTOR OF PHILOSOPHY

In the Graduate College

THE UNIVERSITY OF ARIZONA

2014

THE UNIVERSITY OF ARIZONA
GRADUATE COLLEGE

As members of the Dissertation Committee, we certify that we have read the dissertation

prepared by Deping Huang, titled

Design Techniques for Timing Circuits in Wireline and Wireless Communication Systems

and recommend that it be accepted as fulfilling the dissertation requirement for the Degree of Doctor of Philosophy.

_____ Date: 11/12/2014
Janet Meiling Roveda

_____ Date: 11/12/2014
David Cox

_____ Date: 11/12/2014
Hao Xin

_____ Date: 11/12/2014
Jeffrey Rodriguez

_____ Date: 11/12/2014

Final approval and acceptance of this dissertation is contingent upon the candidate's submission of the final copies of the dissertation to the Graduate College.

I hereby certify that I have read this dissertation prepared under my direction and recommend that it be accepted as fulfilling the dissertation requirement.

_____ Date: 11/12/2014
Dissertation Director: Janet Meiling Roveda

STATEMENT BY AUTHOR

This dissertation has been submitted in partial fulfillment of the requirements for an advanced degree at the University of Arizona and is deposited in the University Library to be made available to borrowers under rules of the Library.

Brief quotations from this dissertation are allowable without special permission, provided that an accurate acknowledgement of the source is made. Requests for permission for extended quotation from or reproduction of this manuscript in whole or in part may be granted by the head of the major department or the Dean of the Graduate College when in his or her judgment the proposed use of the material is in the interests of scholarship. In all other instances, however, permission must be obtained from the author.

SIGNED: Deping Huang

ACKNOWLEDGEMENTS

This work would not have been possible without the help and support of many people. It is my pleasure to have this opportunity to acknowledge the inspiring and gracious individuals I have met during my doctoral studies.

First of all, I would like to express my sincere appreciation to my advisor, Dr. Janet Meiling Roveda. I am thankful to her for having shared her knowledge and experience through my research work. Her encouragement and guidance have been of great help for me to complete my doctoral studies and develop my future career goal. I am very grateful to have the opportunity to work with her and learn from her.

I would also like to thank all the dissertation committee members, Dr. David Cox, Dr. Hao Xin and Dr. Jeffrey Rodriguez for their continual support and encouragement. Their advice has been a great help to my research.

I am very thankful to my previous graduate advisor Wei Li at Fudan University. She is the one who first guided me to the field of PLL and taught me the art of analog IC design. Her dedication with research and courage has inspired and supported me throughout my doctoral studies.

I would like to extend my sincere gratitude to Dr. Ping Gui at Southern Methodist University. Her constructive comments and insightful suggestions played an important role in my research. She is also a great friend who always shows great care and support when I run into difficulties.

All my colleagues and friends at The University of Arizona and Southern Methodist University have made my past four years a memorable experience in my life. I would like to thank Rui Wang, Yang You, Guoying Wu, Xiaoke Wen, Lei Chen, Jingxiao Li, Siyu Wang, Seok Min Jung, Long Huang, Yue Yu and Chen-Wei Huang for many interesting discussions and great helps on my research and life.

I would like to thank Jinghong Chen for his support and helpful suggestions in my research. I would like to acknowledge TxACE/SRC for funding of the CDR project and Texas Instruments for chip fabrication. I would also like to take this opportunity to show my gratitude to Sudipto Chakraborty, Yanli Fan, Mark Morgan, Huawen Jin, Yuxiang Zhen, Richard Gu and Archie. Hu. They are the great people I met during my internship at Texas Instruments. They have provided great help and beneficial discussions for my research.

Finally, my deepest gratitude goes to my mother, my father and my two lovely sisters. My love for them is beyond words and will last forever.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

GLOSSARY

AFC	AFC refers to automatic frequency calibration. It is a circuit in the frequency synthesizer for oscillator tuning curve selection.
DLL	DLL refers to delay-locked loop. It is a circuit which is used to change the phase of a clock signal.
FLL	FLL refers to frequency locking loop. It is a circuit that locks the frequency of an oscillator, which is also controlled by a PLL, to the desired value.
JGEN	JGEN refers to jitter generation. It is the jitter generated by CDR itself in the absence of jitter in the input data.
JTOL	JTOL refers to jitter tolerance. It indicates the CDR data recovery performance when the input data is phase modulated.
JTRAN	JTRAN refers to jitter transfer. It quantifies the jitter filtering effect of the CDR.
K28.7	K28.7 is a special data pattern in the 8B/10B coding table.
SAR	SAR refers to successive approximation register. It is a counter circuit that counts by trying all values of bits starting with the most-significant bit and finishing at the least-significant bit.
TDC	TDC refers to time-to-digital converter. It is a circuit that quantizes the phase difference of the input clocks into digital value.
TVC	TVC refers to time-to-voltage converter. It is used to convert the phase difference of the input clocks into voltage.

ABSTRACT

Clock and data recovery (CDR) circuit and frequency synthesizer are two essential timing circuits in wireline and wireless communication systems, respectively. With multi-gigabits/s high speed links and emerging 4G wireless system widely used in communication backbone infrastructures and consumer electronic devices, effective design of CDR and frequency synthesizer has become more and more important. The advanced scaled-down CMOS process has the limitations of leakage current, low supply voltage and process variation which pose great challenge to the analog circuit design. To overcome these issues, a digital intensive CDR solution is needed. Besides, it is desirable for the CDR to cover a wide range of data-rate and to be reference-less for improved flexibility. As for the frequency synthesizer design, the support for multi-standard to reduce the cost and area is desirable.

In this work, a digital reference-less CDR is proposed to support continuous data-rate ranging from 1 Gbps to 16 Gbps. The CDR adopts an 8 GHz~16 GHz DCO to achieve low random noise performance. A reference-less digital frequency locking loop is included in the system as the acquisition assistance for the CDR loop. To address the difficulty of jitter and stability evaluations for bang-band CDR, a Simulink model is developed to find out the jitter transfer (JTRAN), jitter generation (JGEN) and jitter tolerance (JTOL) performances for the CDR. The prototype CDR is implemented in a 65 nm CMOS process. The core area is 0.68 mm^2. At 16 Gbps, the CDR consumes a power of 92.5 mW and is able to tolerate a sinusoidal jitter with an amplitude of 0.4 UI and a frequency of 4 MHz.

The second part of this dissertation develops a frequency synthesizer for multi-standard wireless receivers. The frequency synthesizer is based on an analog fractional-N PLL. Optimally-coupled quadrature voltage-controlled-oscillator (QVCO), dividers and harmonic rejection single sideband mixer (HR-SSBmixer) are combined to synthesize the desired frequency range without posing much phase noise penalty on the QVCO. The QVCO adopts a new phase-shift scheme to improve phase noise and to eliminate bimodal oscillation. Combining harmonic rejection and single sideband mixing, the HR-SSBmixer is developed to suppress spurious signals. Designed in a 0.13-μm CMOS technology, the synthesizer occupies an active area of 1.86 mm^2 and consumes 35.6 to 52.62 mW of power. Measurement results show that the synthesizer frequency range, the phase noise, the settling time and the spur performances meet the specifications of the wireless receivers for the above standards.

For a wide range frequency synthesizer, an automatic frequency calibration circuit (AFC) is needed to select proper oscillator tuning curve before the PLL settling. An improved counter-based AFC is proposed in this dissertation that provides a more robust and faster tuning curve searching process. The proposed AFC adopts a time-to-digital converter (TDC), which is able to captures the fractional VCO cycle information within the counting window, to improve the AFC frequency detection accuracy. The TDC-based AFC is designed in a 0.13-μm CMOS technology. Simulation results show that the TDC-based AFC greatly improves the frequency detection accuracy and consequently for a given frequency detection resolution reduces the AFC calibration time.

CHAPTER 1. INTRODUCTION

1.1 Motivation

Wireline and wireless communication technologies have been the driving force of the information technology revolution. The evolving portable consumer electronics such as laptops, tablet computers, smart phones and wearable devices benefitting the most from the revolution have gradually become commonplace. Integrated systems are the key to the advancement of these commodities. The ever-growing communication traffic leads to higher requirements on the data transfer rate and the number of end users that the devices or the backbone infrastructures can support.

In wireline communication systems, the speed of I/O interfaces is the bottleneck of the system data transfer rate. For communication speeds of 2.5 Gbps and higher, the dominant implementation of I/O interfaces is the high-speed serializer/deserializer devices which only transfer data in the channel and rely on a clock and data recovery circuit to determine the optimal sampling point in the receiver side for the locally generated clock.

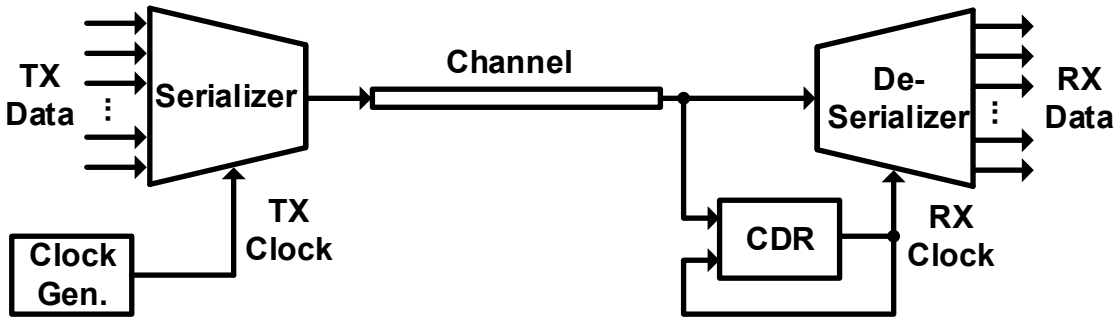


Fig. 1.1: Block diagram of a high speed wireline communication system.

Fig. 1.1 illustrates a simplified block diagram of the high speed wireline communication system. Data to be sent are bundled into a high speed stream in the

transmitter. In the receiver, the CDR dynamically aligns the received data with the sampling clock to recover the transmitted data. As the data-rate increases, the speed as well as the jitter requirement for the CDR also increases. For the last two decades, analog phase lock loop (PLL) has been widely used in CDR circuits to meet the high performance requirements. However, as the CMOS technology scales down, the limitations such as leakage current, low supply voltage, process variation pose great challenge to the analog circuit design. To overcome these limitations, digital PLL has been proposed to replace its analog counterpart [1] [2] [3]. Unlike the analog loop filter, the digital loop filter in the digital PLL does not have the problem of leakage current. Further, digital intensive circuit such as digital PLL is more tolerable to process variation, and scalable and portable across standard digital processing technologies. Therefore, the study of the digital intensive solution for CDR circuits is in great demand.

For wireless communication systems, the integration of multiple standards into a single chip is an important step toward Software-Defined Radio (SDR). The most commonly used wireless communication standards include cellular communication standards such as GSM, WCDMA and LTE and short range communication standards such as Bluetooth and WLAN. The emergence of multiple communication standards adopted in different country areas around the world inspires the study of multi-mode RFIC solutions to reduce chip area, power and increase competitiveness of the new devices [4]. Fig. 1.2 illustrates a direct conversion wireless receiver architecture. Wireless signal is received by the antenna and amplified by the low noise amplifier (LNA). The mixer is responsible for signal frequency down-conversion. The local oscillator (LO) signal for the mixer is provided by the frequency synthesizer. The low pass filter (LPF) removes unwanted

frequency components from the signal and maintains the baseband information. The variable gain amplifier adjusts the signal amplitude to accommodate the ADC dynamic range. Then the ADC converts the analog received signal into digital signal which is further processed by the digital baseband circuit for demodulation.

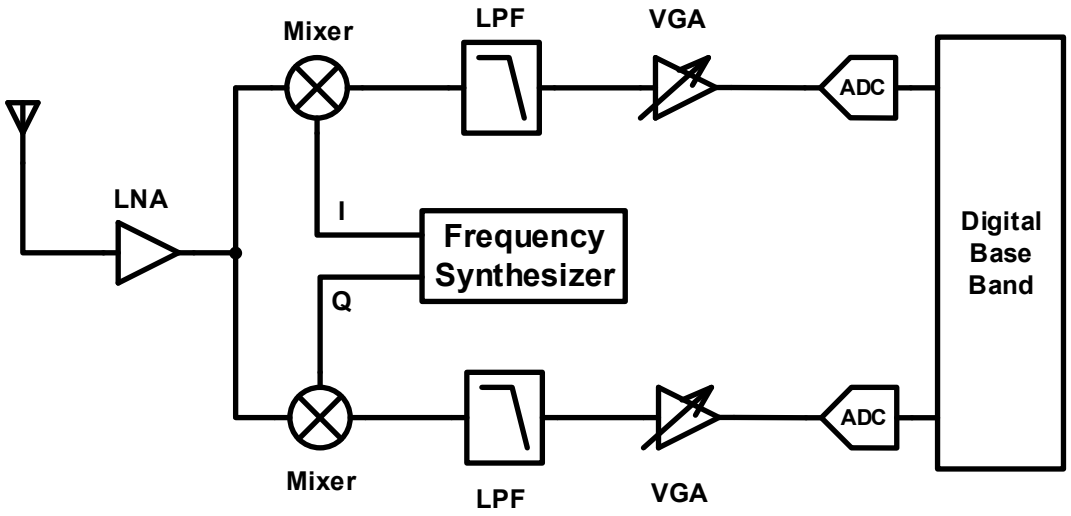


Fig. 1.2: Block diagram of a direct conversion receiver.

One of the challenging blocks of such a radio supporting multiple standards is the frequency synthesizer that needs to generate clean and stable LO signals fulfilling the requirements of the major wireless communication standards. To support multiple standards, the frequency synthesizer needs to have a wide frequency tuning range. However, this conflicts with the stringent phase noise requirements of some standards such as GSM. Design techniques that balance programmability, electrical performance and cost need to be studied.

1.2 Research Contribution

This research investigates a digital reference-less clock data recovery circuit for multi-Gigabit/s serial link and frequency synthesizer circuits for multi-standard wireless communications. The thesis mainly focuses on the design techniques that balance the circuit performance and the application generosity for the CDR and the frequency synthesizer. The contributions of this work are summarized as follows:

1) Proposes a continuous rate digital reference-less CDR that is able to support multiple wireline communication protocols. Explores the design and simulation techniques of the digital non-linear CDR.

2) Proposes a frequency synthesizer for cellular and short range communication standards. Studies the optimal quadrature VCO design technique and application of harmonic-rejection technique to frequency synthesis.

3) Proposes a robust AFC technique for multi-standard frequency synthesizers. Analyzes the conventional AFC techniques and provides a general design guideline for AFC circuits. Gives the improved solution.

1.3 Dissertation Organization

This dissertation is organized as follows:

Chapter 2 reviews the background of timing circuits in wireline and wireless communication systems. The analysis provides a discussion on three basic structures of CDR, CDR jitter performance, architecture of PLL-based frequency synthesizer and AFC circuits.

Chapter 3 presents the proposed digital PLL-based reference-less CDR. Design of wideband digital controlled oscillator and digital reference-less frequency locking loop are discussed. The analysis and simulation of the non-linear CDR loop are developed. Implemented in a 65 nm CMOS process, the CDR is verified by simulations.

Chapter 4 describes the proposed frequency synthesizer for multi-standard wireless receivers. The specification and architecture design of the synthesizer are discussed. The circuit is designed in a 130 nm CMOS process with experimental verifications.

Chapter 5 explores the design technique for AFC circuit in wide-range frequency synthesizers. A design guide line is developed for the counter-based AFC. And TDC-based AFC is proposed to improve the AFC accuracy and robustness. Circuits are designed in a 130 nm CMOS process and verified by simulations.

Chapter 6 summarizes this research and discusses the future work.

CHAPTER 2. TIMING CIRCUITS FOR WIRELINE AND WIRELESS COMMUNICATIONS

2.1 Clock and Data Recovery Circuit

2.1.1 Architectures of Clock and Data Recovery

CDR circuit is an essential block for high speed wireline communication systems such as optical links, backplane channel and chip to chip interconnect. In such systems, CDR generates a clock that is aligned to the incoming data and recovers the transmitted data from the distorted received signal. Feedback phase tracking is the most commonly used CDR topology that helps to achieve these targets. Based on the approach of phase adjustment within the CDR, the topology can be categorized as DLL-based CDR, PLL-based CDR and DLL/PLL-based CDR.

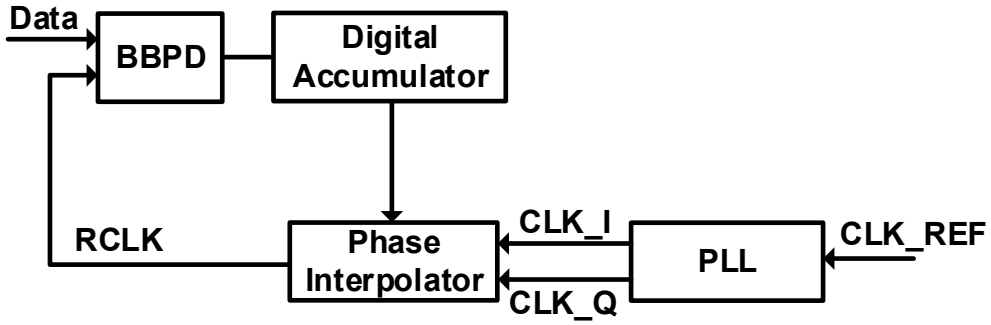


Fig. 2.1: DLL-based CDR.

Fig. 2.1 shows a digital DLL-based CDR [5] [6]. The DLL-based CDR directly adjusts the clock phase via a phase interpolator or a voltage controlled delay line. DLL is a first order system, so it is unconditionally stable. However, the DLL is not capable to do clock synthesis and it only performs phase alignment. Thus, a PLL is needed to generate

clocks for the phase interpolator in the DLL. This architecture is commonly used in multi-channel systems where the PLL can be shared by channels. As the PLL requires a reference clock for clock generation, the DLL-based architecture is not suitable for reference-less CDR design. Further, for single channel applications, it is more cost-effective to perform the clock generation and the phase alignment by a single loop which is the case in the PLL-based CDR.

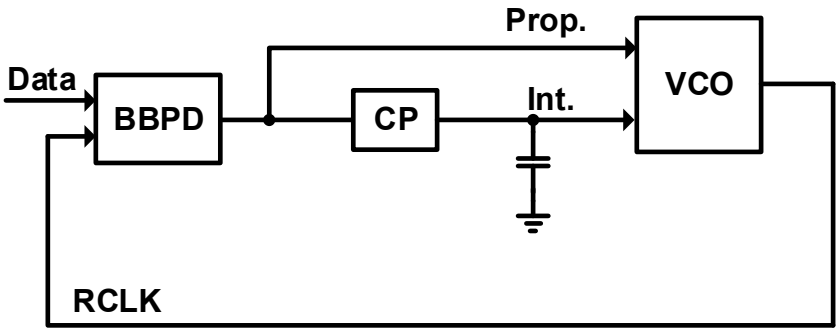


Fig. 2.2: PLL-based CDR.

Fig. 2.2 shows a PLL-based CDR where the clock phase adjustment is carried out by tuning the VCO frequency [7] [8] [9]. There are two tuning paths for the VCO in the PLL. One is the proportional path which is responsible for phase tracking. The other one is the integral path which is used for slow input jitter tracking and frequency locking. The PLL-based CDR does not require a reference clock, thus it is a possible solution for the reference-less CDR design. Compared to the DLL-based CDR, the PLL-based CDR is a single loop topology, therefore consumes less power especially for a single-link system where only one CDR is needed.

The third feedback phase tracking topology is the DLL/PLL-based CDR where the phase tracking is jointly performed by a phase shifter and a VCO [10] [11]. The loop that

contains the phase shifter is the DLL loop where part of the phase error is neutralized. The PLL, on the other hand, eliminates the residual phase error by adjusting the VCO frequency in such a way that its phase is aligned to the data at the phase shifter output. The benefit of splitting the phase adjustment into two loops is that the jitter transfer and jitter tolerance can be de-coupled [11]. As can be seen in Fig. 2.3, the input jitter tracking is completed by two loops and the tracking bandwidth is determined by the fast loop--DLL. The recovered clock, on the other hand, is controlled by the PLL which is only able to pass through slow jitter. In fact, to keep the overall system stable, the PLL bandwidth should be much smaller than the DLL bandwidth [7]. Therefore, the DLL/PLL CDR achieves the best jitter performance in the above there topologies. It is also a possible solution for the reference-less CDR design as no reference clock is needed. However, its power consumption is higher than the PLL-based CDR. Especially for the input with a wide range of data rate, the design of a phase shifter that covers a wide range of tunable delay becomes very challenging and power consuming.

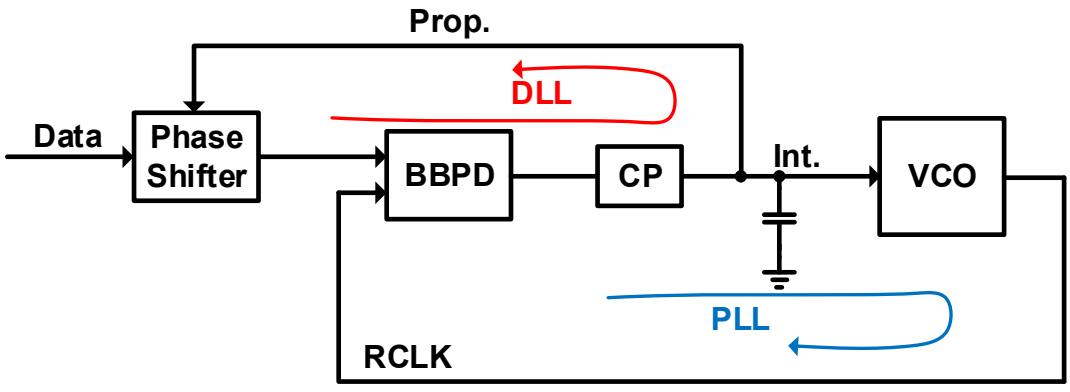


Fig. 2.3: DLL/PLL-based CDR.

2.1.2 Jitter Performance of Clock and Data Recovery

Jitter is the deviation in arrival time of a signal from its ideal or expected arrival time. As can be seen in Fig. 2.4, jitter in a clock signal represents the deviation of the zero crossings from their ideal position in time. The origin of this timing uncertainty can either be deterministic or random. Deterministic jitter (DJ) has a non-Gaussian distribution and is always bounded in amplitude. It is quantified by peak-to-peak value of the jitter. Random jitter (RJ) follows a Gaussian distribution. It is quantified using the standard deviation of the distribution, *i.e*. RMS value.

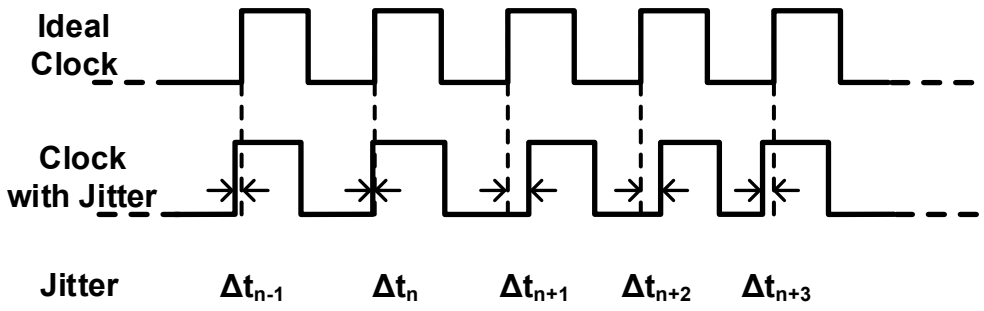


Fig. 2.4: Jitter on a clock signal.

The total jitter (TJ) in a practical system is usually composed of RJ and DJ. TJ is generally specified as a peak-to-peak value and is related to the target bit error rate (BER) of the serial link. It can be quantified by the following equation.

$$TJ_{PP} = DJ_{PP} + Q_{BER} RJ_{RMS} \tag{2.1}$$

where DJ_{pp} is the peak-to-peak value of the deterministic jitter; RJ_{RMS} is the standard deviation of the random jitter; Q_{BER} specifies the amount of eye closure due to random jitter that we must account for at a given *BER*. A common *BER* in wireline communication standards is 10^{-12}. The corresponding Q_{BER} is 14.

CDR recovers data from the received signal with jitter. The clock generated by the CDR also has a certain amount of jitter. The *BER* related to the data recovery operation is affected by the CDR jitter performance which is characterized by JTRAN, JGEN and JTOL.

2.1.2.1 JTRAN

JTRAN quantifies the jitter filtering effect of the CDR. It is the ratio of output to input jitter as a function of frequency. For CDR implemented by a linear loop, it is the same as the system transfer function from the input to the output. The JTRAN of the CDRs discussed in the previous section exhibits a low-pass characteristic. Therefore, slow jitter in the data passes through without attenuation allowing it being tracked by the sampling clock. On the other hand, high frequency jitter is filtered and may cause sampling error if its amplitude is large enough. The jitter transfer function of a CDR is shown in Fig. 2.5.

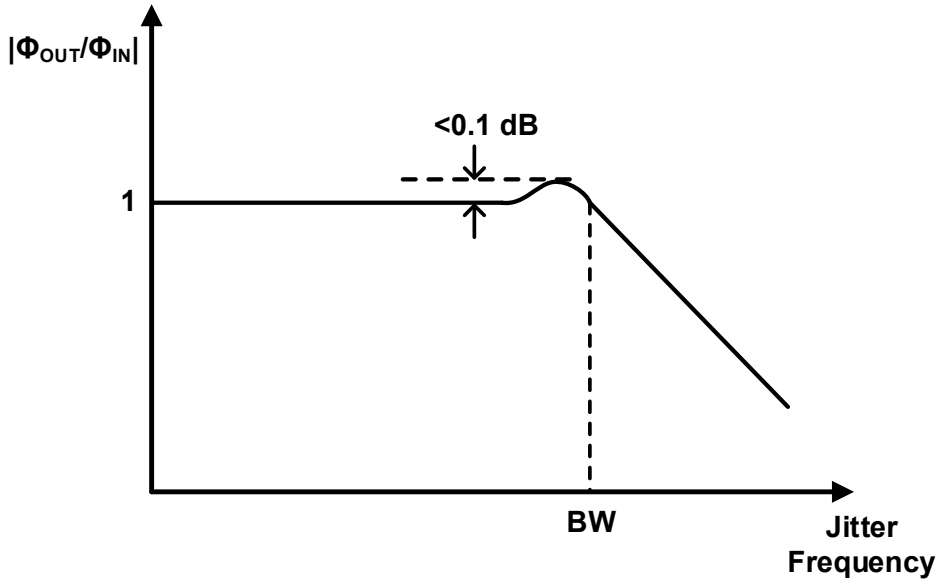


Fig. 2.5: Jitter transfer of a CDR.

At low frequency, the CDR output tracks its input. Therefore, the ratio of the output phase over the input phase at low frequency is 1. As the jitter frequency increases and becomes higher than the CDR loop bandwidth, the CDR loop cannot respond fast enough to the input, then the output tracks the input to a less extent. Therefore, the JTRAN starts to roll off. The JTRAN bandwidth is an important specification which determines the CDR loop parameter design. Another specification in the JTRAN is jitter peaking. When the CDR is implemented with the PLL-based architecture or a jitter-cleaning-PLL is used for the recovered clock, the zero in the PLL close loop transfer function causes jitter peaking. Long-haul communications require a strict control of jitter peaking to prevent jitter accumulation through the repeaters along the links. For example, Synchronous Optical Network (SONET) requires the CDR to have a jitter peaking less than 0.1 dB.

2.1.2.2 JGEN

JGEN is the jitter generated by CDR itself in the absence of jitter in the input data. The CDR jitter is also composed of RJ and DJ. The random jitter sources include VCO phase noise, charge pump current noise, thermal noise of the loop filter resistor and power supply noise. The deterministic jitter comes from the limit cycle oscillation when the bang-bang phase detector is used. JGEN of a CDR can be measured with an oscilloscope in the time domain or a spectrum analyzer in the frequency domain. The relationship between absolute jitter $Jitter_{\text{abs}}$ acquired by the oscilloscope and phase noise $L(\text{f})$ acquired by the spectrum analyzer is given by (2.2).

$$Jitter_{abs} = \left(\frac{T_0}{2\pi} \right)^2 \int_0^{\infty} 2L(f)df \tag{2.2}$$

where T_0 is the clock period.

2.1.2.3 JTOL

JTOL indicates the CDR data recovery performance when the input data is phase-modulated. It is measured by observing the data recovery *BER* under the condition of sinusoidal jitter of various magnitudes and frequencies applying to the input data. The JTOL specification is described by a mask as a function of jitter frequency. If the CDR jitter transfer function is available, then the JTOL can be derived as follows.

To guarantee no data sampling error, the phase error between the clock and the data should be smaller than 0.5 UI.

$$\phi_{in} - \phi_{out} < 0.5\ UI \tag{2.3}$$

Replace the output phase Φ_{out} with Φ_{in} and the jitter transfer function H(f).

$$\phi_{in}(1 - H(f)) < 0.5\ \text{UI} \tag{2.4}$$

Then, the input phase boundary that guarantees no bit error as a function of frequency is

$$\phi_{in} < 0.5/(1 - H(f)) \tag{2.5}$$

The right term in (2.5) is the CDR JTOL. For a typical jitter transfer function shown in section 2.1.2.1, H(f) is equal to 1 at low frequency and starts to roll off as the frequency becomes higher than the CDR bandwidth. Therefore, the CDR JTOL curve descends from infinite at DC and starts to flatten out at the bandwidth frequency. The boundary set by (2.5) needs to be larger than the JTOL mask specification. Fig. 2.6 shows the JTOL of a Type-II 2$^{\text{nd}}$-order PLL-based CDR and a typical JTOL mask.

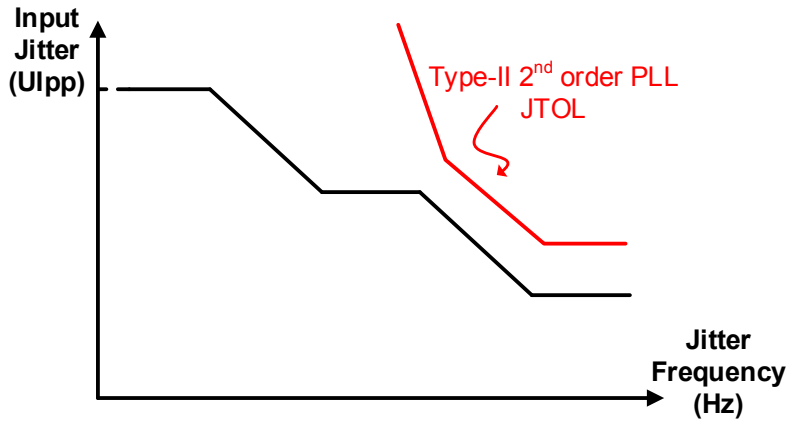


Fig. 2.6: JTOL of a Type-II 2nd-order PLL-based CDR and a typical JTOL mask.

Notice that the above derivation is only valid when the jitter transfer function is available. For CDR with a non-linear PD, the JTOL cannot be expressed explicitly with an equation. In that case, the JTOL should be acquired by simulations.

2.2 Frequency Synthesizer for Wireless Applications

2.2.1 PLL-based Frequency Synthesizer

A frequency synthesizer is a device that generates any range of frequencies from one or a few frequency sources. Frequency synthesizer can be implemented with direct synthesis topology such as direct digital synthesizer (DDS) or indirect synthesis topology such as PLL-based frequency synthesizer and DLL-based frequency synthesizer. Among them, the PLL-based frequency synthesizer is the most widely used as a communication system IC building block. It serves as an LO for the transmitters and receivers. The LO generates carrier signals which are used for signal spectrum up-conversion and down-conversion.

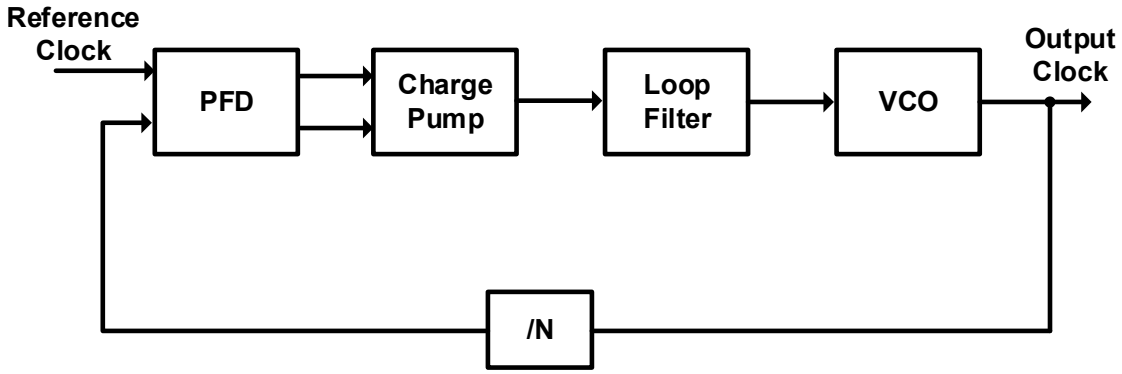


Fig. 2.7: Block diagram of a PLL-based frequency synthesizer.

As can be seen in Fig. 2.7, the PLL is composed of phase frequency detector (PFD), charge pump (CP), loop filter (LF), VCO and frequency divider. The input of the PLL-based frequency synthesizer is a reference clock which is usually generated by a crystal oscillator. The reference clock is characterized with high accuracy but low frequency. The free-running VCO can generate a high frequency clock but its accuracy is much worse than the reference clock. When the VCO is placed at the PLL, its output phase is locked and regulated by the reference clock via the PLL feedback loop. Therefore, the PLL is able to generate an accurate high frequency clock.

The division ratio of the frequency divider in Fig. 2.7 is usually programmable. So the output clock frequency can be adjusted by changing the feedback division ratio. The relationship between the reference clock frequency and the output clock frequency is given by (2.6).

$$f_{out} = Nf_{ref} \tag{2.6}$$

For an integer-N frequency divider, the frequency resolution of the synthesizer is equal to the reference frequency f_{ref} which should be at least 10 times of the PLL bandwidth

to keep the loop stable [12]. The PLL bandwidth is determined by the settling time requirement while the specification of frequency resolution is determined by the channel space of the communication standard. The two requirements may conflict with each other for some standards. In order to improve the PLL frequency resolution without reducing the reference clock frequency, the fractional-N PLL architecture can be used.

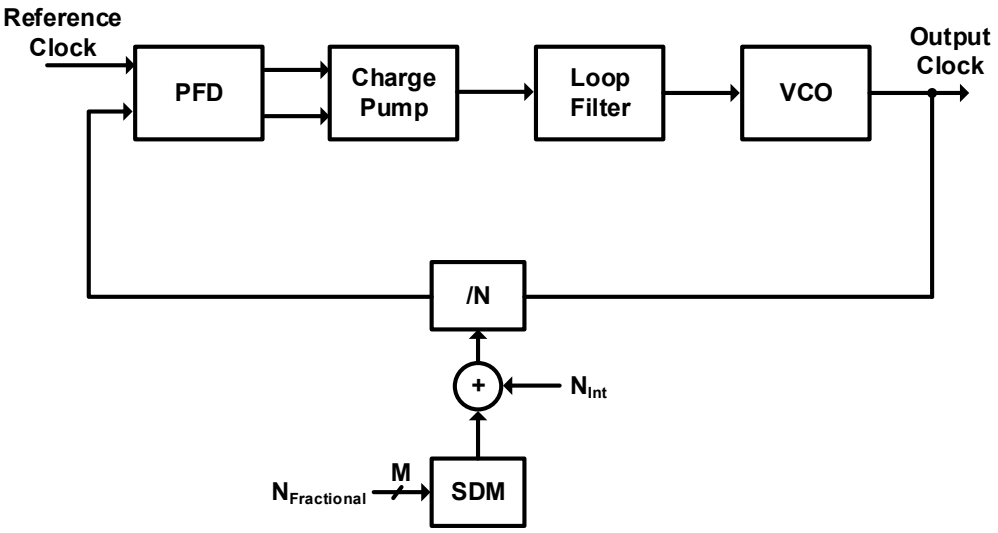


Fig. 2.8: Block diagram of a fractional-N frequency synthesizer.

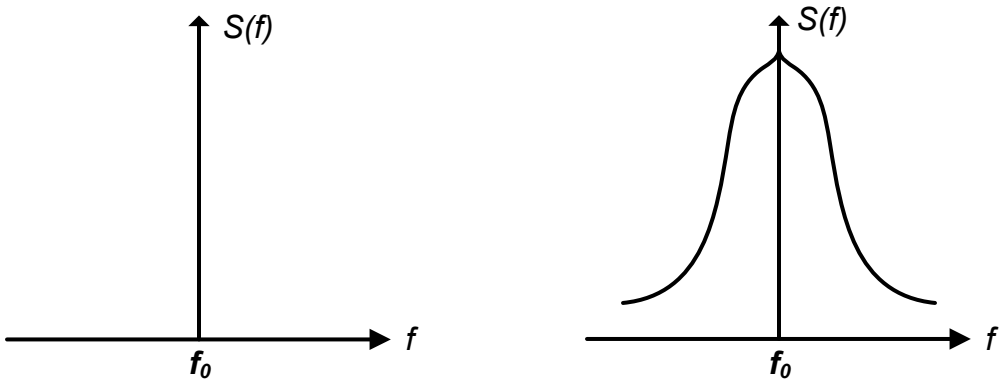
Fig. 2.8 shows the block diagram of a fractional-N frequency synthesizer. The feedback division ratio in the fractional-N frequency synthesizer is not fixed but dynamically adjusted by a digital sigma-delta modulator (SDM). The SDM dithers the programmable divider in such a way that its average division ratio is equal to the desired value. The frequency quantization noise due to dithering is high-pass-shaped. Therefore, the loop filter can extract the average division ratio information by low-pass filtering the charge pump output and suppress the quantization noise at high frequency. The relationship between the reference clock frequency and the output clock frequency of the fractional-N frequency synthesizer is given by (2.7).

$$f_{out} = (N_{Int} + k / 2^{M}) f_{ref} \tag{2.7}$$

where N_{Int} is the integer part of the desired division ratio; M is the SDM input word length; k is the binary representation of the fractional part of the desired division ratio. The frequency resolution of the fractional-N frequency synthesizer depends on the SDM input word length and is much higher than that of the integer-N frequency synthesizer.

2.2.2 Phase Noise of PLL-based Frequency Synthesizer

Phase noise is the frequency domain representation of random fluctuations in the phase of a waveform. For an ideal clock signal whose frequency is f_0, its spectrum contains no energy at any frequency other than f_0. However, due to random or deterministic disturbances from the electronic circuits, the realistic clock spectrum exhibits "skirts" around the carrier frequency and spreads into nearby frequencies. Fig. 2.9 illustrates an ideal clock spectrum and a realistic clock spectrum.



(a) (b)

Fig. 2.9: Spectrum of (a) ideal clock (b) realistic clock.

The phase fluctuation manifests itself in the time domain as jitter which has been discussed in section 2.1.2. For frequency synthesizers in wireless communications, it is more useful to treat its output clock phase uncertainty in the frequency domain. That is because the clock signal is fed to the mixers in the wireless transceiver for frequency down-conversion or up-conversion. The "skirts" in the clock spectrum contaminates the mixer output by down-converting or up-converting undesired signals from other channels. By quantifying the phase fluctuations in the frequency domain, the signal-to-noise degradation due to the "skirts" can be conveniently evaluated.

The mathematical representation of a realistic clock signal is given by (2.8).

$$V(t) = V_0 \cos[2\pi f_0 t + \phi_n(t)] \tag{2.8}$$

where V_0 is the clock signal amplitude; $\Phi_n(t)$ is the phase fluctuation. For a small value of phase fluctuation, $|\Phi_n(t)| \ll 1$ rad, (2.8) can be simplified as

$$V(t) \approx V_0 \cos(2\pi f_0 t) - V_0 \phi_n(t) \sin(2\pi f_0 t) \tag{2.9}$$

It can be seen in (2.9) that the spectrum of $\Phi_n(t)$ is up-converted to $\pm f_0$. The phase noise $L(\Delta f)$ is quantified by normalizing the average noise power in a 1-Hz bandwidth at an offset frequency Δf from f_0 of the "skirts" to the carrier power. From (2.9), it can be derived that

$$L(\Delta f) = 10 \log_{10}(S_{\Phi_n}(\Delta f)/2) \tag{2.10}$$

where $S_{\Phi n}(\Delta f)$ is the single sideband power spectral density (PSD) of $\Phi_n(t)$.

The phase noise performance of a PLL-based frequency synthesizer can be found using the PLL linear phase noise model. The noise generated by each building block in a

PLL is first acquired via circuit simulation. Then all the noise contributions are mapped to the PLL output and summed using the s-domain linear model shown in Fig. 2.10.

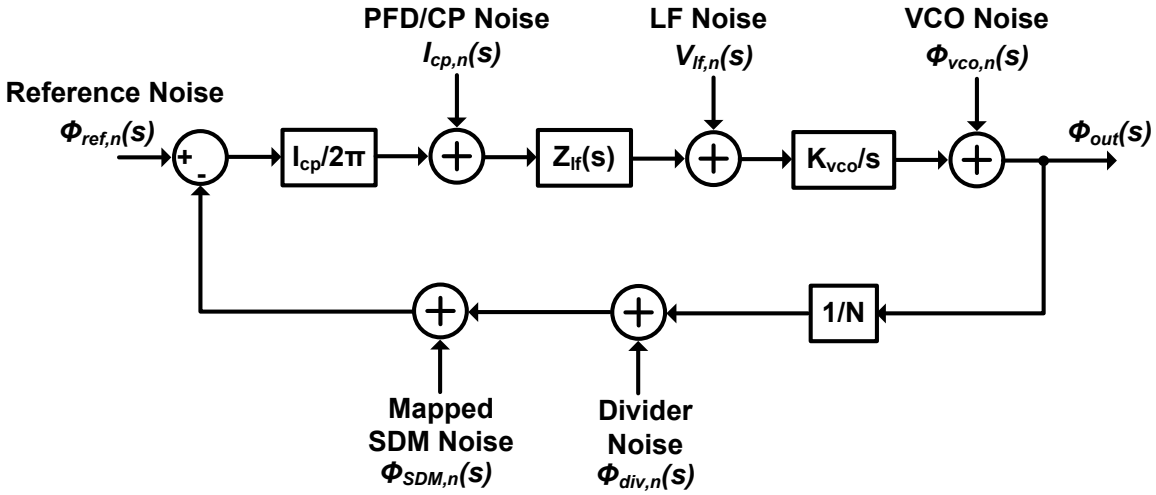


Fig. 2.10: Linear phase noise model of the fractional-N frequency synthesizer.

The noise transfer function for each noise source in Fig. 2.10 is summarized in Table 2.1.

Table 2.1: PLL noise transfer functions

Noise source	Noise transfer function		
Reference noise	$\Phi_{out}(s)/\Phi_{ref,n}(s)$	$N\dfrac{H_{open}(s)}{1+H_{open}(s)}$	Low-pass
PFD/CP noise	$\Phi_{out}(s)/I_{cp,n}(s)$	$\dfrac{2\pi N}{I_{cp}}\dfrac{H_{open}(s)}{1+H_{open}(s)}$	Low-pass
LF noise	$\Phi_{out}(s)/V_{lf,n}(s)$	$\dfrac{K_{vco}}{s}\dfrac{1}{1+H_{open}(s)}$	Band-pass
VCO noise	$\Phi_{out}(s)/\Phi_{vco,n}(s)$	$\dfrac{1}{1+H_{open}(s)}$	High-pass
Divider noise	$\Phi_{out}(s)/\Phi_{\mathrm{div},n}(s)$	$-N\dfrac{H_{open}(s)}{1+H_{open}(s)}$	Low-pass
SDM noise	$\Phi_{out}(s)/\Phi_{\mathrm{SDM},n}(s)$	$-N\dfrac{H_{open}(s)}{1+H_{open}(s)}$	Low-pass

$H_{open}(s)$ in Table 2.1 is the open loop transfer function of the PLL which is defined as

$$H_{open}(s) = \frac{I_{cp}}{2\pi} Z_{lf}(s) \frac{K_{vco}}{sN} \tag{2.11}$$

For a typical PLL frequency synthesizer, the in-band phase noise is usually dominated by the reference noise and the PFD/CP noise while the phase noise outside the bandwidth is dominated by the VCO phase noise. The PLL bandwidth should be carefully selected to balance the above noise contributions. In addition, the mapped sigma-delta noise is high-pass shaped, the PLL bandwidth should be small enough to suppress the SDM noise and to keep it smaller than the VCO phase noise contribution.

2.2.3 Automatic Frequency Calibration for Wide-Range Frequency Synthesizers

Frequency synthesizers for wireless communications usually adopt LC-oscillator as the VCO due to its lower phase noise compared to the ring-oscillator. For frequency synthesizers which are required to cover a wide frequency range, switched capacitor array is often utilized in designing the wideband LC-VCO. In this approach, a fixed varactor or a varactor array is continuously tuned by an analog control voltage to achieve fine frequency tuning, while the switched capacitor array is digitally controlled to carry out coarse frequency tuning. In doing so, a wide frequency range can be accomplished by multiple VCO tuning curves with each of them exhibiting a relatively smaller VCO transfer gain K_{vco}, thus improving the VCO noise performance. In this approach, an AFC circuit is required to properly select one of the VCO tuning curves at the startup of the phase locking process.

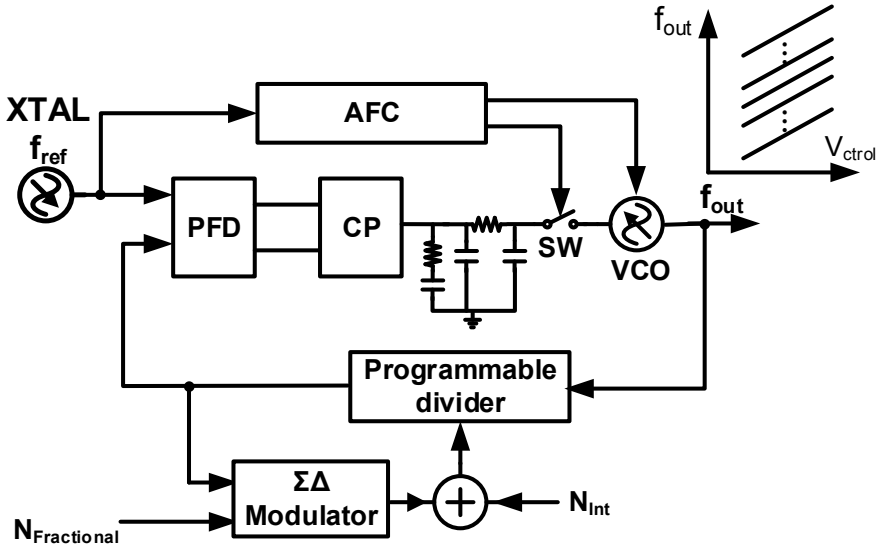


Fig. 2.11: Block diagram of a fractional-N PLL with an AFC loop.

One method to select the proper tuning curve is to monitor the VCO control voltage V_{ctrol} [13]. When the correct tuning curve is selected, the V_{ctrol} should be within a pre-defined voltage range. However, in this method the PLL must be settled first before one can monitor the V_{ctrol} voltage and each of the VCO tuning curves has to be examined. If the tuning curve being examined is not the correct one, the V_{ctrol} will be pushed to either VDD or VSS causing the PLL to be operated in the non-linear region. This makes binary search impossible leading to a long calibration time. This approach can hardly be used in systems such as GSM and Bluetooth, where the frequency synthesizers have a stringent settling time requirement. Another widely used method is to design a dedicated AFC loop as shown in Fig. 2.11 for coarse frequency calibration [14] [15] [16] [17] [18] During the AFC process, the VCO control node is disconnected from the loop filter and is set at half of the VDD. The VCO frequency is then detected and compared with a reference signal. A binary search algorithm is commonly used in this approach to reduce the number of comparisons

and thus the calibration time. Depending on the frequency detection approach, the time-to-voltage converter (TVC)-based AFC [15] and the counter-based AFC [16] [17] have been previously designed.

2.2.3.1 TVC-based AFC

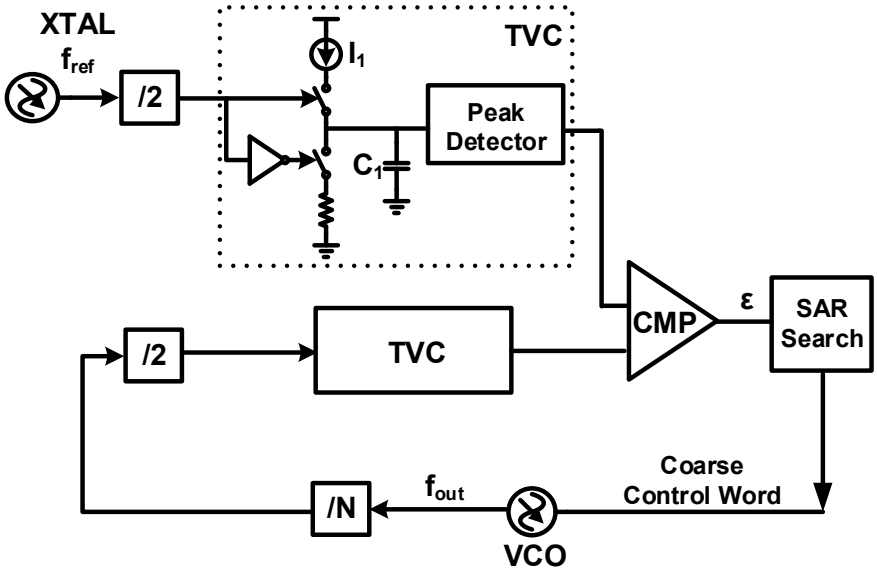


Fig. 2.12: TVC-based AFC.

The TVC-based AFC first converts the reference clock frequency and the VCO frequency into voltages and then performs the comparison in the analog domain. As can be seen in Fig. 2.12, the time-to-voltage converter is constructed by a charge pump and a peak detector [15]. The divide-by-2 circuits at the input of TVCs ensure that the signals entering the TVCs have 50% duty cycle. The positive or negative pulse at the TVC input represents one signal period, which is also the charging/discharging period of the charge pump. The peak voltage of the charge pump output signal is proportional to the input signal period and thus can serve as an indicator of the signal frequency. The comparator compares the peak

detector output and then feeds the result to a state machine to generate the final control word of the VCO.

Since the charge pump charging/discharging operation only takes several reference clock cycles to complete, the calibration time can be very small, often in the order of a few micro seconds. However, the correctness of the frequency comparison in this approach heavily depends on the matching performance of the analog circuit components. For example, assuming that the mid-frequencies of two consecutive VCO tuning curves are 4000 MHz and 4020 MHz, respectively, and the PLL division ratio is 100; then the difference of the two TVC input signal periods is about 124 ps. The corresponding voltage difference is calculated as $\Delta V = I_1 T / C_1 \times (\Delta T / T)$, where I_1 is the charge pump current, C_1 is the capacitance, T is the signal period and ΔT is the period difference, respectively. Notice that $I_1 T / C_1$ is the peak detector output and is limited by the supply voltage. With $I_1 T / C_1$=0.9 V, the comparator needs to detect an input voltage difference of 4.5 mV. This can hardly be satisfied without an offset calibration circuit. With the component mismatch, the requirement becomes even more severe. Although, the relative-period-based calibration technique is proposed in [15] to relax the component matching requirement by a factor of 2, the comparator offset still significantly limits the frequency detection resolution.

Another disadvantage of the TVC-based AFC is that the divider in the PLL loop can only work as an integer divider during the calibration process. With the loss of fractional component of the division ratio, the target frequency could be wrongly determined. As will be discussed in chapter 5, the inaccuracy of the target frequency in the AFC loop can cause a sub-optimal tuning curve selection.

2.2.3.2 Counter-based AFC

Fig. 2.13 shows the block diagram of the counter-based AFC. The PLL reference clock is divided down by a factor of 2^M and a half period of the divided-down signal is used as the counting interval. Thus, the length of the counting window is $2^{M-1} \times T_{ref}$, where T_{ref} is the period of the PLL reference clock. The result is then compared with the expected number of VCO cycles, which is $2^{M-1} \times N.\alpha$ where 2^{M-1} is the number of PLL reference clock cycles in the counting window and $N.\alpha$ is the division ratio of the fractional-N PLL with N being the integer part and α being the fractional part. Based on the comparison results, a successive approximation algorithm is used to find out the optimal VCO tuning curve. The calibration time in such a counter-based frequency detection scheme, however, is limited by the frequency detection accuracy, which is also observed in previous designs [14] [17]. In the counter-based AFC, one comparison takes 2^{M-1} reference clock cycles which is typically longer than that of the TVC-based AFC.

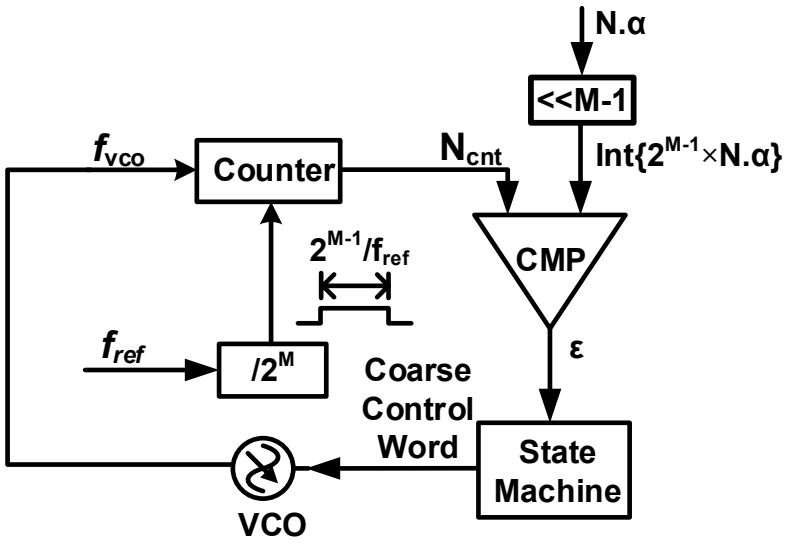


Fig. 2.13: Counter-based AFC.

The counter-based AFC is a digital-intensive solution. It does not require well-matched analog circuitries and also occupies less chip area. The drawback of the counter-based AFC method is that it requires a long counting time in order to reduce the frequency detection error.

2.3 Summary

The timing circuits for wireline and wireless communications are introduced in this chapter. The three commonly used CDR architectures for high speed wireline communications are discussed. They all have their own advantages and disadvantages. It is the application that decides which architecture should be adopted for a particular system. Jitter performance, which includes JTRAN, JGEN and JTOL, is one of the most important specifications of a CDR circuit. It can be evaluated by the linear phase noise model if the CDR is implemented with a linear phase detector. For CDRs with bang-bang phase detectors which is the case for most of the links supporting data rate higher than 10 Gbps, the jitter performance should be found by simulations. The timing circuit for wireless transceivers is the frequency synthesizer which generates LO signals for frequency up-conversion and down-conversion. The phase uncertainty of the clock generated by a frequency synthesizer is quantified as phase noise which can be found by the PLL linear phase noise model. Besides the PLL circuit, the AFC circuit for wide-range frequency synthesizers is also introduced.

The discussion indicates that there exists some limits associated with the conventional CDR circuits and the wide-range frequency synthesizer circuits. The

following chapters will target at solving the issues and proposing design techniques for the CDRs and frequency synthesizers.

CHAPTER 3. A 1~16 GBPS REFERENCE-LESS DIGITAL PLL-BASED CLOCK AND DATA RECOVERY CIRCUIT

3.1 Introduction

For a wireline communication standard, there exists different data-rate variants among which hardware compatibility is desired. For example, the SONET includes a set of signal rate multiples for digital signal transmission on optical fiber. The base rate (OC-1) is 51.84 Mbps. The data-rate progression starts at 155 Mbps and increases by multiples of four. For OC-768, the data rate reaches 39.8 Gbps. Another example is Fibre Channel which is a high-speed network solution for computer data storage communication. Fibre Channel products are available at 1, 2, 4, 8, 10, 16 and 20 Gbps. Products based on the 1, 2, 4, 8, 16 Gbps variants should be interoperable and backward compatible [19]. CDR, as an essential block for high speed wireline communication systems, should support a wide range of bits rates to recover the data for various speed variants.

A challenge in the wide range CDR design is the frequency acquisition loop. For multi-rate CDR with a reference clock, this is not a big issue as the data rate is known and the reference clock can be synthesized simply with a PLL. However, the need for a reference clock incurs additional cost. And the CDR operating range is limited to a few discrete data-rates dictated by the divider ratio in the PLL. To obviate the need for a reference clock and improve the CDR flexibility, the reference-less CDR that supports continuous data-rate is more desired. For continuous-rate CDR without an external reference clock, the design of the frequency acquisition loop is much harder. It needs to extract the data rate from the data stream. And the wide range of possible data rate makes

it more challenging. For the CDR loop itself, the difficulty lies in the wide range clock generation.

CDR can be implemented with the DLL-based, PLL-based or DLL/PLL-based architectures. [6] presents a DLL-based CDR which supports a data rate from 5.75 to 44 Gbps. The multi-sampling-rate approach adopted in [6] is a promising technique to expand the range of CDR data rate. However, [6] does not solve the problem of wide range clock generation. And the DLL-based architecture is not suitable for reference-less CDR design. The DLL/PLL-based architecture serves as a possible solution to reference-less design [11]. However, as mentioned previously, the design of a phase shifter that covers a wide range of tunable delay is very challenging and power consuming. The PLL-based architecture is another possible solution to reference-less design [20] [21]. Its power consumption is less than the other two architectures when the CDR is used for the single link applications. As for the VCO implementation, it is natural to adopt the ring architecture because of its area saving characteristic and wide tuning range [20] [21]. However, its poor random jitter performance keeps it away from the application where low jitter generation is required. Furthermore, [20] and [21] use an analog PLL as the CDR feedback loop. The loop filter in the analog PLL is area consuming.

The focus of this chapter is to design a low power digital reference-less CDR circuit that supports continuous data-rate from 1 Gbps to 16 Gbps for a single channel system. Based on the aforementioned analysis, the PLL-based CDR architecture is more appropriate for this wide range of data rate as long as its jitter performance satisfies the specifications. A digital architecture is proposed to save chip area by eliminating the large on-chip capacitor in its analog counterpart. To achieve low jitter performance and enable

more supported applications, LC oscillator is adopted in the design. The key circuits to implement such digital reference-less CDR is the wideband digital controlled oscillator and the digital reference-less frequency locking loop. Their design details are presented in the following sections.

3.2 Proposed CDR Architecture

The proposed digital PLL-based CDR architecture is illustrated in Fig. 3.1. It consists of a digital PLL and a digital reference-less FLL. The PLL includes a 1-to-16 de-serializer, a bang-bang phase detector followed by a majority voter, a digital accumulator, a binary-to-thermometer converter, a sigma-delta modulator and a digital-controlled oscillator followed by a divide by 2. At startup, the FLL drives the DCO towards target frequency until the frequency error is within the PLL locking range. Then, the PLL takes over the DCO control and finely tunes the DCO frequency until phase acquisition.

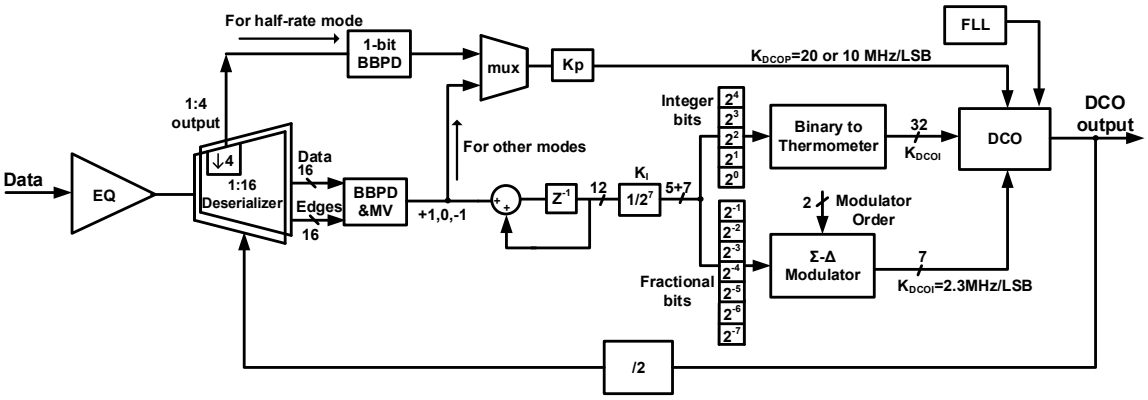


Fig. 3.1: Proposed CDR architecture.

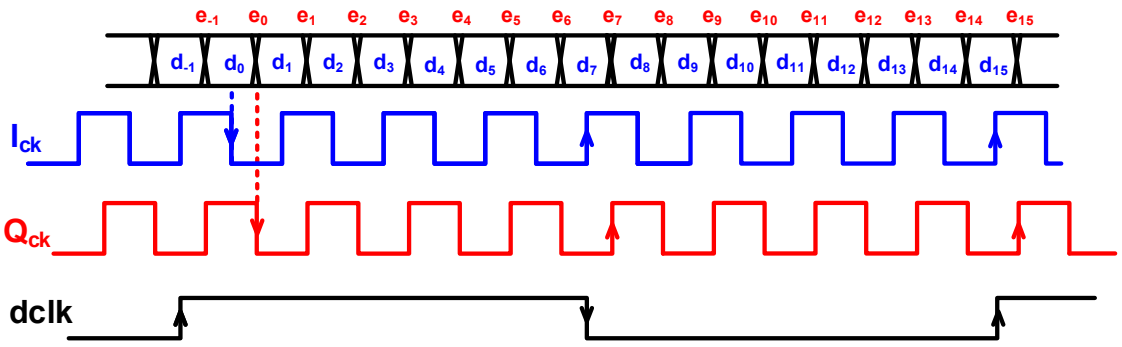
The proposed CDR design is shown in Fig. 3.1. The received data first goes through a continuous time linear equalizer (CTLE) which compensates losses from the feeding channel. Then the feedback clock from the DCO and divider samples the incoming data.

To do phase detection, two samples for each data period are needed. One is data sample, the other is edge sample. These two samples are de-serialized by two 1-to-16 de-serializers. The deserialization converts the high speed sample stream into parallel low speed streams, therefore, enabling the following operation to be performed by semi-custom-designed digital circuits. The bang-bang phase detector, majority voter, accumulator, binary-to-thermometer converter and sigma-delta modulator are all implemented with synthesized CMOS logics and are placed and routed with digital design tools. These circuits operates at a clock rate of $1/16^{th}$ of the DCO output frequency. In each clock period, there are 16 data samples and 16 edge samples. The bang-bang phase detector determines the clock and data phase relationship for each data samples and combines them into one early/late/hold result with the majority voting logic. The detection result is used as the input of the PLL proportional path and integral path. Similar to [6], the proposed CDR takes advantage of the flexibility of synthesized digital circuits and supports multiple data rate sampling modes. In the proposed CDR, there is another phase detection path pulling data/edges from the second stage of the 1-to-16 de-serializer. This is a path that has a shorter processing delay and is exclusively used in the proportional path for half-rate sampling mode to improve the CDR tracking jitter performance. This will be discussed in more detail in the following section. The loop filter in the PLL integral path is a 12-bit saturated accumulator. The accumulator output is scaled by $1/2^7$ which is implemented by feeding the 7 LSBs of the accumulator output to a digital sigma-delta modulator. The sigma-delta modulator dithers the DCO control word and reduces the phase noise due to the frequency quantization effect [22]. The integer bits after the scaling are thermometer-coded. The fractional bits, after being dithered by the sigma-delta modulator, are inherently

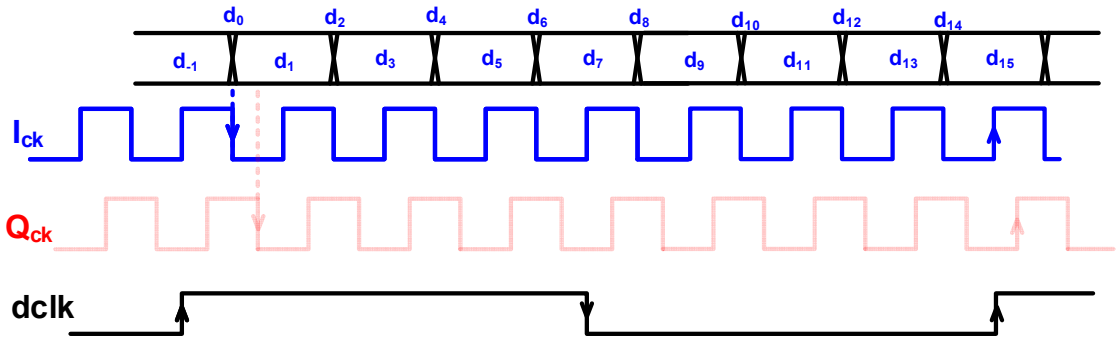
thermometer-coded [22]. The summation of integer and fractional control bits is carried out inside the DCO.

3.2.1 Sampling Rate Selection and Phase Detection

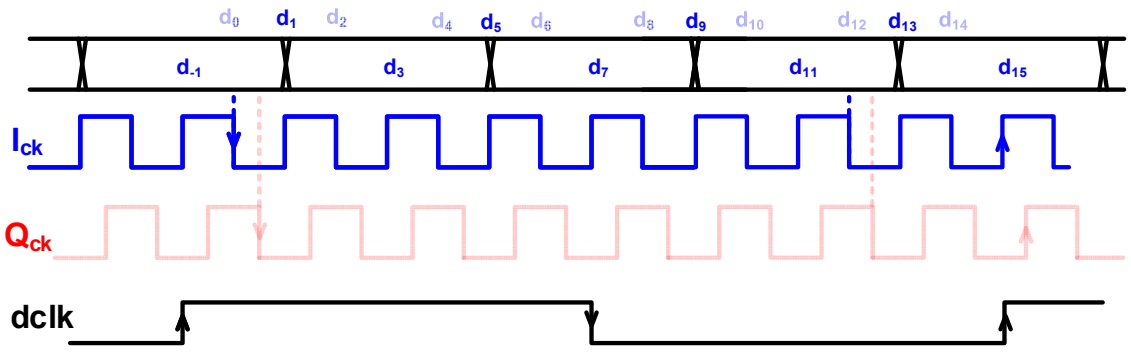
The frequency tuning range of the DCO in Fig. 3.1 is from 8 GHz to 16 GHz. After divide-by-2, 4~8 GHz I/Q clocks are generated. With half-rate phase detection, the CDR is able to support data-rate from 8 Gbps to 16 Gbps. In order to extend the supported data rate to be lower than 8 Gbps, multi-sampling-rate technique is adopted in this design. Fig. 3.2 shows the four sampling modes in the proposed CDR.



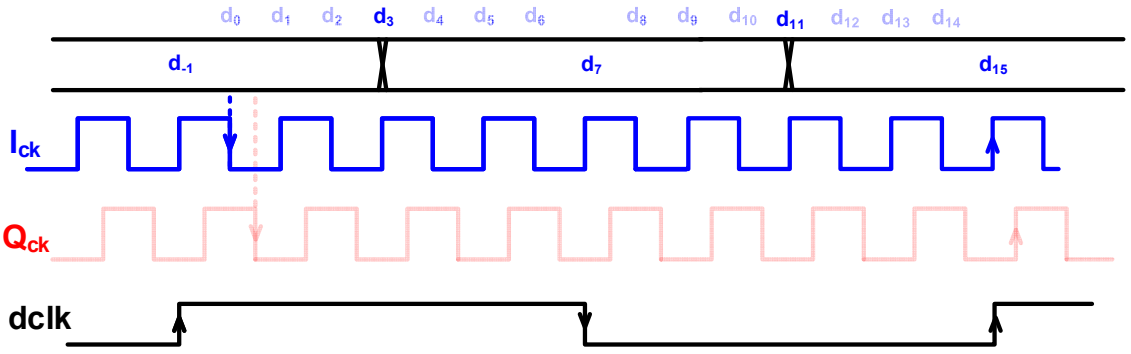
(a)



(b)



(c)



(d)

Fig. 3.2: Sampling modes of the CDR (a) Half-rate sampling (b) Full-rate sampling (c) Oversampling-by-2 (d) Oversampling-by-4.

In half-rate sampling mode, as shown in Fig. 3.2(a), the data period is half of the clock period. The edges of the in-phase clock I_{ck} are used to capture the data samples while the quadrature-phase clock Q_{ck} captures the edge samples. *dclk,* which has a rate of 1/16th of the DCO frequency, is the clock output from the 1:16 de-serializer. In each period of *dclk*, there are 16 samples of data and edges. The bang-bang phase detector determines the clock-data phase relationship by solving the Alexander equations [23].

$$Early_n = (d_n \oplus d_{n-1}) \& (d_n \oplus e_{n-1}) \tag{3.1}$$

$$Late_n = (d_n \oplus d_{n-1}) \& (d_n \odot e_{n-1}) \tag{3.2}$$

where d_n, d_{n-1}, e_{n-1} are samples in Fig. 3.2. When d_n, d_{n-1} are identical, both results from (3.1) and (3.2) are zero. In this case, the bang-bang PD output is *hold*. The 16 phase detection results are combined into one using the majority voter.

In full-rate sampling mode (Fig. 3.2(b)), the data period is equal to the clock period. Only the samples from the 1-to-16 de-serializer that is clocked by the in-phase clock is needed in this case. Therefore, one of the de-serializers can be turned off to save power. Among the samples d_0~d_{15} acquired by I_{clk}, $d_0, d_2, d_4, d_6, d_8, d_{10}, d_{12}, d_{14}$ are edge samples while $d_1, d_3, d_5, d_7, d_9, d_{11}, d_{13}, d_{15}$ are data samples. The Alexander equations are used to determine the clock-data phase relationship. In each d_{clk} period, there are 8 phase detection results.

In oversampling-by-2 sampling mode (Fig. 3.2 (c)), the data period is twice of the clock period. All the samples acquired by Q_{ck} and some samples acquired by I_{clk} are redundant. Among the samples d_0~d_{15}, d_1, d_5, d_9, d_{13} are edge samples, d_3, d_7, d_{11}, d_{15} are data samples. They are used to do the phase detection according to (3.1) and (3.2). Other samples are discarded. In each d_{clk} period, there are 4 phase detection results.

In oversampling-by-4 sampling mode (Fig. 3.2(d)), the data period is four times of the clock period. All the samples acquired by Q_{ck} and some samples acquired by I_{clk} are redundant. Among the samples d_0~d_{15}, d_3, d_{11} are edge samples, d_7, d_{15} are data samples. They are used to do the phase detection according to (3.1) and (3.2). Other samples are discarded. In each d_{clk} period, there are 2 phase detection results.

Using the above multi-sampling-rate technique, the supported data rate is extended from 8~16 Gbps to 1~16 Gbps. Thanks to the flexibility of the digital architecture, the phase detector with programmable sampling mode can be easily implemented with a semi-custom-designed digital circuit.

3.2.2 CDR Loop Parameter Design

For the proposed CDR in Fig. 3.1, several loop parameters need to be determined according to the constraints of jitter specifications. They are the proportional path gain factors, K_P and K_{DCOP}; the integral path gain factors, K_I and K_{DCOI}; and the clock rate of the digital loop filter. The proportional path gain is equal to the PLL output phase slew rate which determines the CDR jitter tolerance. The integral path gain affects the PLL frequency tracking capability. A large integral path gain helps the proportional path to acquire phase tracking but can cause instability to the loop. The integral path gain needs to be much smaller than the gain of the proportional path to keep the loop stable [24]. The clock rate of the digital loop filter is constrained by the CMOS process speed. It determines the deserialization ratio. From the jitter performance point of view, it is desirable to have a higher clock frequency for the digital loop filter. As it means a shorter de-serializer delay and DCO control update period, and the bang-bang tracking jitter will be smaller. For the 65-nm CMOS process used in this design, the highest clock rate that the digital loop filter can support is 1 GHz. Because the highest input data rate is 16 Gbps, the de-serializer should have a ratio of 1:16.

For jitter tolerance specifications, SONET standard is used as the design target. The jitter tolerance mask defined in the SONET standard is shown in Fig. 3.3 and Table 3.1 [25].

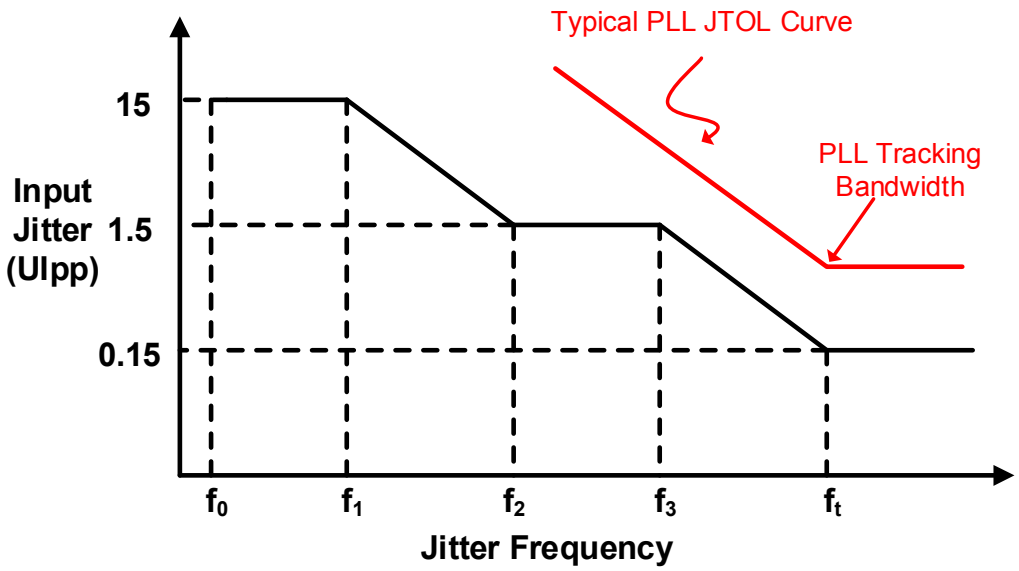


Fig. 3.3: Jitter tolerance mask.

Table 3.1: SONET jitter tolerance definition

Data Rate	f_0 [Hz]	f_1 [Hz]	f_2 [Hz]	f_3 [kHz]	f_t [kHz]
OC-3 155Mbps	10	30	300	6.5	65
OC-12 622 Mbps	10	30	300	25	250
OC-48 2.488 Gbps	10	600	6000	100	1000
OC-192 9.953 Gbps	10	2400	24000	400	4000

Notice that the proposed CDR covers OC-48 and OC-192. The JTOL that a typical PLL achieves is also shown in Fig. 3.3. For jitter frequency higher than the PLL bandwidth, the clock is not able to follow the data and the tolerable input jitter is no larger than 1 UIpp.

For jitter frequency slightly lower than the PLL bandwidth, the JTOL falls at a rate of 20 dB/dec [26]. Therefore, among all the corner frequencies of the two covered network lines in Fig. 3.3, f_t is the most important as it determines the required minimum jitter tracking bandwidth of the CDR loop. As bang-bang PD is used in this design, the tracking bandwidth is dictated by the slew rate of the PLL. Assume that the sinusoidal jitter applied to the input is given by

$$\phi_{in}(t) = \phi_{\text{mod}} \sin(2\pi f_{\text{mod}} t) \tag{3.3}$$

Then, the highest data phase changing rate is

$$\left(\frac{d\phi_{in}(t)}{dt} \right)_{\max} = 2\pi f_{\text{mod}} \phi_{\text{mod}} \tag{3.4}$$

As the gain of the PLL integral path is much smaller than that of the proportional path, only the proportional path control is considered for the jitter tracking behavior. In the worst case situation, the data phase drifting in a rate of (3.4) within the proportional path update period $1/f_{R,P}$ should be caught up by the clock to guarantee a correct sampling. Therefore, the following equation needs to be satisfied.

$$\frac{2\pi f_{\text{mod}} \phi_{\text{mod}}}{2\pi} \frac{1}{f_{R,P}} \frac{1}{F_B} = \frac{K_{DCOP} K_P}{2\pi} \frac{1}{f_{R,P}} \frac{1}{f_{DCO}} \tag{3.5}$$

where f_{DCO} is the DCO frequency and F_B is the data rate. The term in the left of (3.5) is the drifted data phase expressed in the unit of *second*. The term in the right of (3.5) is the adjusted clock phase, also expressed in *second*. Notice that the PD in this design gathers 16 data samples before making a phase detection. It is reasonable to assume that the data transition density has no impact and the DCO frequency can be updated in each clock period. If the jitter modulation frequency f_{mod} becomes higher, then the adjusted clock

phase is smaller than the drifted data phase and the clock is losing track of the data. The CDR jitter tracking bandwidth f_{tracking} is defined as the f_{mod} that satisfies (3.5).

$$f_{tracking} = \frac{K_{DCOP}K_P}{2\pi}\frac{1}{\phi_{\text{mod}}}\frac{F_B}{f_{DCO}} \tag{3.6}$$

Two observations need to be made for the jitter tracking bandwidth in (3.6). Firstly, f_{tracking} depends on the input jitter amplitude. This is because bang-bang PLL is a non-linear system. Secondly, f_{tracking} is inversely proportional to $f_{\text{DCO}}/F_{\text{B}}$. This leads to different jitter tracking bandwidth for different sampling mode. For example, f_{tracking} in the half-rate sampling mode ($f_{\text{DCO}}/F_{\text{B}}$ =1) is four times of that in the oversampling-by-2 mode ($f_{\text{DCO}}/F_{\text{B}}$ =4). Interestingly, the corner frequency f_{t} in the SONET JTOL requirements is also scaled with the data rate. Therefore, the proposed CDR, if designed for OC-192 JTOL, also meets the OC-48 JTOL requirement. For OC-192, the CDR works at the half-rate sampling mode. To get enough design margin, Φ_{mod} is set as 0.4 UI (0.8 UIpp). f_{tracking} is 4 MHz. From (3.6), $K_{\text{DCOP}}K_{\text{P}}$ can be computed as 10 MHz/LSB. K_{P} is usually set to be 1, then K_{DCOP}=10 MHz/LSB. In order to keep the loop stable, the phase change due to the proportional path should be much larger than the phase change from the integral path [24]. Similar to [24], a stability factor ξ is defined for the proposed CDR.

$$\xi = \frac{2K_{DCOP}K_P}{K_{DCOI}K_I} \tag{3.7}$$

As will be shown later, the stability needs to be larger than 800 to maintain a jitter peaking less than 0.1 dB. A small K_{DCOI} and K_{I} is good to reduce the DCO frequency quantization impact. However, it requires more bits in the digital accumulator. Therefore, they will be constrained by the process speed limit and the DCO frequency cover range

requirement. K_{DCOI} and K_I is set to be 2.3 MHz/LSB and $1/2^7$ in this design, respectively. Thus the stability factor define in (3.7) is 1113.

Up to this point, all the loop parameters have been determined. The CDR bang-bang tracking jitter is next calculated given the above loop parameters.

The JGEN due to bang-bang tracking jitter can be evaluated with the PLL proportional path gain.

$$J_{BB,p-p}\ (\text{UIpp}) = (1+D)\cdot\frac{2K_{DCOP}K_P}{2\pi}\frac{1}{f_{R,P}}\frac{F_B}{f_{DCO}} \tag{3.8}$$

where D is the loop delay factor. It represents the number of proportional path update period that needed for the phase detection result to propagate to the DCO control node. D is 1 for the de-serializing operation. From (3.8), $J_{BB,p\text{-}p}$ is computed as 66 mUI for a 10 Gbps data. In the cases of 5 Gbps, 2.5 Gbps and 1.25 Gbps when the DCO frequency is twice, four times, and eight times of the data rate, $J_{BB,p\text{-}p}$ is scaled down accordingly.

The SONET standards in Table 3.1 all require a CDR JGEN to be less than 100 mUI peak-to-peak. However, from the above analysis, it can be seen that the bang-bang tracking jitter of OC-192 already uses 66 % of the budget leaving 34 mUI for the random jitter. This represents a jitter due to the random noise being less than 3.4 ps peak-to-peak which is difficult to achieve. The exclusive proportional path for the half-rate sampling mode, as can be seen in Fig. 3.1, solves this problem by shortening the update period of the proportional path. Fig. 3.4 shows the block diagram of the 1-to-16 de-serializer. In half-rate sampling mode, the data for phase detection is pulled out from the second stage of the de-serializer. The proportional path update period is then shortened from $16/f_{DCO}$ to $4/f_{DCO}$. This path is called fast BB-path in this design. As the data rate at the output of the 2-to-4

de-serializer is up to 4 Gbps, the phase detection logic in the fast BB-path is implemented with custom-designed circuits. To avoid complex logic circuits in this path, down-sampling instead of majority voting is used. In this case, the data transition density will affect the CDR JTOL performance. To maintain the JTOL, K_{DCOP} in the half-rate sampling mode is doubled as the transition density of random data is 50 %. Using (3.8), the peak-to-peak bang-bang tracking jitter for the half-rate sampling mode becomes 32 mUI which is a great improvement in the jitter performance. Table 3.2 summarizes the calculated bang-bang tracking jitter when the fast BB-path is disabled and enabled for the half-rate sampling mode.

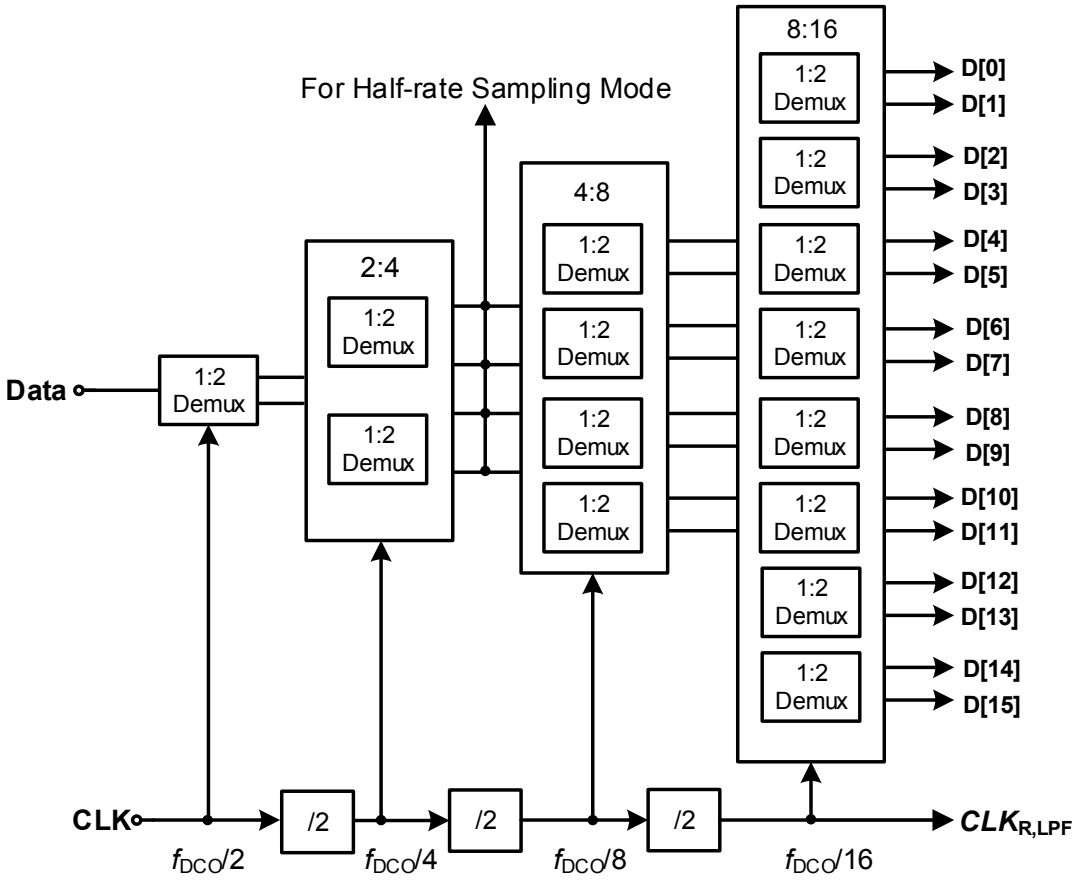


Fig. 3.4: Block diagram of the 1-to-16 de-serializer.

Table 3.2: Theoretical bang-bang tracking jitter

Sampling Mode	$J_{BB,p\text{-}p}$ (mUI)	$J_{BB,p\text{-}p}$ (mUI) (Fast BB-path enabled)
Half-rate (OC-192)	66	33
Full-rate	33	33
Oversampling-by-2 (OC-48)	16.5	16.5
Oversampling-by-4	8.25	8.25

3.3 Wideband Digitally Controlled Oscillator

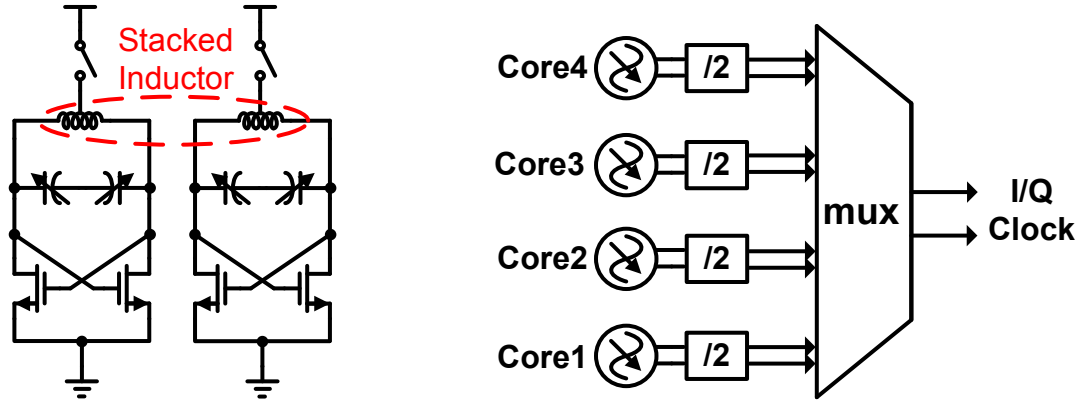
A wideband digitally controlled oscillator (DCO) with an octave frequency tuning range is required to enable the CDR to support a continuous data rate. In the proposed CDR, the DCO needs to cover a frequency range from 8 GHz to 16 GHz. Similar to the VCO in an analog PLL, there is a tradeoff between the DCO tuning range and its phase noise performance. The DCO uses small unit capacitors in the LC tank to discretely adjust its output frequency. Because the DCO relies on switching on and off small unit capacitors and it is designed to cover an octave frequency range from 8 to 16 GHz, the capacitor tank in the DCO can be very large. A large capacitor tank involves more switches thus resistance losses. This lowers the quality factor (Q) of the LC tank and degrades the phase noise performance. The capacitance due to the interconnect and the switching transistors as well as the capacitance of the "off-state" varactors will eventually limit the DCO tuning range. Thus, the design of a DCO to cover a wide output frequency range is a challenging task. Before the discussion of the DCO in the CDR, a brief review of existing wideband DCO designs will be first presented.

3.3.1 Existing Wideband DCOs

Fig. 3.5(a) and Fig. 3.5(b) show the two existing wideband DCO implementations [27] [28]. The DCO in Fig. 3.5(a) is implemented in a 45 nm SOI CMOS technology. The DCO consists of two oscillator cores and covers a frequency range from 5.85 GHz~11.64 GHz. To save the chip area, two inductors are stacked together. Though, only one DCO core is activated in normal operations, yet the tuning of the inactive tank has a pushing effect to the active tank due to the coupling between two stacked inductors. This effect is exploited to expand the DCO tuning range from 5.85~11.64 GHz to 5.67~12.09 GHz. Thus, an octave frequency tuning range is achieved. As the pushing effect is relatively weak, the tuning range improvement is limited (6% in this design). Fig. 3.5(b) shows a DCO implemented in a 0.13 μm CMOS technology. It covers a frequency range from 5.6 GHz to 11.5 GHz. The DCO uses four oscillator cores. Each oscillator core is directly coupled to its own divide-by-2 circuit to produce the in-phase and quadrature-phase (I/Q) LO signals. One of the four I/Q signal is selected as the final output via a multiplexer circuit. Each DCO core has three digitally controlled varactor tuning blocks with each of them corresponding to a different tuning range. Because each DCO core is optimized for its own output range, the phase noise performance is better than the DCO shown in Fig. 3.5(a). The downside of this approach is the large area and power consumption. The circuit occupies an area of about 1 mm^2, mostly consumed by the LC tank.

The LC tanks shown in Fig. 3.5(a) is a multimode resonator where the problem of concurrent oscillation exists. To generate a correct output frequency, the inactive oscillation mode needs to have its effective impedance to be much smaller than that of the active mode and the oscillation frequencies of two modes should be far away from each other. This requires a well-controlled coupling resonator and the oscillator becomes more

sensitive to the parasitic capacitors. The multi-core approach has the best phase noise performance. However, the chip area consumption is too large for the wireline interface applications.



(a) (b)

Fig. 3.5: Existing wideband DCO architecture (a) DCO with stacked inductors (b) DCO with multiple cores.

3.3.2 Inductive Tuning Approach

Besides the above two approaches, inductive tuning is another technique to increase the oscillator tuning range [29]. The inductive tuning can be achieved by switches that are used to vary the number of turns of a spiral inductor or by switched-coupled inductors [30] [31]. The inductive tuning approach is known to worsen the oscillator phase noise performance as the switch loss de-Q the LC tank [31]. Capacitive-tuned oscillators, on the other hand, are able to achieve low phase noise and low power dissipation. However, these are only true for oscillators that work in the low frequency range in which inductive quality factor is significantly lower than that of the capacitances. For higher operating frequencies, the capacitive quality factor becomes a limitation. The DCO in this design targets a

frequency range of 8 GHz~16 GHz. The Q-factor of the capacitor tank in this frequency range is comparable or even lower to that of the inductor. Therefore, it is desirable to have a small capacitor tank in the DCO to keep the loss of the capacitor tank to be less dominant. However, this conflicts with the wideband octave tuning range requirement. Consequently, inductive switching methods becomes a viable solution to increase the tuning range while achieving a higher tank Q. Furthermore, the inductive tuning approach does not increase the chip area consumption as the switches and the coupling coils can be placed within the main inductor. Based on the above analysis, inductive tuning is adopted in the DCO of the proposed CDR.

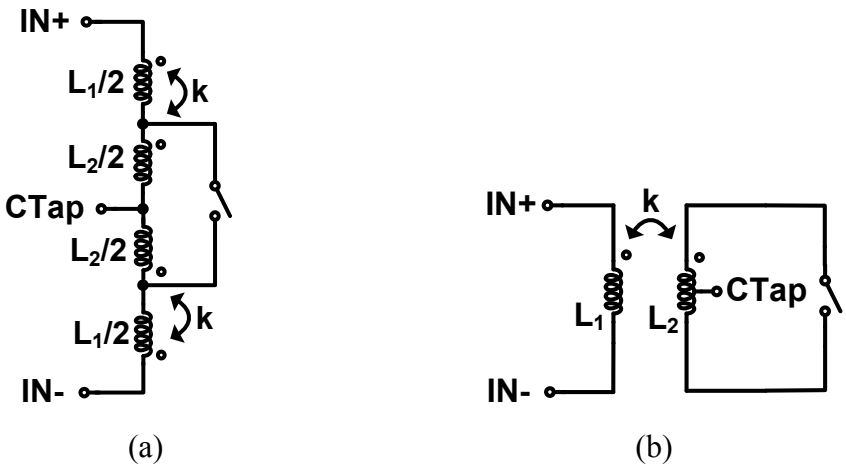


Fig. 3.6: Inductance tuning methods (a) switched inductor (b) switched mutual coupling.

Fig. 3.6 shows the two inductive tuning methods. In Fig. 3.6(a), a switch is connected between two symmetric nodes inside the inductor winding. The two-winding inductor can be seen as two inductors L_1 and L_2 in series. The switch enables or disables the inner winding allowing the inductance to be programmed. The approach in Fig. 3.6(b) is based on mutual inductance tuning in a transformer. A switch is connected to the

secondary winding in the transformer. When the switch is open, the effective inductance seen by the capacitor tank is the primary coil inductance L_1. When the switch is closed, a current is induced that runs in the direction opposite to the current in the primary coil. As a consequence, a negative mutual inductance is generated that superimposes to the self-inductance of the primary coil and reduces the overall inductance.

As mentioned previously, both methods in Fig. 3.6 degrade the inductive Q when the switch is on. In Fig. 3.6(a), the MOS switch channel resistance de-Q the inductor as it is directly connected to the windings. In Fig. 3.6(b), switch loss is transferred to the primary coil via magnetic coupling. However, the mutual coupling switched inductor is a better approach for practical circuit implementation. For wideband LC oscillator design, NMOS-only cross-coupling pair are typically used because of its lower parasitic capacitance. And this requires the center tap (CTap) of the spiral inductor to be connected to power supply voltage which necessitate a PMOS switch in Fig. 3.6(a). For the same channel resistance, a PMOS switch has 2 to 3 times of parasitic capacitance compared to its NMOS counterpart. Therefore, a PMOS switch should be avoided in order to get the best tuning range performance. On the other hand, the DC bias of the primary winding and secondary winding in Fig. 3.6(b) can be different. Thus, an NMOS switch can still be used even the primary winding is biased at the power supply voltage. Considering the above analysis, the inductive tuning based on switched mutual coupling (transformer-based) method is adopted in the DCO circuit.

The layout of the switched mutual coupling inductor is shown in Fig. 3.7(a). It can be analyzed with the T-model which is shown in Fig. 3.7(b) [31]. In this model, L_1 and L_2 represent the self-inductances of the primary coil and the secondary coil. M is the mutual

inductance between the two coils and it is proportional to the coupling factor k. Z_{sw} is the impedance of the non-ideal switch and resistors R_1 and R_2 model the losses of inductors L_1 and L_2, respectively. It is also assumed that the non-ideal switch has an on-resistance R_{on} and off-capacitance C_{off}. From this T-model, the impedance, Z_{in}, can be found as (3.9).

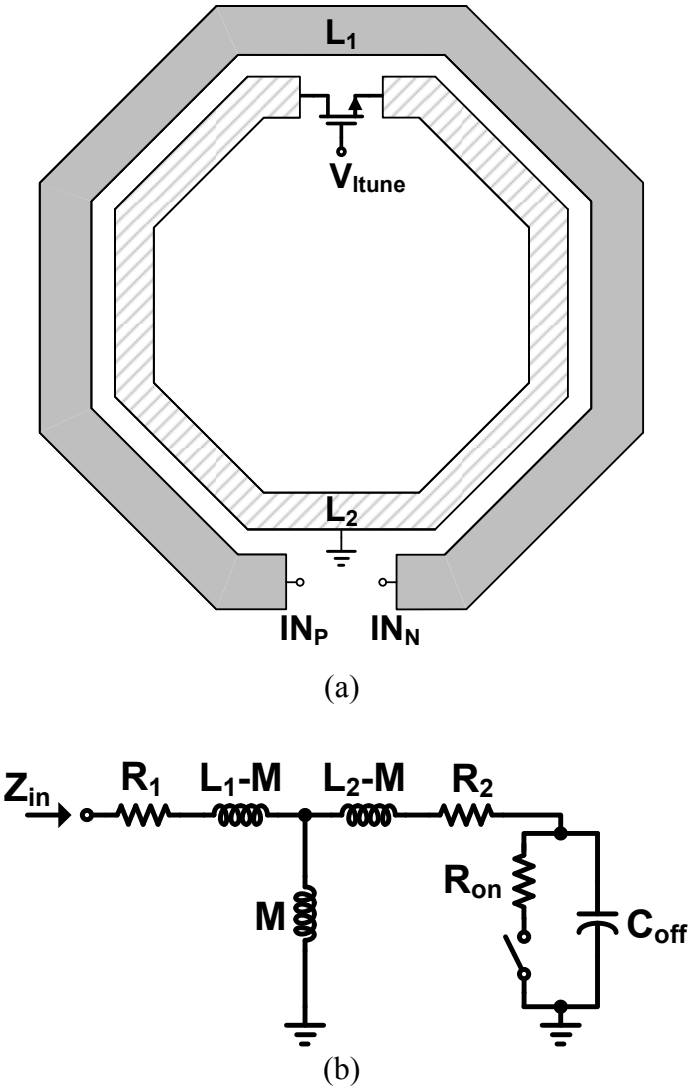


Fig. 3.7: (a) Switched mutual-coupling inductor and (b) its equivalent model.

$$Z_{in} = R_1 + j\omega L_1 + \frac{(\omega M)^2}{R_2 + j\omega L_2 + Z_{sw}} = R_1 + j\omega L_1 + \frac{(\omega k)^2 L_1 L_2}{R_2 + j\omega L_2 + Z_{sw}} \tag{3.9}$$

When the switch is on, $Z_{sw} \approx R_{on}$, and the Q of the secondary coil is sufficiently high. Thus, $(\omega L_2)^2 >> (R_L + R_{on})^2$. Then the equivalent inductance and resistance are

$$L_{eq,on} \approx (1-k^2)L_1 \tag{3.10}$$

$$R_{eq,on} \approx R_1 + k^2 \frac{L_1}{L_2}(R_2 + R_{on}) \tag{3.11}$$

It can be seen in (3.10) that the effective inductance can be reduced by turning on the switch. The losses of the switch and the secondary coil are transferred to the primary coil and degrade the inductor Q due to the coupling as shown in (3.11). In order to reduce the loss, the switch should be large enough to minimize R_{on}. (3.10) and (3.11) show the tradeoff between inductance tuning range and the Q degradation. A tight coupling (large k) between the primary and secondary coils is desirable to increase the inductance tuning range, but that also leads to more losses coupled from the secondary coil.

When the switch is off, $Z_{sw} \approx 1/j\omega C_{off}$, and R_2 is sufficiently small. Then, the equivalent inductance and resistance are

$$L_{eq,off} \approx L_1 - \frac{\omega k^2 L_1 L_2}{\omega L_2 - (\omega C_{off})^{-1}} \tag{3.12}$$

$$R_{eq,off} \approx R_1 \tag{3.13}$$

The second term in $L_{eq,off}$ is usually much smaller than the first term. Therefore, the effective inductance is equal to the self-inductance of the primary coil when the switch is off. Notice that when ω is close to $1/\sqrt{L_2 C_{off}}$, $L_{eq,off}$ becomes negative. This region should be avoided in the circuit operation. Thus, the size of the switch should not be too large to guarantee $\omega \ll 1/\sqrt{L_2 C_{off}}$ across the tuning range when the switch is off.

3.3.3 Wideband DCO Design

The wideband DCO in the proposed CDR is shown in Fig. 3.8. To ensure that the target DCO frequency tuning range 8 GHz~16 GHz is covered over PVT variations, the actual designed tuning range needs to be larger than 8 GHz. Two DCO cores are used considering the tradeoff between tuning range and phase noise performance. Each core is directly coupled to its own divide-by-2 and then multiplexed to produce quadrature differential clocks for the CDR. The core adopts the switched-coupled inductor approach to increase the tuning range. Both core selection and inductor switch are controlled by the FLL and determined before the normal CDR operation.

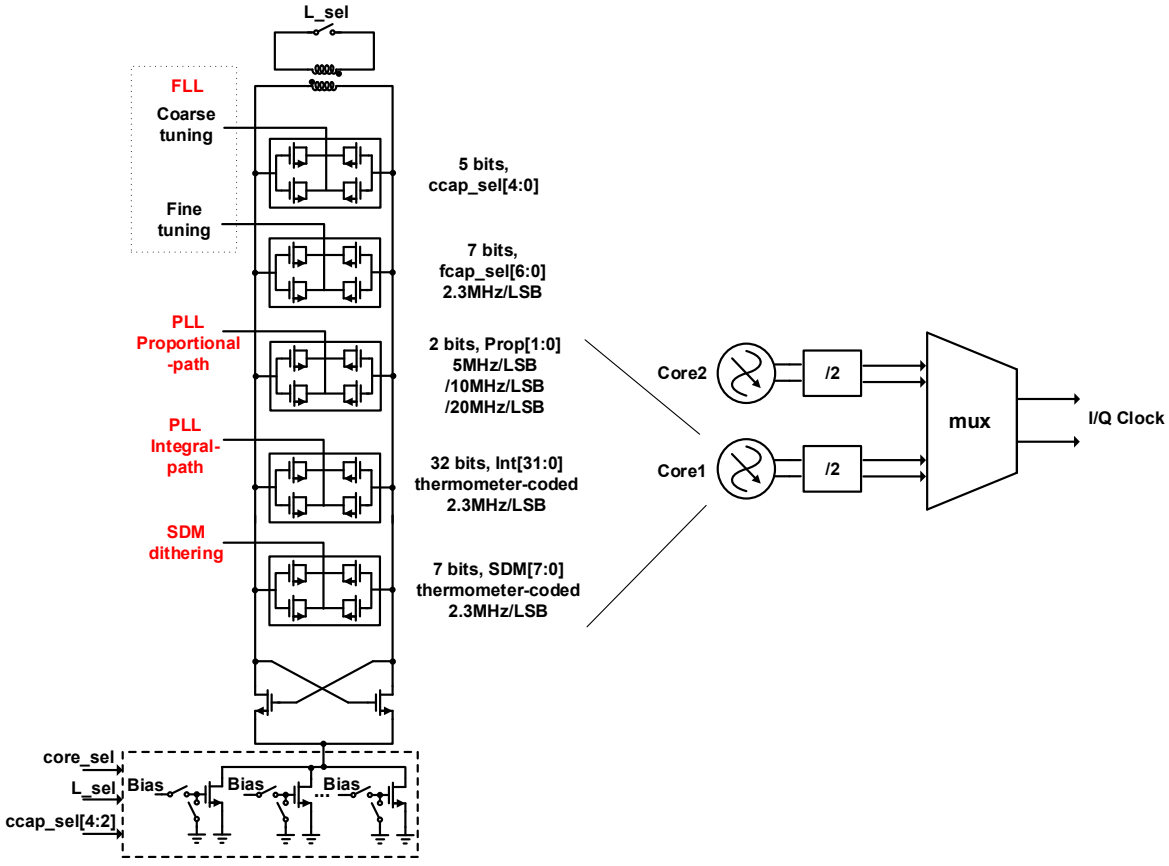


Fig. 3.8: 8~16 GHz Wideband DCO.

There are 5 capacitor arrays in each DCO core. The FLL controls the coarse tuning array and the fine tuning array. Each of these two arrays corresponds to 32 tuning curves (5-bit for coarse tuning) with each curve containing 127 frequency steps (7-bit for fine tuning). The resolution of the fine tuning array has been chosen to be the same as that of the PLL integral path gain, 2.3 MHz/LSB.

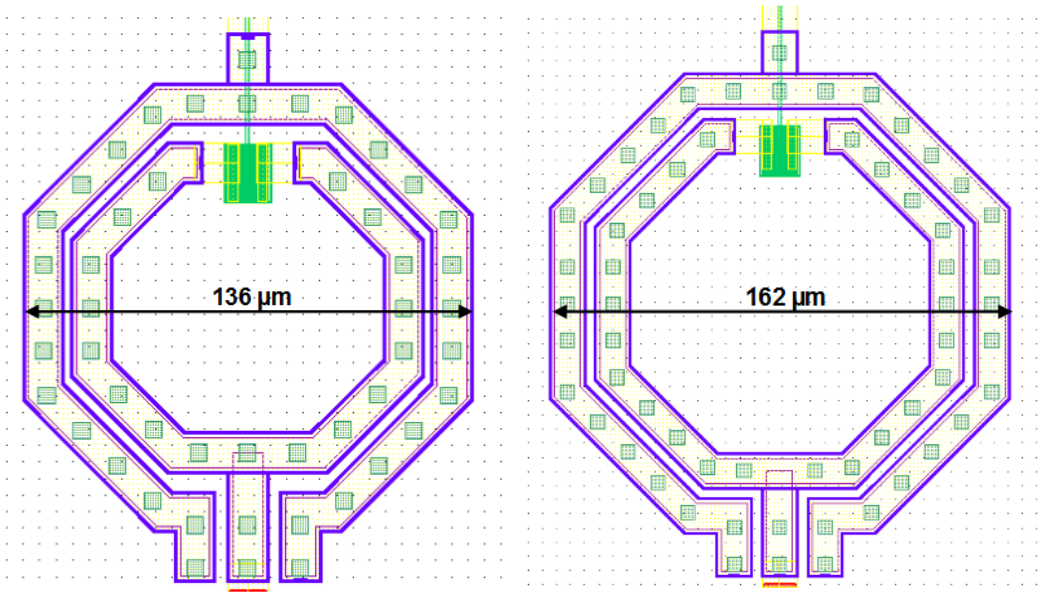
The third capacitor array is controlled by the PLL proportional path. Its tuning gain is can be programmed from 5 MHz/LSB to 20 MHz/LSB and determines the CDR JTOL. The PLL integral path controls the fourth and the fifth arrays which are responsible for the PLL frequency locking and slow jitter tracking. One array is directly controlled by the digital accumulator and the tuning bits of the other array are dithered by a sigma-delta modulator in order to reduce the DCO frequency quantization effect. They are both with a gain of 2.3 MHz/LSB and their control bits are both thermometer-coded.

The DCO biasing current, which is controlled by IDAC, is adjustable to compensate variation of the LC tank resonant resistance. The IDAC control signal comes from the core selection tuning bit *core_sel*, the inductor tuning bits *L_sel* and 3 MSBs of the coarse capacitor tank tuning bits *ccap_sel [4:2]*.

3.3.3.1 Inductor Layout

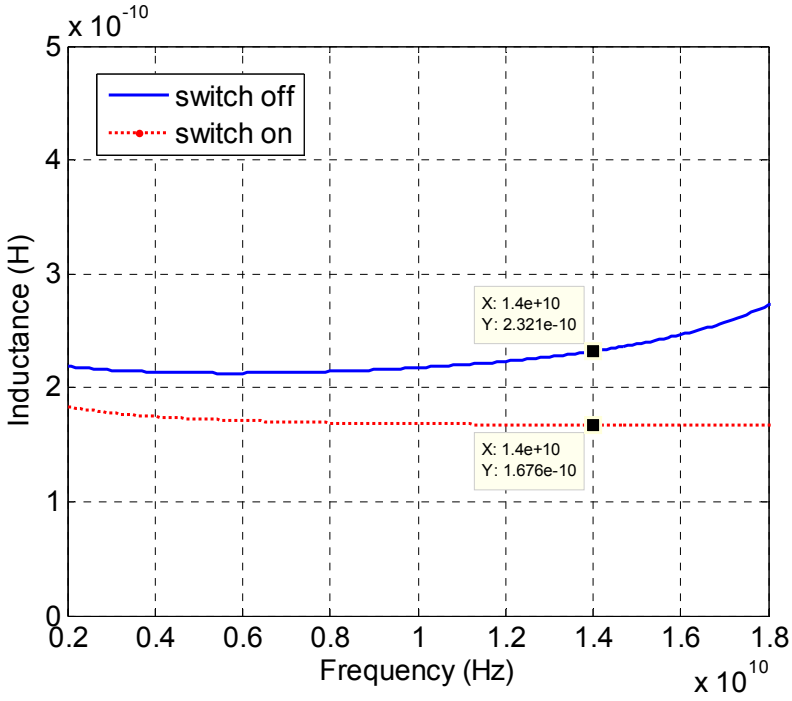
The switched-coupled inductor layouts for the two DCO cores are shown in Fig. 3.9. The switched-coupled inductor is a transformer with the secondary coil connected to a switch. In this design, both primary coils and secondary coils are single-turn inductors implemented with 12-μm top layer metal and aluminum capping layer. To minimize the parasitic inductance due to the routings, the switches are placed inside the primary coils.

Fig. 3.10 and Fig. 3.11 plot the inductance and Q of the above two switched-coupled-inductors. For the inductor in the high frequency core, the diameter is 136 µm. The effective inductance is 0.232 nH when the switch is off and 0.168 nH when the switch is on. According to (3.10) and (3.12), the coupling factor k is 0.525. The Q-factor is degraded from 20.09 at 12 GHz to 13.99 at 16 GHz. Because the inductor operates at a higher frequency when the switch is turned on, the Q degradation is still acceptable. For the inductor in the low frequency core, the diameter is 162 µm. The effective inductance is 0.292 nH when the switch is off and is 0.207 nH when the switch is on. The coupling factor k is 0.539. The Q of the inductor is degraded from 17.42 at 8 GHz to 12.23 at 12 GHz.

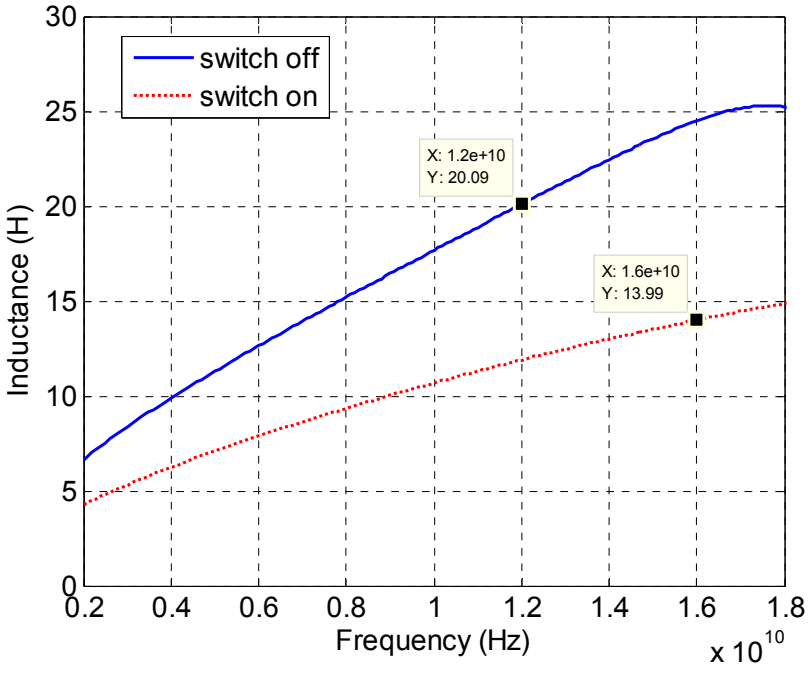


(a) (b)

Fig. 3.9: Switched-coupled-inductors in (a) high frequency core (b) low frequency core.

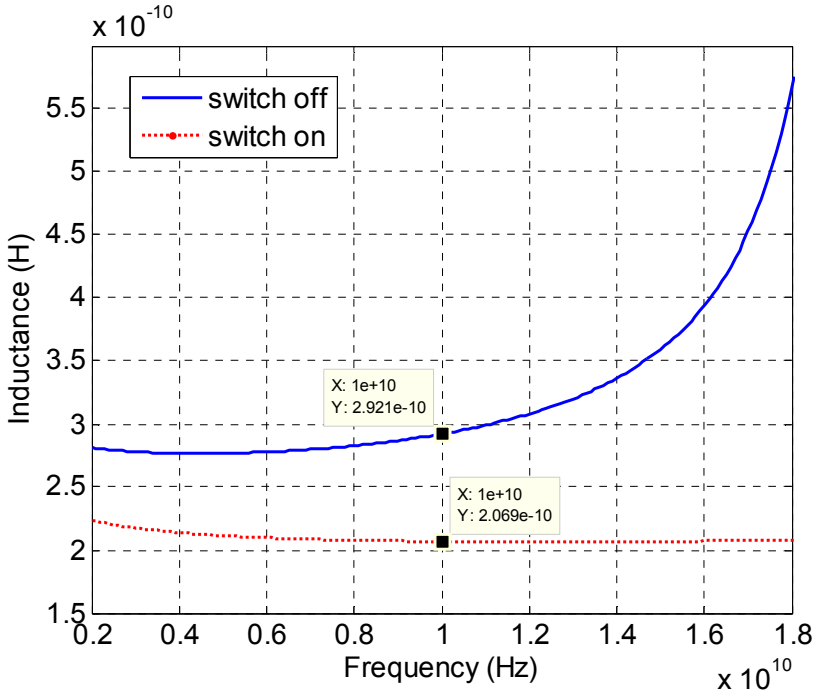


(a)

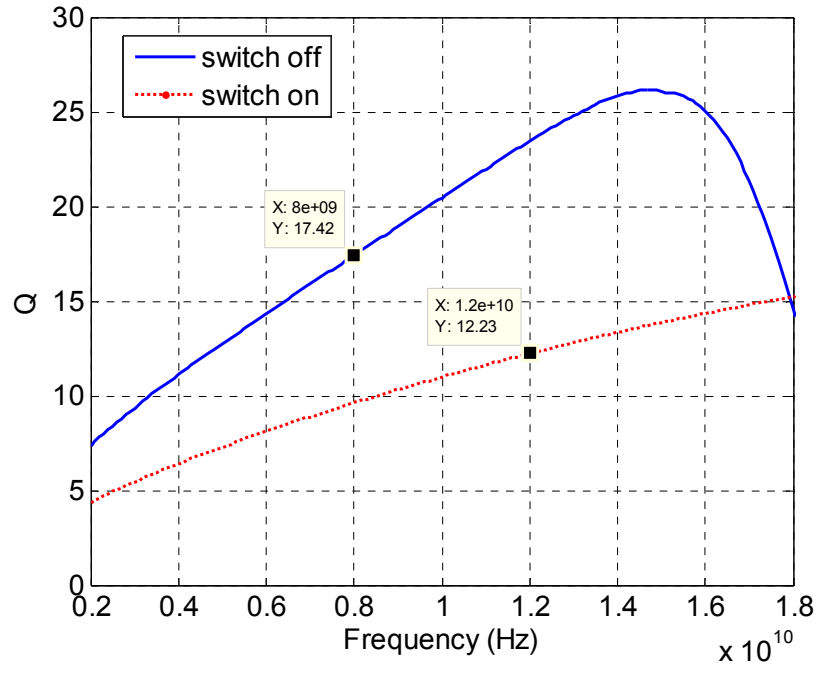


(b)

Fig. 3.10: (a) Inductance (b) Q of the high core inductor.



(a)



(b)

Fig. 3.11: (a) Inductance (b) Q of the low core inductor.

3.3.3.2 Capacitor Tank Design

Each DCO core has five digitally controlled varactor tuning blocks as shown in Fig 3.8. To minimize the extra tuning range required to trim PVT variations, all the varactors are implemented with NMOS device because of its tighter process control compared to that of metal capacitors [28].

The fine tuning capacitor array has a resolution of $f_{\text{step,fine}}$=2.3 MHz/LSB which is determined in the loop parameter design. If an overlapping ratio of two coarse tuning curves is required to be 50%, then (3.14) should be satisfied.

$$\frac{(2^7-1)f_{\text{step,fine}} - f_{\text{step,coarse}}}{(2^7-1)f_{\text{step,fine}}} = 50\% \tag{3.14}$$

The resolution of the coarse tuning capacitor array can be computed as

$$f_{step,coarse} = 0.5\times(2^7-1)f_{step,fine} \approx 2^6 f_{step,fine} \tag{3.15}$$

$f_{\text{step,coarse}}$ found by (3.15) should be large enough to cover the tuning range. If not, the number of coarse capacitor tuning bit needs to be increased. In this design, 5-bit coarse capacitor tuning together with 1-bit inductive tuning for each core are able to cover the target frequency ranges.

With $f_{\text{step,coarse}}$ and $f_{\text{step,fine}}$, the unit switchable capacitance ΔC_{coarse}, ΔC_{fine} for the coarse and fine tuning capacitor arrays can be computed with the following equations [32].

$$\Delta C_{coarse} = \frac{2f_{step,coarse}C_{total}}{f} \tag{3.16}$$

$$\Delta C_{fine} = \frac{2f_{step,\text{fine}}C_{total}}{f} \tag{3.17}$$

where C_{total} is the total capacitance, f is the operational frequency. In order to cover the required highest frequency, the total off-capacitance of the five capacitor arrays should be small enough. As the capacitance of the PLL proportional-path-controlled and SDM-controlled capacitor arrays is much smaller than other tanks. They are neglected in the calculation. Then, (3.18) needs to be satisfied.

$$(2^5-1)C_{c,off}+(2^7-1)C_{f,off}+2^4C_{f,on}+(2^4-1)C_{f,\text{off}}+C_{\text{p}}=C_{\text{tot,h}} \tag{3.18}$$

where $C_{c,off}$ is the unit off-capacitance of the coarse capacitor array; $C_{f,off}$ is the unit off-capacitance of the fine capacitor array; $C_{f,on}$ is the unit on-capacitance of the fine capacitor array; C_p is the lumped parasitic capacitance which can be found by simulation; $C_{tot,h}$ is the total capacitance when the DCO operates at the highest frequency and it can be computed according to the tank inductance and the target frequency. The first term in (3.18) is the total capacitance of the coarse capacitor array when all of its capacitors are in the off-state. The second term is the total capacitance of the fine capacitor array when all of its capacitors are in the off-state. The third and fourth terms account for the capacitance of the PLL integral-path-controlled capacitor array when half of its capacitors are on and the other half are off. This is the starting point of CDR integral path adjustment after the FLL process. The PLL integral-path-controlled capacitor array has the same unit capacitor as that of the fine capacitor array, so $C_{f,on}$ and $C_{f,off}$ are used for these two terms. Their relationship is given by

$$C_{c,on} = C_{c,off} + \Delta C_{coarse} \tag{3.19}$$

For simplicity, the capacitors in the fine tuning array and coarse tuning array are designed to have the same tuning ratio. In other words, the lengths of the transistors in both arrays are equal. Then, the following equation should be satisfied.

$$\frac{C_{c,off}}{C_{f,off}} = \frac{\Delta C_{coarse}}{\Delta C_{fine}} \tag{3.20}$$

With (3.18), (3.19) and (3.20), $C_{c,off}$, $C_{c,on}$, $C_{f,off}$ and $C_{f,on}$ are calculated. The transistor sizes that have the calculated on-off capacitance can be found by simulations.

Finally, the PLL proportional-path-controlled capacitor bank needs to be determined. As its frequency tuning step is already known. The unit switchable capacitance can be calculated with an equation similar to (3.16). To keep the additional capacitance small, a short transistor length can be used for the PLL proportional-path-controlled capacitor array. And the transistor width is found by simulations.

MOS capacitor arrays for the high core and low core DCOs have been designed. The transistor sizes of the arrays are found by simulations and summarized in Table 3.3.

Table 3.3: Capacitor tank design summary

Core	Capacitor Array	C_{on}/C_{off} (unit)	W/L (μm/ μm)
High Core	Coarse	36.000 fF/8.870 fF	12/0.21
	Fine/PLL Int./SDM	0.600 fF/0.164 fF	0.23/0.18
	PLL Prop.	4.430fF/2.210 fF	4/0.09
Low Core	Coarse	60.400 fF/17.200 fF	25.6/0.17
	Fine/PLL Int./SDM	1.000 fF/0.287 fF	0.42/0.17
	PLL Prop.	8.400 fF/3.780 fF	6.72/0.1

3.4 Digital Frequency Locking Loop

PLL with a bang-bang phase detector and operating with random binary data has a limited capture range. Therefore, a frequency-acquisition-assisted loop is needed to set the DCO frequency to its desired value before the normal CDR operation. At startup, the DCO frequency is driven toward the desired value by the frequency locking loop. When the frequency error reaches the PLL capture range, the PLL takes over and performs phase locking. The difficulty of frequency locking in CDR originates from the fact that NRZ random binary data contains no spectral line at the bit rate. Thus, the tri-state phase frequency detectors which is widely used in frequency synthesizers cannot be applied to CDR. Frequency detection for PLLs operating with random data is usually performed by monitoring cycle slips [33] [11] [34] or statistically estimating the data transition density [35].

3.4.1 Overview of CDR Frequency Detection Techniques

3.4.1.1 Frequency Detection by Cycle Slip Monitor

A frequency difference between the data stream and the sampling clock can be detected by monitoring their phase relationship. As can be seen in Fig. 3.12, each clock period is divided into four quadrants. These four quadrants can be identified with voltage levels of the *I* and *Q* clocks. When the clock frequency is equal to the data rate, the phase relationship between the clock and the data will not change with time and each edge (rising and falling) of the data will sample the same clock quadrant. However, if the clock frequency is higher than the data rate, the sampled clock quadrant rotates with an order

shown in Fig. 3.12(a). On the other hand, if the clock frequency is lower than the data rate, the sampled clock quadrant rotates with a reverse order which is shown in Fig. 3.12(b). Every complete revolution of the sampled quadrant is called a cycle slip. By monitoring the direction of quadrant rotation, the frequency error polarity can be found.

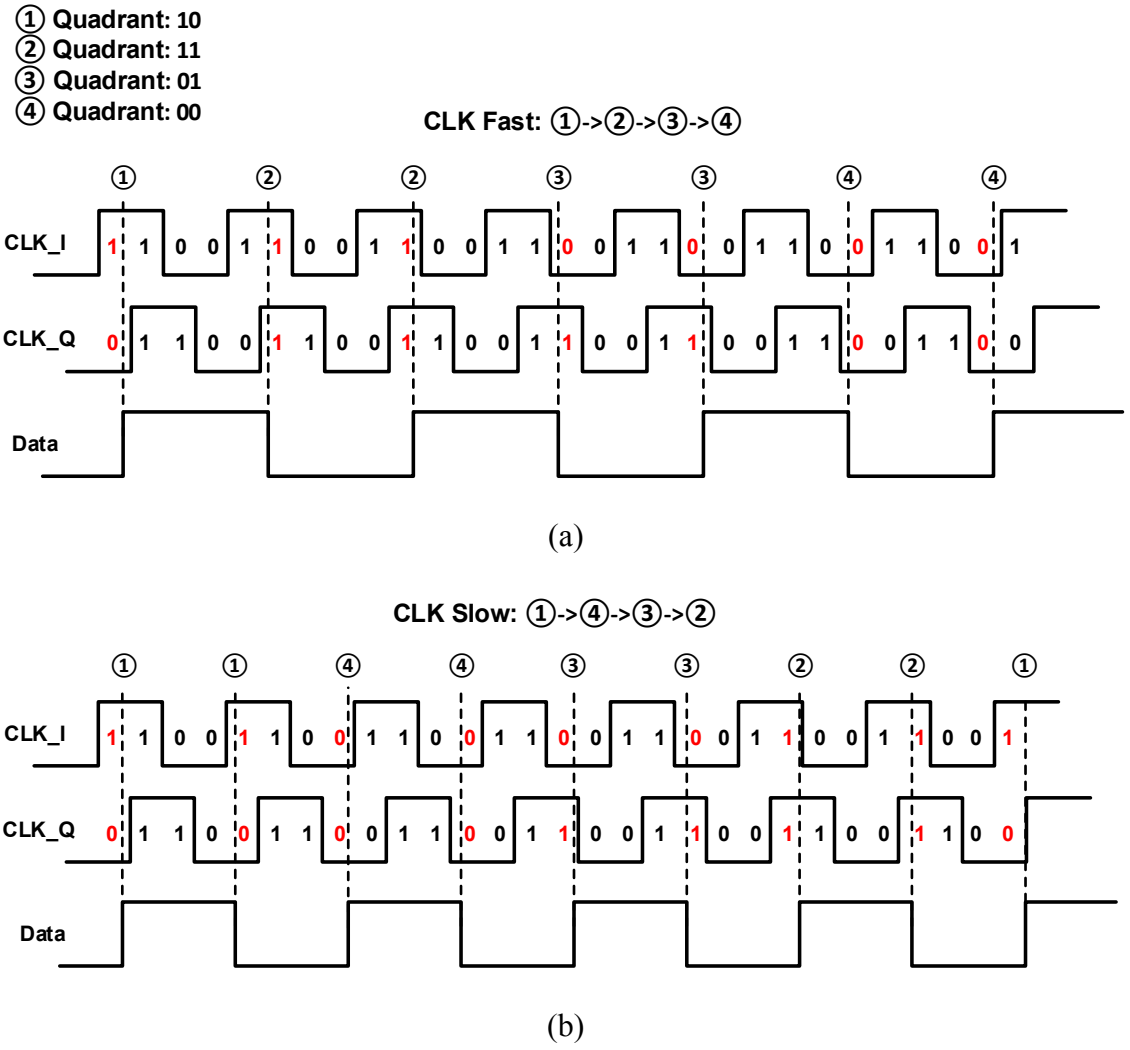


Fig. 3.12: Monitor cycle slip for (a) fast clock and (b) slow clock.

The cycle slip can be detected with Pottbacker frequency detector [33], rotational frequency detector [11] or bang-bang phase detector [34]. The operation of Pottbacker frequency detector and rotational frequency detector are similar to each other. They both

require full-rate I/Q clocks to define the clock quadrants rendering them to be useless in half-rate CDR topologies. The cycle slip detection based on the bang-bang phase detector, on the other hand, can be used in half-rate CDR. The bang-bang phase detector gives early/late decision based on the clock and data phase relationship. If there is no cycle slip, its output should stay in early or late.

The frequency detector implemented by monitoring cycle slip has the potential of false lock when the input is a short repetitive data pattern [36]. The essential feature of this data pattern is long gap of no data transitions that can straddle the point of cycle slip. As can be seen in Fig. 3.13, the situation of slow clock is used as an example. There is a period of data pattern that has a consecutive zeros. If cycle slip happens during that period, the frequency detector gives zero output even the frequency error exists. To avoid this situation, data scrambling has to be used to prevent short repetitive patterns.

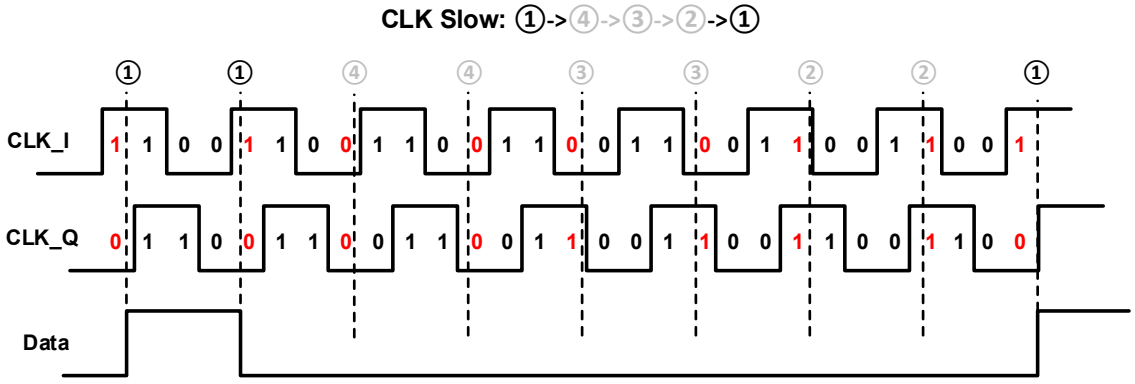


Fig. 3.13: Long gap of no data transition straddles cycle slip.

3.4.1.2 Frequency Detection by Edge Counter

Transition in the binary random data sequence is not regular and cannot be predicted. However, the number of data transitions over a long enough period of time is

expectable and proportional to the data rate and the transition probability P_{tran}. For random data, the transition probability P_{tran} is 50% (25% for rising edge and 25% for falling edge). In Fig. 3.14, numbers of rising edge of a data stream and a clock are counted in a long period of time so the data transition density is close to P_{tran} which is 50%. Then, the relationship between data rate F_{B} and clock frequency F_{clk} can be found by comparing $N_{cnt,data}/(0.5P_{tran})$ and $N_{cnt,clk}$.

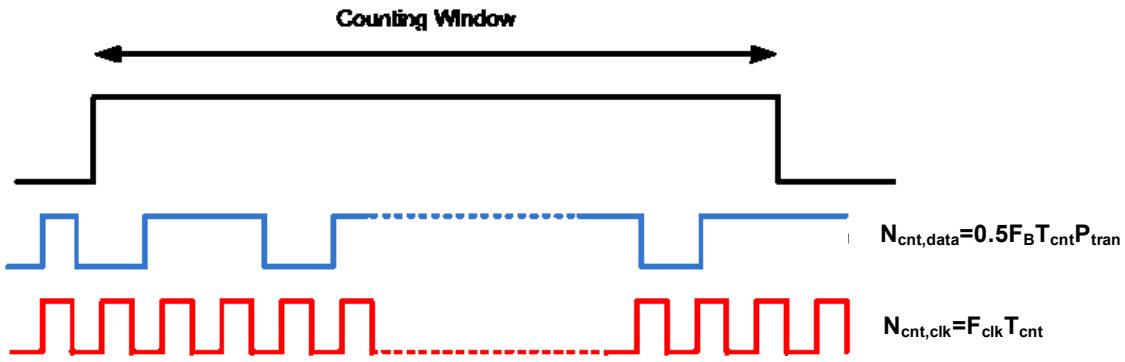


Fig. 3.14: Counting the number of rising edge for data and clock.

From the above analysis, it can be seen that the edge-counter-based frequency detector relies on the statistic property of the data stream instead of the phase information of a particular transition edge to extract the data rate information. Therefore, this frequency detector is insensitive to data pattern. Further, unlike the rotational frequency detector, this is not a sampling system. False lock to harmonics due to multiple nulls in the RFD transfer function does not exist [11].

The proposed CDR supports multiple phase detection modes. And a 16 GHz I/Q clock is not available in the system. Thus, the cycle slip monitor approach is not suitable to this design. The frequency detector based on edge counter in [35] supports half-rate phase detection. However, its supported phase detection mode is not adaptable. And its

application is limited to data streams with 50% transition density, which rules out the application where a non-50% transition data pattern such as K28.7 is used. In this design, a frequency locking loop topology that is adaptive to different phase detection mode is proposed and it also supports input data stream with transition density other than 50%.

3.4.2 Proposed Frequency Locking Loop

3.4.2.1 Architecture

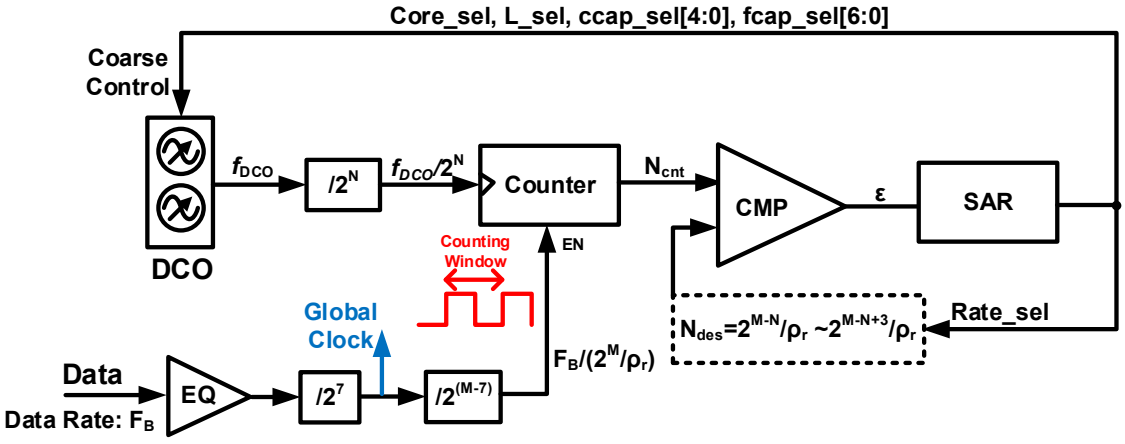


Fig. 3.15: Architecture of the proposed FLL.

The architecture of the proposed FLL is shown in Fig. 3.15. It is similar to a counter-based automatic frequency calibration (AFC) circuit in frequency synthesizers [37]. The data rising edge transition probability is assumed to be ρ_r. The data, after equalized, goes into a rising-edge-triggered divide-by-2 chain whose total division ratio is 2^M. The time period between two consecutive rising edges at the divider output is triggered by 2^M input rising edges. If M is large enough, the rising edge transition density can be assumed to be equal to the transition probability ρ_r. Then, the number of data within the

above time period is $2^M/\rho_r$ bits. As the data rate is F_B bits/sec, the length of the time period can be computed as $(2^M/\rho_r)/F_B$. Therefore, the divider output is a clock-like signal whose frequency is $F_B/(2^M/\rho_r)$. The period of the divider output sets a counting window during which the number of DCO clock cycles is counted. To relax the speed requirement of the counter, the DCO clock is pre-frequency-divided. The counting result in a counting window is $N_{cnt} = (2^{M-N}/\rho_r) \cdot f_{DCO}/F_B$. This result is compared to the counting target N_{des} where f_{DCO}/F_B is set according to the PLL phase detection mode. Then successive approaching algorithm is used to search for the desired DCO coarse tuning bits. The searching process is controlled by a finite state machine which uses the output of the seventh divide-by-2 as the global clock. In Fig. 3.15, the default setting of ρ_r is 25%. When unbalanced data pattern (*e.g.* K28.7, ρ_r=15%) is used, ρ_r in N_{des} can be set to accommodate the requirement.

A critical parameter in the proposed FLL is the length of divider-by-2 chain. The overall division ratio 2^M has to be large enough to justify the approximation of data transition density with data transition probability. Table 3.4 shows the calculation results of rising edge transition density and the approximation error for PRBS-31 and PRBS-15. It can be seen that the approximation is more accurate if more data samples are used to generate the counting window. It should be noted that the approximation error for PRBS-15 is small when M≥13. That is because one complete PRBS-15 period has 2^{13} rising edges. And the rising edge transition density in a complete PRBS-15 period is very close to 0.25. The frequency error due to the approximation error *err* can be computed with (3.21).

$$\frac{2^{M-N}}{\rho_r}\frac{f_{DCO}}{F_B}\frac{1}{1+\frac{err}{\rho_r}}=\frac{2^{M-N}}{\rho_r}\frac{f_{DCO,target}}{F_B} \tag{3.21}$$

Table 3.4: PRBS data transition density

M	2^M	$P_{den,rising}$ (PRBS-31)	Approx. Error (PRBS-31)	$P_{den,rising}$ (PRBS-15)	Approx. Error (PRBS-15)
1	2	0.250000	0.000%	0.333333	33.333%
2	4	0.210526	15.790%	0.400000	60.000%
3	8	0.195122	21.951%	0.285714	14.286%
4	16	0.228571	8.572%	0.262295	4.918%
5	32	0.244275	2.290%	0.278261	11.304%
6	64	0.262295	4.918%	0.260163	4.065%
7	128	0.251969	0.788%	0.258586	3.434%
8	256	0.258586	3.434%	0.251473	0.589%
9	512	0.253340	1.336%	0.251227	0.491%
10	1024	0.256385	2.554%	0.250306	0.122%
11	2048	0.252777	1.111%	0.250459	0.184%
12	4096	0.254016	1.606%	0.248333	0.667%
13	8192	0.252046	0.818%	0.250031	0.012%
14	16384	0.250784	0.314%	0.250019	0.008%
15	32768	0.250923	0.369%	0.250013	0.005%
16	65536	0.250764	0.306%	0.250010	0.004%
17	131072	0.250463	0.185%	0.250009	0.004%
18	262144	0.250328	0.131%	0.250008	0.003%
19	524288	0.250136	0.054%	0.250008	0.003%
20	1048576	0.249881	0.048%	0.250008	0.003%
21	2097152	0.249826	0.070%	0.250008	0.003%
22	4194304	0.249945	0.022%	0.250008	0.003%
23	8388608	0.249944	0.022%	0.250008	0.003%

Then, $f_{DCO}=(1+err/\rho_r)f_{DCO,target}$. Therefore, the approximation error in the 4th and the 6th columns of Table 3.4 is equal to the frequency error. Because the true random data does not have a complete period like PRBS-15, PRBS-31 is used as the design reference. *M* is set to be 22 in this design to keep the frequency error less than 1000 ppm which is the

CDR proportional path gain (lock range). *N* is set to be 3 in this design. The DCO clock frequency will be first divided by 8 before going into the counter.

3.4.2.2 FLL Operation Procedure

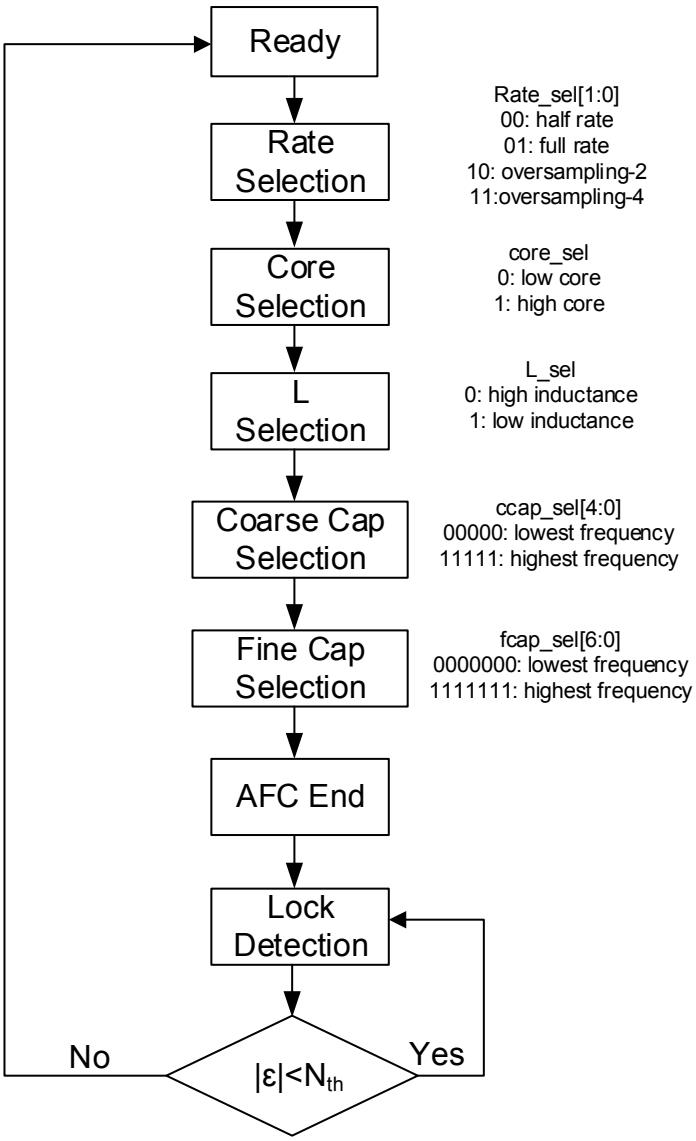


Fig. 3.16: FLL operation procedure.

Fig. 3.16 shows the operation procedure of the proposed FLL. It is an AFC process that sets all the DCO coarse tuning bits and drives the DCO frequency toward the target.

The first step of the AFC process is *Rate Selection* which determines the CDR phase detection mode.

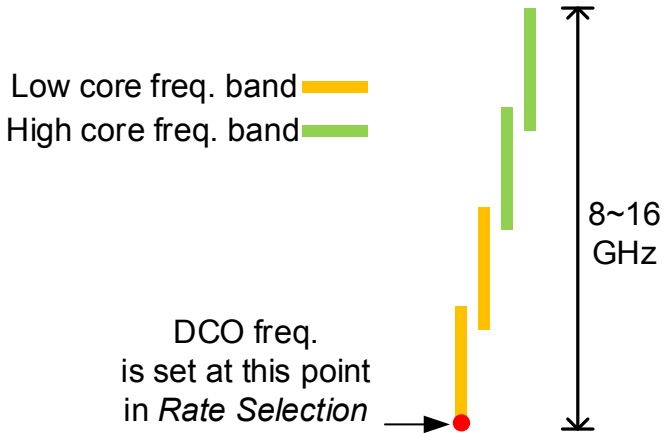


Fig. 3.17: DCO setting during *Rate Selection*.

The DCO in the CDR is composed by two cores and each core has two inductance settings. Therefore, the *core_sel* and *L_sel* tuning bits divide the DCO frequency range into 4 overlap sections. Fig. 3.17 illustrates the DCO frequency arrangement. As mentioned previously, the counting result in a counting window is $N_{cnt} = (2^{M-N}/\rho_r) \cdot f_{DCO}/F_B$. The desired f_{DCO}/F_B for different phase detection mode is shown in Table 3.5. It should be noted f_{DCO} is the clock frequency before the divide-by-2.

Table 3.5: Counting target for different phase detection modes

Phase Detection Mode	f_{DCO}/F_B	N_{des}
Half Rate	1	$2^{M-N}/\rho_r$
Full Rate	2	$2^{M-N+1}/\rho_r$
Oversampling-2	4	$2^{M-N+2}/\rho_r$
Oversampling-4	8	$2^{M-N+3}/\rho_r$

During the *Rate Selection*, the DCO is set at the lowest frequency. The counting result N_{cnt} is the smallest possible counting value for a particular data rate. If it is larger

than N_{des}, then it is not possible find a set of DCO control bits that drives N_{cnt} toward N_{des}. Therefore, the *Rate Selection* starts the comparison from the half-rate N_{des} and ends when $N_{cnt}<N_{des}$ is detected. When it ends, the phase detection mode and N_{des} are determined for the following FLL and PLL operations.

The second step of the AFC process is *Core Selection*. It determines which DCO core should be activated. The DCO frequency is set at the highest frequency point of the low core DCO at the beginning of *Core Selection.* Fig. 3.18 shows the DCO setting. This stage can be completed by one comparison. If $N_{cnt}>N_{des}$, low core will be selected. Otherwise, high core will be selected.

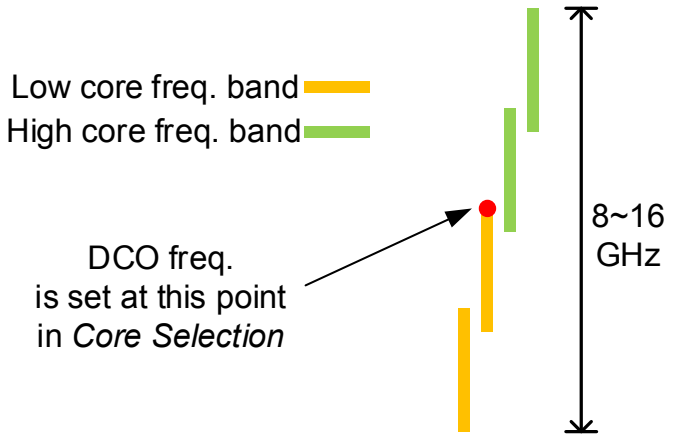


Fig. 3.18: DCO setting during *Core Selection*.

The third step of the AFC process is *L Selection* which determines the inductance tuning bit. In this stage, *core_sel* has been set in the previous searching process. For that selected core, the DCO frequency is set at the highest frequency point when inductor switch is off (high inductance). Assume that low core has been selected, the initial setting of the DCO frequency is illustrated in Fig. 3.19. This stage is also completed by one comparison. If $N_{cnt}>N_{des}$, inductor switch should be off. Otherwise, the switch will be turned on.

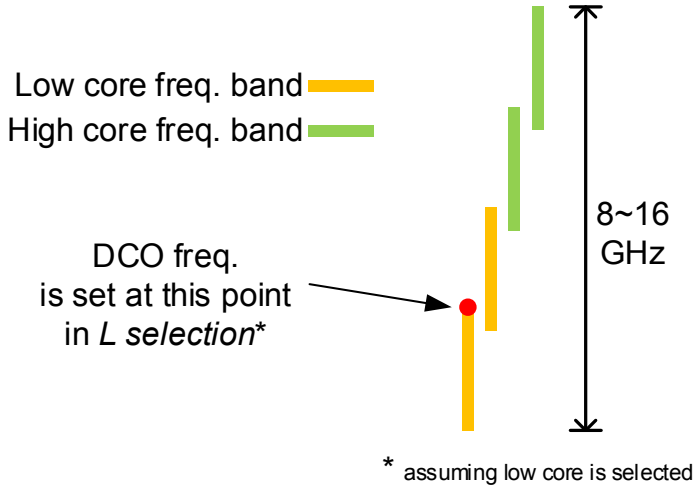


Fig. 3.19: DCO setting during *L Selection*.

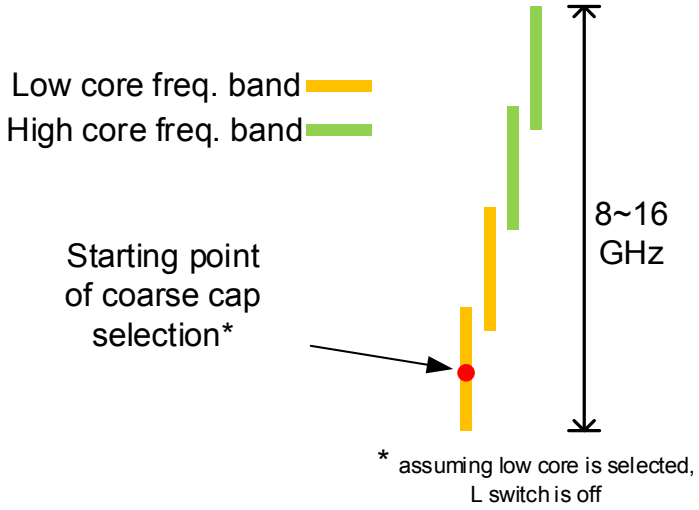


Fig. 3.20: DCO setting at the beginning of *Coarse Cap Selection*.

The fourth step is *Coarse Cap Selection* which sets the coarse capacitor tank tuning bits. This searching process starts at the mid-point of a frequency band for a particular core and inductor switch setting. Assuming that the low core has been selected and the inductor switch is turned off in the previous AFC searching steps, Fig. 3.20 illustrates the initial setting. There are 5 tuning bits for the coarse capacitor tank. SAR binary searching

algorithm is used to find the frequency point that is closest to the target frequency. The frequency step of the coarse capacitor tuning is about 140 MHz. Therefore, the frequency error after this step is in the range from 4375 ppm to 8750 ppm which is not small enough to guarantee phase locking. Another step is needed to drive the DCO frequency to the target with a finer resolution. The fine capacitor tank has a frequency step of 2.3 MHz which leads to a residual frequency error being much smaller than the CDR proportional path frequency step securing a safe phase locking. The final AFC step *Fine Cap Selection* will set the tuning bits for the fine capacitor tank.

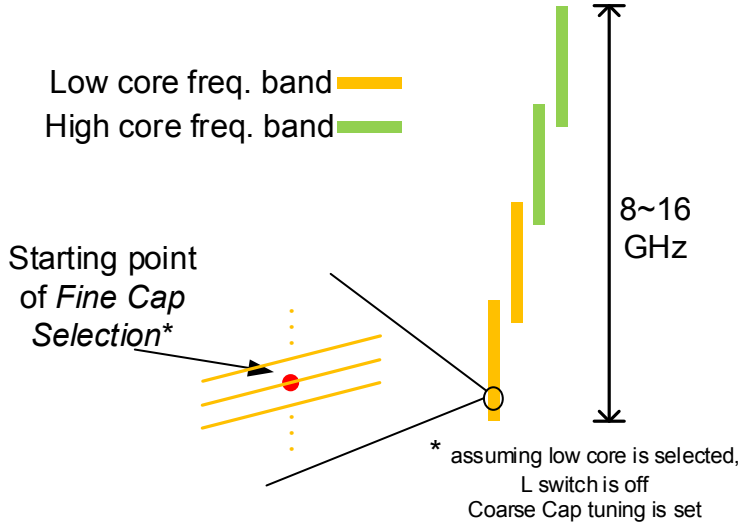


Fig. 3.21: DCO setting at the beginning of *Fine Cap Selection*.

Fig. 3.21 shows the initial setting of *Fine Cap Selection*. It is assumed that the low core has been selected, the inductor switch is turned off and the coarse capacitor tank tuning bits are set in the previous AFC searching steps. For a particular setting of the above tuning bits, the fine capacitor tank extends the frequency point to a frequency tuning curve that contains 127 frequency steps (7-bit). The *Fine Cap Selection* searching process starts at the

mid-point of a tuning curve. Then, SAR binary searching algorithm is used to find the frequency point that is closest to the target frequency.

After the above five steps, the AFC process ends and the FLL-controlled tuning bits are frozen. The DCO control is handed over to the PLL and the FLL stays in *lock detection* mode. In *lock detection* mode, FLL monitors the DCO frequency by evaluating the absolute value of ε, difference of N_{cnt} and N_{des}. Whenever $|\varepsilon|$ is found larger than the pre-defined threshold N_{th}, the DCO is considered to be loss of lock and the FLL process starts again.

3.4.2.3 High Frequency Divider

In the proposed FLL, the first 7 stages of the data transition counters (divide-by-2) should be custom-designed to accommodate the high data rate input. Typically, the high frequency divider can be implemented with CML logic or TSPC logic. However, the wide range of input data rate poses great challenges to their design. The functionality of a CML frequency divider is sensitive to the input signal amplitude. It is characterized with the sensitivity curve shown in Fig. 3.22 which defines the minimum required input swing as a function of the operation frequency [38].

The CML frequency divider has a self-resonance frequency f_{osc} around which the minimum required input swing is small. As the input operation frequency deviates from $2f_{osc}$, the required input swing increases rapidly. In this design, the input data rate ranges from 1 Gbps to 16 Gbps. It is hard to design a CML frequency divider that can safely cover that wide range of data rate across PVT variation.

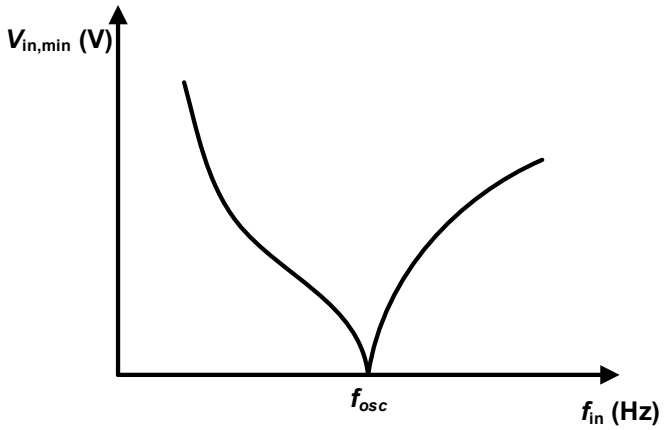


Fig. 3.22: Sensitivity curve for a CML frequency divider.

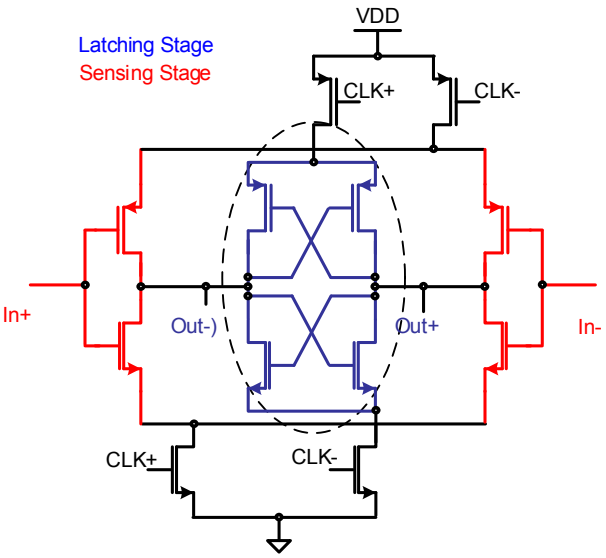


Fig. 3.23: C^2MOS latch.

The TSPC frequency divider is a digital-intensive solution and does not have the problem of the CML frequency divider. However, it is a dynamic logic and is sensitive to leakage current. If the TSPC divider is designed for the highest data rate, then the leakage current becomes a big issue for the lowest data rate, especially when data has long consecutive ‘0’ or ‘1’.

Based on the above discussion, neither CML nor TSPC is used for this design. Instead, a C^2MOS frequency divider is adopted [39]. The C^2MOS frequency divider is composed with two C^2MOS latch which combines the C^2MOS dynamic latch with a latching stage (Fig. 3.23). The sensing stage is simply two CMOS inverters while the latching stage is a pair of back-to-back connected inverters. There is no DC biasing current for the latch, thus no self-oscillation point exists in the frequency divider. Due to the positive feedback of the latching stage, the latch is not sensitive the leakage current. Therefore, as long as the C^2MOS frequency divider is fast enough for the highest input data rate, the lowest input data rate can also be safely covered. In the proposed FLL, the first seven stages of the data transition counters are all implemented with the C^2MOS frequency divider. The following stages of counter are implemented with semi-custom-designed CMOS D-flip-flops.

3.5 Simulation Results

3.5.1 DCO Simulation Results

The DCO shown in Fig. 3.8 is implemented with a 65 nm CMOS technology. The biasing current of the high frequency core varies from 2.5 mA to 12.5 mA; for the low frequency core, its range is from 3 mA to 13 mA. The DCO output range is designed to be 7.6 GHz ~17.5 GHz at room temperature and typical process corners. The frequency tuning range for the two cores is simulated and shown in Fig. 3.24.

Each curve in Fig. 3.24 represents a core selection and an inductor switch setting. The lower two curves are the frequency ranges that the low DCO core covers. The upper

two curves are the frequency ranges that the high DCO core covers. With inductive tuning, the highest frequency that the low DCO core covers has been extended from 10.9 GHz to 12.7 GHz. For the high DCO core, the highest frequency is extended from 15 GHz to 17.5 GHz. Table 3.6 summarizes the frequency range simulation results of the DCO circuit.

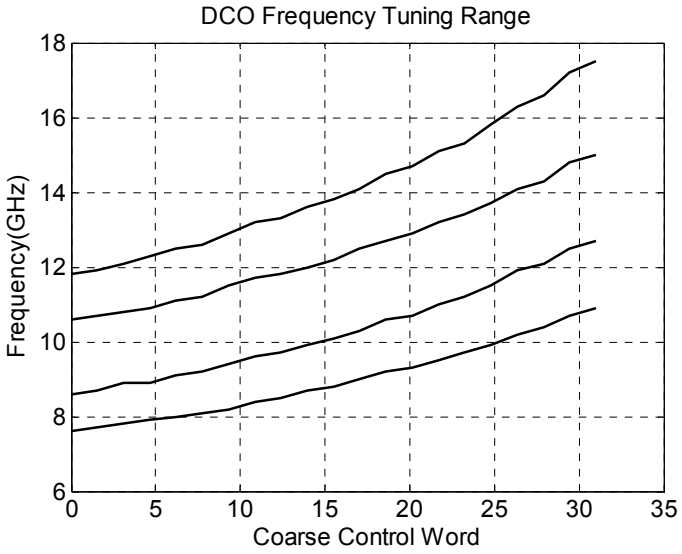
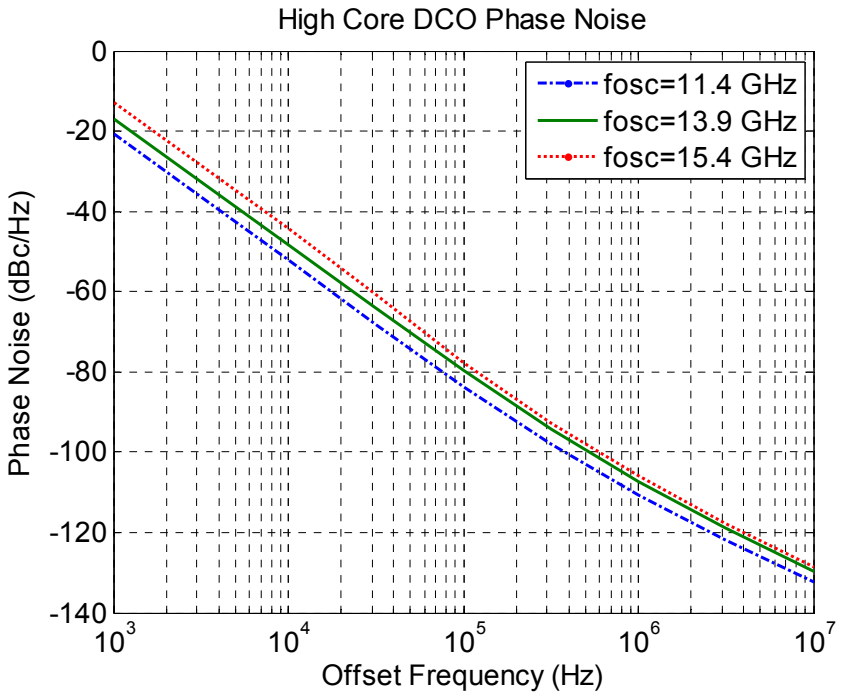
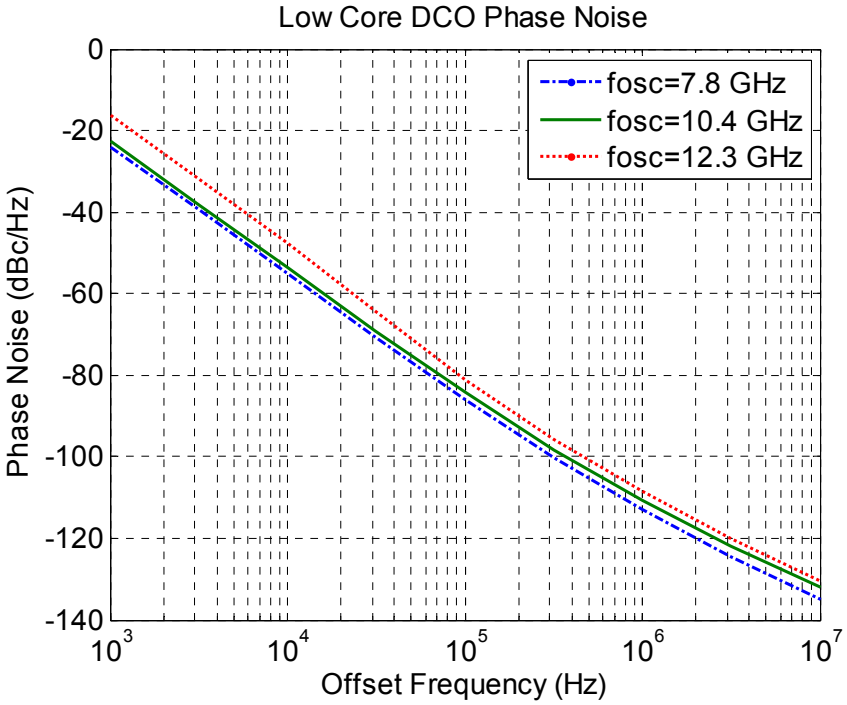


Fig. 3.24: DCO frequency tuning range.

To evaluate the DCO phase noise performance, Fig. 3.25, Table 3.7 and Table 3.8 shows the phase noise simulation results at three operation frequencies for each DCO core. The simulation is run with the divide-by-2 connected to the DCO cores. The Figure-of-Merit (FOM), defined in [40], is above 180 dB across the simulated frequencies. The DCO in this work is compared to the existing wideband DCOs and the result is shown in Table 3.9.



(a)



(b)

Fig. 3.25: Phase noise simulation results (a) high frequency core (b) low frequency core.

Table 3.6: Frequency range of the DCO

Core	L Control	Frequency Range	Frequency Range Extension Ratio due to L tuning
High Core	0	10.6 GHz~15 GHz	54%
	1	11.8 GHz~17.5 GHz	
Low Core	0	7.6 GHz~10.9 GHz	56.8%
	1	8.6 GHz~12.7 GHz	

Table 3.7: High frequency DCO core phase noise post-layout simulation results

L/C_coarse	Temperature /Corner	f_o (GHz)	PN @ 1 MHz (dBc/Hz)	Differential output Amp./Biasing Current	FOM (dB)
0/00111	27 °C, TT	11.4	-110.7	769 mV/6.9 mA	182.6
1/10000	27 °C, TT	13.9	-107.5	723 mV/6.8 mA	181.2
1/11000	27 °C, TT	15.4	-105.9	728 mV/ 5.2 mA	181.7

Table 3.8: Low frequency DCO core phase noise post-layout simulation results

L/C_coarse	Temperature /Corner	f_o (GHz)	PN @ 1 MHz (dBc/Hz)	Differential output Amp./Biasing Current	FOM(dB)
0/00111	27 °C, TT	7.8	-113.1	675 mV/7.2 mA	181.6
0/11111	27 °C, TT	10.4	-110.7	508 mV/2.4 mA	186.5
1/11111	27 °C, TT	12.3	-108.6	714 mV/4.8 mA	182.8

Table 3.9: Wideband DCO comparison

	[27]	[28]	This work
Technology	45nm SOI	130 nm CMOS	65 nm CMOS
Tuning range	5.67 GHz~12.09GHz	5.6 GHz~11.5 GHz	8 GHz~16 GHz
Area	0.111 mm^2	1 mm^2	0.178 mm^2
Power	2.9 mW~3.8 mW	16.8 mW~44.4 mW[1]	3 mW~15 mW
Phase noise(dBc/Hz) @ 1MHz offset freq.	-110 @ 5.98GHz	-116 @ 4.98 GHz	-110.7 @ 11.4 GHz
FOM (dB)	180	NA	182.6

[1] Include divider and mux

3.5.2 Digital FLL Simulation Results

The FLL circuit has been verified with Cadence AMS simulator. Fig. 3.26 shows the simulation setup. The DCO is described by a Verilog-A model. The four sections of the DCO frequency range for the FLL simulation is shown in Table 3.10. The divider and PRBS generator are also described by Verilog-A models. The FLL is described by Verilog netlist.

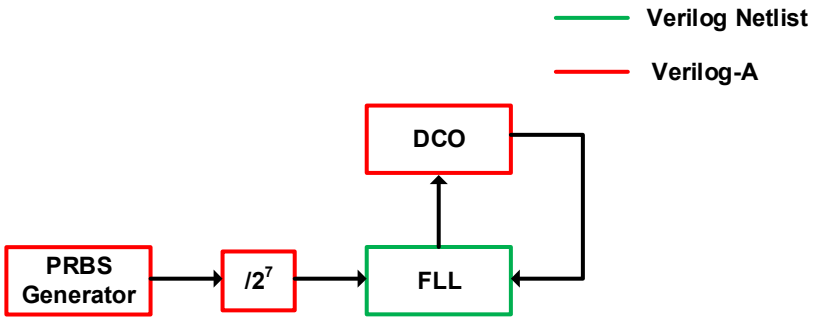


Fig. 3.26. FLL simulation setup.

Table 3.10: Frequency ranges of the Verilog-A-described DCO

Core_sel	L_sel	Frequency
0	0	7.8~10.2 GHz
0	1	9.8~12.2 GHz
1	0	11.8~14.2 GHz
1	1	13.8~16.2 GHz

In order to rule out the DCO frequency quantization impact on the frequency searching accuracy and focus on the effect of the division ratio 2^M, the DCO tuning range and the fine tuning step have been set to be smaller than the designed DCO circuit. They are 7.8 GHz~16.2 GHz and 0.59 MHz in the simulation.

Fig. 3.27 shows the FLL searching process for a 10 Gbps PRBS-31 data stream. *M* is chosen to be 18. The searching process takes 1.8 ms. The DCO frequency is driven to 10 GHz at the end with an error of 96 ppm. This error is smaller than the result predicted by (3.21). That is because what (3.21) shows is the worst case result. Fig. 3.28, Fig. 3.29 and Fig. 3.30 show the FLL process for other phase detection mode. The three simulations are done with PRBS-15 and *M*=15. Fig. 3.31 shows the case when unbalanced data pattern (k28.7) is fed to the FLL. The circuit is programmed for 30% transition density and the DCO is driven to the target frequency when the AFC process ends.

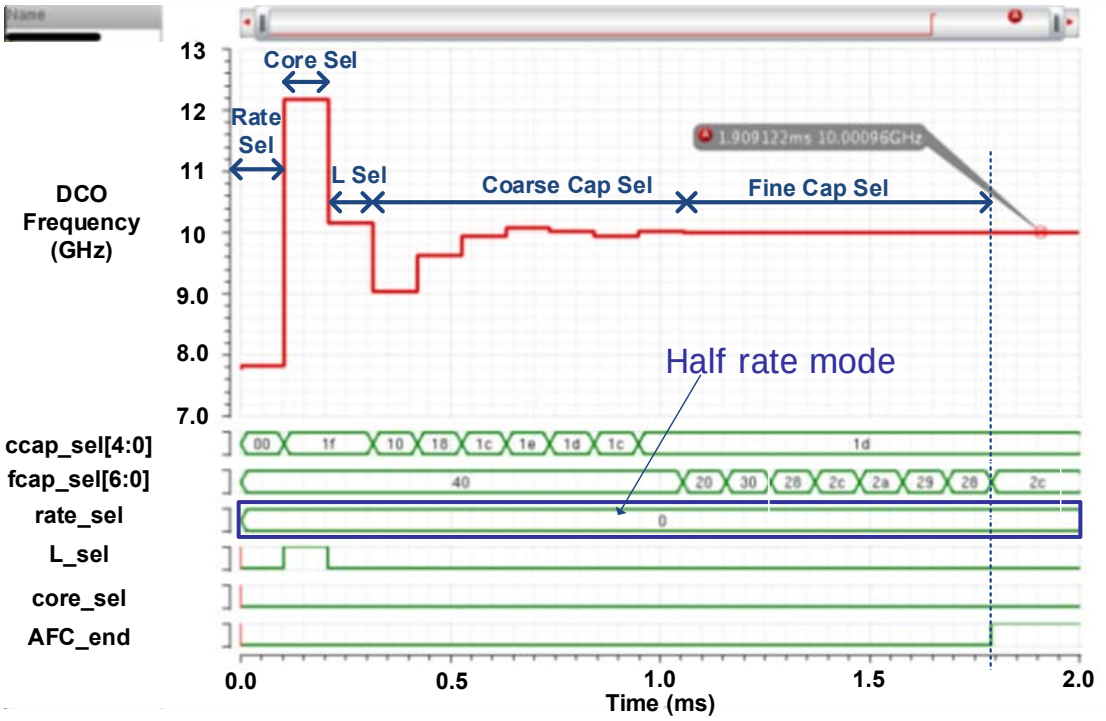


Fig. 3.27: FLL process of 10 Gbps PRBS-31.

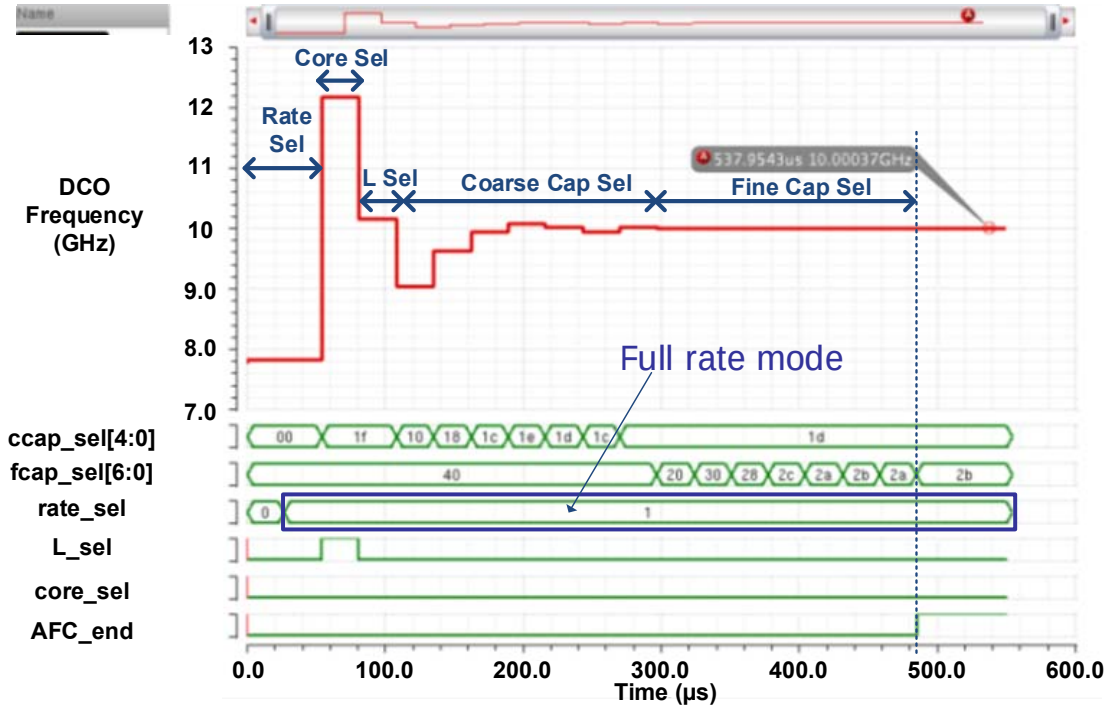


Fig. 3.28: FLL process of 5 Gbps PRBS-15.

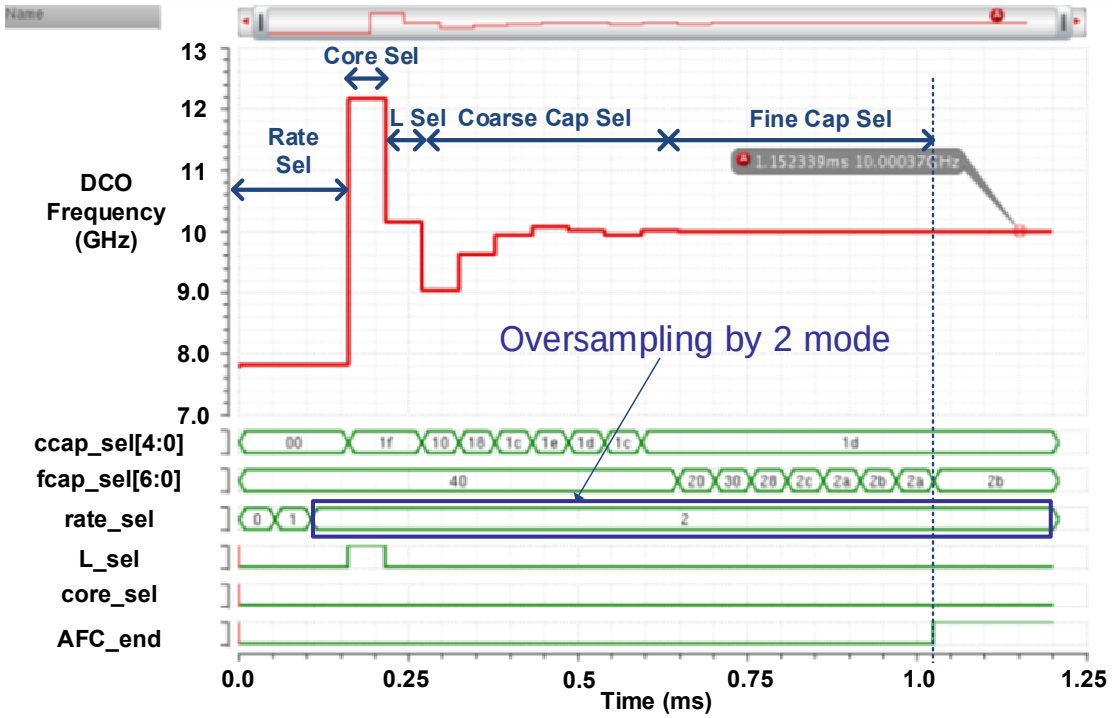


Fig. 3.29: FLL process of 2.5 Gbps PRBS-15.

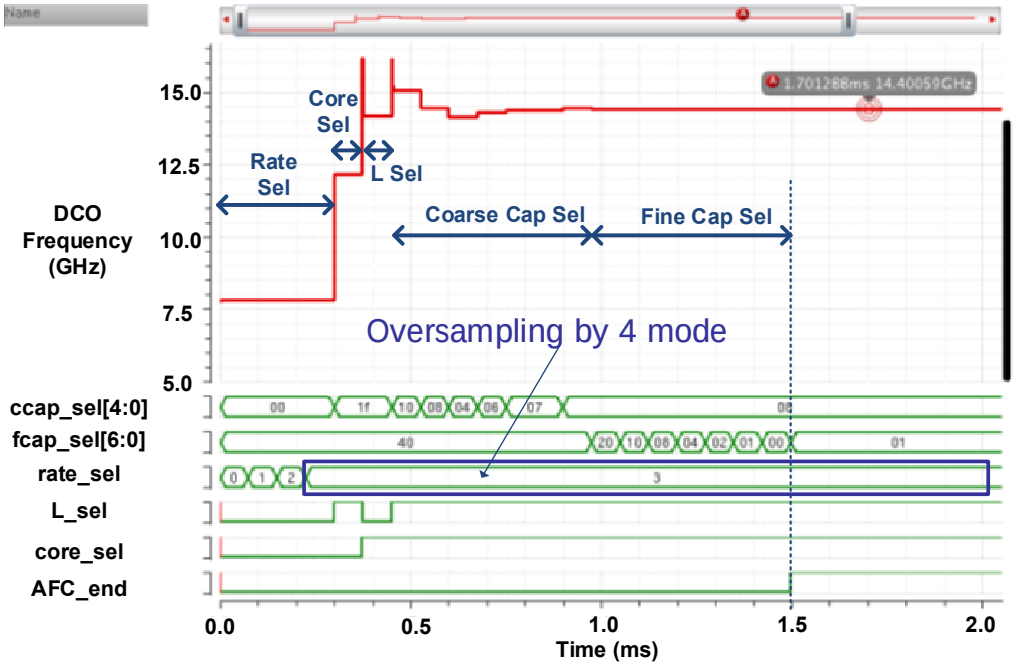


Fig. 3.30: FLL process of 1.8 Gbps PRBS-15.

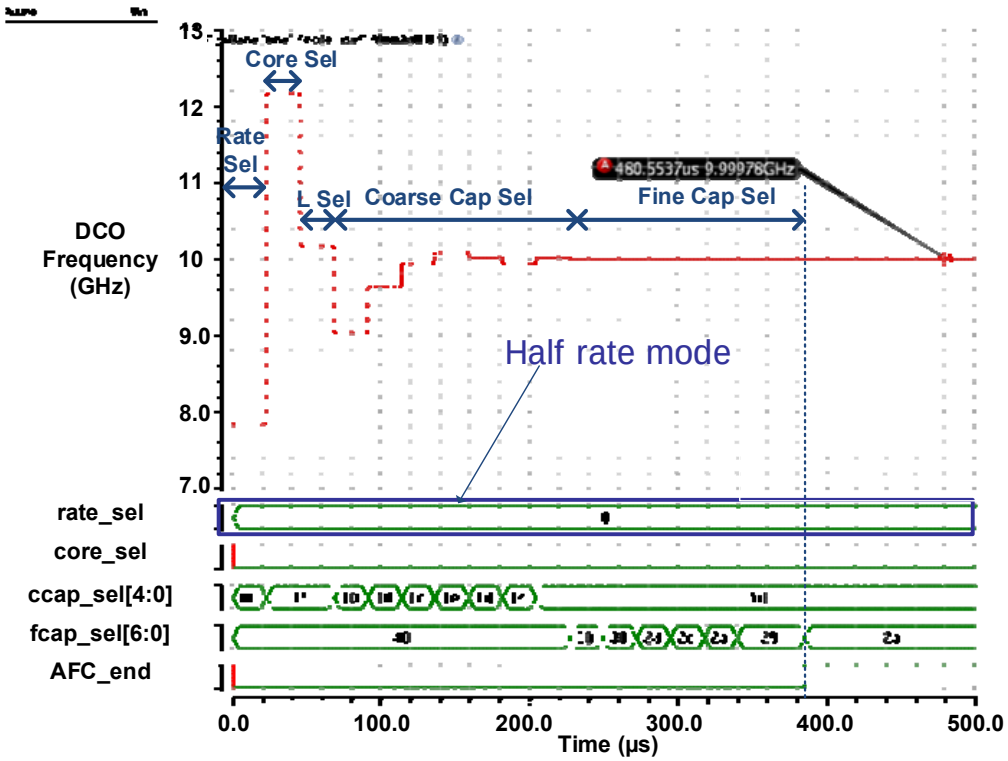


Fig. 3.31: FLL process of 10 Gbps K28.7 data pattern.

3.5.3 CDR Simulation Results

In order to evaluate the CDR loop stability and jitter performance, the CDR needs to be modeled as a frequency domain transfer function. However, the bang-bang CDR does not have a transfer function as the binary phase detector is nonlinear. Technique of linearizing the phase detector transfer curve has been developed to derive an expected transfer function for it [41]. Then the random jitter can be found using traditional linear analysis. Nevertheless, this approach needs to have the knowledge of input jitter and is only valid when the input jitter is large enough to scramble the bang-bang PD quantization error [41]. These pose a problem to practical applications for which the input jitter is not known. Furthermore, the input jitter should be small and ideally be zero when evaluating the CDR jitter generation. In this case, the PD linearization approach is not valid for JGEN calculation [41]. For JTRAN and JTOL evaluations, the input is modulated by sinusoidal jitter. The linearized PD transfer function is also not applicable as it is derived under the assumption of Gaussian distributed random input jitter. Therefore, the frequency domain approach is not used for the CDR in this design. Instead, to tackle the problem of stability and jitter simulations, a time-domain Simulink CDR behavior model is developed.

Fig. 3.32 shows the CDR Simulink model. The model is a multi-rate discrete time system which processes data and clock phases instead of their voltage waveforms. This greatly improves the simulation speed. The bang-bang phase detector is modeled as a subtractor plus a one-bit quantizer. The quantizer output is modulated by a signal which represents whether the consecutive binary data are identical. If the consecutive binary data are identical, the phase detection result is *hold* which is represented by ‘0’. If they are not identical, then *early* or *late* will be determined. The majority voter takes 16 samples of

phase detection results and combines them into one by voting. The other blocks in the CDR are modeled by their z-domain or s-domain models. The jitter due to the quantization effect has been inherently included in the model. For the random noise sources, the DCO and the input are the main contributors. Their noise is injected into the system as illustrated in Fig. 3.32. With all the jitter sources included, the Simulink model can be used to determine the JGEN, JTRAN and JTOL of the CDR.

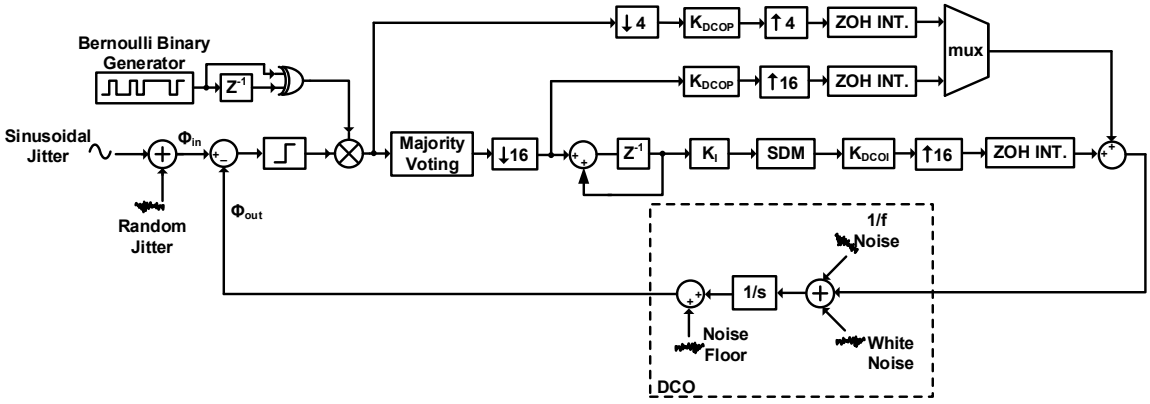


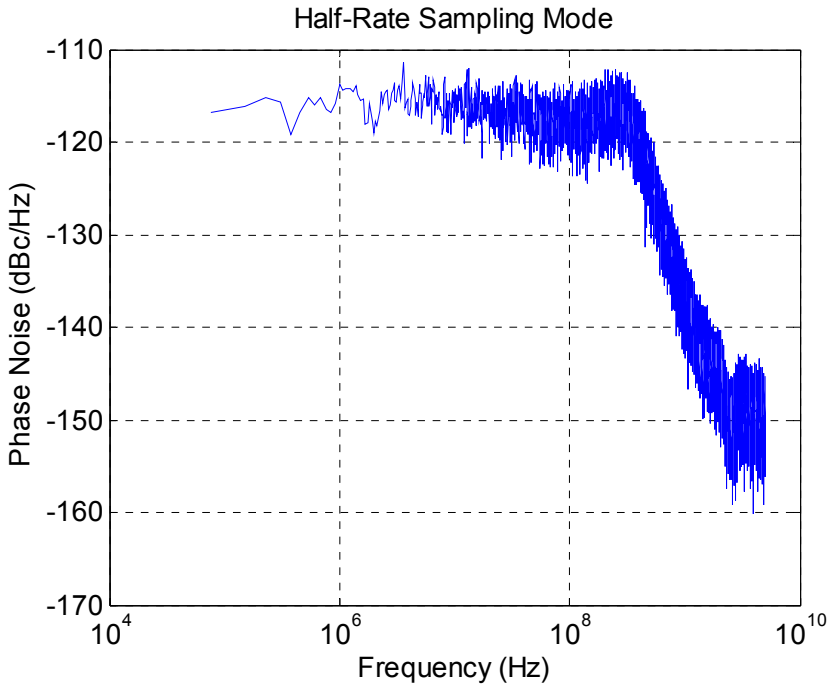
Fig. 3.32: CDR phase domain Simulink model.

For JGEN simulation, the input jitter is disabled. The output phase Φ_{out} contains the DCO phase noise and the loop quantization noise. Its power spectral density (PSD) which is the recovered clock phase noise is estimated using Welch method. Fig. 3.33 shows the simulation results for 10 Gbps and 5 Gbps input data rate. In half-rate sampling mode (10 Gbps), the fast BB-path is used. The bang-bang tracking jitter is small and the limit cycle oscillation is not obvious. Therefore, no spurious tone can be observed in the phase noise plot, Fig. 3.33(a). In full-rate sampling mode (5 Gbps), the slow BB-path is used. The output jitter is dominated by the bang-bang tracking jitter. The spurious tones are obvious in the phase noise plot, Fig. 3.33(b). For other sampling mode, the DCO frequency

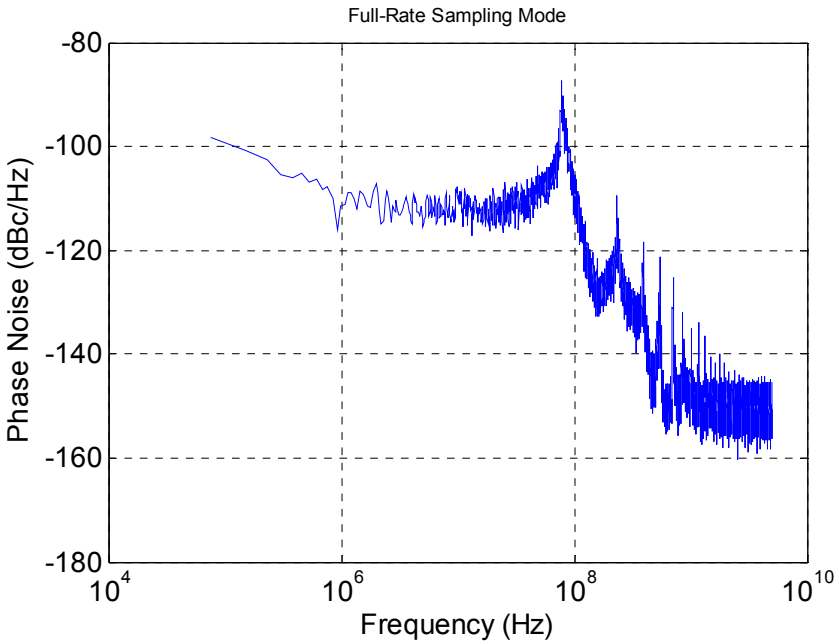
is unchanged and the slow BB-path is used. Therefore, the phase noise is the same as that of the full-rate mode. For wireline communication, it is of more interest to describe the clock phase noise in the time domain. The total jitter of the output clock includes random jitter from the DCO and deterministic jitter from the bang-bang tracking operation. It can be evaluated with the simulated phase errors. Table 3.11 summarizes the simulation results.

Table 3.11: JGEN simulation results.

Data Rate	Total Jitter (RMS, mUI)	Total Jitter (peak-peak, mUI)
10 Gbps (Half-rate)	7	40.2
5 Gbps (Full-rate)	9.2	48.3
2.5 Gbps (Oversampling-2)	4.4	26.6
1.25 Gbps (Oversampling-4)	2.1	14.4



(a)



(b)

Fig. 3.33: Simulated phase noise of the recovered clock (a) Fast BB-path enabled (b) Slow BB-path enabled.

JTRAN is simulated by applying sinusoidal jitter to the CDR model. The CDR output phase tracks the input. Thus, there is a spurious tone in both PSDs of the input and output phases at the jitter modulation frequency. The relative magnitude of the output tone normalized to the input magnitude is the JTRAN magnitude at the modulation frequency. By repeating the simulation for a range of modulation frequencies, the JTRAN plot can be generated. Fig. 3.34 shows the time domain phase tracking behavior of the CDR in the half-rate sampling mode. The input sinusoidal jitter has an amplitude of 0.4 UI and a frequency of 4 MHz. The JTRAN and jitter peaking for the four sampling modes are shown in Fig. 3.35, Fig. 3.36, Fig. 3.37 and Fig. 3.38. The jitter peaking plots are the zoom-in of the JTRAN around the bandwidth frequency.

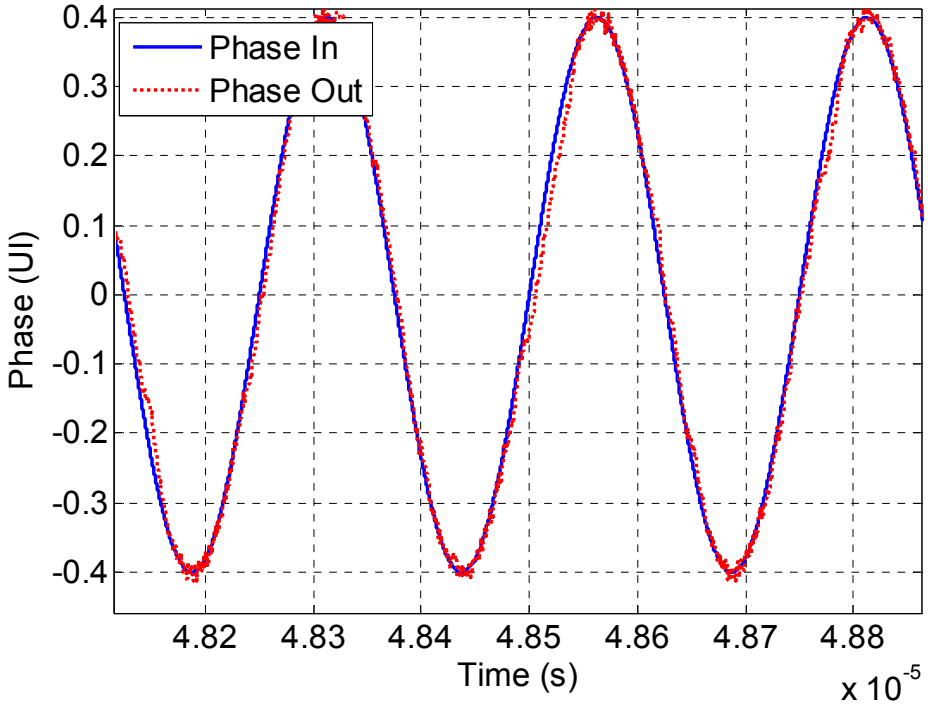
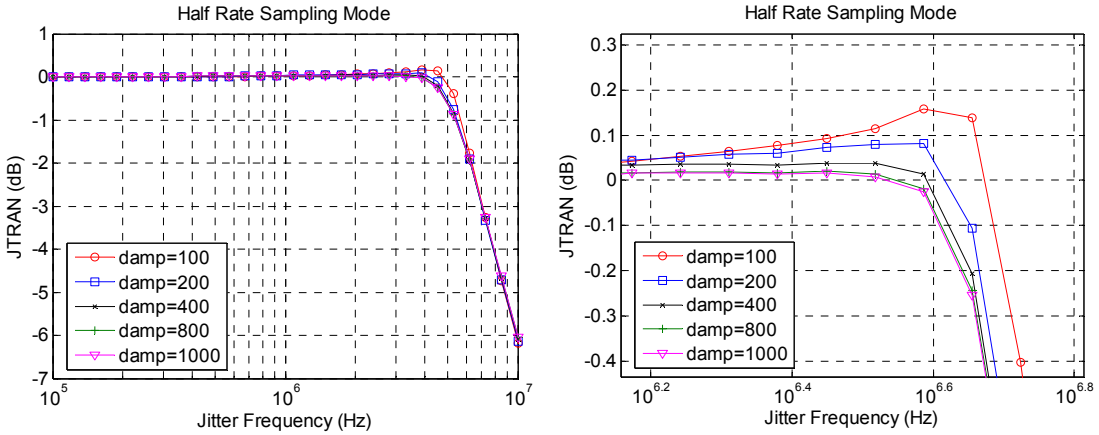
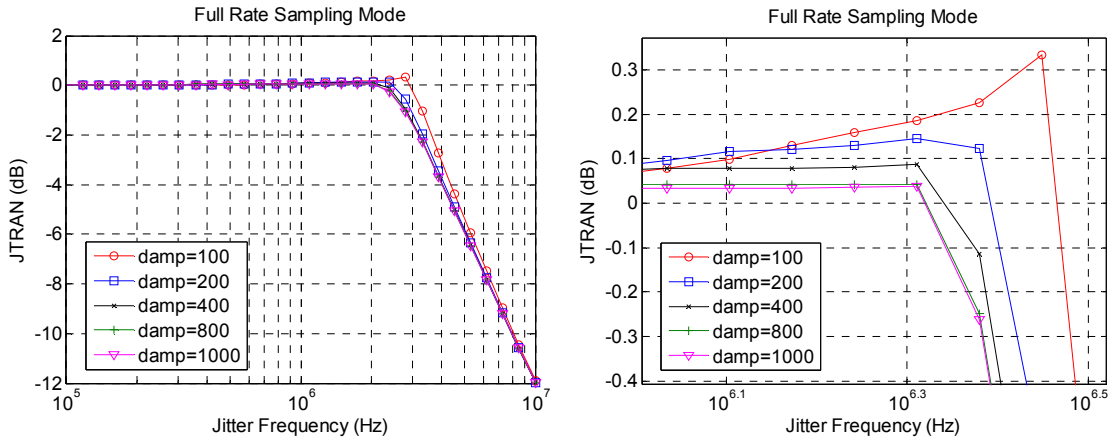


Fig. 3.34: CDR phase tracking behavior.



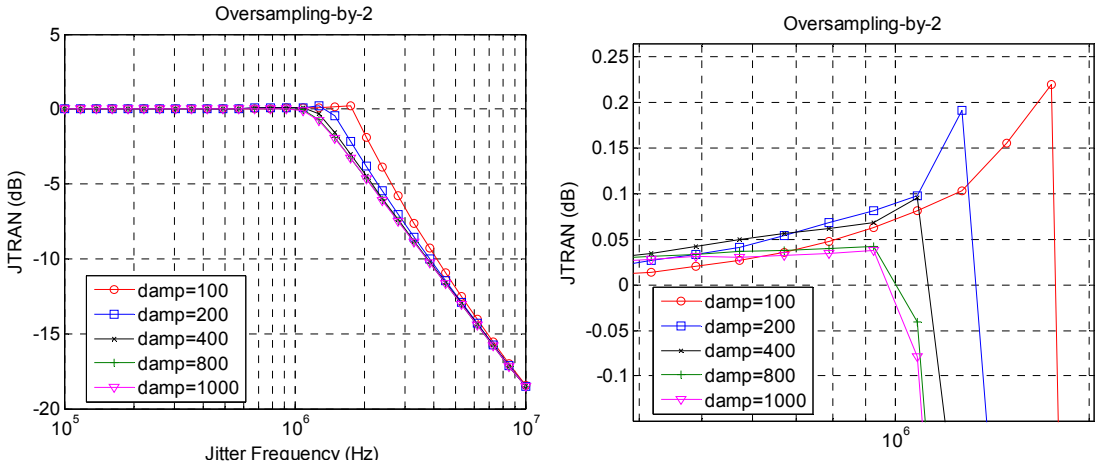
(a) (b)

Fig. 3.35: (a) JTRAN and (b) jitter peaking of CDR in the half-rate sampling mode.



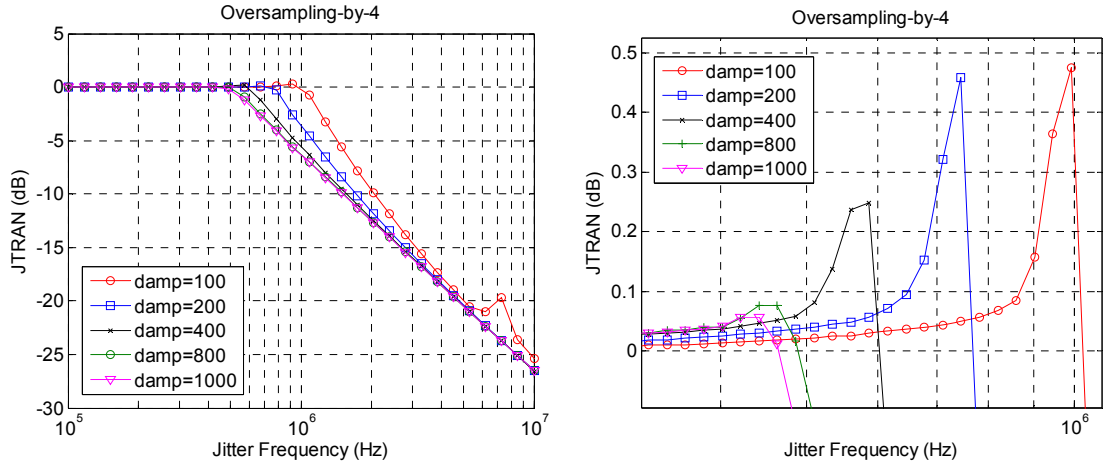
(a) (b)

Fig. 3.36: (a) JTRAN and (b) jitter peaking of CDR in the full-rate sampling mode.



(a) (b)

Fig. 3.37: (a) JTRAN and (b) jitter peaking of CDR in the oversampling-by-2 mode.



(a) (b)

Fig. 3.38: (a) JTRAN and (b) jitter peaking of CDR in the oversampling-by-4 mode.

All the above simulations are run with a jitter amplitude of 0.4 UI. As can be seen in the JTRAN curves, the bandwidth is scaled from 4 MHz to 500 kHz as the ratio of DCO frequency over data rate is increased. The tracking bandwidth is mainly determined by the proportional path gain. A higher gain of the integral path is able to extend the bandwidth, but the jitter peaking becomes higher. The parameter *damp* in this simulation is the stability factor which is defined in (3.7). It needs to be larger than 800 to ensure a jitter peaking being less than 0.1 dB. As mentioned above, the stability factor is 1113 in this design.

The JTOL performance is achieved by applying sinusoidal jitter to the CDR model and finding out the maximum jitter amplitude that gives a phase error which is less than the jitter budget. If the jitter budget is 0.2 UI (0.6 UI input eye closure), then the JTOL in the four sampling modes can be drawn in Fig. 3.39. The proposed CDR satisfies the SONET JTOL requirements defined in Table 3.1.

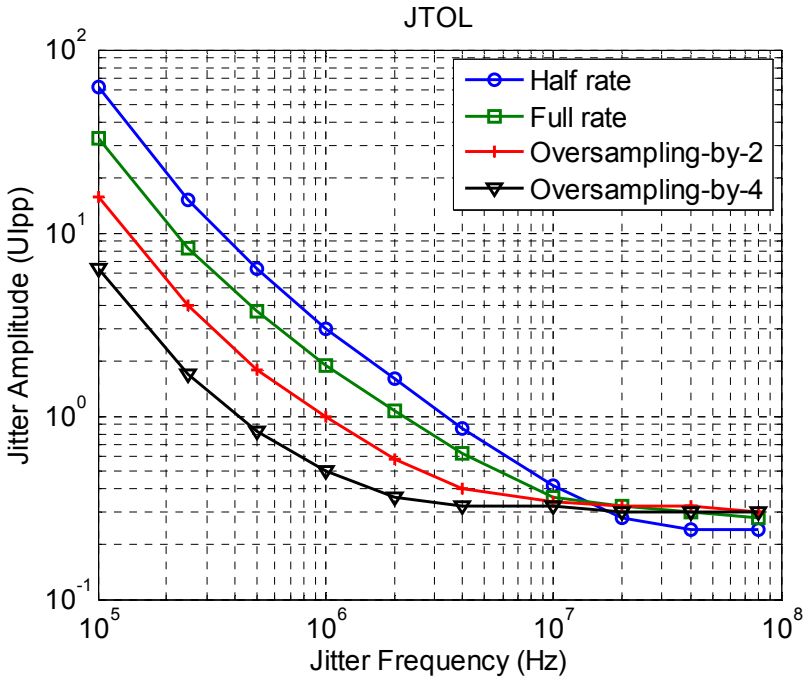


Fig. 3.39: Jitter tolerance simulation results.

Next, the post-layout simulation results of the CDR are shown. The proposed CDR has been implemented with a 65-nm CMOS technology. The layout is shown in Fig. 3.40. The core area of the CDR is 0.67×1.01 mm^2. The supported data rate is from 1 Gbps to 16 Gbps. The CDR operates from a single 1.2 V supply and the overall power consumption ranges from 67.2 mW to 92.5 mW in the half-rate sampling mode. The de-serializers, divide-by-2/multiplexer, DCO and synthesized digital blocks consumes 34.1 mW, 11.5 mW~20.0 mW, 3.6 mW~15.6 mW and 18 mW~22.8 mW, respectively. For the sampling modes other than the half-rate, one of the de-serializers can be turned off to save 17.05 mW of power. Besides the circuit blocks shown in Fig. 3.1, the system also includes a 16-to-1 serializer and a first-in-first-out (FIFO) register which are used to combine the recovered data back into a high speed data stream for bit error rate simulation and future measurements.

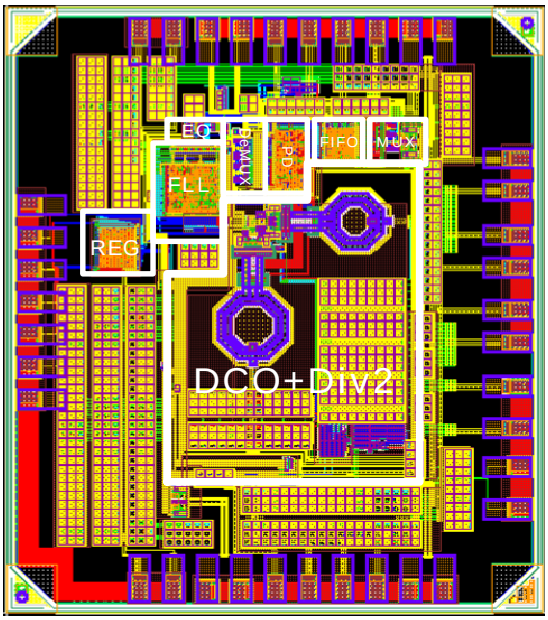


Fig. 3.40: CDR layout.

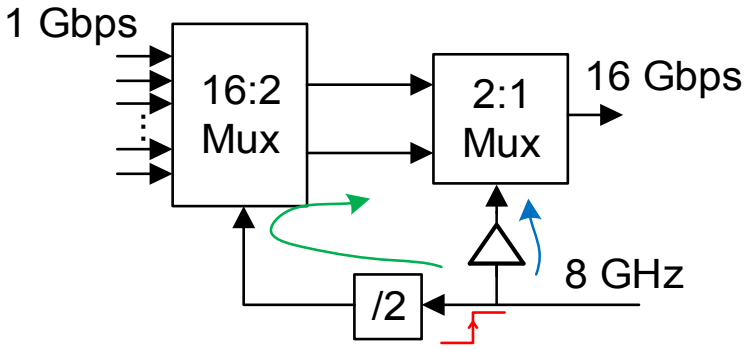


Fig. 3.41: 16-to-1 serializer.

The serializer which is composed of cascased 2-to-1 serializers is shown in Fig. 3.41. In the clock path for the last 2-to-1 serializer stage, a clock buffer is inserted to balance the data path delay from the divide-by-2 and the previous 2-to-1 serializer stage. By doing so, the data serializing operation in the last stage can have enough timing margin.

Although the clocks for the 1-to-16 de-serializer and the 16-to-1 serializer are both from the DCO, the delays of the clock paths in these two blocks are different due to the

circuit and loading mismatch. To guarantee a correct timing for data transfer between the 1-to-16 de-serializer and the 16-to-1 serializer, a FIFO is needed to buffer the recovered data from the 1-to-16 de-serializer. The FIFO schematic is shown in Fig. 3.42 [42]. The FIFO contains eight banks of DFF registers. Each bank is 16-bit wide receiving data from the de-serializer. The write address pointer and the read address pointer are designed to have an offset of 4 rows. Therefore, the phase of writing clock and reading clock is allowed to drift by $\pm$ 2 UI.

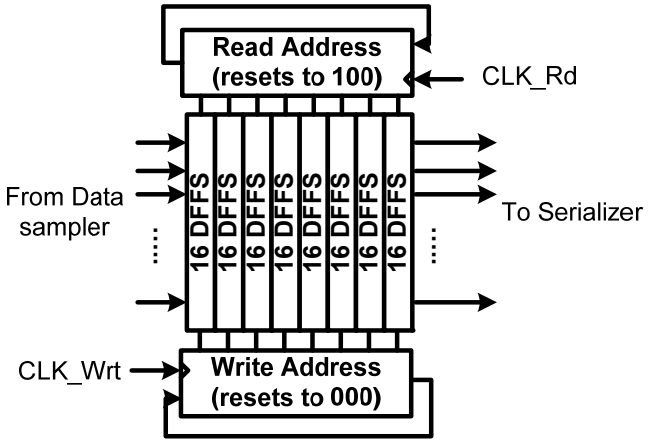


Fig. 3.42: 8×16-b FIFO memory.

With the FIFO and serializer, the CDR becomes a system that receives and sends a single lane high speed data stream. Therefore, it can be fitted into the BER simulation setup which is shown in Fig. 3.43 [43]. The simulation setup consists of a phase modulator, a PRBS generator, a PRBS tracker and the CDR under test. The phase modulator provides a clock whose phase is modulated by a sinusoidal source. The PRBS generator is based on a linear feedback shift register (LFSR) whose *XNOR_OUT* terminal is connected to the *DIN* terminal. The phase modulated clock is used to clock the PRBS generator, thus the sinusoidal jitter is added to the data stream. The recovered data from the CDR is fed to

another LFSR whose configuration is the same as the PRBS generator but its *XNOR_OUT* output is compared to its *DIN* input. If the recovered data is the same as the transmitted data, then the *ERROR* signal will stay in '0'. Therefore, by observing the output of the PRBS tracker, the CDR functionality can be evaluated.

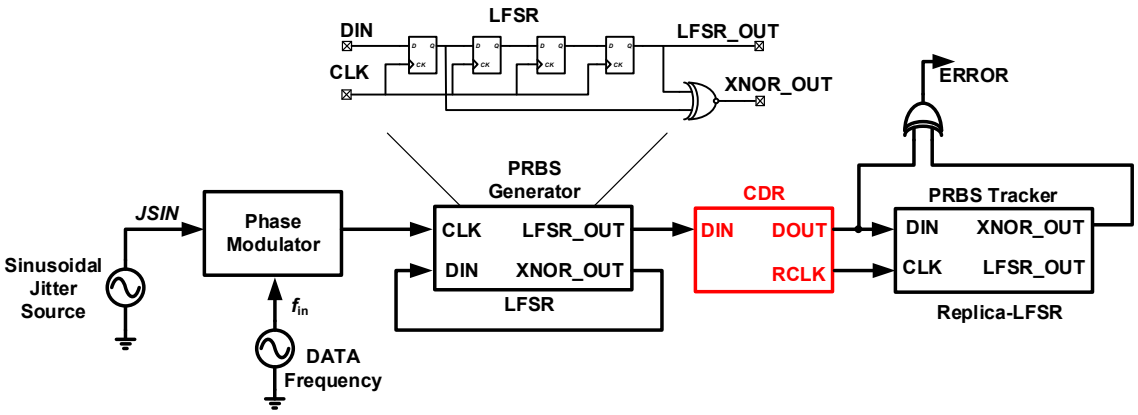


Fig. 3.43: CDR BER simulation setup.

For the CDR post-layout simulation, PCB trace and package models are added. Fig. 3.44 shows the simulation setup for the CDR under test. In the simulation, all the custom-designed circuit blocks use post-layout spice netlists which include the parasitic. The semi-custom-designed blocks uses post-place-and-route verilog netlists and standard delay format (SDF) files. The PCB trace and package models are described by S-parameters. The input is a PRBS-31 data pattern modulated by the sinusoidal jitter which has an amplitude of 0.4 UI and a frequency of 4 MHz. The CDR is set at the half-rate sampling mode. Fig. 3.45 shows the transient simulation result under the slow process corner and 85 ˚C temperature.

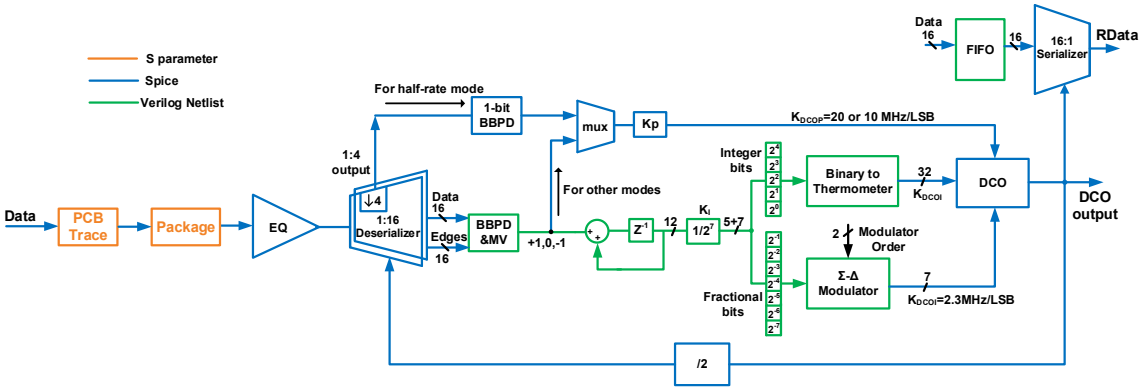


Fig. 3.44: CDR simulation setup.

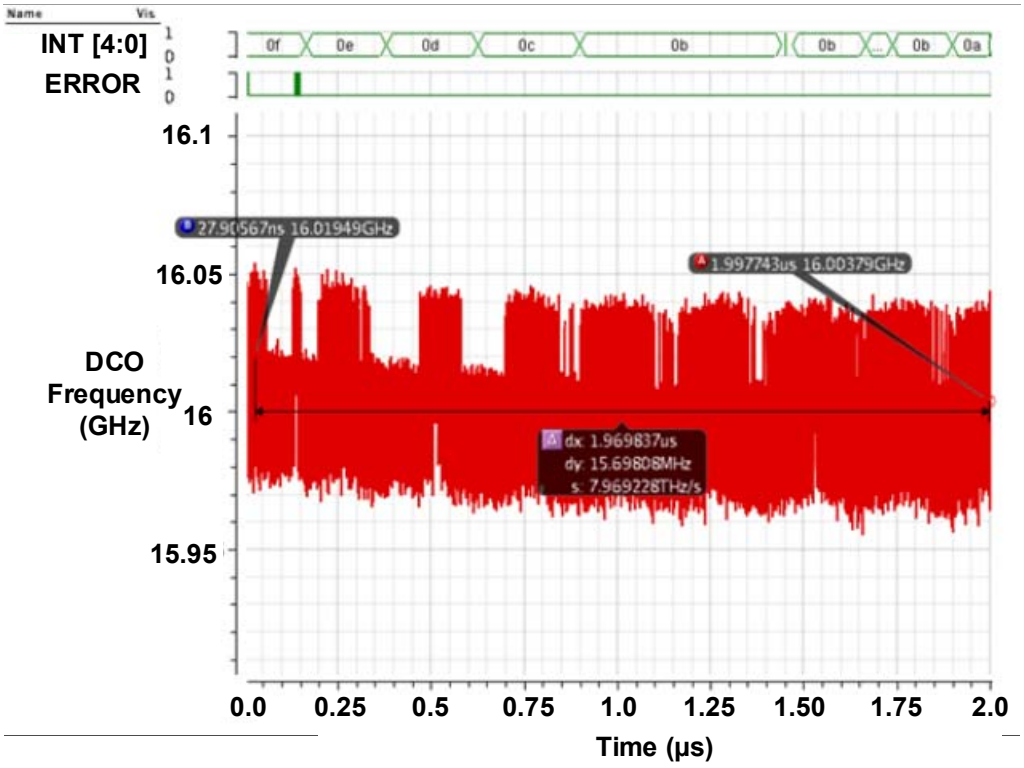
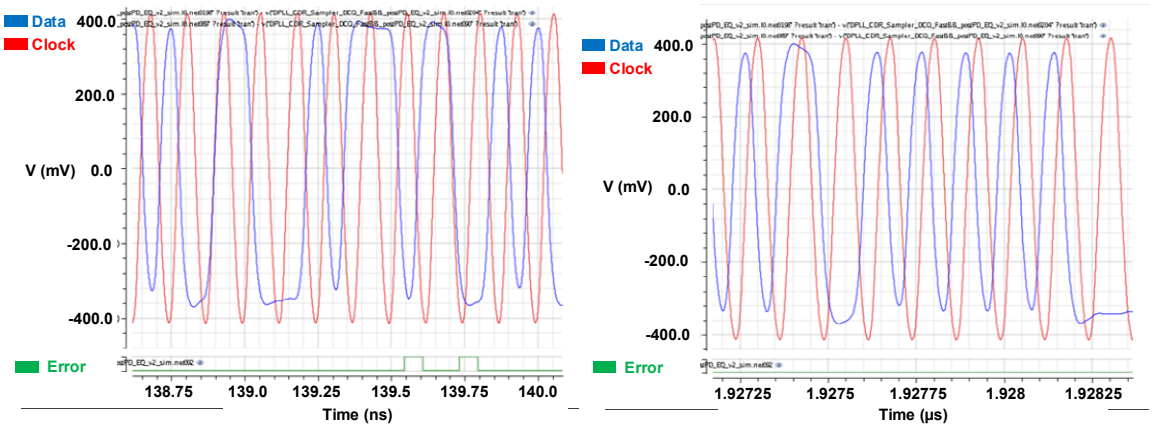


Fig. 3.45: CDR transient simulation result.

The first waveform in Fig. 3.45 is the 5 MSBs of the PLL integral path accumulator output which controls the average DCO frequency. When the CDR is locked, the control word is dithered to accommodate the transient frequency variation due to the sinusoidal

jitter in the data. The second waveform is the error output of the PRBS tracker. In the beginning of CDR locking, some errors are observed. After the CDR is settled, the error signal stays at '0' which means the data are correctly recovered and the CDR is able to tolerate the sinusoidal jitter applied to the data stream. The third waveform is the transient DCO frequency. Due to the proportional path, the DCO frequency is dithered to track the data phase. The initial DCO frequency error is about 19.5 MHz and the error is reduced to 3.79 MHz at the end of the simulation.



(a) (b)

Fig. 3.46: CDR 1:16 deserializer inputs (a) CDR is unlocked (b) CDR is locked.

To observe the phase relationship between the data and clock before and after the CDR locking, Fig. 3.46 shows the data and clock inputs of the CDR de-serializer. In Fig. 3.46(a), CDR is unlocked and the clock is asynchronous with the data. Its rising and falling edges are not aligned to the middle of the data and error signal is observed at the PRBS tracker output. Fig. 3.46(b) shows the case when the CDR is locked. In this case, the rising and falling edges of the clock are aligned to the middle of the data which are correctly

sampled. Thus, no error can be seen. The post-layout simulation result is consistent with the JTOL simulation in Simulink.

Table 3.12: Performance summary and comparison of the CDRs

	JSSC'09 [6]	TCASII'11 [20]	ISSCC'14 [34]	This work
Process	90 nm	0.13 μm	65 nm	65 nm
Supply (V)	1.0	1.5	1.2/1.0	1.2
Architecture	Digital DLL	Analog PLL	DLL/PLL	Digital PLL
Data Rate (Gbps)	5.75~44	1~16	4~10.5	1~16
Power (mW)	230[2]	160	22.5	67.2~92.5
Oscillator	NA	Ring	Ring	LC
Area (mm^2)	0.2[3]	0.134[4]	1.63	0.68
Reference-less	NO	YES	NO	YES
JGEN (ps, rms)	NA	2.84 @ 16 Gbps	2.2 @ 10 Gbps	0.7 @10 Gbps

The performance summary and comparison of the proposed CDR with the state-of-the-art designs are shown in Table 3.12. The proposed CDR exhibits competitive advantages on the performance of jitter and power consumption.

[2] Not include the clock generator power.
[3] Not include the clock generator area.
[4] Not include the loop filter area.

3.6 Summary

In this chapter, a reference-lesss digital-PLL-based CDR is presented. By using the multi-sampling-rate technique, the CDR supports a continuous wide range of data rate which is from 1 Gbps~16 Gbps. The CDR adopts an 8~16 GHz LC-DCO. The LC-DCO shows a much lower random noise compared to its ring oscillator counterpart. To increase the DCO tuning range without area penalty, the switched-coupled-inductor is used. The CDR also contains a digital FLL which combines the stochastic-counter-based data rate detection and the AFC techniques. Compared to the stochastic-counter-based approach, the proposed FLL is able to support multiple phase detection modes and accommodate the unbalanced data pattern such as k28.7. To address the difficulty of jitter and stability evaluations for bang-band CDR, a Simulink model is developed. The model is able to conveniently find out the JTRAN, JGEN and JTOL performances for the CDR. The post-layout simulation results validate the proposed design techniques. Specially, the CDR operating at 16 Gbps is able to tolerate a sinusoidal jitter with an amplitude of 0.4 UI and a frequency of 4 MHz. The JGEN at 10 Gbps is 7 mUI RMS.

CHAPTER 4. A FREQUENCY SYNTHESIZER FOR MULTI-STANDARD WIRELESS RECEIVERS

4.1 Introduction

One of the major trends of wireless communication is the chip-level integration of multiple communication standards in a low-cost technology. The demand for integrating multiple wireless standards into a single reconfigurable radio is growing together with the proliferation of wireless communication standards. Simply implementing such a radio device with multiple dedicated front-ends integrated in parallel is not a viable solution since power consumption and die area and thus system cost will be unaffordable. The more desirable solution is a flexible multi-standard radio system with high re-configurability and programmability. One of the challenging blocks of such a reconfigurable radio is the frequency synthesizer that needs to generate clean and stable LO signals fulfilling the requirements of the major wireless communication standards. In [44, 45, 46, 47, 48], fractional-N frequency synthesizers covering major communication standards such as GSM, WCDMA, WLAN and Bluetooth have been developed. However, they require multiple VCOs, power-hungry poly-phase filters or high-frequency LO buffers and dividers.

This chapter presents another frequency synthesizer designed in a 0.13-μm CMOS technology for multi-standard wireless receivers that support communication standards including DCS1800, WCDMA, TD-SCDMA, Bluetooth, and WLAN 802.11a/b/g [49] Architecture design and frequency planning are carefully performed to tradeoff wide frequency range and power efficiency. A QVCO is used in the proposed frequency

synthesizer. Conventional QVCO, however, suffers from the problems of bimodal oscillation and poor phase noise. To improve the QVCO's performance, the introduction of phase shifters to the coupling stage [50] [51] or the use of capacitive coupling instead of transistor coupling [52] have been previously proposed. The use of a phase shifter in the coupling stage is preferred in this design because capacitive coupling requires more than two LC oscillator stages to ensure a well-defined oscillation mode [52]. A new phase shifter scheme is proposed to effectively eliminate the bimodal oscillation and at the same time significantly improve the QVCO phase noise and the output phase accuracy. In addition, by combining harmonic rejection and single sideband mixing, a harmonic-rejection SSBmixer is developed to suppress unwanted sidebands and spurious signals. It serves as a power-saving solution to generate the LO signal for 802.11a by avoiding power-hungry poly-phase filters or high-frequency LO buffers and dividers.

4.2 Architecture Design and Frequency Planning

4.2.1 Synthesizer Specifications

The synthesizer specifications typically include frequency range, phase noise, spur and settling time requirements. The proposed Σ-Δ fractional-N frequency synthesizer is designed for a direct conversion receiver and supports standards including DCS1800, WCDMA, TD-SCDMA, Bluetooth, and WLAN 802.11a/b/g. The synthesizer thus needs to cover a frequency range from 1.8 GHz to 5.9 GHz. Adjacent channel selectivity (ACS) and blocking characteristics of the receiver set the LO phase noise and spur requirements. Due to the strong power allowed for adjacent channels and the requirement of a large

signal-to-noise ratio (*SNR*), cellular communications such as DCS1800 have very stringent spot phase noise and spur requirements. As shown in Table 4.1, to ensure that the reciprocal mixing is kept below the noise floor, the phase noise for DCS1800 at 3 MHz offset has to be less than -136 dBc/Hz. The WCDMA standard uses direct sequence spread spectrum, the *SNR* and the spot phase noise requirements can be relaxed. However, WCDMA is a frequency division duplex (FDD) system. For UTRA-FDD Band I, the Tx and Rx bands are 130 MHz apart. The Tx leakage at the receiver input can mix with the receiver LO signal. The phase noise is thus usually set to be less than -150 dBc/Hz at 130 MHz offset to minimize the reciprocal mixing effect [4]. Wideband communication systems such as WLAN, on the other hand, occupy a much larger bandwidth and therefore the LO phase noise specification is often set by the integrated phase noise which is determined by the PLL close-in phase noise. Assuming that the phase noise is constant within the PLL bandwidth ($f_{\mathrm{BW,PLL}}$) and then decreases by -20 dB/dec, the double sideband integrated phase noise $P_{\mathrm{pn,int}}$ can be approximated as:

$$P_{pn,\mathrm{int}}\Big|_{dBc} = 10\log(\pi f_{BW,PLL}) + L(f_{in}) \tag{4.1}$$

where $L(f_{\mathrm{in}})$ is the PLL close-in phase noise in dBc/Hz, and $P_{\mathrm{pn,int}}$ should be larger than the required *SNR*. Eq. (4.1) sets the RMS phase noise requirements for Bluetooth and 802.11b. For 802.11b, the 11 Mbps operation mode sets the most stringent receiver specification and the required *SNR* is 11.5 dB [4]. In the case of Bluetooth, the specified 10^{-3} maximum bit-error-rate (*BER)* can be achieved with a 21 dB *SNR* [4]. For OFDM system such as 802.11a/g, the LO phase noise causes inter-carrier interferences and the phase noise specification is derived from numerical simulations. Typically, one leaves enough design

margin and sets $P_{pn,int}$ = -35 dBc, which is integrated from 10 kHz to 10MHz [53], and this results in a RMS phase noise of 1° and a close-in phase noise of -90 dBc/Hz with $f_{BW,PLL}$=100 kHz. The out-of-band phase noise specification for WLAN is determined by the blocking characteristics and is listed in Table 4.1. One can find that the toughest phase noise requirement for WLAN is the close-in phase noise. In summary, the specification of close-in phase noise of our frequency synthesizer is set by the WLAN standards and the out-of-band phase noise requirement is set by the cellular standards such as DCS1800 and WCDMA.

Table 4.1: Specifications for the multi-standard frequency synthesizer

Standards	**DCS1800**	**WCDMA**	**TD-SCDMA**	**Bluetooth**	**802.11b**	**802.11a**	**802.11g**
Frequency Range/MHz RX	1805~1880	2110~2170	1880~1920 2010~2025 2300~2400	2400~2484	2400~2484	5150~5350 5725~5850	2400~2484
Channel Spacing	200 kHz	5 MHz	1.6 MHz	1 MHz	25 MHz	20 MHz	25 MHz
Frequency Accuracy	0.1 ppm	0.1 ppm	0.1 ppm	75 kHz	25 ppm	20 ppm	25 ppm
Phase Noise (dBc/Hz)	-119@0.6 M -129@1.6 M -136@3 M	-108.8@7.6 M -120.8@15 M -150@130 M	-111@3.2 M -123@5 M	-81@1 M -111@2 M -121@3 M	-90@10 k -121@14 M	-90@10 k -100.2@20 M -116.2@40 M	-90@10 k -100.2@20 M -116.2@40 M
Spur (dBc)	-66@0.6 M -76@1.6 M -83@3 M	-43@7.6 M -55@15 M	-50@3.2 M -62@5 M	-21@1 M -51@2 M -61@3 M	-49.5@14 M	-28@20 M -44@40 M	-28@20 M -44@40 M
Settling Time	865 μs	NA	NA	229 μs	NA	NA	NA

Settling time of the frequency synthesizer is determined by the PLL loop bandwidth. The settling time for a synthesizer in a time division multiplexed (TDM)

cellular system such as GSM is often set by the time required between adjacent transmission packets. In GSM, the most critical switching time for the LO to take place is between the transmission and the system monitoring slots and is about 865 μs. It should be mentioned that not every standard requires a specification on the settling time. For example, in direct-sequence spread spectrum (DSSS) WLAN transceivers, if the transmitter and the receiver share the same LO signal and adopt the same architecture, then there is no need to specify settling time for the synthesizer. We summarize the synthesizer design specifications in Table 4.1. In the table, a 3 dB design margin has been assigned for the *SNR* when deriving the phase noise and the spur requirements.

4.2.2 Synthesizer Architecture and Frequency Planning

According to the design specifications, the synthesizer needs to provide I/Q LO signals over a frequency range from 1.8 GHz to 5.9 GHz. A single VCO alone cannot achieve such a wide frequency tuning range with a reasonable phase noise. Also in direct conversion architecture, it is desirable to set the receiver LO frequency apart from the transmitter operating frequency to avoid LO pulling. One common method to achieve wideband frequency synthesis is to use multiple VCOs with a set of frequency dividers [45] [46]. The advantage of this synthesizer architecture is its simplicity and good spur performance. However, multiple VCOs can be very sensitive to parasitic capacitance; the VCO and the VCO buffers which operate at twice the LO frequency and the high frequency dividers can all consume a significant amount of power. This approach is a practical solution only when advanced technologies such as 45 nm CMOS [45], 40 nm CMOS [46] and BiCMOS [47] are adopted. Operating the VCO at the LO frequency in combination

with dividers and mixers is proposed in [44] [48]. A drawback of such an approach is that the mixing will generate spurs due to input harmonics. As the multi-standard receiver is a wideband system, the spurs in the LO signal can cause *SNR* degradation via reciprocal mixing. To reduce the spurious tones, single-sideband (SSB) mixers are used with quadrature inputs generated by a polyphase filter in [48]. Furthermore, input components to the SSB mixer are first linearized by filtering out the third-order harmonic through another polyphase filter. Passive polyphase filter in wideband systems often adopts multi-level configurations. As a result, multiple power-hungry buffers need to be inserted to compensate the power loss. This causes significantly more power consumption and greatly degrades the overall power efficiency of the synthesizer. In addition, the spur performance even with polyphase filtering is rather poor. The reported spur performance in [48] is less than -30 dBc.

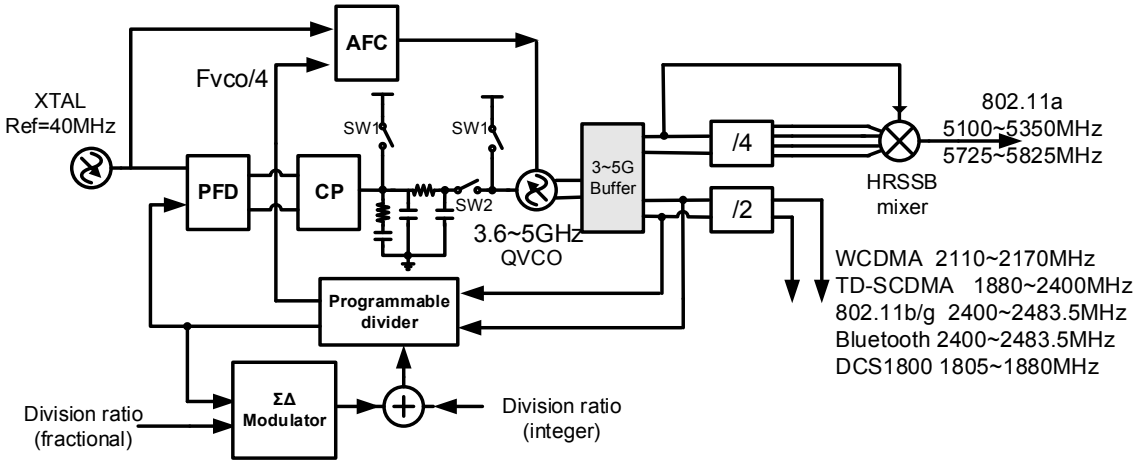


Fig. 4.1: Block diagram of the proposed multi-standard frequency synthesizer.

The proposed frequency synthesizer is based on an Σ-Δ fractional-N PLL, as shown in Fig. 4.1. The fractional-N architecture allows an arbitrary output frequency resolution, and is appropriate for multi-standard wireless applications. Since the direct conversion

topology is adopted, the synthesizer needs to generate quadrature LO signals for complex signal processing. As previously discussed, the CMOS process technology and the communication standards to support play an important role in choosing the synthesizer architecture. The synthesizer is designed in a 0.13-μm CMOS technology, and the highest LO frequency required is from 5.15 to 5.85 GHz set by the 802.11a standard. If using the divide-by-2 approach [45] [46] [47], the VCO needs to operate up to 11.7 GHz. Both the tuning range and the power consumption are issues in this approach as the high-frequency VCO and its buffers as well as the high-frequency dividers significantly lower the overall synthesizer power efficiency. Therefore, in the proposed synthesizer, a QVCO combining with an HR-SSBmixer is adopted. The QVCO is designed to have a tuning range from 3.6 GHz to 5.0 GHz. For the WCDMA, GSM, TD-SCDMA, WLAN 802.11b/g and Bluetooth standards, the LO signals are generated by a divide-by-2 circuit following the QVCO. As shown in Table 4.1, standards including WCDMA, GSM, TD-SCDMA and Bluetooth have very stringent LO spot phase noise and spur requirements. It is unacceptable to use the Divide and Multiply in Quadrature approach as developed in [48] to generate their LO frequencies. To generate the LO signal for WLAN 802.11a, an SSBmixer combined with harmonic rejection technique [54] is developed. The inputs of the HR-SSBmixer are 45°-spaced clocks generated by the divide-by-four circuit. The HR-SSBmixer effectively suppresses spurious tones resulted from the third- and fifth-order harmonics. As discussed previously, the LO phase noise requirement for the 802.11a mode is set by the integral noise. The spurious tone specification can thus be relaxed and this allows the 802.11a LO signal to be generated by the SSBmixer approach.

Table 4.2 summarizes the relations between the oscillator frequencies and the synthesizer output frequencies. The QVCO does not oscillate at the same frequency as that of the synthesizer output. As a result, the LO pulling is avoided. The synthesizer avoids the use of power-hungry high frequency LO path or broadband polyphase filters, and at the same time offers better spurious performance supporting major cellular and short-range wireless communication standards. Given the design being implemented in a 0.13-μm CMOS technology, the proposed synthesizer architecture and the frequency planning scheme offer a good tradeoff among synthesizer performance, hardware complexity and power efficiency.

Table 4.2: Frequency planning

Standards	f_{min}~f_{max}(MHz)	Relation
WCDMA	2110~2117	$f_{vco}/2$
Bluetooth	2400~2483	$f_{vco}/2$
WLAN802.11a	5015~5850	$5f_{vco}/4$
WLAN802.11b	2400~2484	$f_{vco}/2$
WLAN802.11g	2400~2484	$f_{vco}/2$
TD-SCDMA	1880~1920 2010~2025 2300~2400	$f_{vco}/2$
DCS1800	1805~1880	$f_{vco}/2$

4.3 Circuit Implementation

4.3.1 QVCO with Proposed Phase Shifter

A QVCO consisting of two cross-coupled LC oscillator cores is adopted in designing the frequency synthesizer. The HR-SSBmixer uses the quadrature signals to carry out single sideband up-conversion and provides the LO signal for the 802.11a mode. Conventional cross-coupled quadrature oscillator has not been widely used because of its poor phase noise performance and potential bimodal oscillation. When two LC VCOs are coupled, the LC tanks operate away from the resonance frequency and thus the optimal quality factor (Q-factor) of the LC tanks is not reached [50]. As a result, the phase noise performance is degraded. Also the QVCO output frequency depends on the coupling strength of the two LC cores. Thus, there exists an additional flicker noise up-conversion mechanism due to the coupling transconductance and the cross-coupling transconductance modulation [40] leading to a $1/f^3$ phase noise degradation.

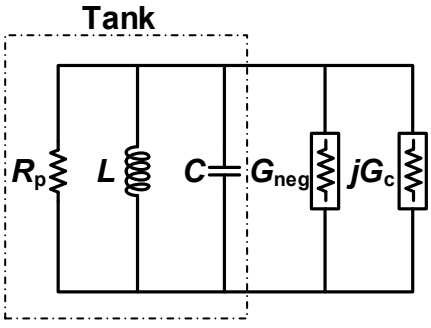


Fig. 4.2: One port model of the QVCO.

The issues mentioned above can be explained by the one-port model of a QVCO [55], as is shown in Fig. 4.2. At steady state, the cross-coupling transistors produce a

negative resistance $1/G_{neg}$ canceling out the R_p while the coupling transistors produce a quadrature resistance $1/jG_c$ that acts on the LC tank and sets the frequency shift. The oscillation frequencies are calculated as

$$\omega_{osc1,2} \approx \omega_0 \pm \frac{G_c}{2C} \tag{4.2}$$

where the ± signs are due to the output phase uncertainty of the two LC VCOs and ω_0 is the resonant frequency of the ideal LC tank. It can be seen from (4.2) that as the coupling strength increases, the oscillation frequency deviates from ω_0 by a larger amount. Since the tanks operate at a frequency that is different from the resonance frequency, the Q-factor is reduced deteriorating the QVCO phase noise. It is desirable to minimize the coupling strength to achieve a better phase noise. However, the mismatch between the two oscillators determines the minimum allowable coupling strength [56]. There exists a tradeoff between the phase noise and the output phase accuracy in the conventional transistor-coupled QVCO design.

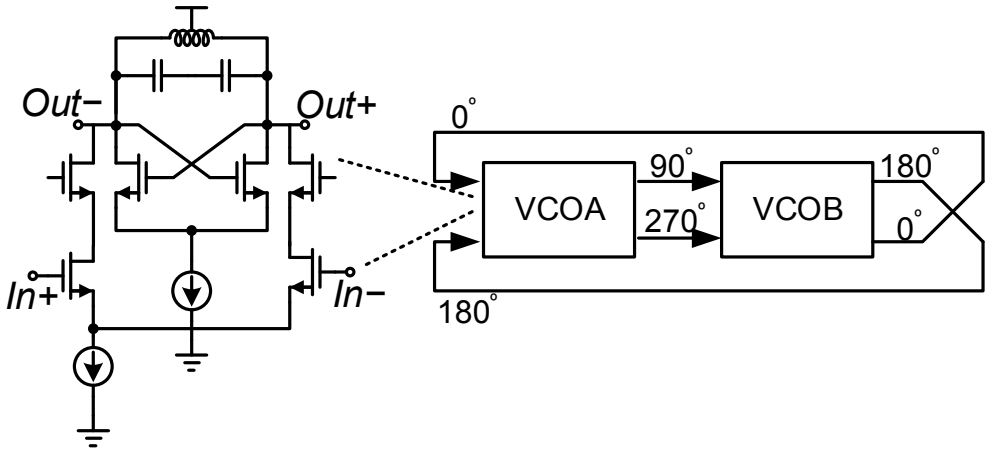
Also can be seen from (4.2), there are two possible oscillation frequencies. Each output frequency corresponds to a lead or a lag phase relation between the outputs of the two VCOs [55]. In reality, asymmetric frequency response of the LC tanks due to the series inductive and capacitive losses results in a dominant mode which corresponds to a higher loop gain of the positive feedback in the oscillator [57]. However, the asymmetry introduced by the parasitic resistance does not guarantee a complete elimination of the unwanted oscillation. Various delays contributed by interconnect RC parasitics in the coupling path, and process and temperature variations may cancel the effect of the asymmetric frequency response of the LC tanks. Consequently, bimodal oscillation can

still exist. This phenomenon is experimentally observed in [51]. Since the outputs of the QVCO serve as the inputs of the HR-SSBmixer, the phase relation of the quadrature outputs should be clearly defined in order to carry out a correct single sideband up-conversion operation.

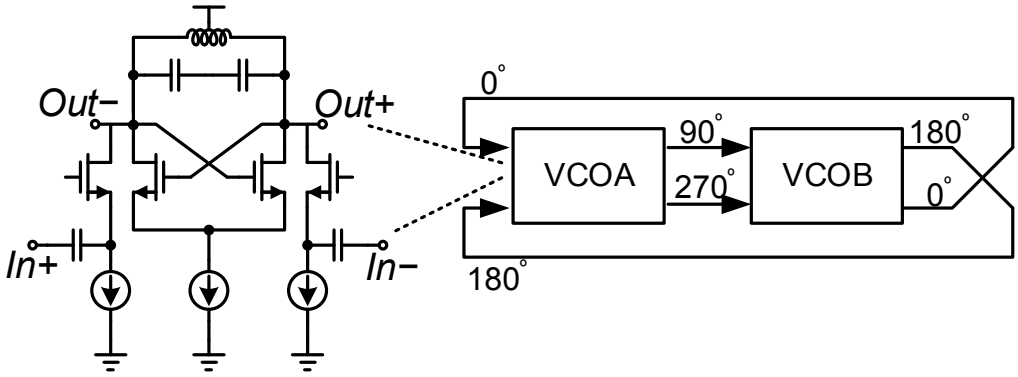
To solve the problems mentioned above, a phase shifter can be used. The quadratrue output phases are still ensured by the coupling transistors, but the coupling currents are phase-shifted by 90°. This can be seen from the one port model in Fig. 4.2. If jG_c is multiplied by j, then it becomes part of the negative resistance and will not disturb the ideal LC tank. In fact, it will strengthen the negative resistance and improve the power efficiency. In addition, the phase-shift in the coupling path moves the QVCO operation away from the unstable boundary and effectively eliminates the bimodal oscillation [51]. Thus, introducing a phase shifter greatly decouples phase accuracy and phase noise performance, as it de-sensitizes the QVCO output phase error to the mismatches of the tail current and the tank Q-factor [56].

Introducing a phase-shift into the coupling path has been previously used to improve QVCO phase noise [50] and to avoid bimodal oscillation [51]. In Fig. 4.3(a), the coupling stage is constructed by a differential cascaded common-source common-gate configuration [51]. The cascode configuration creates a phase delay and moves the QVCO operation away from the unstable boundary, which eliminates the bimodal oscillation. However, the phase-shift from the cascode stage is limited to about 20°. It is enough to avoid the bimodal oscillation, but the phase noise improvement is limited. In addition, the noise from the cascode transistors is not negligible at high frequencies because of the parasitic capacitances. In Fig. 4.3(b), the $1/g_m$ of the coupling transistor and the coupling

capacitor are combined as a high-pass filter to introduce the phase-shift [50]. However, the *Q*-factor of the LC tank can be severely degraded due to the $1/g_m$ input resistance of the coupling transistors.



(a)



(b)

Fig. 4.3: (a) Phase shifter using cascode coupling stage, (b) Phase shifter using common gate coupling stage.

In this design a new phase shifter is proposed as shown in Fig. 4.4. It is similar to the capacitive degeneration technique used in broadband amplifiers [58]. The tail current source of the coupling stage is first split and then a parallel R-C network between the source

terminals of the coupling transistors is added. The resistors in the phase shifter consume no dc voltage drop which is appropriate for low-voltage applications. Since the R-C degeneration is not directly connected to the LC-tank, the *Q*-factor of the tank thus is not affected. The transconductance of the coupling stage is calculated as

$$G_{mc} = \frac{g_{mc}}{1+g_{mc}R_s} \cdot \frac{1+sR_sC_s}{1+sR_sC_s/(1+g_{mc}R_s)} \tag{4.3}$$

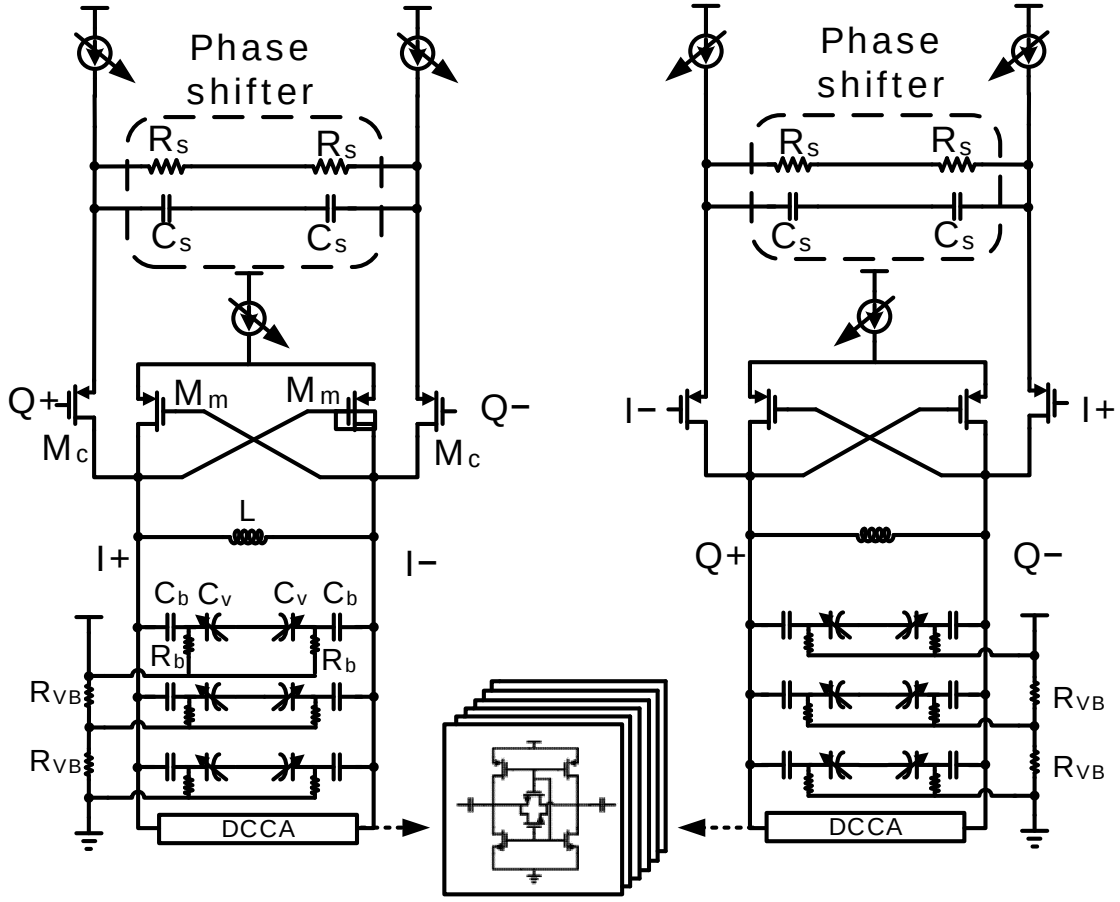


Fig. 4.4: QVCO with the proposed phase shifter.

In (4.3), g_{mc} is the transconductance of the coupling transistor, and R_s and C_s are the resistance and capacitance in the phase-shift network. The transconductance has one zero and one pole. The zero frequency is $\omega_z = 1/R_sC_s$ and the pole frequency is $\omega_p \approx g_{mc}/C_s$.

The zero results in a phase-lead to the transconductance while the pole results in a phase-lag. The total phase-shift thus can be derived as

$$\phi \approx \arctan\left(\omega R_s C_s\right) - \arctan\left(\frac{\omega C_s}{g_{mc}}\right) \tag{4.4}$$

Ideally, the shifted phase needs to be 90° at the operating frequency to align the current and the voltage of the tank. This requires that (4.5) is satisfied.

$$\frac{10}{R_s C_s} \le \omega_{osc} \le \frac{g_{mc}}{10 C_s} \tag{4.5}$$

Eq. (4.5) requires that the pole frequency is much larger than the zero frequency to have a 90° phase-shift. From (4.3), the magnitude of the coupling stage transconductance G_{mc} is source degenerated by R_s. If $g_{mc}R_s$ is too large, the resistive degeneration will result in a very small coupling transconductance at the resonance frequency and this may cause the phase accuracy of the QVCO to be degraded. Theoretically, if the coupling current is phase-shifted by 90°, then the bias current mismatch and the *Q*-factor mismatch between the two LC VCO cells will have no effect on the phase accuracy of the output signals. However, the phase accuracy can still be sensitive to the resonant frequency mismatch between the two tanks and the mismatch due to the two phase shifters [56]. Therefore, practically, the coupling strength cannot be too small even with the phase shifters adopted. A phase-shift of 50° is strong enough to increase the effective tank *Q*-factor and to improve the QVCO phase noise performance [56]. Therefore, considering the tradeoff between the phase noise and the phase accuracy, the phase shifter in the QVCO is designed to have a 40°~50° phase-shift at the operating frequency. It should be mentioned that R_s will introduce additional noise, but compared to the phase noise improvement due to the phase

shifter, the noise degradation due to R_s can be neglected. Simulation also indicates that the noise contribution of R_s is negligible. It should be also noted that the discussions above are based on small-signal analysis. In actual design, the effective large-signal transconductance should be used. The small-signal analysis nevertheless provides a good explanation about the operating principle of the proposed phase shifter.

In this design, the QVCO operating frequency is from 3.6 GHz to 5 GHz. The width of the coupling transistor is set as one half of that of the cross-coupling transistor. The coupling coefficient m is defined as $G_{mc,LS}/G_{m,LS}$, where $G_{mc,LS}$ is the effective large-signal transconductance of the coupling stage and $G_{m,LS}$ is the effective large-signal transconductance of the cross-coupling transistor. Due to the resistor degeneration, m is less than 1/2. Periodic Steady-State (PSS) simulations show that m is 0.28 and the phase of the coupling current is shifted by 40°~50° at the operating frequency. The proposed phase shifter significantly improves the QVCO performance, which is verified by simulations.

Simulation results of the QVCO with the proposed phase shifter scheme are compared with those of two circuits shown in Fig. 4.5. The first circuit is a conventional QVCO while the other is two LC oscillators coupled in an "in-phase" style. It has been proved that the in-phase coupled VCOs operate at the tank resonance frequency, and the phase noise performance is improved compared to a single VCO [59]. The transistor sizes, bias currents and LC tanks are all identical in these three circuits. Fig. 4.6 shows the phase noise comparison result. With the proposed phase shifter, the phase noise is improved by about 3 dB compared to the conventional QVCO. At some frequency points, the phase noise is even better than the LC-VCOs coupled in the "in-phase" style. It is also observed that the proposed QVCO operates at a frequency much closer to the LC tank resonance

frequency while the conventional QVCO operates at a frequency which is 115 MHz apart from the ideal LC tank resonant frequency. This indicates the proposed QVCO has a larger effective *Q*-factor. Fig. 4.7 shows Monte Carlo simulation results. A coupling factor of 0.5 is assumed for the conventional QVCO which is larger than that of the proposed QVCO. Yet, the standard deviation of the output phase of the proposed QVCO is less than that of the conventional QVCO, which indicates that the proposed QVCO has a much better output phase accuracy.

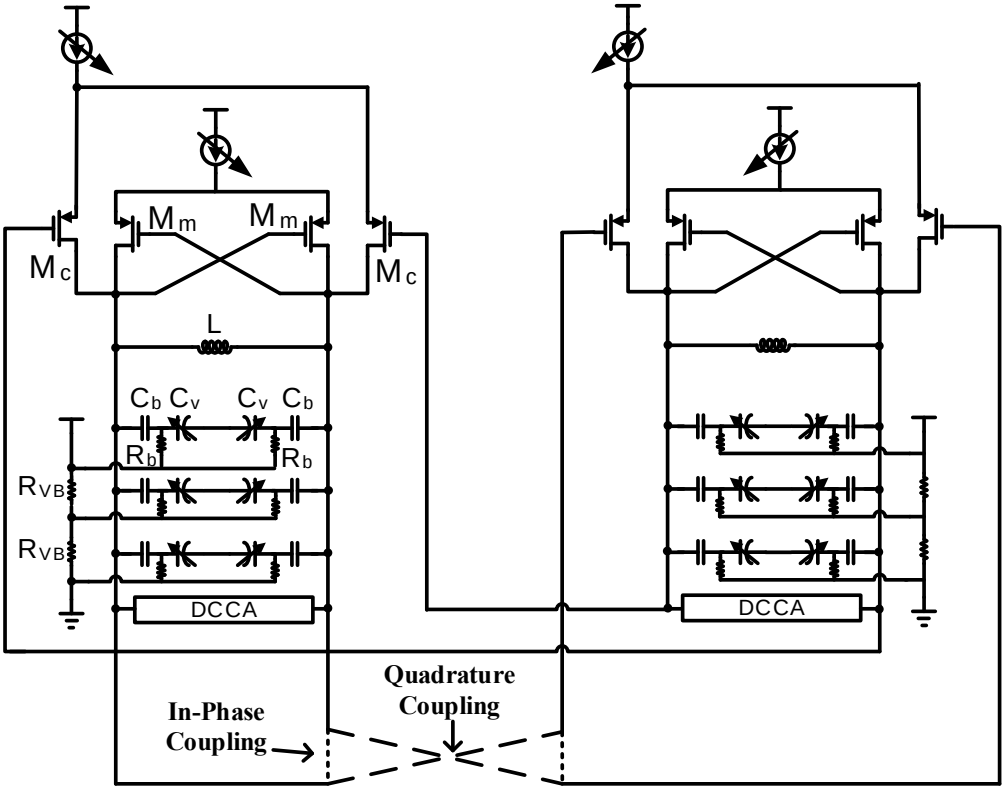


Fig. 4.5: Two oscillators coupled to operate in quadrature and in phase.

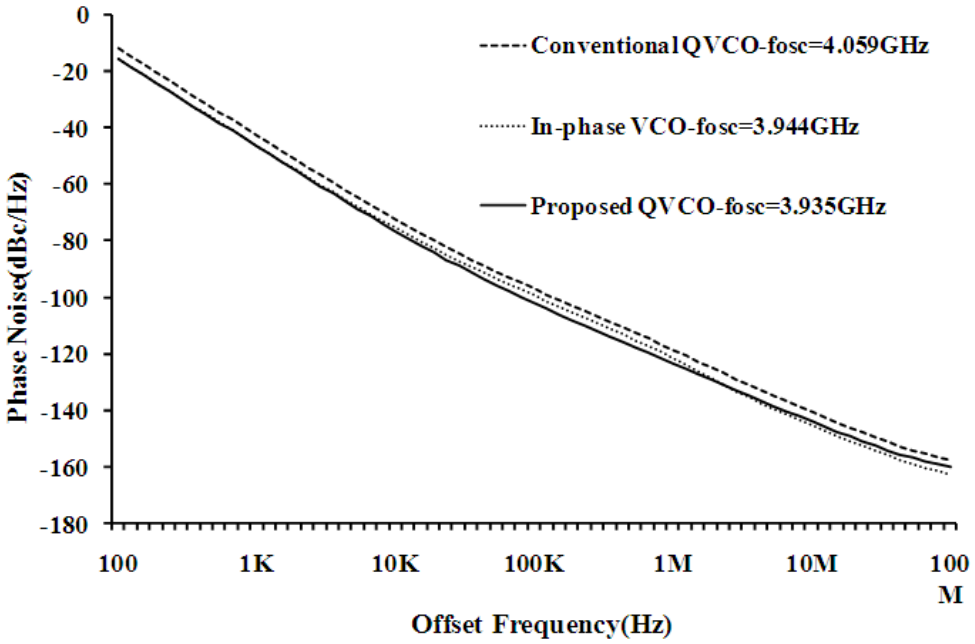


Fig. 4.6: Comparison of the phase noise simulation results.

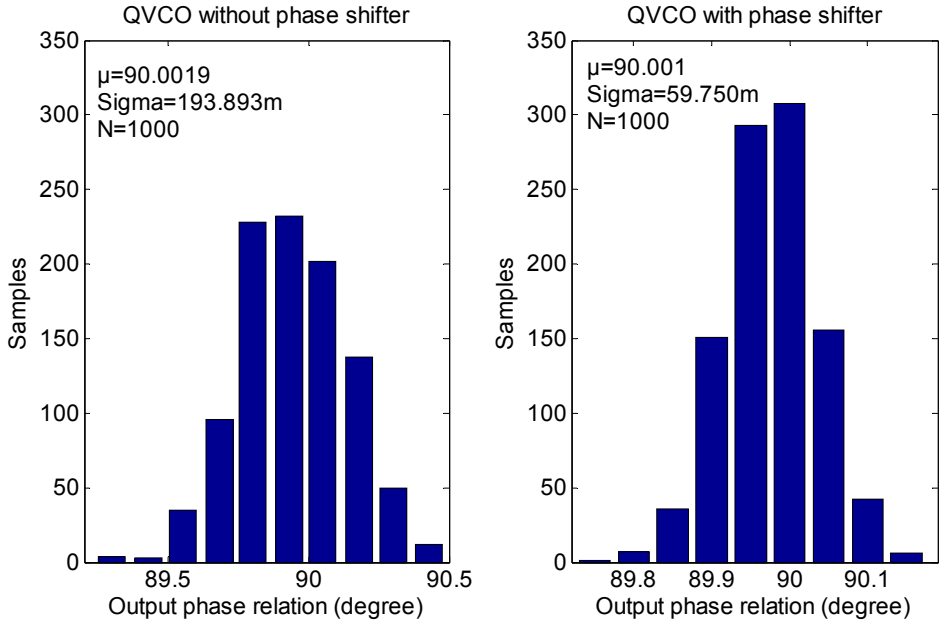


Fig. 4.7: Comparison of the output phase accuracy.

4.3.2 HR-SSB Mixer

The HR-SSBmixer combining harmonic rejection and single sideband mixing is developed to generate the 5 to 6 GHz LO frequency and avoid the use of broadband polyphase filters. The HR-SSBmixer carries out single sideband up-conversion to produce a $5\times f_{vco}/4$ LO frequency supporting the 802.11a standard and no filter is needed to reject the unwanted sidebands. The concept of harmonic rejection is firstly proposed in [54], which focuses on canceling harmonic components of a square-wave. It has also been used to solve the problem of harmonic mixing in the VHF and UHF TV bands [60]. The HR-SSBmixer, which is shown in Fig. 4.8, requires 8-phase inputs which are inherently generated by the divide-by-4 circuit following the QVCO. It is constructed by three SSB sub-mixers. Currents with different phases from the three SSB sub-mixers are summed at the common load to generate the output voltage, and the third- and fifth-order harmonics of V(t) are canceled. A band-pass load which consists of an inductor and a 3-bit binary-coded capacitor array is used to reduce the power consumption and to suppress the residual spurious signals. It should be noted that two HR-SSBmixers are needed to generate the I/Q LO signals.

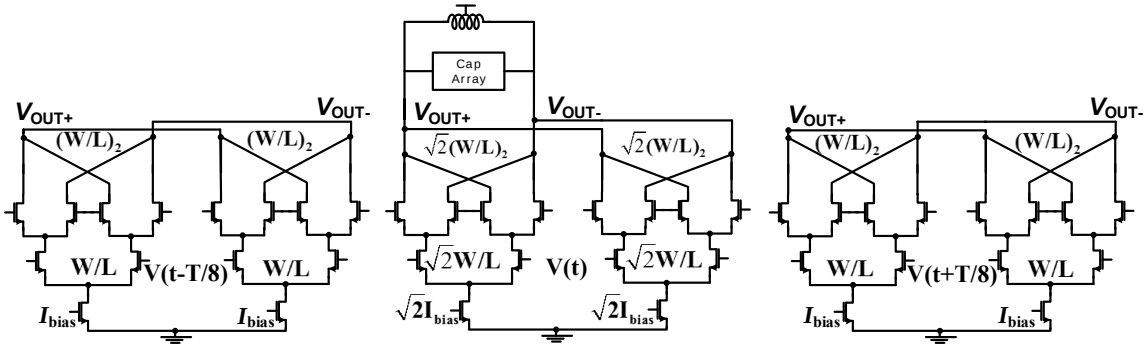
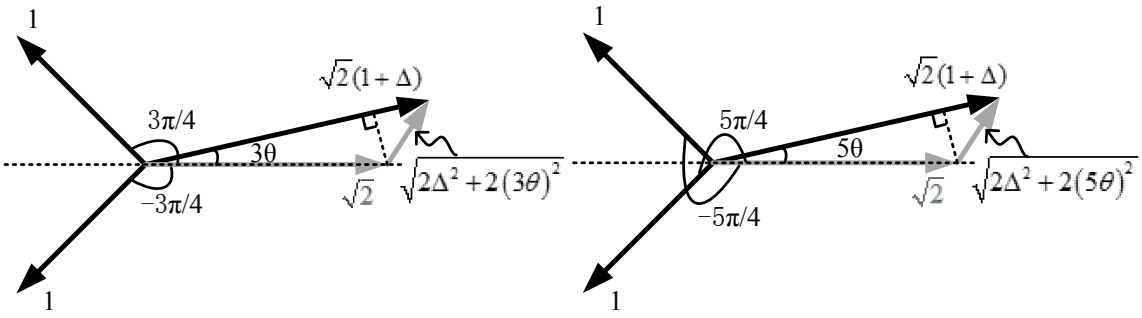


Fig. 4.8: Harmonic rejection SSBmixer.

According to the time-shifting property of the Fourier Transform, for a periodical signal x(t) with T being its period, the spectrum of $x(t\text{-T}/8)$ is $e^{-j\omega T/8}X(\omega)$. The phase-shift of the fundamental component is $\omega T/8 = \pi/4$. For the third- and fifth-order harmonics, the phase-shifts are $3\pi/4$ and $5\pi/4$, respectively. The phase-shifts of these three tones are different and this property can be used to linearize the SSBmixer's input signal, which is often a square-wave. By a summation of the signal $x(t)$ scaled by a factor of $\sqrt{2}$ and two time-shifted signals $x(t\pm T/8)$ having $\pm\pi/4$ phase-shifts relative to $x(t)$, the resulting signal eliminates the third and fifth harmonics while strengthens the fundamental component. In the single sideband conversion, quadrature signal of $x(t)$ is needed. The multi-phase signals are generated by the divide-by-4 circuit.



(a) (b)

Fig. 4.9: Residual harmonics due to phase and gain mismatches: (a) third-order harmonic,and (b) fifth-order harmonic.

As the cancellation is performed in the current domain, the amplitude scaling of $\sqrt{2}$ is implemented by scaling the gain of the transconductance stage of the corresponding sub-mixer. Hence, for the circuit in Fig. 4.8, the harmonic rejection ratio highly depends on the phase matching of the input signals and the gain matching of the SSB sub-mixers [54]. Fig.

4.9 shows the phasor diagrams which illustrate the incomplete third- and fifth-order harmonic cancellations due to the gain and phase mismatches. Using the phasor diagrams, we derive the third- and fifth-order harmonic rejections as:

$$HRM_3 \approx \frac{1}{9}\frac{[2\Delta^2 + 2(3\theta)^2]}{\left(2\sqrt{2}\right)^2} \tag{4.6}$$

$$HRM_5 \approx \frac{1}{25}\frac{2\Delta^2 + 2(5\theta)^2}{\left(2\sqrt{2}\right)^2} \tag{4.7}$$

where Δ is the gain mismatch and θ is the phase mismatch. The approximation holds for Δ << 1 and θ <<1 rad.

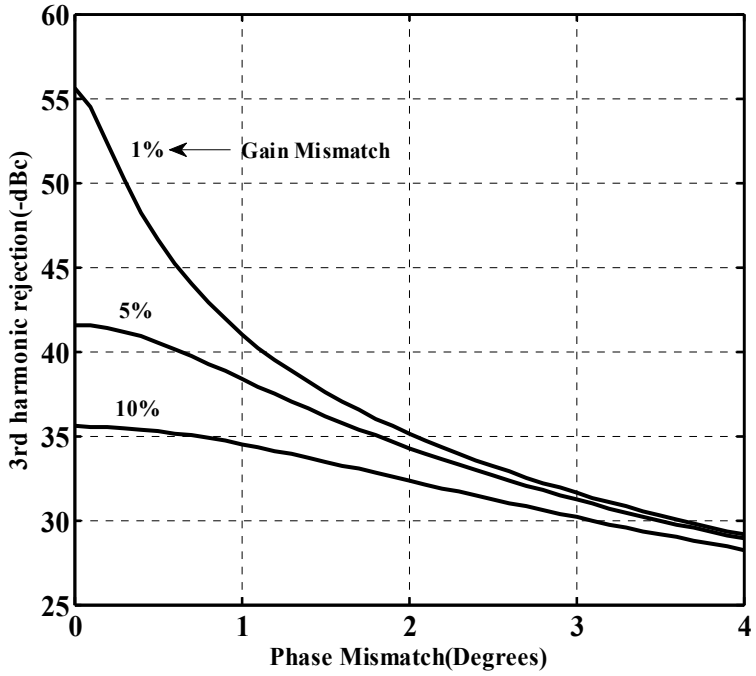


Fig. 4.10: Third-order harmonic rejection with respect to gain and phase mismatches.

The input frequencies of the HR-SSBmixer are f_{vco} and $f_{vco}/4$. Harmonic rejection is applied to the input whose frequency is $f_{vco}/4$. The third- and fifth-order harmonics of

this input will result in spurious signals at f_{vco}-3f_{vco}/4 = f_{vco}/4 and f_{vco}+5f_{vco}/4 = 9f_{vco}/4 due to the incomplete harmonic cancellations. The effect of the fifth-order harmonic can be neglected since 9f_{vco}/4 is far away from the supported frequency bands and any interference signals at that frequency can be suppressed by the receiver pre-filter. On the other hand, the interferences below 6 GHz may not be attenuated by the receiver front-end pre-filter, thus the spurious signals due to the third-order harmonic needs to be minimized. Using (4.6), the HRM_3 with respect to the phase and gain mismatches is plotted in Fig. 4.10. As can be seen from the figure, a better than 40 dB third-order harmonic rejection requires a less than 1% gain mismatch and a less than 1° phase mismatch.

The requirements of the third-order harmonic rejection and the sideband rejection for the HR-SSBmixer are determined by the frequencies of the spurious signals and the possible interferences. In the design, the output frequency of the HR-SSBmixer is from 5.15 GHz to 5.85 GHz. Therefore, the frequency of the image sidebands is from 3.09 GHz to 3.51 GHz, and the third-order harmonic frequency is from 1.03 GHz to 1.17 GHz. The third-order harmonic does not fall into any major wireless communication standards. When the receiver operates in the 802.11a U-NII upper band (5.725~5.825GHz), the WiMax signal whose frequency is from 3.3 GHz to 3.8 GHz could interfere with the receiver operation since the image sideband of the HR-SSBmixer is from 3.435 GHz to 3.495 GHz. The 802.11a U-NII lower- and middle-band (5.15~5.35 GHz) operations with an image sideband from 3.09 GHz to 3.21 GHz will not be affected by the WiMax signal. The required image sideband rejection ratio of the HR-SSBmixer is thus set by the WiMax signal interference and possibly the amount of interference suppression from the receiver front-end pre-filter.

4.3.3 Other Circuits

In order to increase the QVCO tuning range and reduce the QVCO gain, a switched capacitor bank is used in the resonator. An automatic frequency calibration technique is adopted in the synthesizer to ensure that a proper tuning curve of the QVCO can be selected. The detailed implementation of the AFC is shown by Fig. 4.11. The QVCO output signal is divided by 4 to lower the input frequency of the AFC. The divide-by-4 circuit reuses the first two stages of the programmable divider to save area and power. Differential signals are used for frequency detection to improve the counting accuracy. In generating the differential signals, a transmission gate is inserted to compensate the inverter delay. An AFC and QVCO co-design scheme is also developed to ensure a correct PLL locking.

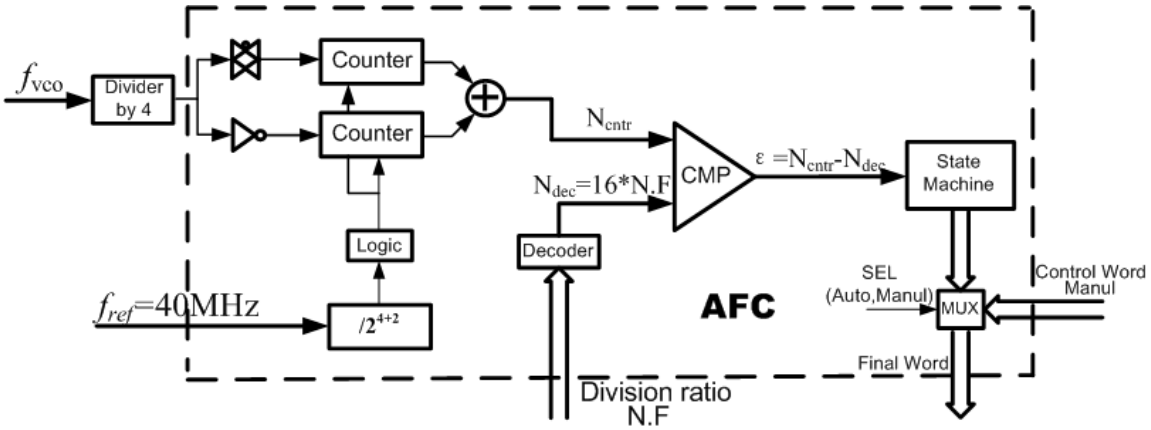


Fig. 4.11: AFC for coarse frequency tuning.

The programmable divider in this fractional-N frequency synthesizer is shown in Fig. 4.12. It is based on a modular architecture described in [61]. A total of seven stages of div2/3 cells are cascaded with one division ratio extension cell. The first two stages are implemented using CML logic circuits. The programmable divider is dynamically controlled by the sigma-delta modulator. The sigma-delta modulator, on the other hand, is

clocked by the output of the programmable divider. Thus, it is important to ensure that the control bits of the programmable divider are updated at the right time [62]. Fig. 4.13 shows the timing diagram of the fractional-N PLL. f_{out} is the output of the programmable divider. The sigma-delta modulator is triggered by the falling edge of f_{out} and the control bits of the programmable divider are updated by the rising edge of f_{out}. With this arrangement, the division ratio is safely updated at every reference cycle without interfering with the operation of the programmable divider. In addition, the divider swaps between a 6-cell mode and a 7-cell mode when the division ratio is between 124 and 129. Since the output of the divider needs to have no phase hopping to ensure a proper sigma-delta control [45], a multiplexer dynamically chooses f_6 or f_7 as the divider output. Reset (*RST*) of the seventh div2/3 cell ensures its output will stay at zero when it is disabled.

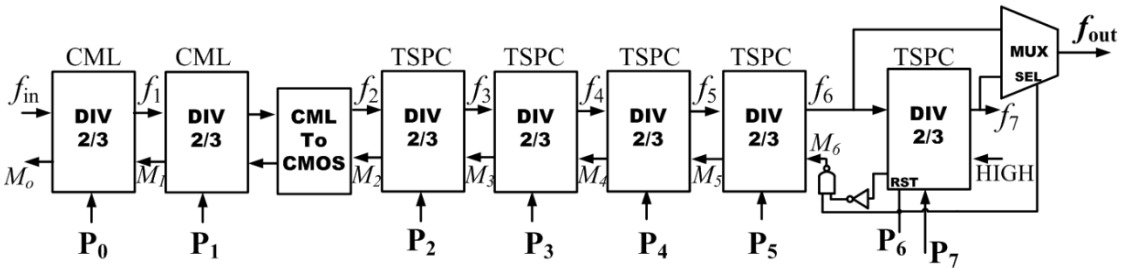


Fig. 4.12: Modular programmable divider.

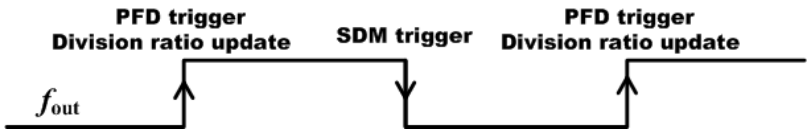


Fig. 4.13: Timing diagram of the fractional-N PLL.

4.4 Measurement Results

The wideband multi-standard frequency synthesizer is implemented in a TSMC 0.13-μm CMOS technology, with all the circuit blocks integrated on chip. A die microphotograph of the chip is shown in Fig. 4.14. The chip area is 1.86 mm×1.8 mm with an active core area of 1.86 mm^2.

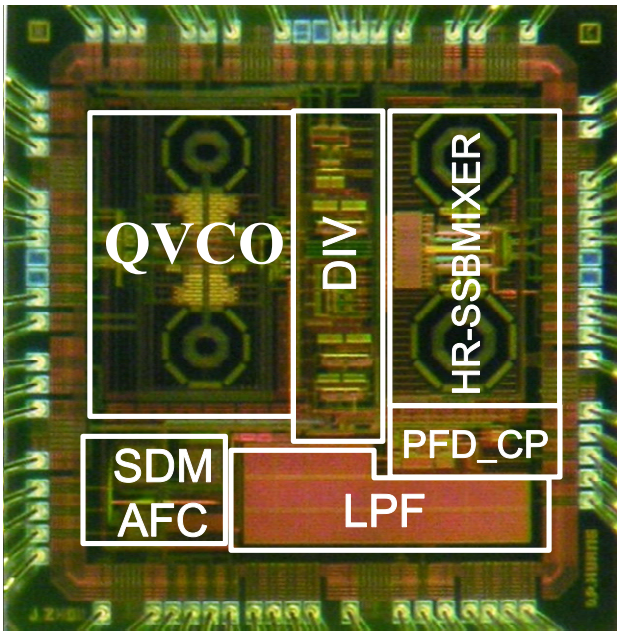


Fig. 4.14: Die microphotograph.

The bandwidth of the PLL ranges from 60 kHz to 90 kHz. The reference frequency is 40 MHz. All circuit blocks are powered by a 1.2 V supply. Power consumption is measured for different standards. For the 802.11a mode, the HR-SSBmixer is turned on and the total power consumption ranges from 49.12 to 52.62 mW. For other supported standards, the power consumption is from 35.6 to 44 mW. The measurement results of the frequency synthesizer are summarized in Table 4.3. The performance of the proposed QVCO is measured with a fixed control voltage. The output spectrum is measured by an

Agilent E4440A spectrum analyzer. The frequency tuning curves are shown in Fig. 4.15. The measured QVCO gain is 25 MHz/V to 105 MHz/V. As shown in Fig. 4.4, the varactors with three different DC biasing voltages are connected in parallel to achieve more linear tuning curves. The measured VCO tuning curves in Fig. 4.15 validate the linearization technique. The *FOM* of the QVCO, as defined in [40], is from 179.5 dB to 185.2 dB with power consumptions ranging from 7.68 mW to 17.76 mW. As shown in Table 4.4, except for this work, the oscillators in other publications are all non-quadrature VCOs. The *FOM* of the proposed QVCO is comparable to those of the single LC-VCOs. To validate the simulation results, the simulated and measured QVCO phase noises are compared. The phase noise is measured by an Agilent E5052B signal source analyzer. The simulated and measured QVCO phase noises at a frequency of 4.09 GHz are shown in Fig. 4.16 and they agree very well with each other.

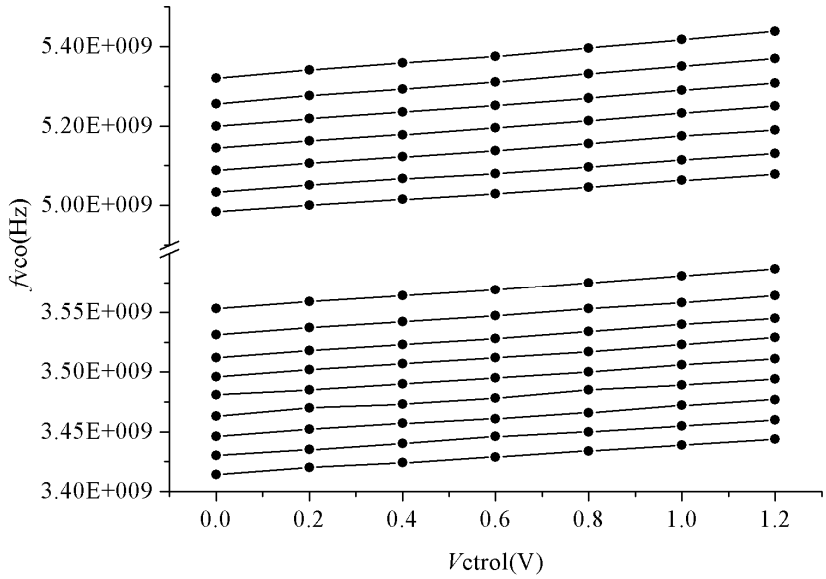


Fig. 4.15: Measured tuning curves of the QVCO.

The overall locking time of the frequency synthesizer is the sum of the AFC time and the PLL settling time. The locking process of the PLL is measured by an Agilent E5052B signal source analyzer. Fig. 4.17 shows the transient response at the QVCO output when the PLL is in the locking process. The clock frequency of the AFC is 40 MHz. It takes 8 cycles for the AFC to complete the tuning curve searching. Each cycle contains 32 AFC clock periods. The first 7 cycles are used for AFC counting and the last cycle is used to determine the correct tuning curve which is the closest to the target frequency. Therefore, the theoretical AFC search time is about 6.4 μs which is validated by the measurement result. The overall locking time is less than 50 μs.

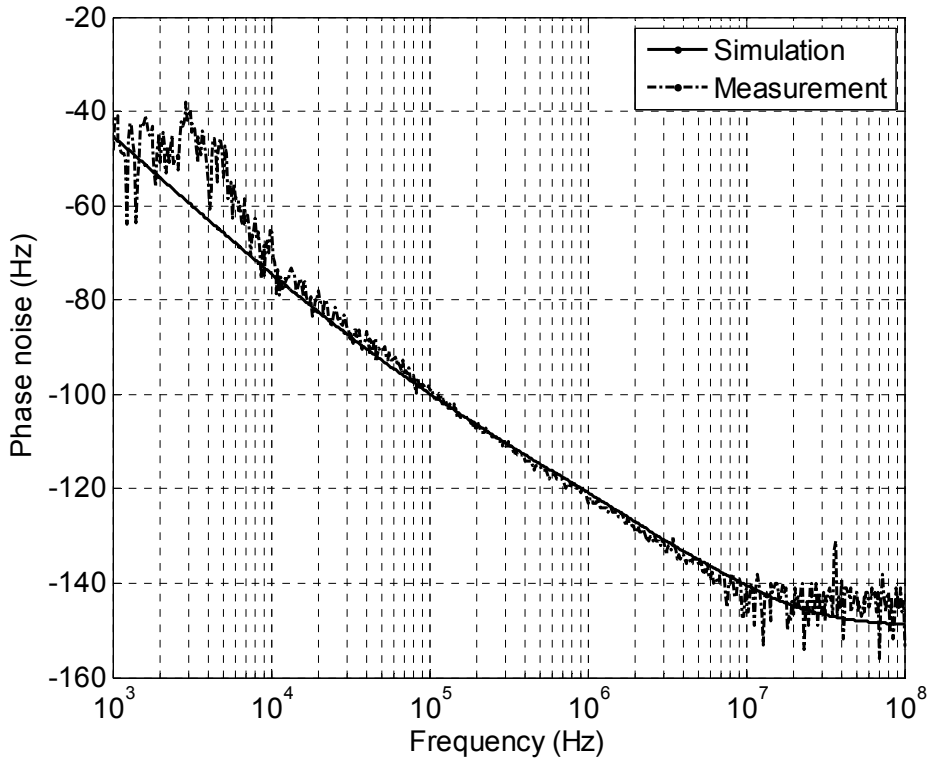


Fig. 4.16: Comparison between simulated and measured QVCO phase noise at 4.09 GHz.

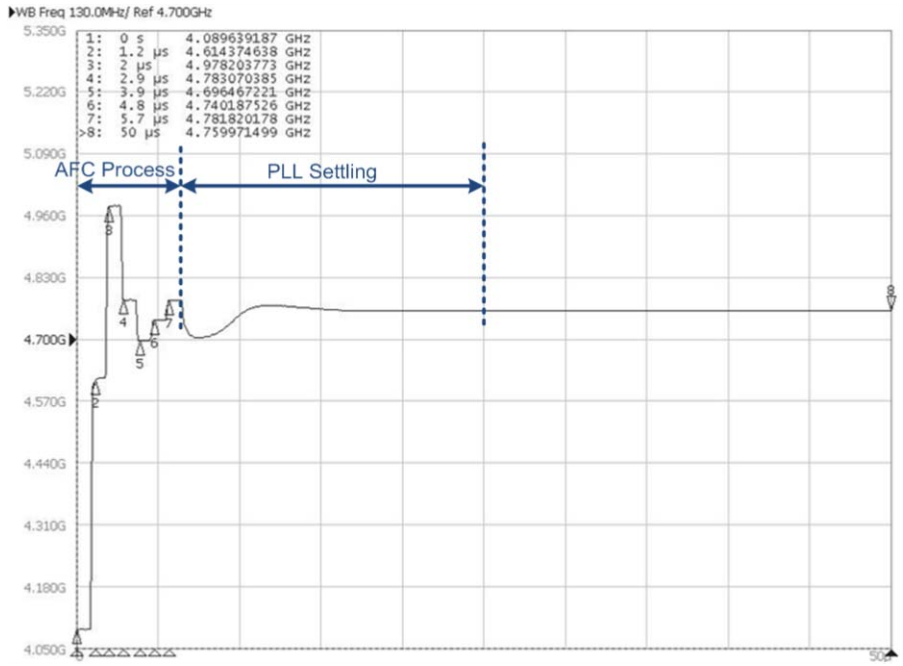
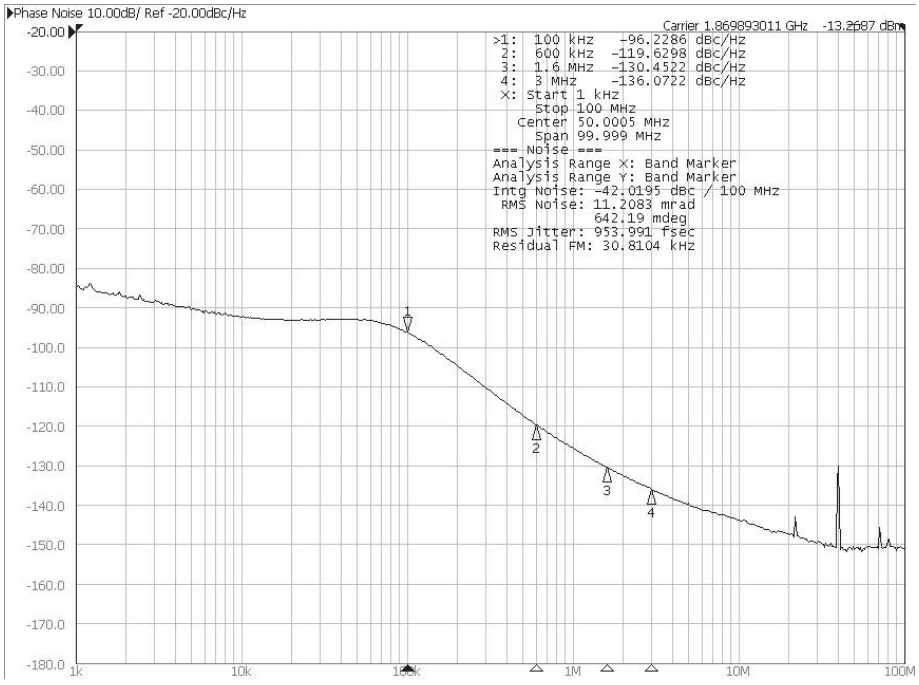
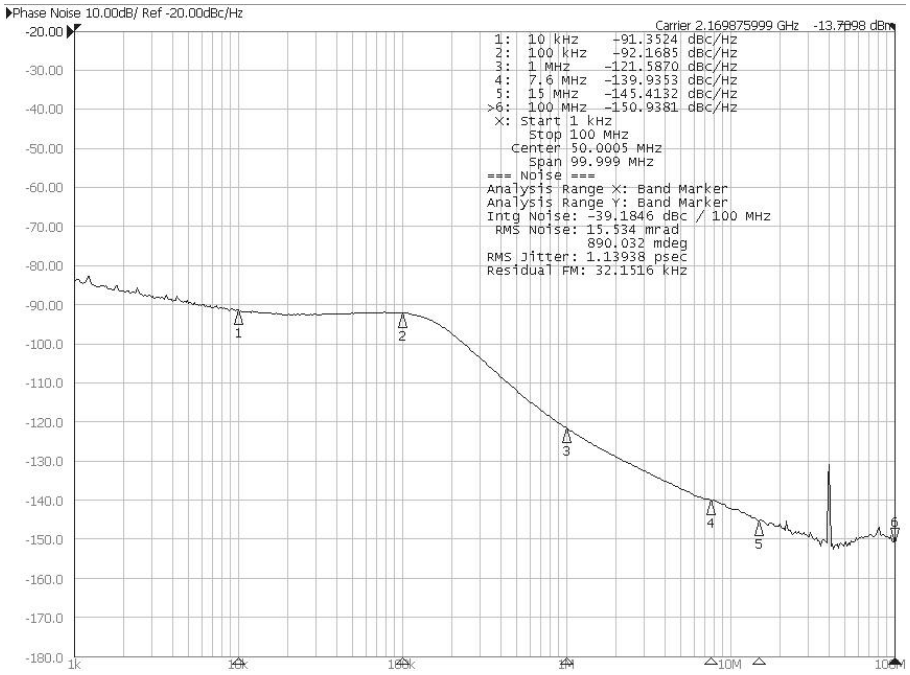


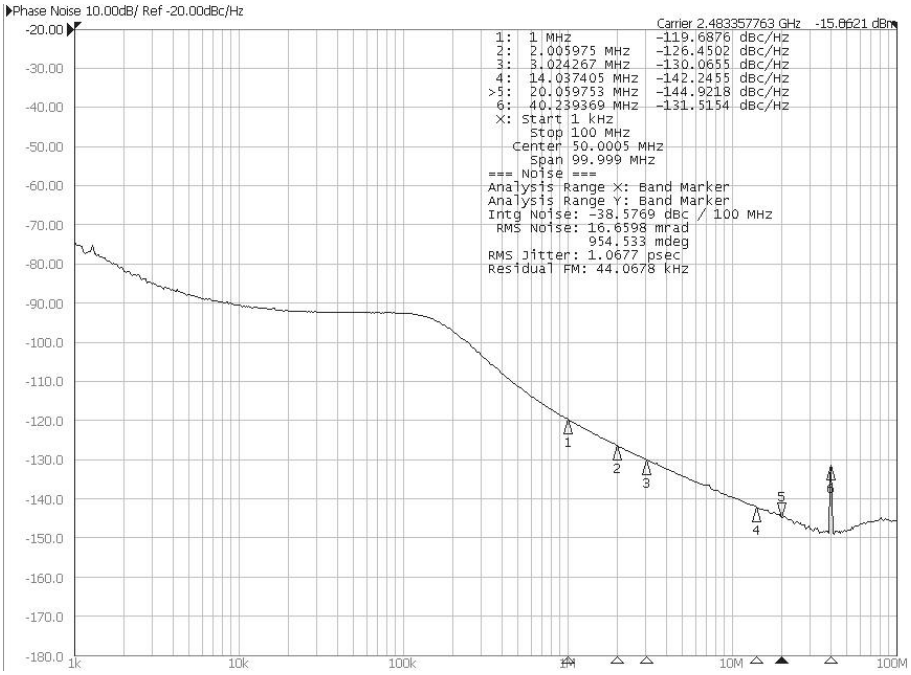
Fig. 4.17: Measured PLL settling time.



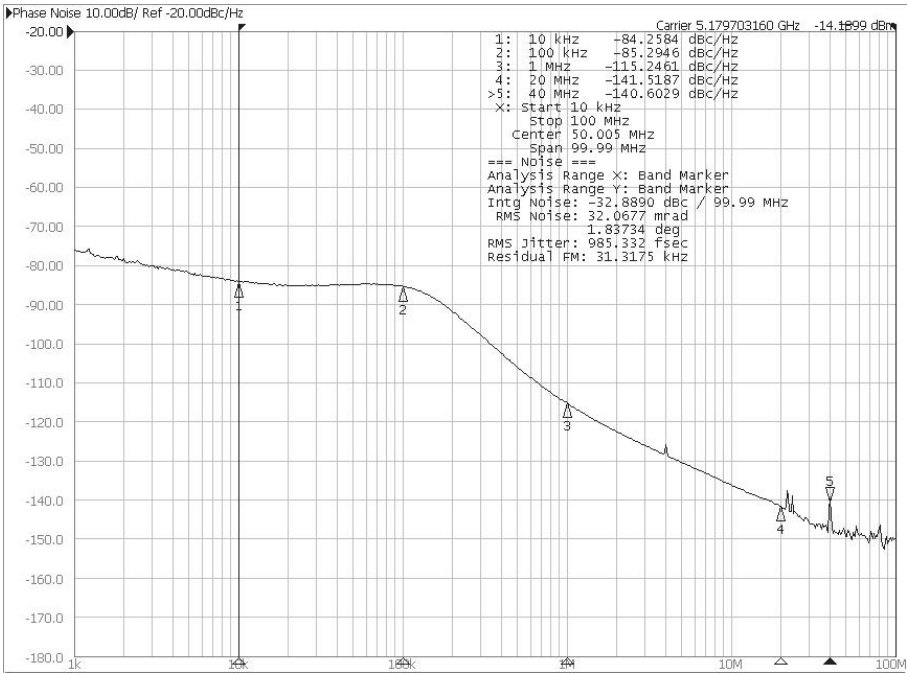
(a)


Phase Noise 10.00dB/ Ref -20.00dBc/Hz
Carrier 2.169875999 GHz -13.7098 dBm
1: 10 kHz -91.3524 dBc/Hz
2: 100 kHz -92.1685 dBc/Hz
3: 1 MHz -121.5870 dBc/Hz
4: 7.6 MHz -139.9353 dBc/Hz
5: 15 MHz -145.4132 dBc/Hz
>6: 100 MHz -150.9381 dBc/Hz
X: Start 1 kHz
Stop 100 MHz
Center 50.0005 MHz
Span 99.999 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -39.1846 dBc / 100 MHz
RMS Noise: 15.534 mrad
890.032 mdeg
RMS Jitter: 1.13938 psec
Residual FM: 32.1516 kHz
-20.00
-30.00
-40.00
-50.00
-60.00
-70.00
-80.00
-90.00
-100.0
-110.0
-120.0
-130.0
-140.0
-150.0
-160.0
-170.0
-180.0
1k
10k
100k
1M
10M
100M

(b)


Phase Noise 10.00dB/ Ref -20.00dBc/Hz
Carrier 2.483357763 GHz -15.8621 dBm
1: 1 MHz -119.6876 dBc/Hz
2: 2.005975 MHz -126.4502 dBc/Hz
3: 3.024267 MHz -130.0655 dBc/Hz
4: 14.037405 MHz -142.2455 dBc/Hz
>5: 20.059753 MHz -144.9218 dBc/Hz
6: 40.239369 MHz -131.5154 dBc/Hz
X: Start 1 kHz
Stop 100 MHz
Center 50.0005 MHz
Span 99.999 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -38.5769 dBc / 100 MHz
RMS Noise: 16.6598 mrad
954.533 mdeg
RMS Jitter: 1.0677 psec
Residual FM: 44.0678 kHz
-20.00
-30.00
-40.00
-50.00
-60.00
-70.00
-80.00
-90.00
-100.0
-110.0
-120.0
-130.0
-140.0
-150.0
-160.0
-170.0
-180.0
1k
10k
100k
1M
10M
100M

(c)



(d)

Fig. 4.18: Phase noise measurement results: (a) DCS1800, (b) WCDMA, (c) Bluetooth/802.11b/g, and (d) 802.11a.

The synthesizer phase noise measurement is carried out by an Agilent E5052B signal source analyzer. Fig. 4.18 shows the measured phase noises. The in-band phase noise of the 1.87 GHz LO corresponding to the DCS 1800 standard is -92 dBc/Hz. The spot phase noises are -119.6, -130.4 and -136 dBc/Hz at 600 kHz, 1.6 MHz and 3 MHz frequency offset, respectively, satisfying the design specifications. Measurement results show that a -121.58 dBc/Hz phase noise at 1 MHz offset frequency is achieved at 2.17 GHz which is in the WCDMA frequency band. As mentioned in the system design section, the far-out phase noise is also important for the WCDMA mode. The phase noise measurement shows that the noise floor is -150 dBc/Hz, which satisfies the requirement. There exists a ~10 dB difference between the simulated and measured noise floors. The deterioration is

due to the test buffer. The simulated QVCO phase noises before and after the test buffer confirm the noise floor difference. For TD-SCDMA, Bluetooth and 802.11 b/g standards, the phase noise is from -118 to -121 dBc/Hz at 1 MHz and the in-band phase noise is about -90 dBc. For the 802.11a standard, the measured phase noise at 1 MHz offset frequency ranges from -113 to -115 dBc/Hz. However, the close-in phase noise is -85 dBc/Hz and the resulting RMS noise, which is integrated from 10 kHz to 100 MHz, is about 2°, or -29 dBc. This result does not meet our design target. This, however, can be corrected by reducing the charge pump noise. The RMS noises of other standards integrated from 1 kHz to 100 MHz are also shown in Fig. 4.18 and are less than 1°. The phase noise and the fractional spurs are degraded when the integer number of the division ratio is around 128. The reason is that the non-linearity of the divider becomes important in this situation due to the divide-modulus-dependent delay. The programmable divider in Fig. 4.12 swaps between the 6-cell and 7-cell configurations and the delays from the input to the output of multiplexer are different in these two configurations. The non-linearity of the divider degrades the SDM output pattern's randomness and folds the quantization noise into in-band frequency. This problem can be solved by adding a retiming flip-flop at the output of the multiplexer.

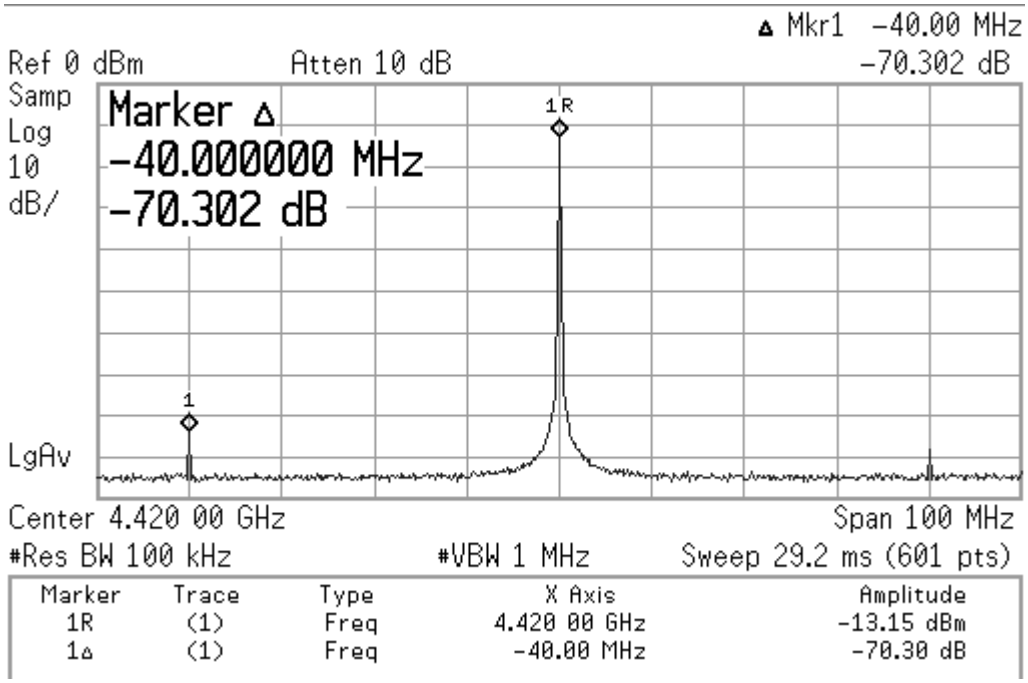


Fig. 4.19: Measured reference spurs.

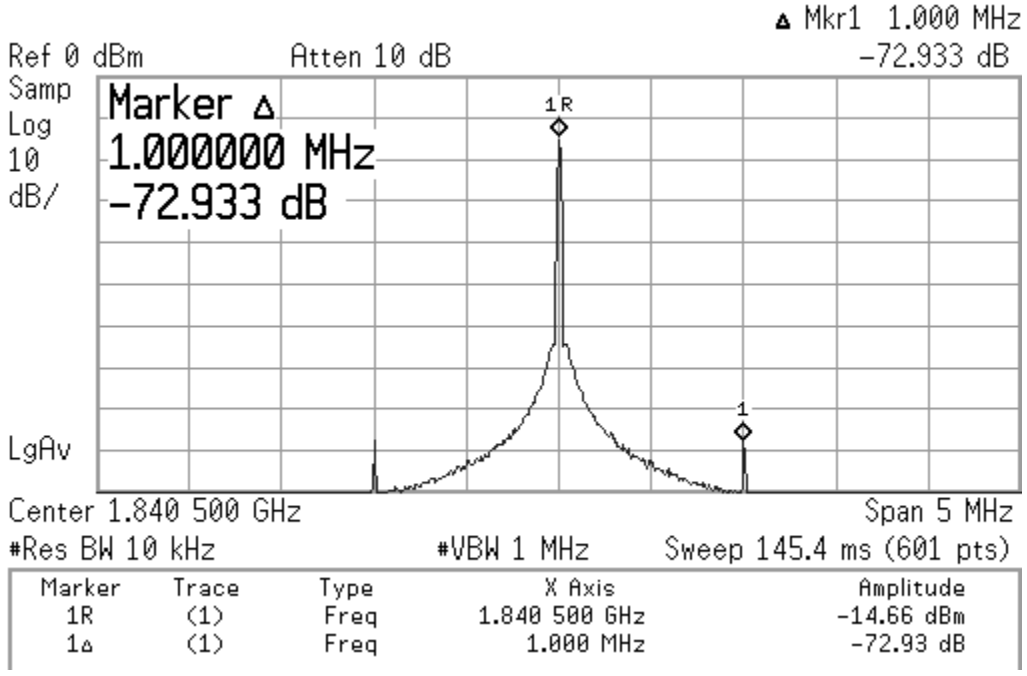


Fig. 4.20: Measured fractional spurs.

Table 4.3: Summary of the measurement results

Standards	Measured phase noise		Simulated phase noise	Phase noise design target
	Spot phase noise	RMS phase noise		
DCS1800 (1805~1880MHz)	-119.6 dBc/Hz@600 kHz -130.4 dBc/Hz@1.6 MHz -136.1 dBc/Hz@3 MHz	0.64°	-119.5 dBc/Hz@600 kHz -130.2 dBc/Hz@1.6 MHz -136.2 dBc/Hz@3 MHz	-119 dBc@600 kHz -129 dBc@1.6 MHz -136 dBc@3 MHz
WCDMA (2110~2170MHz)	-92.2 dBc/Hz@100 kHz -121.5 dBc/Hz@1 MHz -150 dBc/Hz@100 MHz	0.89°	-95 dBc/Hz@100 kHz -122.5 dBc/Hz@1 MHz -160 dBc/Hz@100 MHz	-108.8 dBc@7.6 MHz -120.8 dBc@15 MHz -150 dBc@130MHz
TD-SCDMA (1880~2400MHz)	-93.5 dBc/Hz@100 kHz -121.4 dBc/Hz@1 MHz -132.4 dBc/Hz@3.2 MHz	0.8°	-92.4 dBc/Hz@100 kHz -122.1 dBc/Hz@1 MHz -134 dBc/Hz@3.2 MHz	-111 dBc@3.2 MHz -123 dBc@5 MHz
Bluetooth/802.11 b/g (2400~2480MHz)	-92 dBc/Hz@100 kHz -119.6 dBc/Hz@1 MHz -144.9dBc/Hz@20 MHz	0.95°	-91.6 dBc/Hz@100 kHz -120.1 dBc/Hz@1 MHz -149dBc/Hz@20 MHz	-81 dBc@1 MHz -111 dBc@2 MHz -121 dBc@3 MHz
802.11a (5180~5805MHz)	-85.2 dBc/Hz@100 kHz -115.2 dBc/Hz@1 MHz -141.5 dBc/Hz@20 MHz	1.8°	-85.2 dBc/Hz@100 kHz -115.2 dBc/Hz@1 MHz -142.5 dBc/Hz@20 MHz	-90 dBc@10 kHz -100.2 dBc@20 MHz -116.2 dBc@40 MHz
Loop bandwidth	60 kHz ~ 90 kHz			
Locking time	<50 μs (BW = 90 kHz)			
Reference Spur	<-69 dBc@40 MHz			
Fractional Spur	-72.93 dBc@1 MHz			
Power Dissipation mW	49.12~52.62(802.11a);35.6~44(standards except 802.11a)			
	QVCO: 7.68~17.8		HR-SSBmixer: 8.35	
	QVCO Buffer: 11~12.7		Divide-by-2(incl. buffer): 4.58	
	PLL (without osc.): 11.08		Divide-by-4(incl. buffer): 8.11	
Die Area	1.36×1.37 mm^2 (core circuits)			

The measured reference spur at 40 MHz as shown in Fig. 4.19 is about -70 dBc. Fig. 4.20 shows that the measured fractional spur at 1 MHz is -72.93 dBc. The reference spur at the 40 MHz offset frequency is important for the 802.11a/g modes. The measured reference spurs safely meet the design requirements listed in Table 4.1. The measured in-band fractional spurs are from -33 dBc to -42 dBc. The in-band fractional spurs are worse

than those measured at 1 MHz frequency offset since they are less attenuated by the PLL. The in-band fractional spurs can be further reduced by improving the charge pump linearity. Table 4.3 summarizes the measurement results mentioned above. It also includes the simulated phase noise results, and the design targets of the spot phase noise.

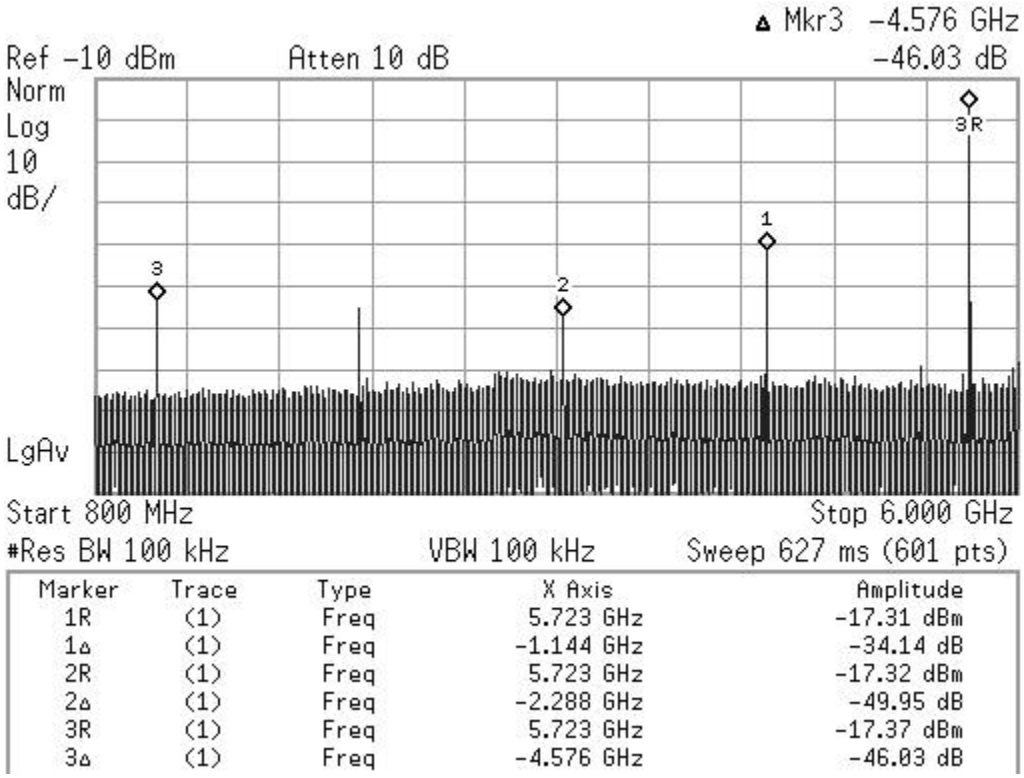


Fig. 4.21: HR-SSBmixer output spectrum.

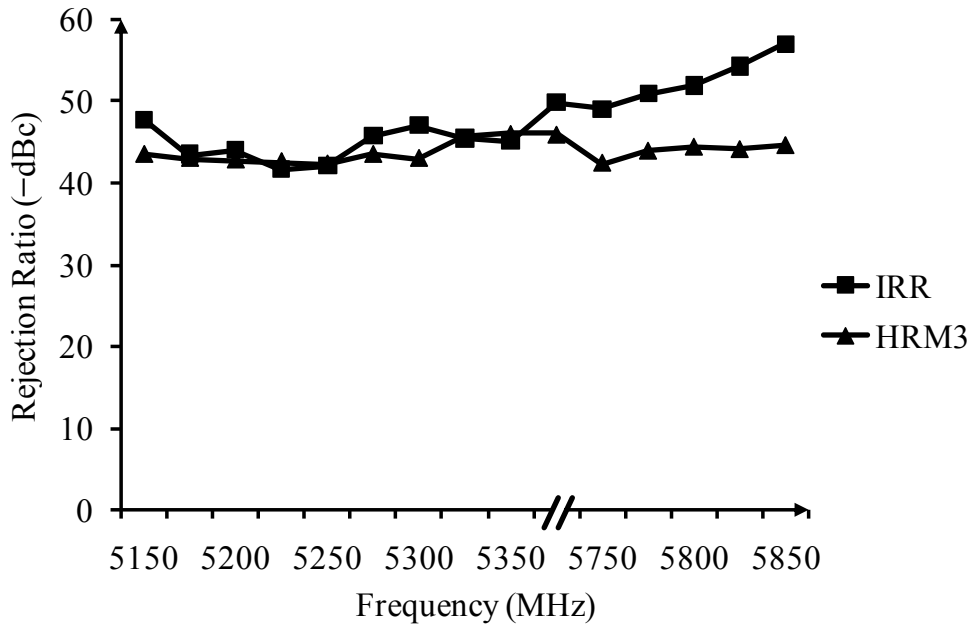


Fig. 4.22: Third-order harmonic rejection and image rejection of the HR-SSBmixer.

The output spectrum of the HR-SSBmixer is shown in Fig. 4.21. The markers 1, 2 and 3 indicate the suppression of the QVCO signal feed-through from the HR-SSBmixer's input to its output, the image signal suppression and the third-order input harmonic suppression, respectively. The QVCO signal feed-through can be further improved. However, since the QVCO does not oscillate at any of the frequency bands of the supported standards, the QVCO signal feed-through itself is not a major issue. The results of the third-order harmonic rejection (HRM_3) and the image rejection ratio (IRR) are plotted in Fig. 4.22. The rejection ratios across the entire 802.11a frequency band are all greater than 40 dB. Simulations, however, find that the HRM_3 and the IRR in the same frequency band are over 50 dB and the QVCO signal feed-through is less than -65 dBc. We believe that the QVCO signal leakage is due to the substrate leakage and the electric-magnetic coupling between the two inductors, which are not included in the post-layout simulations. The

intermodulation between the QVCO leakage signal and the desired LO can deteriorate the HRM_3 and the IRR through the test buffer non-linearity. As discussed previously, the image sideband of the HR-SSBmixer falls into the WiMax frequency band when the receiver operates in the 802.11a U-NII upper-band mode. The measured IRR is from 49.1 dBc to 57.1 dBc for this frequency band. The *SNR* specification for 802.11a is 28 dB [4]. Thus, the maximum allowed WiMax interference signal level is 21~29 dB greater than the desired signal level assuming no suppression by the receiver front-end pre-filter. This number can be further improved to 52 dB by adding a calibration circuit to the HR-SSBmixer [63]. If the interference signal level is much stronger than the above numbers, then a dedicated SAW filter for the 802.11a mode is needed at the receiver front-end to further suppress the WiMax interference signal. To estimate the phase accuracy of the LO signals, the IRR of the SSBmixer of the transmitter can often be used [12]. However in our case, the IRR is affected by many factors. The I/Q amplitude/phase mismatches of the QVCO signals and the divide-by-4 output signals as well as the test buffer non-linearity all can deteriorate the sideband rejection while the band-pass frequency response of the HR-SSBmixer's load improves the rejection ratio to some extent. As a rough estimation, we assume that the QVCO phase mismatch mainly causes the image sideband. Since the sideband rejections shown in Fig. 4.22 are all larger than 41.7 dBc, the worst-case QVCO output phase mismatch can thus be estimated to be 0.94° [12]. In Fig. 4.21 a spurious signal is found at $f_{vco}/2$ which falls into the WCDMA frequency band. It is due to the signal leakage from the divide-by-2 circuit's output to the output of the HR-SSBmixer. This can be solved by separating the power supplies of the divide-by-2 and the divide-by-4 circuits. The divide-by-2 circuit can then be turned off when the HR-SSBmixer is activated for

generating the 802.11a carrier frequency. Table 4.4 compares the proposed synthesizer design with published state-of-the-art multi-standard analog LO generation systems for wireless applications. In the comparison table, it should be mentioned that [45] [48] [64] use lookup tables instead of AFC to search the VCO tuning curves. The lookup table method, however, often requires extra on-chip process-voltage-temperature (PVT) detection circuits to update the table contents, while the AFC approach inherently counteracts the PVT variations.

Table 4.4: Performance comparison of frequency synthesizers

	[44]	[64]	[48][5]	[45]	**This work**
Technology	0.25-µm BiCMOS	0.13-µm CMOS	0.13-µm CMOS	45-nm CMOS	0.13-µm CMOS
Power(mW)	NA	40.8~69.6	5.28~28.8	21.45~31.35[6]	35.60~52.62
Area(mm^2)	1.7×1.5	NA	NA	1.02×0.4	1.36×1.37
Output Range(GHz)	0.8~5.8	0.1~6	0.1~6	0.1~5	1.8~6
Phase Noise @1 MHz	-123 dBc/Hz (LO:3.77 GHz)	-115 dBc/Hz (LO:4 GHz)	-115dBc/Hz (LO:5 GHz)	-112 dBc/Hz (LO:7.2 GHz)	-115 dBc/Hz (LO:5.18 GHz)
VCO/QVCO *FOM*(dB)	189.25	178~188	179~185	183	179.5~185.2
AFC Integration	NO	NO	NO	NO	YES
Spur Performance(dBc)	NA	NA	<-30 @SSBmixer	NA	-69@40 MHz -72.93@1 MHz <-42.4@HR-SSBmixer

[5] Power consumption of the PLL is not included. Phase noise and VCO data are from [67]
[6] Power consumption of the LO generation circuits outside the PLL is not included.

4.5 Summary

A fractional-N frequency synthesizer for cellular and short-range wireless communication receiver is presented. The synthesizer supports the standards of DCS1800, WCDMA, TD-SCDMA, WLAN 802.11 a/b/g and Bluetooth. Architecture design and frequency planning are carefully performed to ensure that the synthesizer meets the specifications of the above mentioned standards and at the same time achieves an optimal tradeoff among synthesizer performance, hardware complexity and power efficiency. A new phase-shift scheme to improve QVCO phase noise and to eliminate bimodal oscillation is developed. Combining harmonic rejection and single sideband mixing, the HR-SSBmixer is developed to suppress spurious signals. The residual spurs due to phase and gain mismatches are analyzed. Designed in a 0.13-μm CMOS technology, the synthesizer occupies an active area of 1.86 mm^2 and consumes 35.6 to 52.62 mW of power. Measurement results show that the synthesizer frequency range, the phase noise, the settling time and the spur performances meet the design specifications of the standards mentioned above. It should be mentioned that the synthesizer performance also meet the WLAN and Bluetooth transmitter requirements. This is important since for WLAN and Bluetooth applications, often there is only one frequency synthesizer for both the transmitter and the receiver. The PLL close-in phase noise can be further improved in the 802.11a mode to reduce the RMS noise. This can be achieved by optimizing noise and linearity of the charge pump. A retiming circuit can be added to the programmable divider to ensure that its non-linearity does not impair PLL in-band phase noise. The HR-SSBmixer spur rejection can be further increased by strengthening the isolation between the QVCO and the HR-SSBmixer.

CHAPTER 5. A TIME-TO-DIGITAL CONVERTER-BASED AFC FOR WIDE-RANGE FREQUENCY SYNTHESIZERS

5.1 Introduction

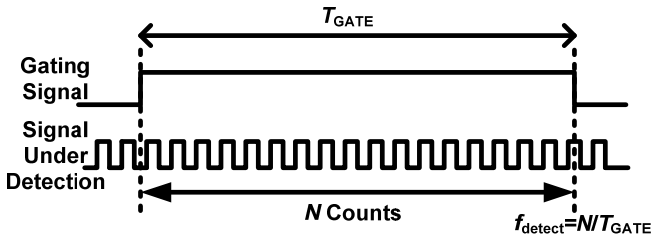
AFC circuit is needed for frequency synthesizers that cover a wide frequency range. Depending on the frequency detection approach, the AFC can be categorized as TVC-based AFC and counter-based AFC. The TVC-based AFC converts the frequency information to an analog voltage. Although it can provide fast AFC calibration, this method is very sensitive to circuit mismatch and comparator offset. The counter-based AFC, on the other hand, relies mainly on digital circuits and thus is more robust to circuit non-ideal effects. It does not require well-matched analog circuitries and also occupies less chip area. However, it requires a long counting time in order to reduce the frequency detection error, which is caused by the initial phase uncertainties between the two input signals of the counter. In this chapter, a TDC-based AFC technique is proposed to improve the frequency detection accuracy for the counter-based AFC method [37].

5.2 Counter-based AFC Design Analysis

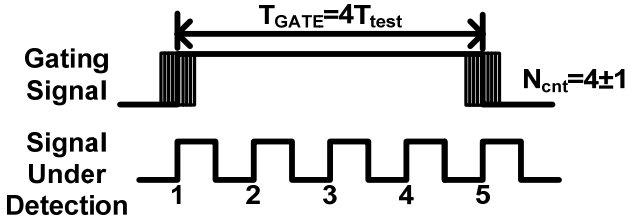
5.2.1 Error Mechanisms in the Counter-based AFC

The frequency calibration accuracy of the AFC is mainly determined by the frequency detection accuracy, which is based on cycle counting. As shown in Fig. 5.1(a), if there are N cycles of signal under detection in a given counting window T_{GATE}, then the detected signal frequency f_{detect} is N/T_{GATE}. However, due to the initial phase uncertainty,

the jitter in the gating signal and the integer counter rounding effect, the counting result for a signal with a frequency f_{detect} can become $round(f_{detect} \cdot T_{GATE}) \pm 1$ as indicated in Fig. 5.1(b), where the *round* function returns the closest integer to the argument. It should be noted that since the gating signal is derived from the PLL reference clock whose peak-to-peak jitter is at least one order smaller than the VCO output period, the rounding error is usually less than 1. The frequency detection error of $\pm 1/T_{GATE}$ caused by the initial phase uncertainty and jitter of the input signal is the frequency resolution that the counter-based frequency detector can provide [17]. To reduce the error, a long counting time is required, which unfortunately increases the synthesizer locking time.



(a)



(b)

Fig. 5.1: (a) Counter-based frequency detection; (b) Frequency detection error.

Besides the frequency detection error, the finite-precision numerical effect of the division ratio $2^{M-1} \times N.\alpha$ can also cause an incorrect AFC operation. As shown in Fig 2.13

and Fig. 5.2, only the integer part of $2^{M-1} \times N.\alpha$ is treated as the expected number of VCO cycles in the conventional counter-based AFC method. The omitted fractional component, however, may cause errors in determining the target frequency through the binary searching process [16]. The worst-case numerical truncation error is $1/2^{M-1}$.

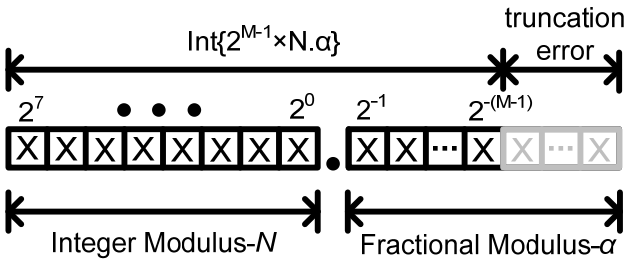


Fig. 5.2: Truncation of the division ratio in the counter-based AFC.

To evaluate the effect of these two error mechanisms, the minimally required error-free counting time for the counter-based AFC method will next be derived.

5.2.2 Minimum Counting Time Requirement

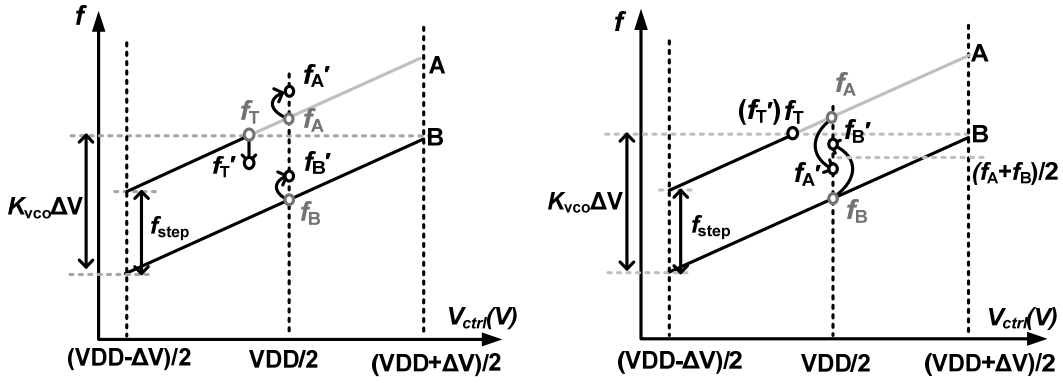


Fig. 5.3: Two worst-case scenarios causing incorrect AFC operation.

The AFC counting time should ensure that the VCO tuning curves covering the target frequency can be selected even with the frequency detection error. In deriving the counting time requirement, two worst-case scenarios of incorrect AFC operations as shown in Fig. 5.3 are considered. The curves A and B are two VCO tuning curves with f_A and f_B being their midpoint frequencies. During the AFC operation, f_A and f_B are detected and then compared with the target frequency f_T. The curve with its midpoint frequency closer to the target frequency needs to be selected. However, due to the frequency detection and the division ratio truncation errors, the AFC may select a wrong tuning curve. If the selected curve does not cover the target frequency, then the PLL cannot be locked after it takes over the VCO control. Fig. 5.3 shows the above situation as well as its causes. Fig. 5.3(a) depicts the scenario where the frequency detection error causes the detected frequencies to both exhibit a positive error relative to their true value, i.e., the detected frequencies become f_A' and f_B', respectively, and simultaneously the target frequency due to the division ratio truncation error becomes f_T'. In this case, the AFC will mistakenly choose curve B if f_T' is closer to f_B' than f_A'. Fig. 5.3(b) depicts another worst-case scenario where the detected frequency errors have opposite signs and there is no division ratio truncation error. Then, if f_A' and f_B' cross over $(f_A + f_B)/2$, then the AFC will also mistakenly choose tuning curve B.

To avoid these two situations, we need to ensure that $|f_A' - f_T'| < |f_B' - f_T'|$ under the frequency detection and the division ratio truncation errors. Therefore, the following two equations need to be satisfied.

$$f_{step} - 0.5K_{vco}\Delta V + 2/(2^{M-1}T_{ref}) < 0.5K_{vco}\Delta V - 2/(2^{M-1}T_{ref}) \tag{5.1}$$

$$f_{step}/2 > 1/(2^{M-1}T_{ref}) \tag{5.2}$$

In deriving the inequalities, the frequency detection error of $1/T_{GATE}=1/(2^{M-1}T_{ref})$ as discussed in Section 5.2.1 is assumed. The worst-case error of f_T due to the division ratio truncation error as discussed in 5.2.1 is also $1/(2^{M-1}T_{ref})$. Eq. (5.1) ensures that f_T' is closer to f_A' than f_B' in Fig. 5.3(a) while (5.2) guarantees that f_A' and f_B' do not cross over the frequency point $(f_A + f_B)/2$ in Fig. 5.3(b). From (5.1) and (5.2), the minimally required counting window width can thus be derived as

$$2^{M-1}T_{ref} = \max\left\{\frac{4}{K_{vco}\Delta V - f_{step}}, \frac{2}{f_{step}}\right\} \tag{5.3}$$

In this derivation, $K_{vco}\Delta V$ is assumed to be larger than f_{step}, which is typically true since no frequency gap is allowed between two adjacent tuning curves in the VCO design. According to (5.3), the required AFC counting time for one comparison can be calculated. For instance, assuming that f_{ref} = 40 MHz, $K_{vco}\Delta V$ = 35 MHz, and the f_{step} is 17.5 MHz, then from (5.3), 2^{M-1} needs to be larger than 9.1. Since M is an integer, M = 5 is required, and thus the width of the counting window needs to be $2^{M-1} \times T_{ref} = 16 \times T_{ref.}$

Next, we study how to reduce the AFC calibration time. Define the VCO tuning curve overlapping ratio (*OLR*) as

$$OLR = 1 - \frac{f_{step}}{K_{vco}\Delta V} \tag{5.4}$$

The OLR represents the ratio of the overlapping portion of two adjacent VCO tuning curves over the frequency range covered by a single tuning curve. Then, (5.1) can be rewritten as

$$2^{M-1}T_{ref} > \frac{4}{(K_{vco}\Delta V)OLR} \tag{5.5}$$

From (5.5), it can be observed that reducing the calibration time can be achieved by increasing the *OLR*. This can be done by expanding the frequency covering range of a single tuning curve (i.e. larger $K_{vco}\Delta V$) or reducing the tuning curve distance (i.e. smaller f_{step}) . Although, reducing the f_{step} can increase the *OLR*, yet the minimum f_{step} is constrained by the second term in (5.3). Therefore, the most effective approach to reduce the calibration time is to use a larger VCO gain K_{vco}. This, however, is at the expense of degrading the VCO phase noise performance.

In the above analysis, constant f_{step} and K_{vco} for adjacent tuning curves are assumed. However, in a real VCO design, the tuning curves are often not equally spaced and K_{vco} varies for different frequencies. The following analysis is performed to show that (5.3) can still be applied to find the minimally required counting window width as long as f_{step} and K_{vco} of the lowest frequency tuning curve are used. Firstly, f_{step} and K_{vco} for different midpoint frequencies can be written as

$$f_{step} = 2\pi^2 f_0^3 L C_{step} \tag{5.6}$$

$$K_{vco} = 4\pi^3 f_0^3 L \frac{\partial C_v}{\partial V_{ctrl}} \tag{5.7}$$

where f_0 is the midpoint frequency for a tuning curve, L is the inductance; C_{step} is the unit capacitance of the binary switch capacitor array; C_v is the varactor in the LC tank. In (5.6) and (5.7), L, C_{step} and $\partial C_v / \partial V_{ctrl}$ are weak functions of the VCO frequency f_0 and can be considered as constant. Therefore, the denominators in the two variables of (5.3) are both proportional to f_0. As long as (5.3) is satisfied for the lowest frequency tuning curve, the AFC counting window will be wide enough for other curves.

5.3 Proposed TDC-Based AFC

According to the above analysis, it can be found that the AFC frequency detection principle is quite similar to the time-to-digital converter in an all-digital phase-locked loop (ADPLL) [2]. In the divider-less ADPLL, the TDC compares the digitally-controlled oscillator (DCO) output signal with the reference signal by computing the number of DCO periods between two adjacent reference edges, i.e. the ratio between the DCO frequency and the PLL reference frequency. This can be implemented by an integer counter, but the resolution is limited to the DCO period which is too coarse for most applications. To improve the resolution, a fractional counter computing the residual time distance between the two reference edges after integer counting has been proposed in [2]. The fractional counter measures the residual time distance between each reference edge and the last DCO edge by using a multi-phase DCO output signal. This concept can be applied to the AFC design to reduce the counting error due to the initial phase uncertainty and the jitter of the VCO output.

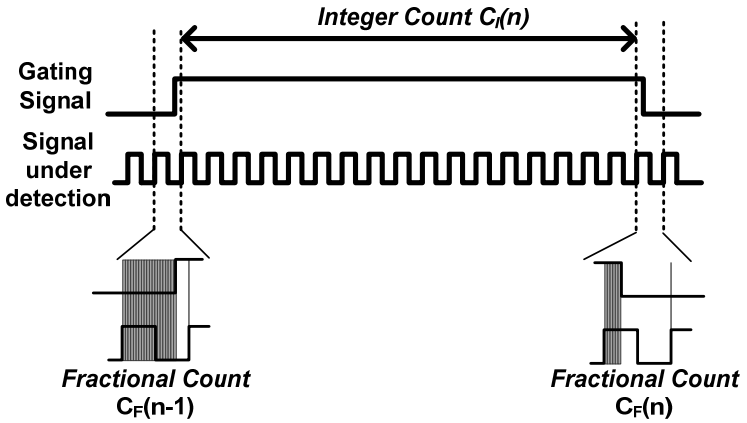


Fig. 5.4: Fractional-counter-assisted frequency detection.

The concept is shown in Fig. 5.4. Similar to Fig. 5.1(a), the frequency detection is carried out by counting the number of VCO signal's rising edge in the counting window. In the conventional counter-based AFC, the integer counting result $C_I[n]$ is used as the indicator of the VCO frequency and fed to the finite state machine. This, however, is not accurate since it only indicates that there are $C_I[n]-1$ complete VCO cycles in the counting window. To measure the residual fractional VCO cycle, the fractional counter quantifies the shaded area in Fig. 5.4 as the number of delay unit at the beginning and the end of the counting window. The residual time distance in the counting window thus becomes $C_F[n]+(1-C_F[n-1])$. Therefore, $N_{int+frac}[n]$, the ratio of the counting period over the VCO period can be computed as

$$N_{int+frac}[n] = C_I[n] + (C_F[n] - C_F[n-1]) \tag{5.8}$$

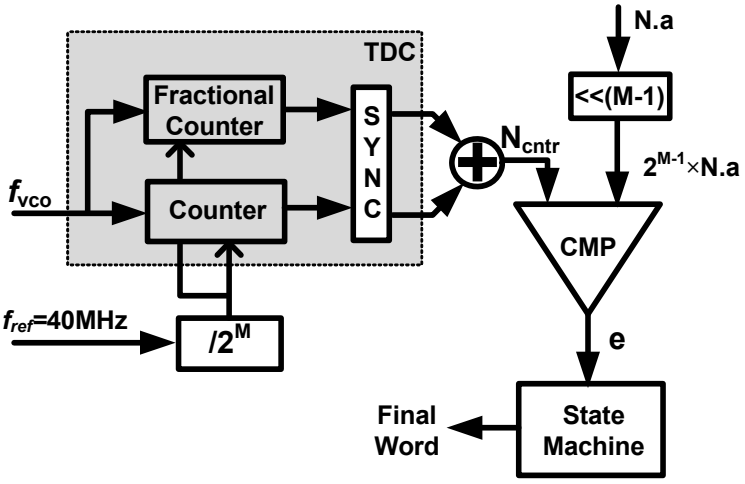


Fig. 5.5: Proposed TDC-based AFC.

Fig. 5.5 shows the proposed AFC circuit that uses the TDC. It is similar to the integer-counter-based AFC shown in Fig. 2.13. The difference is that it adds a fractional counter to assist the AFC to evaluate the VCO frequency. Doing so enables the N_{cntr} to

contain the complete VCO cycle information with both the integer and fractional results. The N_{cntr} can then be compared with the PLL division ratio avoiding the truncation error. There are two improvements in this design that uses the TDC for the frequency detection. First, the frequency detection accuracy is increased because of the fractional period estimation. Second, the comparison in the AFC is no longer limited to the integer part of $2^{M-1} \times N.\alpha$. The fractional part of the division ratio is also included in the comparison, thus the target frequency offset caused by division ratio truncation is reduced. These improvements significantly improve the AFC accuracy and reduce the calibration time.

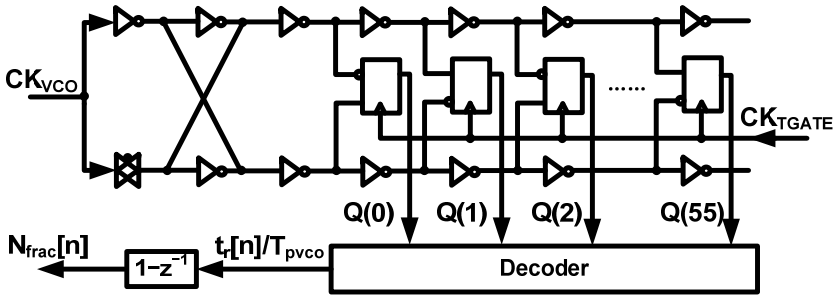


Fig. 5.6: Fractional counter implementation in the TDC-based AFC.

The TDC in this work shown in Fig. 5.5 adopts a configuration similar to that in [65], where an integer counter is used in conjunction with a fractional counter. The fractional counter implementation is shown in Fig. 5.6. The digital fractional phase is obtained by passing the VCO clock through a chain of inverters. In Fig. 5.6, $t_r[n]$ is the time distance between each counting edge and the last VCO edge. After being normalized to the VCO period T_{pvco}, it is equal to $C_F[n]$ in Fig. 5.4. The $N_{frac}[n]$ is the residual fractional VCO period in the counting window.

The smallest time interval T_{res} that can be resolved in the fractional counter is the TDC inverter delay. For a typical 130-nm CMOS technology, it is about 30 ps. The

counting resolution now becomes T_{res}/T_{vco}, where T_{vco} is the VCO output period. Therefore, the frequency detection resolution is reduced to $(T_{res}/T_{vco})/(2^{M-1}T_{ref})$. If all the bits of the division ratio are used in the comparison, then the truncation error becomes zero. Eq. (5.3) for the TDC-based AFC can thus be derived as

$$2^{M-1}T_{ref} = \max\left\{\frac{2T_{res}/T_{vco}}{K_{vco}\Delta V - f_{step}}, \frac{2T_{res}/T_{vco}}{f_{step}}\right\} \tag{5.9}$$

Assume that T_{res} = 30 ps and the VCO output frequency is 5 GHz, then for the same set of VCO tuning curves in Section 5.2.2, the minimally required 2^{M-1} is reduced to 0.68, which is much smaller than that of the integer counter-AFC method.

A typical TDC design in the ADPLL usually involves a calibration loop for the delay cells to compensate their mismatch and PVT variation [2]. They are the major contributions to the in-band spur of the PLL output clock whose performance is critical to wireless communication systems. Therefore, it is needed to carry out the TDC calibration in the ADPLL. The TDC in this design, on the other hand, does not include any calibration loop, The AFC only performs a one-time binary searching process instead of a dynamic locking. The delay cell mismatch and PVT variation are handled by the above counting time calculation using the worst case TDC delay unit.

It should be noted that the proposed TDC-based AFC is not bounded to be used within analog fractional-N PLLs only; it can be implemented for the digital PLL in which a TDC is already embedded in the circuit. For analog PLL, the multi-phase counting requires more hardware than the integer counter-AFC approach. However, the AFC is only activated at the startup of the PLL. Therefore, there is no power penalty during the normal PLL operation.

5.4 Circuit Design

Fig. 5.7 shows the AFC design in a fractional-N PLL whose output frequency ranges from 3.5 GHz to 5 GHz. In order to relax the speed requirement of the AFC counter designed in a 0.13-μm CMOS technology, the VCO output is first divided by 4. The frequency division of the VCO signal degrades the frequency detection resolution to $4(T_{res}/T_{vco})/(2^{M-1}T_{ref})$. T_{res} in this design is about 22 ps, thus the worst-case (i.e. largest T_{vco}) resolution is $0.308/(2^{M-1}T_{ref})$. The programmable divider of the PLL is based on the modular architecture described in [49]. In the startup, the switch SW is open and the programmable divider serves as a divide-by-4 circuit with its first two stages of divide-2/3 cell set at the divide-by-2 mode. We next describe the transistor-level implementation of the TDC and the AFC digital signal processing algorithm.

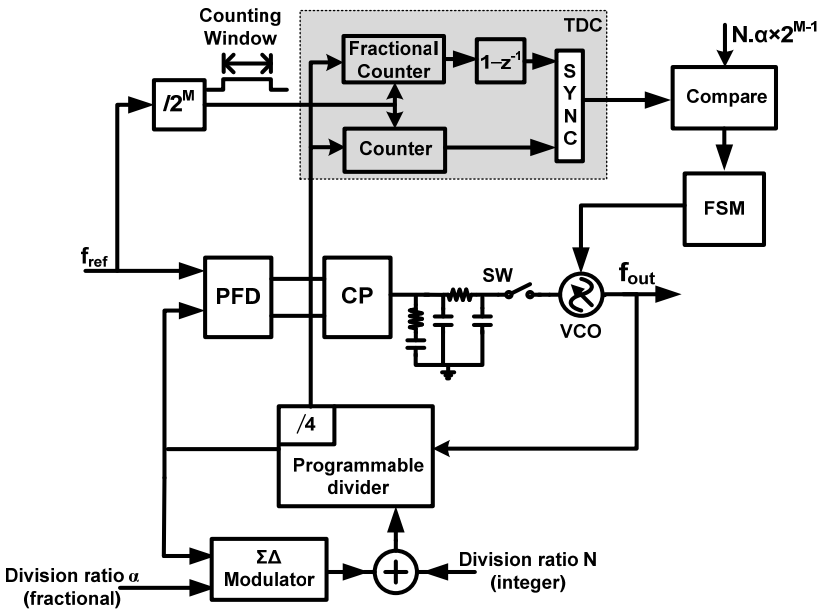


Fig. 5.7: Fractional-N PLL with the TDC-based AFC.

5.4.1 Integer Counter

The integer counter, shown in Fig. 5.8, is based on the asynchronous architecture due to the high frequency property of the input signal. The cascaded TSPC divide-by-2 circuit relaxes the speed requirement of the following synchronous CMOS counter and provides the 3 LSBs of the counting result. A selector before the counter enables/disables the input signal according to the counting window control signal. At the end of the counting interval, the first stage counter input is kept at logic low, and the counter output is frozen. It should be noted that the counter output is not valid at the end of the counting window due to the asynchronous operation. The comparison will not be started until the next FSM clock cycle arrives.

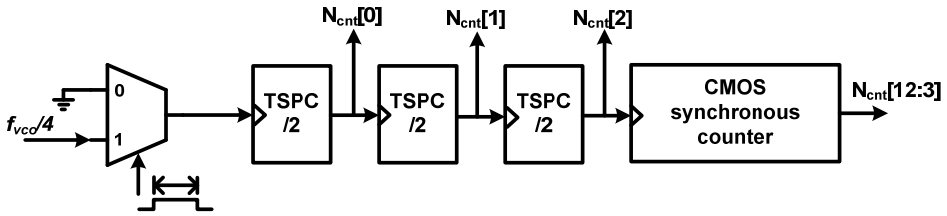


Fig. 5.8: Integer counter.

5.4.2 Fractional Counter

The fractional counter shown in Fig. 5.6 passes the frequency-divided-VCO clock through a chain of delay cells. By comparing the sampling results in two consecutive gating clock sampling edges, the fractional phase information can be quantized as the number of delay cells [65]. To improve the fractional counter resolution, we use inverters instead of buffers as the delay cells. However, this causes a change of signal polarity and makes it harder for the decoder to determine the residual fractional time distance. A sampling

operation based on the differential D-flip flop is adopted to solve this issue [65]. As can be seen in Fig. 5.9, the D-flip flop is constructed by two stages. The first stage is a sense amplifier which generates the output pulses according to the D/Db inputs when the CLK is at a logic high level. The second stage is a latch. During the sense phase (CLK=1), the cross-coupled inverter in the latch is disabled and the latch works as an inverter buffer feeding the Sb/Rb to the D-flip flop output. When CLK=0, the path to GND is blocked while both output nodes are pulled up to VDD by the PMOS transistors, thus the sense amplifier stage outputs logic-high values. The inverter buffers are disabled while the cross-coupled inverters latch the sensed results. Compared to the typical CMOS flip-flop, the sensed amplifier-based fully differential D flip-flop has identical resolution of the rising/falling edge metastability and a smaller metastability window [65].

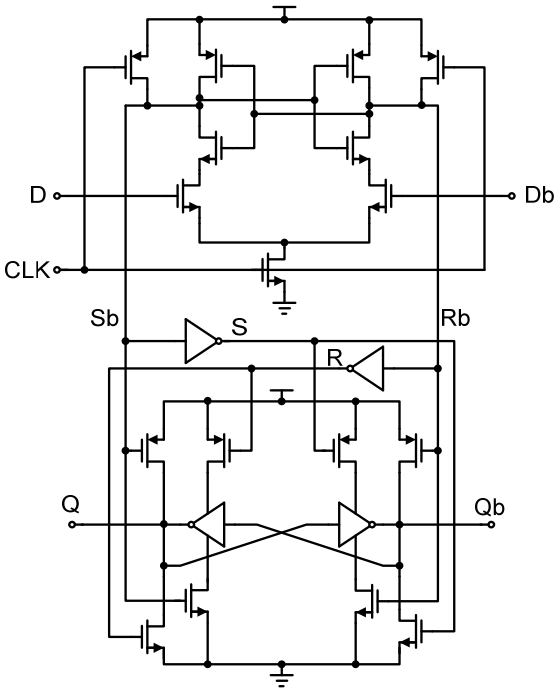


Fig. 5.9: Sense amplifier-based differential D flip-flop.

In designing the TDC, we need to pay attention to the time skew between the inputs of the integer counter and the fractional counter. The input time skew causes misalignment between the respective outputs from the two circuits [2]. Due to the misalignment, an error of 1 appears in the final counting result. This error diminishes the advantage of using fractional counter in AFC frequency detection. To address this issue, dummy circuits have been added to the input stages of the integer counter and the fractional counter. This helps to minimize the time skew caused by the loading effect. It is also important to perform careful layout to ensure identical routing distance between the input signals of the two counters. It should be noted that the re-synchronize circuit in [66] which corrects the error by monitoring the results from the integer and fractional counters cannot be applied in this design because the correction technique in [66] is based on the assumption that the VCO is locked to the target frequency and the frequency error is sufficiently small ($\varepsilon \ll 1$). AFC process is a coarse frequency acquisition where this condition cannot be met.

5.4.3 Decoder

The decoder in the fractional counter calculates the residual fractional phase according to the sampled results. Two cases of the fractional phase estimation are shown in Fig. 5.10. The procedure is similar to [65]. The $t_r[n]$ has been defined in Fig. 5.6 while $t_f[n]$ is the time distance between the counting edge and the last CK_{VCO_d4} falling edge, where CK_{VCO_d4} is the TDC input. The 1 to 0 transition in the sampled result represents a rising edge in the CK_{VCO_d4} and the 0 to 1 transition indicates a falling edge. Therefore, the time distances between the CK_{TGATE} edge and the rising/falling edges of CK_{VCO_d4} can be found by computing the numbers of 1 and 0 before the 1/0 transition in the sampled results.

However, the absolute time distance $t_r[n]$ is not enough to evaluate the fractional phase. Since the integer counter result in (5.8) is given in terms of the number of cycles of CK_{VCO_d4}, $t_r[n]$ needs to be normalized to the CK_{VCO_d4} period before it can be added to the integer counter result. As can be seen in Fig. 5.10, the CK_{VCO_4} period can be computed as

$$T_{pCKVCO\_d4} = 2 \times \left| t_r[n] - t_f[n] \right| \tag{5.10}$$

Normalizing $t_r[n]$ with T_{pCKVCO_d4}, we can obtain $C_F[n]$. The fractional phase $N_{frac}[n]$ is then calculated according to Fig. 5.6.

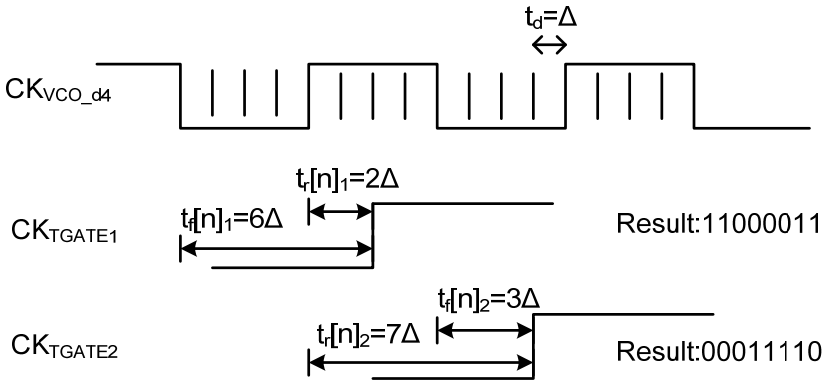


Fig. 5.10: Fractional phase evaluation.

5.5 Simulation Results

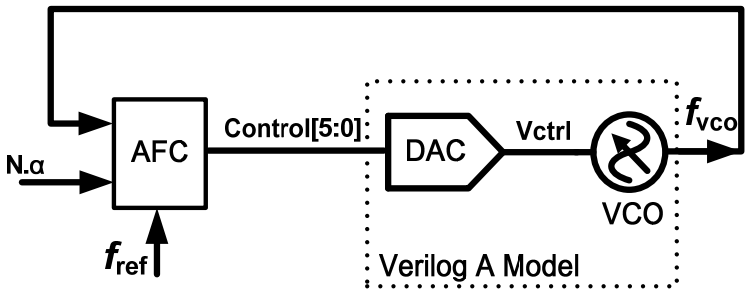


Fig. 5.11: Simulation setup.

The integer counter-based AFC and the TDC-based AFC methods have been designed in a 0.13-μm CMOS technology to verify the above analysis. The TDC in Fig. 5.5 is designed with custom circuits while the FSM and comparator are designed with synthesized digital circuits. A simulation setup shown in Fig. 5.11 is developed to find out the frequency searching behavior of these two methods. The VCO described with a Verilog-A model generates 64 discrete frequency bands ranging from 3.5 GHz to 5 GHz. The f_{step} is about 23.5 MHz. To close the loop with the AFC, an ideal 6-bit DAC is inserted between the AFC and VCO. The reference clock frequency is 40 MHz.

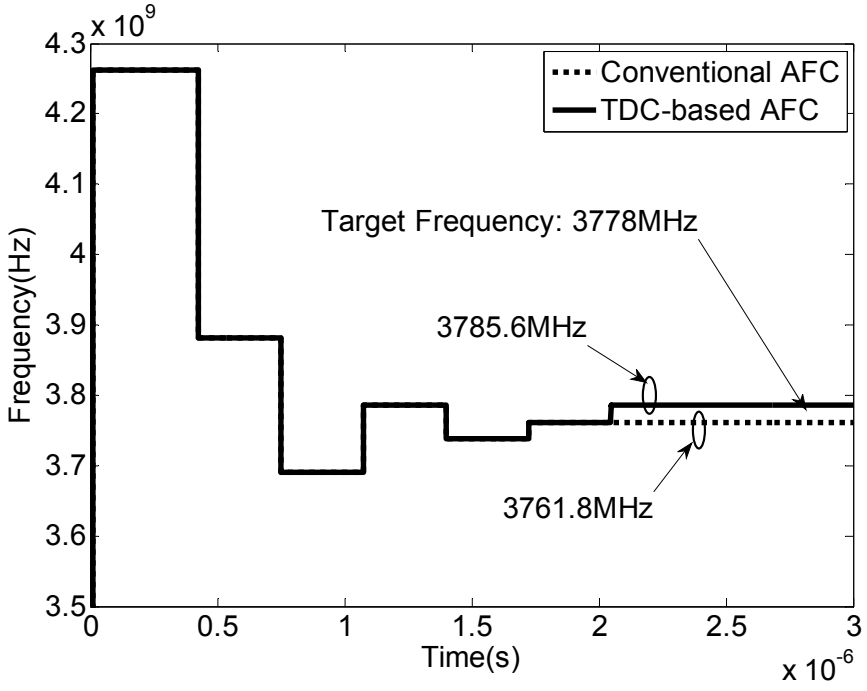


Fig. 5.12: Division ratio truncation effect on the AFC operation.

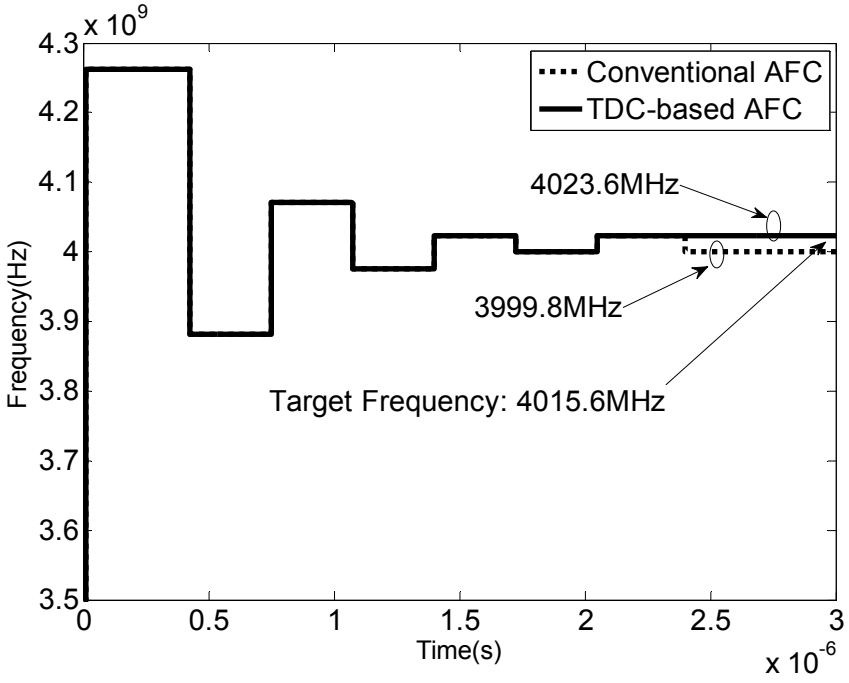


Fig. 5.13: Effect of initial phase uncertainty on the AFC operation.

Fig. 5.12 and Fig. 5.13 show the simulation results of the frequency calibration processes. In the simulation, the calibration accuracies of the two AFC methods are compared for a given counting time, which is set as $2^3 \times T_{ref}$. Fig. 5.12 shows the division ratio truncation effect on the frequency calibration process. The target frequency f_T is 3778 MHz, which is between the two VCO output frequencies of 3761.8 MHz and 3785.6 MHz. The 3785.6 MHz tuning curve should be selected since it is closer to the target frequency. However, because of the division ratio truncation error, the 3760 MHz is considered as the target frequency in the integer counter-based AFC. As a result, the AFC incorrectly chooses the 3761.8 MHz tuning curve. On the other hand, the TDC-based AFC correctly chooses the 3785.6 MHz tuning curve as it has no division ratio truncation error.

Fig. 5.13 shows the initial phase uncertainty effect on the calibration process. A delay element is introduced to the VCO output in the simulation setup to adjust its phase.

The target frequency is set at 4015.6 MHz. Simulation finds that when the delay ranges from 260 ps to 340 ps, the optimal tuning curve cannot be selected in the case of the integer counter-based AFC method. This is because the 4023.6 MHz VCO output is detected as 4040 MHz under this initial phase condition. This causes the AFC to mistakenly determine that the 3999.8 MHz tuning curve is closer to the target frequency. The TDC-based AFC, on the other hand, is less sensitive to the counting signal initial phase uncertainty due to its fractional phase estimation. Thus the frequency is accurately detected and 4023.6MHz frequency is correctly identified to be closer to the target frequency. In summary, the simulation results show that the TDC-based AFC correctly chooses the optimal tuning curves with a $2^3 \times T_{ref}$ counting window due to the improved frequency detection accuracy and the smaller target frequency offset. The integer counter-based AFC, on the other hand, mistakenly selects the suboptimal tuning curves in both simulations because of the frequency detection error and the target frequency truncation error.

Table 5.1 compares the proposed TDC-based AFC with the existing AFC techniques. The TVC-based AFC frequency detector resolution is limited by the matching performance of the analog circuit components. The reported 1% VCO frequency resolution is much worse than the proposed approach. Compared with the integer counter-based AFC method, the proposed AFC also provides much finer VCO frequency detection resolution due to the fractional period estimation with the TDC. As for the calibration time, the calibration for one bit in the proposed design only takes $2^3 \times T_{ref}$ counting time due to the improved frequency detector resolution. This leads to an error-free calibration time of 2.3 μs. It is comparable to the integer-counter-based and the TVC-based AFCs even though a resolution of an order higher has been reached. If keeping the same frequency detection

resolution, *e.g.* as that of [17], then the proposed AFC only takes 0.46 µs calibration time which is much faster than other AFC solutions.

Table 5.1: Comparison of AFC schemes

	This work (Simulation)	[15] (Measurement)	[16] (Measurement)	[17] (Measurement)
AFC Architecture	TDC-based	TVC-based	Counter-based	Counter-based
Calibration Algorithm	Binary search	Linear search	Binary search	Binary search
Frequency Resolution	$0.308f_{ref}/2^{M-1}$ *(M=4)*	$0.01f_{vco}$	$f_{ref}/2^{M-1}$ *(M=5)*	$f_{ref}/2^{M-1}$ *(M=3)*
Frequency Resolution (normalized to f_{vco})	0.04%	1%	0.16%	0.2%
N.α Truncation Error	0	f_{ref}	$f_{ref}/2^4$	0
Calibration Time	2.3 µs	4 µs	6.4 µs	2.03 µs
PLL Reference Frequency	40 MHz	40 MHz	25 MHz	19.2 MHz
VCO Frequency (GHz)	3.5 ~5	8.6 ~10.1	0.97 ~1.96	2.34 ~3.94
Process	0.13-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.13-µm CMOS

5.6 Summary

A TDC counter-based AFC is presented. The TDC counter captures the fractional VCO cycle information within the counting window, which significantly improves the frequency detection accuracy. In addition, the error mechanisms of the counter-based AFC are analyzed and a quantitative model determining the minimally required error-free AFC calibration time for a given VCO tuning curve characteristic is theoretically developed. An AFC circuit using the proposed TDC-based counter is designed in a 0.13-µm CMOS technology. Simulation results show that the TDC-based AFC method is more robust than

the integer counter-based and the TVC-based AFC methods. It greatly improves the frequency detection accuracy and consequently for a given frequency detection resolution reduces the AFC calibration time.

CHAPTER 6. CONCLUSION

6.1 Summary

This research work studies the timing circuits--the CDR for wireline communications and the frequency synthesizer for wireless communications. Both of them are targeted to support multi-standards and therefore need to balance the circuit performance and application generosity. The CDR designed in deep-submicron CMOS technology needs to overcome the limitations of PVT variation and leakage current problem. The frequency synthesizer should meet the stringent phase noise requirement of the cellular standards and cover the wide output range at the same time.

The digital-intensive CDR solution is proposed to overcome the design challenge in deep-submicron CMOS process. To increase the system flexibility and provide multi-mode support, it is designed to support continuous data rate ranging from 1 Gbps~16 Gbps. Thanks to the programmability of digital circuitries, the multi-sampling-rate technique can be conveniently adopted to extend the supported data rate. The design of 8~16 GHz LC-DCO in the CDR is discussed in detail. To increase the DCO tuning range without area penalty, the switched-coupled-inductor is used. The CDR also contains a digital FLL which combines the stochastic-counter-based data rate detection and the AFC techniques. Compared to the stochastic-counter-based approach, the proposed FLL is able to support multiple phase detection modes and accommodate the unbalanced data pattern such as k28.7. To address the difficulty of jitter and stability evaluations for bang-band CDR, a Simulink model is developed to find out the JTRAN, JGEN and JTOL performances for the CDR. The proposed design techniques is validated by the post-layout simulation results.

Specially, the proposed CDR operating at 16 Gbps is able to tolerate a sinusoidal jitter with an amplitude of 0.4 UI and a frequency of 4 MHz. The JGEN at 10 Gbps is 7 mUI RMS.

The proposed frequency synthesizer supports the standards of DCS1800, WCDMA, TD-SCDMA, WLAN 802.11 a/b/g and Bluetooth. Architecture design and frequency planning are carefully performed to ensure that the synthesizer meets the specifications of the above standards. Optimally-coupled wideband QVCO, divider and HR-SSBmixer are combined to synthesize the desired frequency range without posing much phase noise penalty on the QVCO. The QVCO adopts a new phase-shift scheme to improve phase noise and to eliminate bimodal oscillation. Combining harmonic rejection and single sideband mixing, the HR-SSBmixer is developed to suppress spurious signals. Designed in a 0.13-μm CMOS technology, the synthesizer occupies an active area of 1.86 mm^2 and consumes 35.6 to 52.62 mW of power. Measurement results show that the synthesizer frequency range, the phase noise, the settling time and the spur performances meet the specifications of the wireless receivers for the above standards.

A TDC counter-based AFC is proposed for the wide range multi-standard frequency synthesizer. The design guideline and limitations of the integer-counter-based AFC are discussed. The TDC is proposed to use in the AFC to improve its frequency detection accuracy. The TDC counter captures the fractional VCO cycle information within the counting window. An AFC circuit using the proposed TDC-based counter is designed in a 0.13-μm CMOS technology. Simulation results show that the TDC-based AFC method is more robust than the integer counter-based and the TVC-based AFC methods. It greatly improves the frequency detection accuracy and consequently for a given frequency detection resolution reduces the AFC calibration time.

6.2 Future Work

With the increasing development of deep-submicron CMOS technology and ever-growing demand on the data transfer rate of the wireline and wireless devices, further development on the dissertation topics can be explored as follows:

1) The trend in wireline communication circuit is low power and high data-rate in low cost CMOS technology. For example, the SONET OC-768 is a network line with transmission speeds up to 40 Gb/s. The Fibre Channel 32GFC operates at 32 Gb/s. As the data-rate increases, the speed requirement for the CDR becomes tougher. Therefore, it is necessary to investigate digital intensive CDR solution for speed higher than 16 Gb/s. For higher data-rate input, the timing margin for circuit operation is smaller. The CDR is more sensitive the noise and environment changes. Therefore, besides the speed, the improvement of circuit resistance to temperature drift, supply and substrate noise should also be taken into account.

2) The integration of multiple standards into a single chip-set is an important trend in wireless communication systems. The performance of analog intensive design of fractional-N frequency synthesizers for such systems are more and more limited by the downsides of the deep-submicron CMOS process. Therefore, it is necessary to study the digital PLL application in the frequency synthesizer for wireless communications. The issues of digital-PLL-based frequency synthesizer is the quantization noise and spurious tones due to the quantization and non-linearity of the loop. As the phase noise and spur requirements for the frequency synthesizer in wireless communications are stringent, these issues should be given priority attention in the further study.

REFERENCES

[1] R. Staszewski, J. Wallberg, S. Rezeq, C. Hung, S. Eliezer, S. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M. Lee, P. Cruise, M. Entezari, K. Muhammad and D. Leipold, "All-digital pll and transmitter for mobile phones," *IEEE J. of Solid-State Circuits,* vol. 40, no. 12, pp. 2469-2482, Dec. 2005.

[2] E. Temporiti, C. Weltin-Wu, D. Baldi, R. Tonietto and F. Svelto, "A 3 GHz Fractional all-digital PLL with a 1.8 MHz bandwidth implementing spur reduction techniques," *IEEE J. Solid-State Circuits,* vol. 44, no. 3, pp. 824-834, March 2009.

[3] C. Hsu, M. Straayer and M. Perrott, "A low-noise wide-BW 3.6-GHz digital delta-sigma fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," *IEEE J. Solid-State Circuits,* vol. 43, no. 12, pp. 2776-2786, Dec. 2008.

[4] M. Brandolini, P. Rossi, D. Manstretta and F. Svelto, "Toward multistandard mobileterminals—fully integrated receivers requirements and architectures," *IEEE Trans. on Microwave Theory and Techniques,* vol. 53, no. 3, pp. 1026-1038, Mar. 2005.

[5] M. He and J. Poulton, "A CMOS mixed-signal clock and data recovery circuit for OIF CEI-6G+ backplane transceiver," *IEEE J. Solid-State Circuits,* vol. 41, no. 3, pp. 597-606, March 2006.

[6] L. Rodoni, G. Buren, A. Huber, M. Schmatz and H. Jackel, "A 5.75 to 44 Gb/s quarter rate CDR with data rate selection in 90 nm bulk CMOS," *IEEE J. Solid-State Circuits,* vol. 44, no. 7, pp. 1927-1941, July 2009.

[7] R. Walker, C. Stout and C. Yen, "A 2.488 Gb/s Si-bipolar clock and data recovery IC with robust loss of signal detection," in *IEEE Int. Solid State Circuit Conf. Digest of Technical Papers*, Feb. 1997.

[8] J. Cao, M. Green, A. Momtaz, K. Vakilian, D. Chung, K. Jen, M. Caresosa, X. Wang, T. Wee, Y. Cai, I. Fujimori and A. Hairapetian, "OC-192 transmitter and receiver in standard 0.18-µm CMOS," *IEEE J. Solid-State Circuits,* vol. 37, no. 12, pp. 1768-1780, Dec. 2002.

[9] H. Song, D. Kim, D. Oh, S. Kim and D. Jeong, "A 1.0–4.0-Gb/s All-Digital CDR with 1.0-ps period resolution DCO and adaptive proportional gain control," *IEEE J. Solid-State Circuits,* vol. 46, no. 2, pp. 424-434, Feb. 2011.

[10] T. Lee and J. Bulzacchelli, "A 155-MHz clock recovery delay- and phase-locked loop," *IEEE J. Solid-State Circuits,* vol. 27, no. 12, pp. 1736-1746, Dec. 1992.

[11] D. Dalton, K. Chai, E. Evans, M. Ferriss, D. Hitchcox, P. Murray, S. Selvanayagam, P. Shepherd and L. DeVito, "A 12.5-mb/s to 2.7-Gb/s continuous-rate CDR with automatic frequency acquisition and data-rate readback," *IEEE J. Solid-State Circuits,* vol. 40, no. 12, pp. 2713-2725, Dec. 2005.

[12] B. Razavi, RF Microelectronics, NJ: Prentice Hall, 1997.

[13] T. Lin and W. Kaiser, "A 900-MHz 2.5-mA CMOS frequency synthesizer with an automatic SC tuning loop," *IEEE J. Solid-State Circuits,* vol. 36, no. 3, pp. 424-431, March 2001.

[14] H. Lee, J. Cho, K. Lee, I. Hwang, T. Ahn, K. Nah and B. Park, "A Σ-Δ fractional-N frequency synthesizer using a wide-band integrated VCO and a fast AFC technique for GSM/GPRS/WCDMA applications," *IEEE J. Solid-State Circuits,* vol. 39, no. 7, pp. 1164-1169, July 2004.

[15] T. Lin and Y. Lai, "An agile VCO frequency calibration technique for a 10-GHz CMOS PLL," *IEEE J. Solid-State Circuits,* vol. 42, no. 2, pp. 340-349, Feb. 2007.

[16] L. Lu, Z. Gong, Y. Liao, H. Min and Z. Tang, "A 975-to-1960 MHz fast-locking fractional-N synthesizer with adaptive bandwidth control and 4/4.5 prescaler for digital TV tuners," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, Feb. 2009.

[17] J. Shin and H. Shin, "A fast and high-precision VCO frequency calibration technique for wideband fractional-N frequency synthesizers," *IEEE Trans. Circuits and Systems I: Reg. Papers,* vol. 57, no. 7, pp. 1573-1582, July 2010.

[18] D. Huang, W. Li, J. Zhou, N. Li, J. Ren and J. Chen, "A time-to-digital converter based AFC for wideband frequency synthesizer," in *Proc. IEEE ISCAS*, May 2012.

[19] Fibre Channel Industry Association, "Fibre Channel Solution Guide - 2012," 2012.

[20] C. Hsieh and S. Liu, "A 1–16-Gb/s wide-range clock/data recovery circuit with a bidirectional frequency detector," *IEEE Tran. on Circuits and Systems II: Express Briefs,* vol. 58, no. 8, pp. 487-491, Aug. 2011.

[21] S. Lee, Y. Kim, H. Ha, Y. Seo, H. Park and J. Sim, "A 650Mb/s-to-8Gb/s referenceless CDR circuit with automatic acquisition of data rate," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, Feb. 2009.

[22] B. Staszewski, C.-M. Hung, N. Barton, M.-C. Lee and D. Leipold, "A digitally controlled oscillator in a 90 nm digital CMOS process for mobile phones," *IEEE J. Solid-State Circuits,* vol. 40, no. 11, pp. 2203-2211, Nov. 2005.

[23] J. Alexander, "Clock recovery from random binary data," *Electron. Lett.,* vol. 11, no. 10, pp. 541-542, Oct. 1975.

[24] R. Walker, "Designing BangBang PLLs for clock and data recovery in serial data transmission systems," in *Phase-Locking in High-Performance Systems: From Devices to Architectures* , Wiley-IEEE Press, 2003, pp. 34-45.

[25] Telecordia Technologies, "Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria," no. 3, Sept. 2000.

[26] J. Lee, K. Kundert and B. Razavi, "Analysis and modeling of bang-bang clock and data recovery circuits," *IEEE J. Solid-State Circuits,* vol. 39, no. 9, pp. 1571-1580, Sept. 2004.

[27] A. Goel, A. Rylyakov, H. Ainspan and D. Friedman, "A compact 6 GHz to 12 GHz digital PLL with coupled dual-LC tank DCO," in *IEEE Symposium on VLSI Circuits*, June 2010.

[28] W. Titus and J. Kenney, "A 5.6 GHz to 11.5 GHz DCO for Digital Dual Loop CDRs," *IEEE J. Solid-State Circuits,* vol. 47, no. 5, pp. 1123-1130, May 2012.

[29] Z. Safarian and H. Hashemi, "Wideband Multi-Mode CMOS VCO Design Using Coupled Inductors," *IEEE Trans. on Circuits and Systems I: Regular Papers,* vol. 56, no. 8, pp. 1830-1843, Aug. 2009.

[30] Y. Seong-Mo and K. O, "Switched resonators and their applications in a dual-band monolithic CMOS LC-tuned VCO," *IEEE Trans. Microw. Theory Tech.,* vol. 54, no. 1, pp. 74-81, Jan. 2006.

[31] M. Demirkan, S. Bruss and R. Spencer, "Design of Wide Tuning-Range CMOS VCOs Using Switched Coupled-Inductors," *IEEE J. Solid-State Circuits,* vol. 43, no. 5, pp. 1156-1163, May 2008.

[32] R. Staszewski, C.-M. Hung, D. Leipold and P. Balsara, "A first multigigahertz digitally controlled oscillator for wireless applications," *IEEE Tran. on Microwave Theory and Techniques,* vol. 51, no. 11, pp. 2154-2164, Nov. 2003.

[33] A. Pottbacker, U. Langmann and H. Schreiber, "A Si bipolar phase and frequency detector IC for clock extraction up to 8 Gb/s," *IEEE J. Solid-State Circuits,* vol. 27, no. 12, pp. 1747-1751, Dec. 1992.

[34] G. Shu, W.-S. Choi, S. Saxena, T. Anand, A. Elshazly and P. Hanumolu, "A 4-to-10.5Gb/s 2.2mW/Gb/s continuous-rate digital CDR with automatic frequency acquisition in 65nm CMOS," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, Feb. 2014.

[35] R. Inti, W. Yin, A. Elshazly, N. Sasidhar and P. Hanumolu, "A 0.5-to-2.5 Gb/s reference-Less half-rate digital CDR with unlimited frequency acquisition range and improved input duty-cycle error tolerance," *IEEE J. Solid-State Circuits,* vol. 46, no. 12, pp. 3150-3162, Dec. 2011.

[36] L. DeVito, "A versatile clock recovery architecture and monolithic implementation," in *Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design*, Wiley-IEEE Press, 1996, pp. 405-420.

[37] D. Huang, W. Li, J. Zhou, N. Li, J. Ren and J. Chen, "A time-to-digital converter based AFC for wideband frequency synthesizer," *Springer Analog Integrated Circuits and Signal Processing,* vol. 79, no. 2, pp. 207-217, May 2014.

[38] U. Singh and M. Green, "Dynamics of high-frequency CMOS dividers," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2002.

[39] S. Fang, S. Lee and A. Bellaouar, "Differential CMOS latch and digital quadrature LO generator using same". US Patent US20040036541 A1, 26 August 2002.

[40] L. Romano, A. Bonfanti, S. Levantino, C. Samori and A. Lacaita, "5-GHz Oscillator Array With Reduced Flicker Up-Conversion in 0.13 um CMOS," *IEEE J. Solid-State Circuits,* vol. 41, no. 11, pp. 2457-2467, Nov. 2006.

[41] N. Da Dalt, "Linearized analysis of a digital bang-bang PLL and its validity limits applied to jitter transfer and jitter generation," *IEEE Trans. on Circuits and Systems I: Regular Papers,* vol. 55, no. 11, pp. 3663-3675, Dec. 2008.

[42] H.-I. Cong, S. Logan, M. Loinaz, K. O'Brien, E. Perry, G. Polhemus, J. Scoggins, K. Snowdon and M. Ward, "A 10-Gb/s 16:1 multiplexer and 10-GHz clock synthesizer in 0.25-µm SiGe BiCMOS," *IEEE J. Solid-State Circuits,* vol. 36, no. 12, pp. 1946-1953, Dec. 2001.

[43] S. Ahmed, K. Orthner and T. Kwasniewski, "Behavioral test benches for digital clock and data recovery circuits using Verilog-A," in *IEEE Custom Integrated Circuits Conference*, Sept. 2005.

[44] A. Koukab, Y. Lei and M. Declercq, "A GSM-GPRS/UMTS FDD-TDD/WLAN 802.11a-b-g multi-standard carrier generation system," *IEEE J. Solid-State Circuits,* vol. 41, no. 7, pp. 1513-1521, July 2006.

[45] P. Nuzzo, K. Vengattaramane, M. Ingels, V. Giannini, M. Steyaert and J. Craninckx, "A 0.1-5 GHz dual-VCO software-defined ΣΔ frequency synthesizer in 45nm digital CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium*, June 2009.

[46] J. Borremans, K. Vengattaramane, V. Giannini, B. Debaillie and J. Craninckx, "A 86 MHz–12 GHz digital-intensive PLL for software-defined radios, using a 6 fJ/Step TDC in 40 nm digital CMOS," *IEEE J. Solid-State Circuits,* vol. 45, no. 10, pp. 2116-2129, Oct. 2010.

[47] S. Osmany, F. Herzel and J. Scheytt, "An integrated 0.6–4.6 GHz, 5–7 GHz, 10–14 GHz, and 20–28 GHz frequency synthesizer for software-defined radio applications," *IEEE J. Solid-State Circuits,* vol. 45, no. 9, pp. 1657-1668, Sept. 2010.

[48] M. Ingels, C. Soens, J. Craninckx, V. Giannini, T. Kim, B. Debaillie, M. Libois, M. Goffioul and J. Van Driessche, "A CMOS 100 MHz to 6 GHz software defined radio analog front-end with integrated pre-power amplifier," in *IEEE European Solid State Circuits Conference*, Sept. 2007.

[49] D. Huang, W. Li, J. Zhou, N. Li and J. Chen, "A frequency synthesizer with optimally coupled QVCO and harmonic-rejection SSBmixer for multi-standard wireless receiver," *IEEE J. Solid-State Circuits,* vol. 46, no. 6, pp. 1307-1320, June 2011.

[50] J. van der Tang, P. van de Ven, D. Kasperkovitz and A. van Roermund, "Analysis and design of an optimally coupled 5-GHz quadrature LC oscillator," *IEEE J. Solid-State Circuits,* vol. 27, no. 5, pp. 657-661, May 2002.

[51] S. Li, I. Kipnis and M. Ismail, "A 10-GHz CMOS quadrature LC-VCO for multirate optical applications," *IEEE J. Solid-State Circuits,* vol. 38, no. 10, pp. 1626-1634, Oct. 2003.

[52] G. Li and E. Afshari, "A low-phase-noise multi-phase oscillator based on left-handed LC-ring," *IEEE J. Solid-State Circuits,* vol. 45, no. 9, pp. 1822-1833, Sept. 2010.

[53] A. Lacaita, S. Levantino and C. Samori, Integrated frequency synthesizers for wireless systems, UK: Cambridge University Press, 2007.

[54] J. Weldon, R. Narayanaswami, J. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee and P. Gray, "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE J. Solid-State Circuits,* vol. 36, no. 12, pp. 2003-2015, Dec. 2001.

[55] I. Chamas and S. Raman, "A comprehensive analysis of quadrature signal synthesis in cross-coupled RF VCOs," *IEEE Trans. on Circuits and Systems I: Regular Papers,* vol. 54, no. 4, pp. 689-704, April 2007.

[56] A. Mirzaei, M. Heidari, R. Bagheri, S. Chehrazi and A. A. Abidi, "The quadrature LC oscillator: a complete portrait based on injection locking," *IEEE J. Solid-State Circuits,* vol. 42, no. 9, pp. 1916-1932, Sept. 2007.

[57] A. Rofougaran, G. Chang, J. J. Rael, J. Y. Chang, M. Rofougaran and P. J. Chang, "A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS-part I: architecture and transmitter design," *IEEE J. Solid-State Circuits,* vol. 33, no. 4, pp. 515-533, April 1998.

[58] B. Razavi, Design of integrated circuits for optical communications, New York: McGraw-Hill, 2003.

[59] H. Chang, X. Cao, U. K. Mishra and R. A. York, "Phase noise in coupled oscillators: theory and experiment," *IEEE Trans. Microw. Theory Tech.,* vol. 45, no. 5, pp. 604-615, May 1997.

[60] S. Lerstaveesin, M. Gupta, D. Kang and B. S. Song, "A 48–860 MHz CMOS low-IF direct-conversion DTV tuner," *IEEE J. Solid-State Circuits,* vol. 43, no. 9, pp. 2013-2024, Sept. 2008.

[61] C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-µm CMOS technology," *IEEE J. of Solid-State Circuits,* vol. 35, no. 7, pp. 1039-1045, July 2000.

[62] C. Hsu, *Techniques for high performance digital frequency synthesis and phase control,* Cambridge, MA: Ph. D. dissertation, Dept. Elect. Eng. Comput. Sci., Mass. Inst. Technol., 2008.

[63] H. Cha, S. Sone, H. Kim and K. Lee, "A CMOS harmonic rejection mixer with mismatch calibration circuitry for digital TV tuner applications," *IEEE Microwave and Wireless Components Letters,* vol. 18, no. 9, pp. 617-619, Sept. 2008.

[64] J. Craninckx, M. Liu, D. Hauspie, V. Giannini, T. Kim, J. Lee, M. Libois, B. Debaillie, C. Soens, M. Ingels, A. Baschirotto, J. Van Driessche, L. Van der Perre and P. Vanbekbergen, "A fully reconfigurable software-defined radio transceiver in 0.13 um CMOS," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, Feb. 2007.

[65] R. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg and P. Balsara, "1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," *IEEE Trans. Circuits and Systems II: Express Briefs,* vol. 53, no. 3, pp. 220-224, March 2006.

[66] M. Zanuso, S. Levantino, D. Tasca, D. Raiteri, C. Samori and A. Lacaita, "A glitch-corrector circuit for low-spur ADPLLs," in *IEEE Electronics, Circuits, and Systems*, Dec. 2009.

[67] D. Hauspie, E. Park and J. Craninckx, "Wideband VCO with simultaneous switching of frequency band, active core, and varactor size," *IEEE J. Solid-State Circuits,* vol. 42, no. 7, pp. 1472-1480, July 2007.