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Progress on the Numerical Calculation of Electrical Characteristics of Strained SiGe Channel p-MOSFET

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Abstract. Recent progress in the computer simulation of strained SiGe channel p-MOSFET performance is reviewed. The electrical characteristics of strained SiGe channel p-MOSFET, such as threshold voltage, subthreshold characteristics, output characteristics, transconductance, quasistatic *C-V* characteristics and transfer characteristics, and the effects of Ge mole fraction on electrical characteristics, are well discussed. Finally, the development of strained SiGe channel p-MOSFET is prospected.

Introduction

As known in traditional bulk CMOS technologies, the electron mobility is 2-3 times higher than hole mobility. Therefore, in order to realize the matching of driving current and gain characteristics to n-MOSFET in the Schematic-Driven Layout, a greater channel width/length ratio is needed for p-MOSFET, but the integration level and speed of chips will be reduced. At the earliest, Nayak *et al*. proved that the hole mobility of strained $Si_{1-x}Ge_x$ channel p-MOSFET was higher than that of bulk Si p-MOSFET [1]. Recently, Gomez *et al*. reported that higher hole mobility and speed of strained $Si_{0.45}Ge_{0.55}$ channel p-MOSFET on Si-on-insulator (SOI) substrate would be acquired [2]. Therefore, using the $Si_{1-x}Ge_x$ materials as the conductive channel can greatly improve the performance and integration level of CMOS circuits.

Currently, the strained SiGe (sSiGe) channel p-MOSFETs reported in literature can be classified into six groups based on their structures which are shown as Fig. 1, such as Si/sSiGe/Si buried-channel p-MOSFET with poly Si gate, Si/sSiGe/Si buried-channel p-MOSFET with poly $Si_{1-y}Ge_y$ gate, sSiGe channel p-MOSFET without Si cap layer, sSiGe channel p-MOSFET on SOI substrate, sSi/s$Si_{1-x}Ge_x$ grown on a relaxed $Si_{1-y}Ge_y$ layer dual-channel p-MOSFET, and sSiGe channel-on-insulator p-MOSFET. Palmer *et al*. firstly introduced the $Si_{0.64}Ge_{0.36}$ channel p-MOSFET with Si cap layer, the hole mobility had been increased effectively by adjusting the thickness of Si cap layer [3]. Yeo *et al*. designed and manufactured the $Si_{0.7}Ge_{0.3}$ channel p-MOSFET on SOI substrate, the driving current had been improved greatly [4]. Lee *et al*. used high-*k* gate dielectric ($HfSiO_x$) and metal gate (TaN) instead of traditional SiO_2 gate dielectric and poly Si gate, the short-channel effect of $Si/Si_{0.25}Ge_{0.75}/Si$ buried-channel p-MOSFET with gate length of 60 nm was investigated via numerical simulation [5]. The strained $Si_{1-x}Ge_x$ channel p-MOSFETs attract more and more attention because of the production of SiGe layer is compatible with the traditional Si process [6-12]. The structural parameters, physical models, and doping concentration can be modified in the numerical simulation of the device, which can provide a reliable reference for the actual device fabrication. In this paper, recent progress in the numerical calculation of electrical characteristics of sSiGe channel p-MOSFET is introduced, so as review the effects of Ge mole fraction on electrical characteristics. We would like to focus on the threshold voltage and subthreshold characteristics of sSiGe channel p-MOSFET. Finally, the theoretical model for development of sSiGe channel p-MOSFET is prospected.

Electrical characteristics

Threshold voltage. As an important electrical parameter of the MOSFET, threshold voltage is closely related to the carrier concentration in channel, determines the turn-on and turn-off voltages. It is necessary to develop threshold voltage model for simulating the electrical characteristics of the device correctly. Recently, 1-D threshold voltage models [13-18] and 2-D threshold voltage models [19,20] of sSiGe channel p-MOSFET were developed by solving the Poisson's equation.

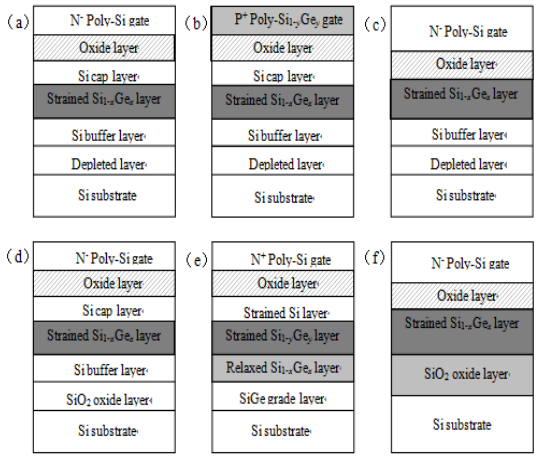

Fig. 1 Six basic structure of sSiGe channel p-MOSFET

Lukic *et al*. developed an analytical model on the threshold voltage of strained Si/SiGe MOSFET shown as Fig. 1(a) by solving the 1-D Poisson's equation [13]. The relations between threshold voltage and the thicknesses of the Si cap layer and the gate oxide layer were simulated and analysed, the simulated results were in good agreement with the developed model. Zou *et al*. took account of the short-channel effect and developed the 1-D threshold voltage models of sSiGe channel p-MOSFETs shown as Fig. 1(a) and Fig. 1(c), respectively [14,15]. When the device with different Ge mole fraction, thickness of Si cap layer and gate oxide layer, substrate doping level, and gate oxide dielectric, the relations between threshold voltage and channel length were simulated and analysed. As the channel length was less than 200 nm, the effects of short-channel effect and drain-induced barrier lowing on threshold voltage were large. However, when the channel length was higher than 500 nm, the effects could be ignored.

Tsang *et al*. developed the threshold voltage model of strained Si/$Si_{1-x}Ge_x$/$Si_{1-y}Ge_y$ ($x \geq y$) CMOS structure shown as Fig. 1(e) [16]. According to the model, the relations between threshold voltage and Ge mole fraction of strained $Si_{1-x}Ge_x$ layer, channel length, and substrate doping level were analysed, the results were in good agreement with the simulated results and the experimental data. Zhang *et al*. developed 1-D threshold voltage model of sSiGe channel p-MOSFET shown as Fig. 1(d) by using depletion layer approximation to solve Poisson's equation [17]. Liu *et al*. developed 2-D threshold voltage model of sSiGe channel p-MOSFET shown as Fig. 1(f) [19]. According to the model, the relations between threshold voltage and Ge mole fraction, the thickness of sSiGe layer, channel doping level, and channel length were simulated and analysed.

Xu *et al*. developed a quasi-2-D threshold voltage model of sSiGe channel p-MOSFET with the channel length of less than 100 nm, which was shown as Fig. 1(a) [20]. The quasi-2-D Poisson's equation was built by considering the lateral and vertical electric field in channel. Then the threshold voltage of SiGe buried-channel (V_{TH}) and surface-channel (V_{TS}) were acquired, respectively. As shown in Fig. 2, because of the decrease of the capability of gate control over the channel, the $|V_{TH}|$ and $|V_{TS}|$ increased with the increase of the thickness of gate oxide layer, and the $|V_{TH}|$ increased with the increase of the thickness of Si cap layer. However, the $|V_{TS}|$ decreased with the increase of the thickness of Si cap layer, it indicated that the threshold characteristics of surface-channel were gradual close to that of the traditional Si MOSFET. Consistent with the theory of classical MOSFET, the $|V_{TH}|$ and $|V_{TS}|$ increased with the increase of substrate doping level. The $|V_{TH}|$ was in good agreement with the numerical simulated result as

different channel length, while the $|V_{TS}|$ was not in agreement with the numerical simulated result as the channel length of less than 200 nm. In addition, the threshold voltage changed with the variation of channel length of sSiGe channel p-MOSFET with Si cap layer, which was compared to that of sSiGe channel p-MOSFET without Si cap layer. Generally, the high-k gate dielectric was used for the device without Si cap layer, such as ZrO_2 and HfO_2. The threshold voltage and its roll-off value of the device without Si cap layer were smaller than that of the device with Si cap layer. It indicated that better threshold characteristics of the device without Si cap layer could be obtained.

Qu *et al*. developed 1-D threshold voltage model for strained $Si_{1-x}Ge_x$ channel p-MOSFET shown as Fig. 1(b) by solving Poisson's equation [18]. Compared to the device with poly-Si gate, the device with poly-$Si_{1-y}Ge_y$ could restrain the gate depletion effect and improve the reliability of the gate oxide. With the change of Ge mole fraction of poly-$Si_{1-y}Ge_y$ gate, a wide range of variation could be obtained for the gate work function. It was conductive to regulating the threshold voltage of the device [27,28]. From the numerical simulated results, it is observed that both the threshold voltage of quantum well channel (V_{TB}) and the turn-on voltage of parasitic surface channel (V_{TS}) increased with the increase of substrate doping level, channel doping level, and thickness of gate oxide layer. The V_{TB} increased with the increase of thickness of Si cap layer, while the V_{TS} decreased with the increase of thickness of Si cap layer. Therefore, in the design of the device, the thickness of Si cap layer should be controlled under a certain range for avoiding the effect of the turn-on of parasitic surface channel on the device performance.

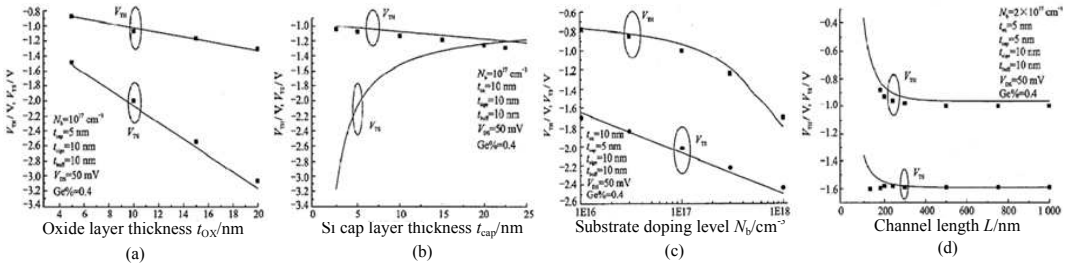

Fig. 2 Threshold voltage versus oxide layer thickness(a), Si cap layer thickness(b), substrate doping concentration(c) and channel length(d)

Subthreshold characteristics. Subthreshold characteristic is an important electrical characteristic of SiGe channel p-MOSFET to the static power consumption and the switching characteristics. In the view of physical mechanism, when the gate bias is between the flat-band voltage and the threshold voltage ($V_{FB}<V_G<V_T$), the semiconductor surface potential (φ_S) is between zero and $2\varphi_F$ ($0<\varphi_S<\varphi_F$). The semiconductor surface is under weak inversion, in which the carriers can also participate in the conductivity, but the current is very small. Subthreshold characteristics can generally be defined by the electrical characteristics of the device with the bias in $V_{FB}<V_G<V_T$ range [29]. Two important indicators of the evaluation of subthreshold characteristics are subthreshold current and subthreshold swing. The subthreshold current includes two parts of the hole diffusion current due to weak inversion in the channel and the drain current under reverse bias, mainly determines the static power consumption in circuits. The subthreshold swing can be expressed as [30]

$$S = \frac{\mathrm{d}V_{GB}}{\mathrm{d}\log I_{DS}} = 2.3V_t(1+\frac{C_d}{C_{ox}}) \tag{1}$$

Where, V_t is the thermoelectric voltage (kT/q), C_d is the depletion-layer capacitance, and C_{OX} is the gate oxide capacitance.

Shi *et al*. reported the subthreshold characteristics of sSiGe channel p-MOSFET shown as Fig. 1(a), the subthreshold swing increased with the increase of Ge mole fraction [31]. Subsequently, they also reported sSiGe channel p-MOSFET shown as Fig. 1(c), used the high-*k* dielectric (HfO_2) instead of SiO_2 for gate oxide layer [32]. Compared to Si channel p-MOSFET, the subthreshold swing of sSiGe channel p-MOSFET was larger.

Kuo *et al*. reported the subthreshold characteristics at 77 K of sSiGe channel p-MOSFET shown as Fig. 1(a), which did show any delayed-turn-off phenomenon [33]. Sophie *et al*. studied the sSiGe channel p-MOSFET shown as Fig. 1(a), simulated the subthreshold characteristics of the device with p-type and n-type gate, respectively [34]. The better subthreshold characteristics of the device with n-type gate could be obtained due to the smaller subthreshold swing. Chleirigh *et al*. reported the sSi/sSiGe dual-channel p-MOSFET with high mobility shown as Fig. 1(e), analysed that small subthreshold swing could be obtained when the thickness of Si cap layer was very thin [35].

Tu *et al*. reported sSiGe p-MOSFET with deep submicron channel shown as Fig. 1(a), used unintentional doping and p-delta-doping to improve the mobility [36]. Compared to Si channel p-MOSFET, the simulated results indicated that the subthreshold current of sSiGe channel p-MOSFET was 1-2 orders of magnitude higher and the subthreshold swing of sSiGe channel p-MOSFET increased slightly. The effects of the thickness of Si cap layer, Ge mole fraction, thickness of sSiGe layer, and p-delta-doping level on subthreshold swing were simulated and analysed. The results indicated that except for Ge mole fraction, the subthreshold swing increased with increase of any parameter of the thickness of Si cap layer, thickness of sSiGe layer, and p-delta-doping level. It should compromise in considering the subthreshold swing of device became worse by adjusting the structure parameters to improve driving current and transconductance of the device.

Output characteristics and other electrical characteristics. Except for threshold voltage and subthreshold characteristics, there are some other electrical characteristics of sSiGe channel p-MOSFET, such as *C-V* characteristics, transfer characteristics, output characteristics, transconductance and breakdown characteristics, etc. The *C-V* characteristics reflect the gate capacitance under different gate bias. The transfer characteristics which reflects cut-off current and subthreshold swing of the device, characterizes the capability of gate control over the channel. The output characteristics which reflects the drain-source saturation current, characterizes the capability of the drain-source voltage control over the channel current. The transconductance reflects the capability of the gate-source voltage control over the drain current.

Philippe *et al*. used Monte Carlo method to simulate the electrical characteristics of sSiGe channel p-MOSFET shown as Fig. 1(a). The results indicated that the channel effective carrier mobility increased 2.6 times because of the holes were constrained in SiGe potential well, then the driving current, transconductance, and cut-off frequency increased at least 55 percent [37]. Irisawa *et al*. studied the electrical characteristics of sSiGe channel p-MOSFET shown as Fig. 1(f). The drain-source saturation current of the device was higher than that of the SOI structure, and the *C-V* characteristics shown a hump-shaped due to the response of the interface states [38].

Yang *et al*. simulated and analysed the transfer characteristics, output characteristics, transconductance and cut-off frequency of the device, which was shown as Fig. 1(a) combined the p-type δ-doping [39]. From the transfer characteristics, it was observed that the drain-source current of sSiGe channel p-MOSFET was 2 times higher than that of Si p-MOSFET, and the cut-off current of sSiGe channel was 4 orders of magnitude higher than that of Si p-MOSFET (Fig. 3(a)). Compared to Si p-MOSFET, the drain-source currents of sSiGe p-MOSFET in the linear region and saturation region of output characteristics curve were higher, and the drain-source saturation current increased about 110 percent (Fig. 3(b)). It indicated that higher driving capability and operating speeds could be obtained. Compared to Si p-MOSFET, the transconductance of sSiGe p-MOSFET rose more quickly with the increase of negative gate bias, and declined more quickly after reaching the peak value (Fig. 3(c)). The cut-off frequency reflected the switching speed, and the changing trend was same to the transconductance (Fig. 3(d)). Subsequently, they simulated and analysed the breakdown characteristics of sSiGe channel p-MOSFET and conventional Si p-MOSFET [40]. The

breakdown voltage of sSiGe p-MOSFET was significantly lower than that of Si p-MOSFET because of the sSiGe layer with narrow bandgap determined the breakdown of the device. The effects of thickness of Si cap layer, thickness of sSiGe layer, and Ge mole fraction on breakdown of the device was remarkable. In addition, the sSiGe channel p-MOSFET with δ-doping showed punch-through breakdown mechanism.

Chen *et al*. studied sSiGe channel p-MOSFET shown as Fig. 1(b), compared the *C-V* characteristics between of poly-SiGe gate and poly-Si gate p-MOSFET [41]. The impurity activation rate of poly-SiGe gate p-MOSFET improved about 10 percent. In addition, from the output characteristics, it was observed that a higher driving current of poly-SiGe gate p-MOSFET could be obtained. Subsequently, Yu *et al*. also studied it, and used high-*k* dielectric (HfO_2) as the gate oxide layer [42]. Compared to poly-Si gate, the transconductance of poly-SiGe gate p-MOSFET improved greatly. It was mainly due to improving the surface resistance of poly-SiGe gate by increasing the impurity activation.

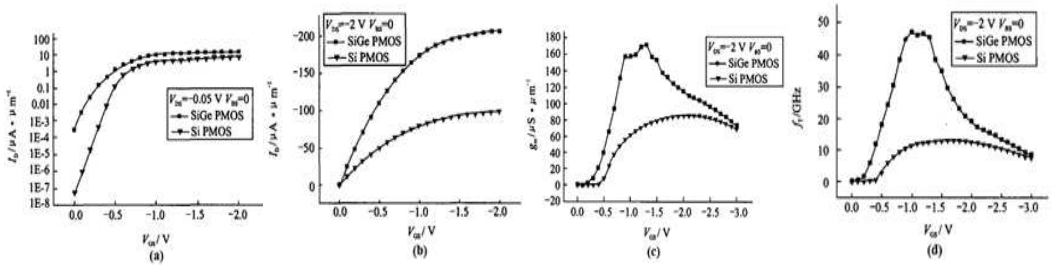

Fig. 3 Comparison of transfer characteristics(a), output characteristics(b), transconductance(c) and cutoff frequency(d) varying with gate bias

Gao *et al*. simulated sSiGe channel p-MOSFET shown as Fig. 1(d), by using 3-D device simulation software [43]. The sSiGe band model, mobility model and density of states model of the classical formulas were used in sSiGe layer [44,45]. Compared to the conventional SOI p-MOSFET, the driving current and transconductance of sSiGe channel SOI p-MOSFET were simulated and analysed. At the gate bias of -1.5 V, the driving current of SiGe SOI structure was about 39.3 percent higher than that of the conventional SOI structure. It suggested that the introduction of SiGe channel above the SOI structure could greatly improve the driving capability of p-tube. Actually the proportional relation between the deviation of transconductance and the gate bias was due to the hole mobility degradation of SiGe channel caused by the high negative gate bias. Therefore, it should avoid using SiGe SOI p-MOSFET at high gate bias for acquiring good gain characteristics in simulated circuits.

Effects of Ge Mole Fraction on Electrical Characteristics

As an important parameter of strained $Si_{1-x}Ge_x$ channel p-MOSFET, Ge mole fraction not only determines the valence band offset of $Si/Si_{1-x}Ge_x$ hetero-junction, but also affects the hole mobility in two-dimensional hole gas (2DHG) formed by the Si buffer layer/$Si_{1-x}Ge_x$ channel/Si cap layer structure, then affects the electrical characteristics of the device. As the threshold voltage and subthreshold characteristics were introduced in before, the effects of Ge mole fraction on threshold voltage and subthreshold swing were studied many [14-16,19,36].

Song *et al*. reported effects of Si cap layer thickness and Ge mole fraction on electrical characteristics of sSiGe channel p-MOSFET shown as Fig. 1(a) [46]. David *et al*. reported sSiGe channel p-MOSFET shown as Fig. 1(a), used metal gate (Ta_xC_y) and high-*k* dielectric ($Hf_xZr_{1-x}O_2$) [47]. From the relations between Ge mole fraction and *C-V* characteristics, it was observed that the gate capacitance shifted towards the positive direction with the increase of Ge mole fraction. In addition, as a negative bias was applied to the gate, the increasing range of gate capacitance decreased with the increase of Ge mole fraction.

Yang *et al*. simulated the *C-V* characteristics, transfer characteristics, threshold voltage, and total channel resistance of strained $Si_{1-x}Ge_x$ channel p-MOSFET with various Ge mole fractions [48]. As shown in Fig. 4, the subthreshold current of the device with high Ge mole fraction was 3-4 orders higher than that of bulk p-MOSFET. With the increase of Ge mole fraction, the change in subthreshold swing was unconspicuous. During the transition process from depletion to strong inversion, the increasing range of gate capacitance decreased with the increase of Ge mole fraction. While in the strong inversion region, the gate capacitance almost not changed with the increase of Ge mole fraction. In the Ge mole fraction range of 0-30 percent, the threshold voltage $|V_T|$ diminished with the increase of Ge mole fraction. Increasing the Ge mole fraction from 30 to 50 percent, threshold voltage was always positive (V_T>0), and increased monotonously. As the Ge mole fraction was constant, the total channel resistance of the device increased with the increase of channel length. While as the channel length was constant, the total channel resistance of the device decreased with the increase of Ge mole fraction.

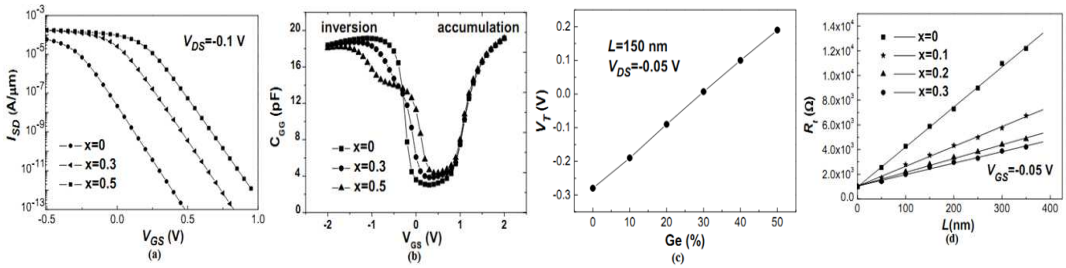

Fig. 4 Transfer characteristics(a), quasi *C-V* characteristics(b), threshold voltage(c) and total resistant as a function of channel length(d) of the device of different Ge mole fraction

Conclusion and Prospect

Recent progress in simulation of electrical characteristics of sSiGe channel p-MOSFET are reviewed, especially on developing threshold voltage model, subthreshold characteristics, output characteristics, and transfer characteristics, etc. In this paper, there are some improved areas of the threshold voltage model, such as the threshold voltage model of more accurate high-k gate dielectric sSiGe surface-channel p-MOSFET need to be further studied. For subthreshold characteristics, the subthreshold model and simulation of SiGe p-MOSFET based on more accurate material physical parameters also need to be further studied. In the device structure, the multi-gate sSiGe channel p-MOSFET can try to be used. It can effectively restrain the short-channel effect and drain-induced barrier lowing. In addition, on the basis of 2-D numerical calculations, the 3-D device structure can try to be used for numerical calculation of electrical characteristics. By this means, the calculated results are more accurate. It can contribute to further studies on electrical characteristics of the device, and also prompt the research work to be more meaningful.

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