Coherent Sinusoid Generation using Novel DDFS Architecture

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Abstract

A promising choice for signal generation in modern communications systems is direct digital frequency synthesis (DDFS) which is capable of well controlled, rapid changes in signal frequency, over a relatively large frequency range. Unfortunately, a conventional DDFS system requires a high frequency read only memory (ROM) which consumes most of the power. This paper describes a novel low complexity DDFS with smaller lookup table size and lesser hardware overhead. It is based on the Taylor series expansion method for sinusoidal and co-sinusoidal functions combined with an approximation algorithm. It has the advantages of high speed, low complexity, low computational delay and high spectral purity. The proposed DDFS has high SFDR (spurious free dynamic range) and the spectral purity can be as good as 135 dBc.

Keywords: *direct digital frequency synthesis; Taylor series; low-complexity; spectral purity; lesser hardware overhead.*

1. Introduction

In several applications of communication systems, it is important to produce and readily control accurate waveforms of various frequencies and profiles. Examples include agile frequency sources with low phase noise and low spurious signal content, having excellent frequency-tuning resolution and spectral performance for communications, and generated frequency stimuli for industrial, biomedical applications, modern digital and wireless communication systems, medical imaging, radar, sonar, modulators and sound synthesizers. In such applications, the ability to generate an adjustable waveform conveniently and cost effectively is a key design consideration.

The frequency synthesizer is one of the basic building blocks in modern communication systems. It is used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Various approaches have been used, but the most flexible one is direct digital frequency synthesis. A DDFS chip, or direct digital synthesizer, produces an analog waveform, usually a sine wave, but triangular and square waves are inherent, by generating a time-varying signal in digital form and then performing a digital-to-analog (D/A) conversion. DDFS devices primarily work in the digital domain, so they can offer fast switching between output frequencies, fine frequency resolution, fast settling time, low phase noise and spurious noise and operation over a broad spectrum of frequencies [3].

Traditional ROM based DDFS have several drawbacks including large chip area and high power consumption. Common methods to reduce the size of the ROM are quarter wave symmetry, magnitude-phase difference and trigonometric approximations which segment the

ROM into coarse and fine segments. These techniques introduce approximation and quantization errors in the output and hence their use is limited. Algorithmic methods such as CORDIC can be used as a replacement for the ROM by calculating the phase to amplitude conversion in digital circuitry. However the additional digital circuits increase the path delay and consume additional power [1].

To overcome the problems associated with look-up table based systems, approximation methods for sine and cosine functions were employed in the design of DDFS. However, computation of the expansion polynomial requires considerable multiplication count. To reduce the complexity, one often subdivides the expansion region into several subintervals. In turns, each subinterval carries out its own polynomial expansion, with less multiplication. However, the reduction of multiplication is at the cost of extra table to store the polynomial coefficients, as well as the function values of the expansion points.

The accuracy of the output signal depends on the degree of the reconstructing polynomial, the number of subsections, the word length of the truncated phase accumulator output, as well as the word length of the DDFS system output [2]. However this leads to an increase in the hardware overhead. The proposed algorithm is aimed at developing DDFS for low power and high speed operation using limited hardware. Thus, considering hardware optimization as well as good performance, sine and cosine functions are approximated using extended Taylor series approximation [8].

2. Proposed DDFS Algorithm

The proposed DDFS design provides two improvements over the traditional DDFS while maintaining the performance. First, minimizing the size of the ROM lookup table by using an approximation algorithm with a judicious choice of polynomial, and second, reducing the complexity of the system [10]. The primary objective for using such an approach is that precision can be achieved with relatively less hardware overhead when compared to other techniques of sine wave generation. The resulting low-power architecture meets the specifications of low power communication standards such as Bluetooth [11].The proposed DDFS design is based on the polynomial approximation method with a judicious choice of polynomial to minimize the hardware requirement.

2.1. Taylor Series Approximation

In the Taylor series expansion, the Sine and Cosine functions can be implemented at a point γ given by,

$$\sin(\theta) = \sin(\gamma) + (\theta - \gamma) * \cos(\gamma) + \ldots . \quad (1)$$

$$\cos(\theta) = \cos(\gamma) - (\theta - \gamma) * \sin(\gamma) + \ldots . \quad (2)$$

Earlier algorithms for synthesizing DDFS are based on Equations (1) and (2) which utilize the sample magnitude of $\sin(\theta)$ stored in a ROM and its slope [5].

Neglecting higher order terms in Equations (1) and (2),

$$\sin(\theta) \sim \sin(\gamma)+(\theta - \gamma)*\cos(\gamma) \quad (3)$$

$$\cos(\theta) \sim \cos(\gamma)-(\theta - \gamma)*\sin(\gamma) \quad (4)$$

where, γ is a constant. Another form of Taylor series expansion for sine and cosine function at a point γ is given by,

$$\sin(\gamma) = \gamma - (\gamma^3 / 3!) + (\gamma^5 / 5!) - (\gamma^7 / 7!) + \ldots . \quad (5)$$

$$\cos(\gamma) = 1 - (\gamma^2 / 2!) + (\gamma^4 / 4!) - (\gamma^6 / 6!) + \ldots . \quad (6)$$

For N-bits precision, the terms after $(1-(\gamma^2/2!))$ in $\cos(\gamma)$ expansion and γ in $\sin(\gamma)$ expansion can be ignored because the magnitude of the higher order terms are less than $2^{-(N+1)}$.

The Equations (5) and (6) are further simplified by neglecting higher order terms as given by

$$\sin(\gamma) \approx \gamma \quad (7)$$

$$\cos(\gamma) \approx 1 - (\gamma^2 / 2!) \quad (8)$$

By applying the Equations (7) and (8) in Equation (3)

$$\sin(\theta) \approx \gamma + (\theta - \gamma) *(1 - (\gamma^2 / 2!))$$

$$= \theta - ((\gamma^2 / 2) * \theta) + \gamma^3 / 2$$

Neglecting higher order terms further,

$$\sin(\theta) \approx (1 - (\gamma^2 / 2)) * \theta \quad (9)$$

The γ value for sine wave, denoted as γ_s, is obtained using Equation (9) as,

$$\gamma_s = \sqrt{} (2 * (1- (\sin(\theta)/ \theta))) \quad (10)$$

where, θ ranges from 0º to 45º.

Similarly, by applying Equation (7) and (8) in Equation (4),

$$\cos(\theta) \approx (1 + (\gamma * \gamma / 2)) - (\theta * \gamma) \quad (11)$$

The γ value is cosine function, denoted as γ_c, is obtained using equation (11) as,

$$\gamma_c^2 - 2 (\theta * \gamma_c) - 2 (\cos(\theta) - 1) = 0 \quad (12)$$

Where, θ ranges from 0º to 45º. The minimum of the two roots from equation (12) is used for the computation.

Since the approximation is for the ranges from 0 to π/4, the remaining quadrant's values are obtained by the principle of sine/cosine symmetry [7]. The sine/cosine waveform is symmetrical between the range [π, 2π] and [0, π]. Also, the sine waveform from π/2 to π/4 is the same as the cosine from zero to π/4, and the cosine waveform from π/2 to π/4 is the same as the sine from zero to π/4. Thus, it is sufficient to compute the sine and cosine values from 0 to π/4 using equations (9) and (11). The entire sine wave is generated from the translations given in Table 1. The first quadrant is regrouped as 1A & 1B and similarly other quadrants are regrouped as 2A & 2B, 3A & 3B and 4A & 4B. When the phase value is 0 to π/4 (0º to 45º), the sine value of the phase is computed from the sine generator straight away. When the phase value is 45º

to 90º, the sine value of the phase is computed by subtracting the phase value from 45º and then by passing to a cosine generator. Similarly for other quadrants the sine values are computed.

Table 1. Translation of Phase Values

Counter value (bits)			Quadrant index	Phase value (θ) Degrees	Sine computation
0	0	0	1A	0≤θ≤45	sin(θ)
0	0	1	1B	45<θ≤90	cos(45- θ)
0	1	0	2A	90<θ≤135	cos(θ)
0	1	1	2B	135<θ≤180	sin(45-θ)
1	0	0	3A	180<θ≤225	-sin(θ)
1	0	1	3B	225<θ≤270	-cos(45- θ)
1	1	0	4A	270<θ≤315	-cos(θ)
1	1	1	4B	315<θ≤360	-sin(45-θ)

2.2. Proposed Architecture

Figure 1 shows the block diagram of the proposed DDFS architecture to complement the above discussed algorithm. It consists of phase generator, quadrant selector, sine/cosine generator, digital multiplexers and a DAC in the output stage. The phase generator (PG) of the proposed DDFS receives a frequency control word (FCW) as an input from the system to which the proposed DDFS is to be integrated. The phase generator output is then fed to a quadrant selector which selects the phase corresponding to the quadrant requirement. The output of the quadrant selector is fed to a sine/cosine generator. The multiplexer in the output stage selects the output either from sine generator or cosine generator to complete a full cycle of sinusoid as given in Table 1. The full cycle is generated by exploiting the symmetry of sine wave with respect to zero crossings over one full period [7].

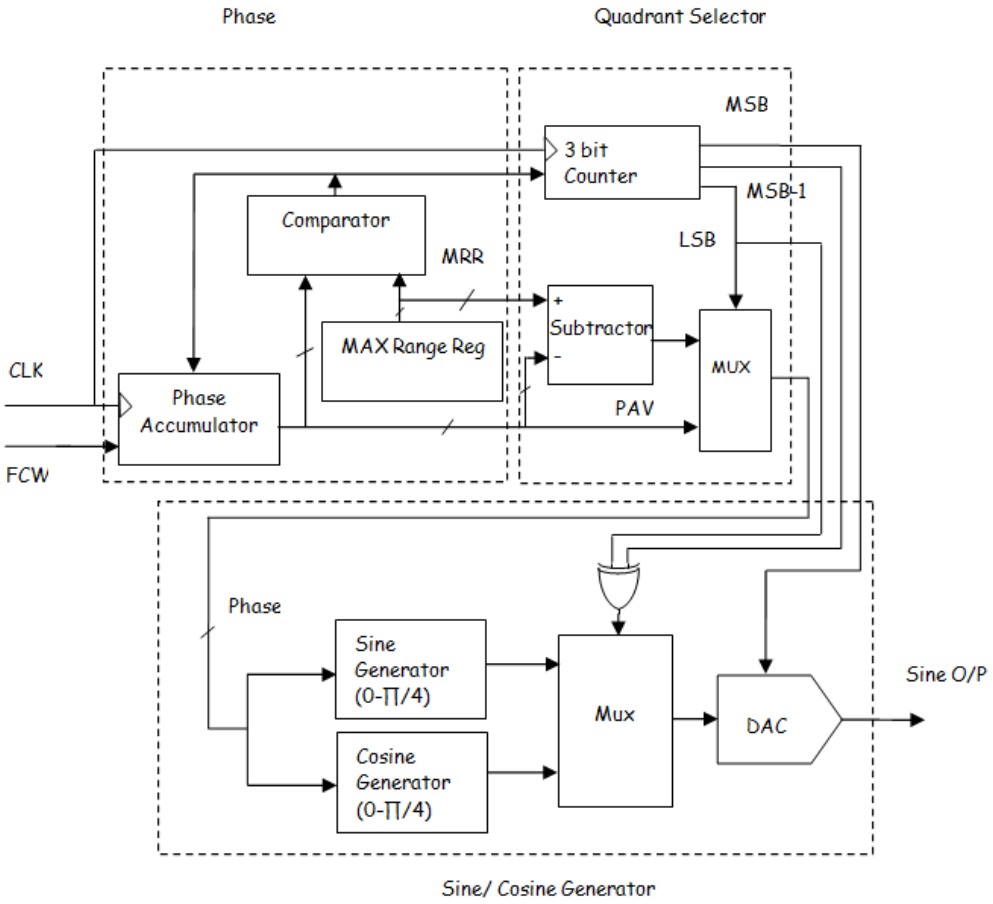

Figure 1. Block Diagram of the Proposed DDFS

2.1.1. Phase Generator: The phase generator consists of a phase accumulator, a maximum range register (MRR), and a digital comparator as shown in Figure 2.The phase accumulator is designed using an adder and a latch. The adder has two inputs and one of the inputs is a frequency control word (FCW) and input is fed back from the latch. The FCW is added with the same value on each clock signal and the value is accumulated in the latch. For digital realization, the phase is quantized as

$$\theta = n/2^N \qquad (13)$$

Where N is the size of the frequency control word and n is the value to be stored in maximum range selector register that takes on integer numbers in the range $0 \le n \le 2^N$. The value of N and n determine the resolution of the phase generator. The phase accumulator output θ is quantized in the range 0 to π/4 periodically (i.e. 0º to 45º). The maximum range value (n) for the maximum phase angle of the phase generator (45º) is $\pi/4 * 2^N$. The integer equivalent of the maximum range is stored in a memory called maximum range register. On each clock signal given to the latch, the phase accumulator generates consecutive phases. The comparator compares the output of the latch with MRR, when they are equal the comparator rises active high signal to reset the accumulated value in the latch. The phase accumulated value (PAV) from the output of the latch, the maximum range register output, and the comparator's output (detect) are connected to quadrant selector.

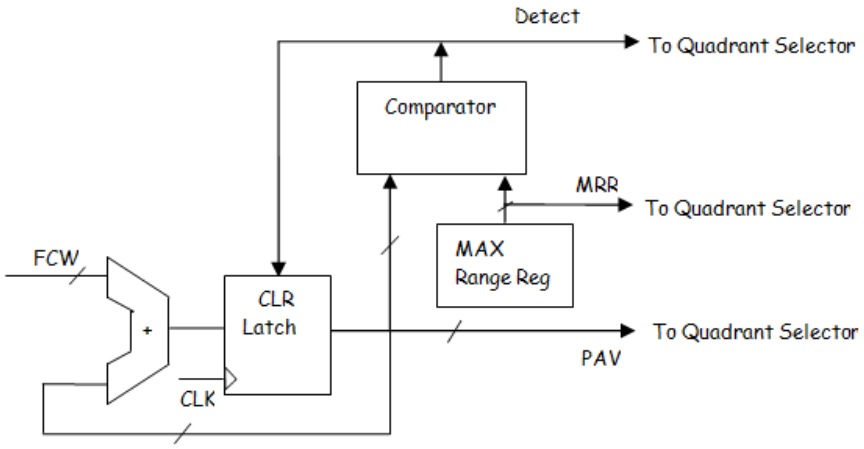

Figure 2. Phase Generator

2.1.2. Quadrant Selector: A quadrant selector consists of a subtractor, a multiplexer and a 3- bit counter as shown in Figure 4.4. It receives the output of the comparator (detect), the value from the MSR and output of the phase accumulator (PAV).

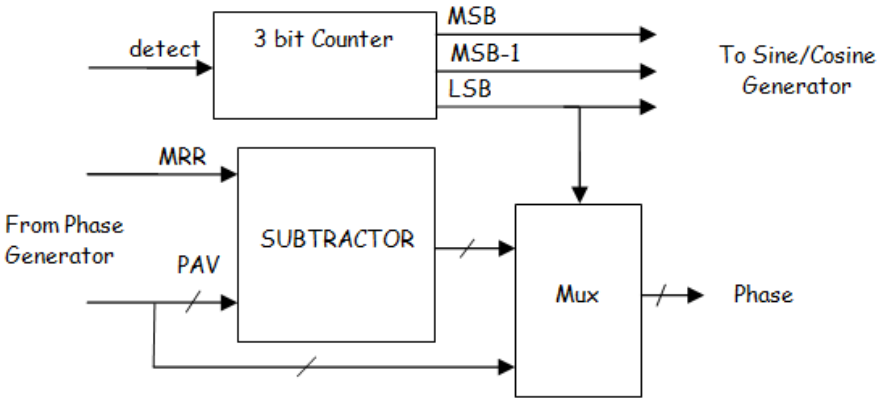

Figure 3. Quadrant Selector

The phase generator is designed for generating phase value from 0 to $\pi/4$, and to generate a full cycle of a sinusoidal the phase generator needs to generate this phase range for 8 times. The comparator in the previous stage detects the maximum range and generates the detect signal 8 times. The detect signal is used as a clock signal to the 3-bit counter so as to count the number of roll-overs and to identify the quadrant indices. The output of the 3-bit counter enables the multiplexer to choose the appropriate phase for sine computation. The MRR value and the phase values of each quadrant indices (1B, 2B, 3B & 4B) are fed to the subtractor in sequence. The phase values of other indices are routed directly to MUX. The phase value of each of the indices and the LSB output of the 3-bit Counter are multiplexed to produce the phase for Sine/Cosine function.

2.1.3. Sine/Cosine Generators: Figure 4 shows the block diagram of the Sine/Cosine generators, which generate sine and cosine value for the input phase between 0 to π/4.The arithmetic circuit is synthesized as per the Taylor expansion (Equation 9) and (Equation 11) for sine and cosine generation respectively. This module receives the phase value and quadrant indices from the quadrant selector. The phase value is in the range from 0 to π/4, and this value is given to two section of arithmetic circuit for generating equivalent sine and cosine value. The two arithmetic circuit computes its equivalent sine and cosine value from the given phase value and γ value. The sine and cosine values are computed using γ_s and γ_c respectively as given by in the Equations 9 and 11. The values of γ_s and γ_c are computed in a separate hardware block given in Figure 5.

A full cycle of sinusoidal signal is generated from two arithmetic sections with the assistance of quadrant index bits namely LSB and MSB-1. These two bits decide the output from any one of these two arithmetic sections. The selection of arithmetic is given in Table 2. It is clear from the table that an EX-OR of LSB and MSB-1 selects a cosine generator, otherwise a sine generator is selected.

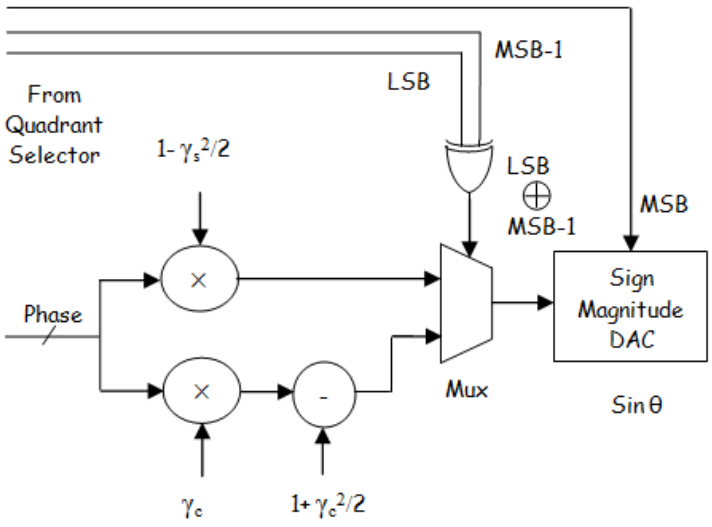

Figure 4. Sine/cosine Generators for 0 to π/4

Table 2. Arithmetic Section Selection for the Quadrant Index Bits

Quadrant Index Bit		Quadrant Index	Phase value (θ) in degree	Arithmetic Section selection
MSB-1	LSB			
0	0	1A	0≤θ≤45	sin section
0	1	1B	45<θ≤90	cosine section
1	0	2A	90<θ≤135	cosine section

1	1	2B	135<θ≤180	sin section
0	0	3A	180<θ≤225	-(sin section)
0	1	3B	225<θ≤270	-(cosine section
1	0	4A	270<θ≤315	-(cosine section)
1	1	4B	315<θ≤360	-(sine section)

The quadrants 3A, 3B, 4A and 4B require negation in the output of the DDFS, and this is done by MSB of the quadrant index bits. Once a full cycle of sinusoidal wave is obtained the entire module starts for a new cycle.

2.1.4. γ Accumulator: Figure 5 shows the block diagram of the γ accumulator employed for generating γ_s values. It consists of an adder, latch, comparator, subtractor and a multiplexer. Also the module comprises of two registers, one register to store the γ_{max} value (γ_s value corresponding to $(\pi/4 * 2^N)^{th}$ clock cycle) and another register to store the γ step value (linear incremental step size of the γ) which is a product of frequency control word (FCW) and $\gamma_{max}/ (\pi/4 * 2^N)$.

For each clock input, the adder with the latch generates an accumulated γ value with the step size of $(\gamma_{max}/ (\pi/4 * 2^N))$*FCW. This accumulated γ value is fed to a comparator and a subtractor.

The comparator compares accumulated γ value with the γ_{max} value for every instance of clock. When the accumulated γ value reaches to γ_{max}, the latch is cleared to zero and γ accumulation is started from initial value.

The subtractor subtracts accumulated γ value with the γ_{max} value for every instance of clock. The subtracted value of the γ accumulator is fed to multiplexer and the accumulated γ value is also given to the multiplexer. One of the inputs of the multiplexer is selected by the LSB of the counter in quadrant selector and given to sine/cosine generator.

Thus, γ accumulator is employed to generate γ_s values between 0 to π/4. Similar hardware architecture is used to generate γ_c values. The primary difference between the architectures employed to generate γ_s and γ_c values lies in the γ_{max} register content. The appropriate values to be stored in the γ_{max} registers are determined from (Equation 10) and (Equation 12).

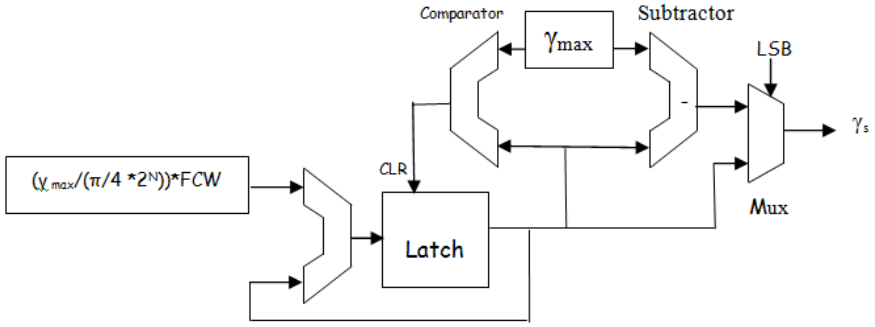

Figure 5. Block Diagram of γ Accumulator

3. Condition for Coherent Sampling

Frequency domain analysis is essential for dynamic characterization of analog and mixed signal circuits. The dynamic characterization of data converters (ADC, DAC) require spectrally pure and coherent sinusoidal signal (IEEE1241). Coherent sampling describes the sampling of a periodic signal, where an integer no of its cycles fits into a predefined sampling window.

Non coherent sampling would make the first and last samples discontinuous with one another resulting in spectral leakage during the spectral estimation of the device under test. This problem could be solved by either windowing or coherent sampling. However, windowing causes problems with Fourier analysis, the most important being spectral spreading, in which the energy in the main frequency component spreads between adjacent bins and increased test time. (A bin is the quantized frequency interval).

For obtaining coherent sine wave samples, the frequency control word has to satisfy the following condition:

$$(360\%FCW)=0 \qquad (14)$$

Thus, this digitally controlled sinusoidal signal generator is proposed to facilitate cost effective and accurate dynamic characterization of data converters by coherent sampling method to reduce the test time.

4. Results and Discussions

4.1. DDFS using LUT Based γ Values

The computed γ values for sine ranging from 0.0003 to 0.4465 and cosine functions ranging from 0.0005 to 0.6091 for 11 bit resolution are stored in a LUT. For each increment of phase accumulator output, the corresponding γ values can be accessed from the ROM for computation. The performance of the DDFS using the LUT based γ values is nearly 293 dBc. Figure 6 shows the spectrum obtained using these values. However, storing all γs and γc values in a lookup table greatly increases the hardware overhead and power consumption.

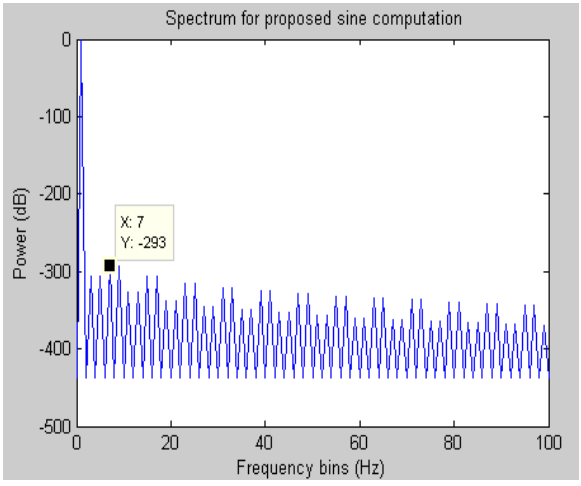

Figure 6. Spectrum of the Proposed DDFS using LUT for γ Values

4.2. DDFS using γ Accumulator

Instead of using look up table for storing γ values, combinational circuits like adder and multiplier are used for the computation of γ values thereby reducing the computational time. Fig.5 shows the architecture of γ accumulator. A simple combinational circuitry can automatically generate the γ values if one knows the range of γ values that is the maximum and minimum values of γ, and the linear equation. Thus, using the linear increment γ values, the ROM size is drastically reduced.

γs is varied from 0 to γmax i.e., 0.4465 in steps of γ max/(π/4*2N). Similarly γc is varied from 0 to γmax i.e., 0.6091 in steps of γ max/(π/4*2N).Figure 7 shows the spectrum for DDFS using γ accumulator. As it is seen from the graph, the SFDR performance of the DDFS using γ_s and γ_c accumulator over the range 0 - π/4 is about 135.6 dBc as compared to LUT γ values set of 293 dBc.

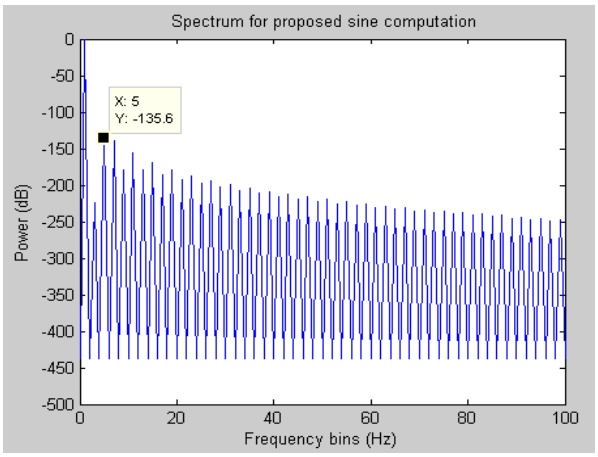

Figure 7. Spectrum of the Proposed DDFS using γ Accumulator in Simulation

4.3. Practical Implementation of Proposed DDFS

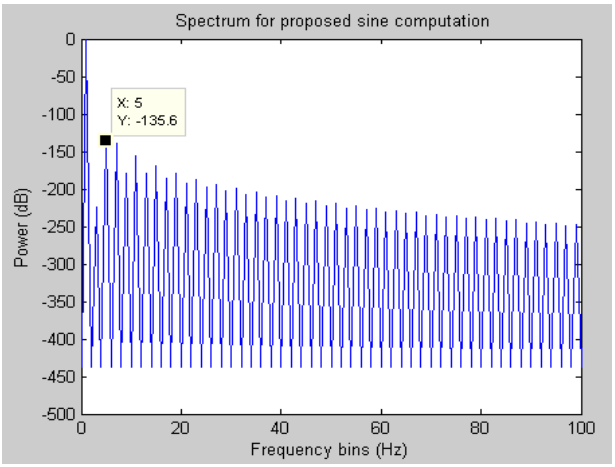

Figure 8. Spectrum of the Proposed Practical DDFS using γ Accumulator

The Phase generator, quadrant selector, sine/cosine generator, and γ accumulator are coded in Verilog and implemented in Altera FPGA DE1 kit. A digital to analog circuit is assembled in a vero board. The DAC board and FPGA kit are interfaced through GPIO. The value of N is assumed to 11 bit, the value of n is computed as in equation 3 using the symmetry of sine and cosine over $0 \leq \theta \leq \pi/4$ varies from 0 to 1608. The resolution of the proposed DDFS is $4.8843e^{-004}$.

The output waveform of the designed DDFS is captured by a computer using Agilent 34401A through RS232 interface. The captured data are fed to the Matlab program for extracting the graph. The spectrum of the captured data is shown in Figure 8. The SFDR from the measured data for the sine wave is 130.3 dBc, which is comparable with theoretical calculation of 135.6 dBc.

5. Conclusion

A novel DDFS architecture has been proposed to generate a sinusoidal signal. The proposed method is implemented based on Taylor Series polynomial approximations and improves the spectral purity remarkably. The replacement of look-up table with a digital combinational and sequential circuits results in the reduction of hardware complexity and also aids in faster computation. Results show that the spectral purity of the proposed DDFS is as high as 135.6 dBc for 11-bit resolution compared to 90 dBc for 14-bit resolution attainable with hybrid CORDIC algorithm.

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