Low Power Design Techniques for the Front End of a Radio Frequency Communication Receiver

by

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I certify that I have read this thesis and that, in my opinion, it is fully adequate in scope and quality as a thesis for the degree of Master of Engineering.

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I certify that I have read this thesis and that, in my opinion, it is fully adequate in scope and quality as a thesis for the degree of Master of Engineering.

(Dr. K. J. Vinoy)

Approved for the University Committee on Graduate Studies.

To all my teachers,

and especially to my parents, the best of them all.

Abstract

With the advent of applications such as mobile systems and sensor networks, low power wireless receivers have become the need of the hour.In this thesis two low power design techniques for the front end (LNA-Mixer) of a Radio Frequency(RF) communication receiver are explored.

First we address the problem of optimal power and noise allocation among the analog and digital sections of the radio receiver, which minimizes the power consumption of the overall RF receiver while mainitaining the Bit Error Rate(BER) constraint. We propose a methodology to arrive at the power-optimal noise and linearity specifications of all the components of the radio receiver, including that of the digital base band.

Next we discuss the concept of adaptive receivers, which adapt their performance in accordance with the channel conditions, thereby offering significant power savings. Using basic receiver performance equations, we analytically derive the specifcations required by the adaptive receiver under various channel conditions. Then using the already developed power-optimal design methodology, we arrive at the optimal-specifications for the front end of an adaptive receiver as a function of the received signal and interferer levels. We show that the front end for an adaptive receiver needs independent tunability of noise figure and linearity. We propose two front end topologies which achieve such independent tunability, one for an 802.15.4 ZigBee receiver with a relaxed noise figure specification and the other suitable for a wireless LAN receiver which requires a stringent noise figure specification. The first topology is a low voltage merged LNA-Mixer structure, which has been taped out in UMC 0.13um 2P8M RFCMOS technology. The second topology is based on the popular inductively degenerated Common Source topolgy, in which the degeneration inductor has been replaced with a novel high Q, g_m tracking active inductor.

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List of Publications

Conference Publications

1. S A Kannan , Manodipan Sahoo, Satyam Dwivedi, Bharadwaj S Amrutur, Navakanta Bhat, "Optimal Power and Noise allocation for Analog and Digital Sections of a Low Power Radio Receiver",Accepted in International Symposium on Low Power Electronic Design, August 2008.

Under Preparation - to be Submitted

1. S A Kannan, Bharadwaj S Amrutur, " A Low voltage Low power merged LNA-Mixer for an adaptive ZigBee Receiver."

2. S A Kannan, Bharadwaj S Amrutur, " A current tunable single transistor high Q active inductor. "

3. S A Kannan, Bharadwaj S Amrutur, " An adaptive inductively degenerated common Source LNA, using a novel active inductor topology suitable for high performance adaptive RF receivers."

4. An improved journal version of "Optimal Power and Noise allocation for Analog and Digital Sections of a Low Power Radio Receiver."

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Chapter 1

Introduction

1.1 Motivation

Low power, low cost radios have become the need of the hour, with the advent of portable systems and wireless sensor networks. The number of portable devices such as cellphones and laptops have increased tremendously in the last decade and continue to increase rapidly.Figure 1.1 show the near exponential growth in the number of cellphone users in India in the past decade. These mobile devices being operated from a battery, demands remarkably low power consumption of the radios in them.The form factor of these devices keeps decreasing over years and hence the available battery energy keeps decreasing, whereas the performance demanded from these devices keep increasing.Hence power consumption has become a major engineering concern in the design of wireless radios for mobile devices.

The other class of wireless systems which demand extremely low power operation, are the radios used in the motes of a wireless senstor network.Wireless sensor networks are spatially distributed autonomous nodes with sensors to cooperatively monitor physical or environmental conditions, such as temperature, sound, vibration and pressure. Sensor networks are typically used in military, office and home automation, industrial control etc.The nature of the environment in which these sensor

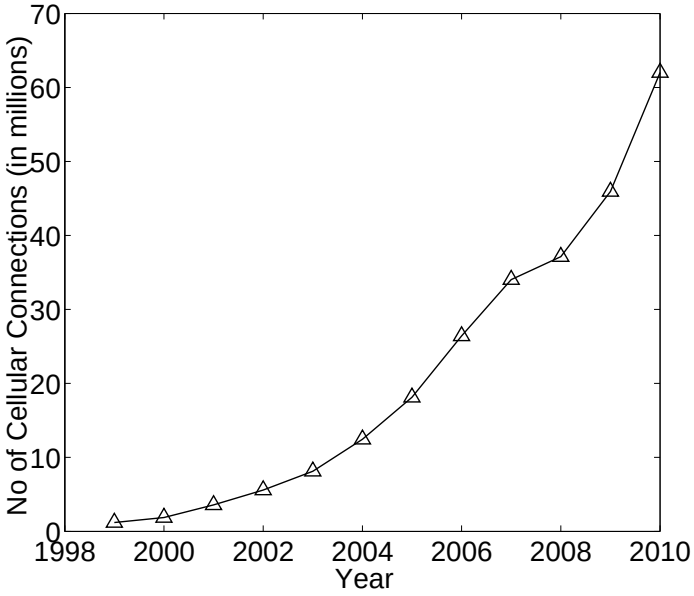


Figure 1.1: Growth of Cellphone Usage in India in the last decade. Source: http://www.bsnl.co.in/network/statistic.htm

networks operate and the possibly high number of sensor nodes in a network , make battery replacement extremely difficult, if not impossible. Hence a sensor node must be self contained in energy either through a one time battery charge or by scavenging energy from its environment.Even if a one time battery-charge is feasible,batteries are detrimental to the form factor of the sensor node. For example at 100 μ W, 1 cm3 of non-rechargeable Lithium-Ion battery does not last even for 6 months[1].Hence scavenging Energy from the atmosphere to power up the sensor nodes has become an active area of research [2] [3] and hopefully most sensor networks in the future will be scavenging their own energy. Summarizing, if low power consumption is a major engineering concern for mobile and hand held devices, it is an absolute necessity for sensor network applications.

A relief to the designer of a radio for sensor network is the fact that compared to the wireless LANs and mobile systems, the data rates in the sensor network applications are low. Table 1 gives a comparison of maximum data rates specified by a few [4] [5] IEEE standards . Such low data rates combined with the relative scarcity of

Table 1.1: Maximum data rates specified by a few communication standards

Standard	Max. Data rate	Application
ZigBee	250 Kbps	Sensor Networks and Wireless Personal Area Networks
EGSM	270 Kbps	Cellular Communication
802.11b	2Mbps	Wireless Local Area Network
802.11g	54Mbps	Wireless Local Area Network

energy, motivates researchers to find innovative ways to lower the power consumption of radios for wireless sensor network motes.

In this thesis we discuss two low power techniques for a radio receiver, one at the system level and other at the circuit level. Although, a 802.15.4 ZigBee compatible low IF(intermediate Frequency) receiver has been mostly used to demonstrate the techniques described, the techniques themselves are generic and are applicable to a wide class of Radio Frequency (RF) receivers. The next section gives a brief overview the thesis.

1.2 Thesis Overview

The issue of power concern in a radio must be addressed at various hierarchies, from system architecture down to circuit technology. The first task in any RF receiver design is to identify a suitable receiver architecture for the application /standard at hand which demands a certain Bit Error Rate(BER) specification. Several architectures like super-heterodyne, low IF , zero IF are described [6].Once an architecture is chosen , the next design step is to arrive at the specification of all the building blocks of the receiver. Traditionally this step in the design process was done iteratively and was heavily dependent on the experience of the system designers. A systematic procedure for deriving the specification of the building blocks of the analog section of the receiver is a very important problem which has been addressed partially in a recent paper by the authors in [7]. The first low power technique discussed in this thesis,

completely solves the problem of arriving at the optimal set of specifications for all the sub-blocks in the analog and digital sections of the receiver, which minimizes the overall power consumption of the radio, while meeting the BER target.

Designers of the current state of the art radio receivers, design all the components to meet the worst case specifications for received signal strength, noise of the devices and interference power. This leads to over design of the receiver components which is often wasteful of power when the conditions are more benign. When signal conditions in terms of received signal power and interference change, most existing receiver designs are not able to fully take advantage and minimize power. An intelligent receiver, will reduce its power consumption during benign channel conditions, while maintaining the required BER at its output.Such adaptive receivers offer significant energy savings,and hence will be a popular choice for the low power radios of wireless sensor networks in the near future. To implement a completely adaptive receiver, one must rethink the RF circuit design for communication receivers in view of adaptability. Novel circuit topologies, which best trade off performance for power must be invented. The second half of this thesis presents two front end circuit topologies suitable for adaptive receivers. One of them is suitable for an adaptive 802.15.4 ZigBee receiver and another for a wireless LAN receiver.

1.3 Thesis organization

This thesis is organized as follows

- Chapter 2 gives a brief description of the basics of a radio receiver and formally reviews the popular performance specifications used in the design of a radio receiver.Next a very brief overview of ZigBee 802.15.4 is given.
- Chapter 3 describes in detail the proposed power optimal design methodology to arrive at the optimal power and noise allocation for the analog and digital

sections of the radio receiver. The methodology is discussed with the example of a Low IF ZigBee receiver.

- Chapter 4 highlights the characteristics of an adaptive receiver. Performance specifications for an adaptive ZigBee receiver as a function of channel conditions are obtained analytically and a low voltage merged LNA-Mixer topology suitable for an adaptive ZigBee receiver is proposed.

- Chapter 5 discusses the chip implementation of the proposed low voltage LNA-Mixer topology in UMC 0.13um process.

- Chapter 6 describes a novel active-inductively degenerated common source LNA for an adaptive receiver for suitable for wireless LAN standards.

Chapter 2

Background

2.1 Introduction

This chapter formally reviews the basic performance metrics used to characterize an RF receiver. A brief overview of the 802.15.4 ZigBee standard follows, since a ZigBee receiver has been used to demonstrate the low power techniques discussed throughout this thesis.

2.2 A Typical Radio Receiver

The goal of any radio receiver is to extract and detect selectively a desired signal from the electromagnetic spectrum. This selectivity in the presence of a plethora of interfering signals and noise is the fundamental attribute that drives many of the tradeoffs inherent in radio design. Several receiver architectures have been used along the long history of radio receivers and an excellent overview of these architectures can be found in [6]. Among all these architectures Low IF/ zero IF architectures have been found to be suitable for our targeted wireless sensor network application[8]. Figure **??** shows a low IF receiver, an architecture used as a demonstrating vehicle throughout this thesis.

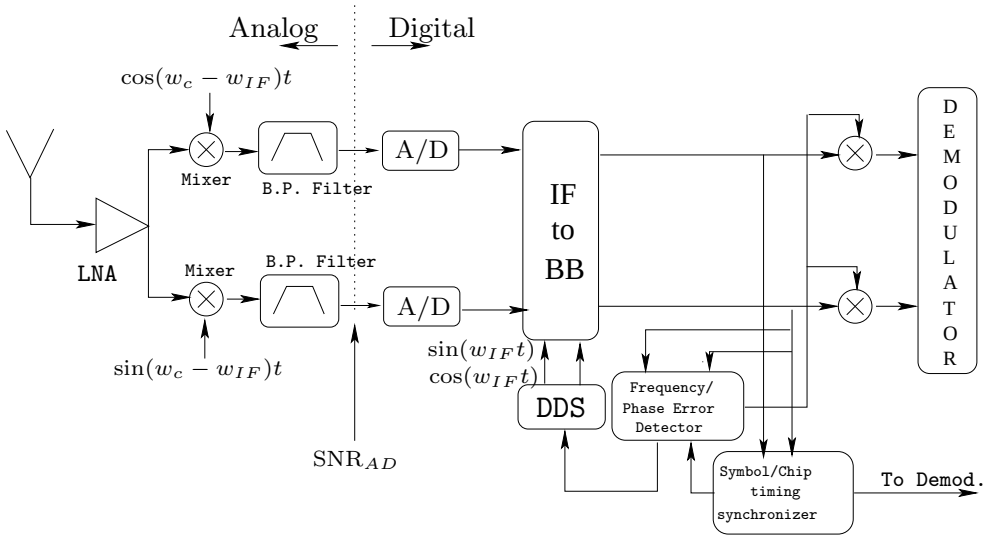


Figure 2.1: Low IF Radio Receiver

The receiver consists of a front end Low Noise Amplifier (LNA), which amplifies the very small signal received by the antenna. The mixer which follows the LNA, downconverts the RF signal into an intermediate frequency(IF) (in the case of zero IF receiver, directly to the baseband). A Channel select filter then selects the appropriate channel to be received. The filter in a low IF receiver will usually be a bandpass filter around the IF. The conversion from IF to the baseband can be done in either the analog or the digital domain. Due to the digital revolution, the current state of art is to perfrom the second conversion in the digital domain. Hence the signal in IF is digitized using an Analog to Digital Converter (ADC). Usually a Variable Gain amplifier (VGA) is used before the ADC to maintain the signal at the input of ADC near full scale. Once digitized, the signal is downconverted to baseband using a digital mixer and then demodulated digitally.

The key performance metric of a modern radio receiver is its Bit Error Rate (BER) . Errors occur in reception due to the noise and other signal distortions occurring in

the receiver.Hence, a given BER specification, usually translates into the noise and signal distortion specifications of the receiver. The next section formally reviews the noise and distortion specifications, relevant to an integrated radio receiver. Since a completely integrated CMOS(Complementary Metal Oxide Semiconductor) radio is the current state of the art, these specifications are reviewed in view of a CMOS implementation of a radio receiver.

2.3 Noise in radio receivers

2.3.1 Sources of Noise in a radio receiver

The sensitivity of any radio receiver is limited by the presence of electrical noise. Thermal noise or Johnson noise, shot noise, flicker noise are a few major kinds of noise encountered in the design of radio receivers. Thermal noise arises due to random fluctuations of thermally agitated charge carriers in a conductor. A mean square open circuit noise voltage in a resistor,R at an absolute temperature T is given by

$$V_n^2 = 4kTR\Delta f \tag{2.1}$$

where k is the Boltzmann constant and Δf is the bandwidth over which noise is measured [9].

MOSFETs also suffer from thermal noise. The thermal noise of mosfet is modelled as a current source between its drain and gate, having a mean square noise current value given by

$$I_{nd}^2 = 4kT\gamma g_{d0}\Delta f \tag{2.2}$$

where g_{d0} is the drain source conductance and γ has the classical value of $\frac{2}{3}$ for long channel devices. [10] For short channel devices γ is generally higher than $\frac{2}{3}$. Usually g_{d0} is proportional to g_m and can be written as $g_{d0} = \frac{g_m}{\alpha}$.

MOSFETs also suffer from flicker noise[11], arising from the random trapping of

charge carriers at the Silicon-Silicon Oxide interface. Flicker noise is usually modelled as a noise voltage source in series with the gate terminal having a mean square noise voltage of

$$V_{n,flicker}^2 = \frac{K}{WLC_{ox}f} \tag{2.3}$$

where K is a process dependent constant, W,L are the width and length of the mosfet, C_{ox} is the oxide capacitance per unit area of the process.Since flicker noise power is negligible at high frequencies, it is usually not considered in radio designs (except in zero IF receivers). In addition to thermal and flicker noise, MOSFETs also exhibit an induced gate noise, which is non-negligible at high frequencies. Vander Ziel presents a detailed study of gate noise[12] and has modelled it as current source between drain and source .Gate noise can be represented as

$$i_{ng}^2 = 4kT\delta g_g \Delta f \tag{2.4}$$

where

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{2.5}$$

2.3.2 Noise Factor

The most important performance metric of a system, which characterizes its noise performance is Noise Factor.The noise factor is a measure of the degradation in Signal To Noise Ratio(SNR) that a system introduces. Noise Factor is defined as

$$F \equiv \frac{total\ output\ noise\ power}{output\ noise\ power\ due\ to\ input\ source} \tag{2.6}$$

This definition is equivalent to the alternate definition

$$F \equiv \frac{SNR\ at\ the\ input}{SNR\ at\ the\ output} \tag{2.7}$$

We can notice that the noise figure is not defined when the input noise to a system is zero. However such a difficulty does not arise while dealing with radio receivers, where the signal input at the first stage itself is corrupted by the noise of the radiation resistance of the antenna. Noise figure of a system is its noise factor expressed in decibels.

$$Noise\ figure,\ NF = 10log_{10}(Noise\ Factor) \tag{2.8}$$

An ideal system which adds no noise has a noise factor of 1 or a noise figure of 0 dB. Although the distinction between terms noise figure and noise factor are maintained in this thesis, in a few places the short form NF may be used to refer to either of them. In such places the distinction can be made from the context.

2.3.3 Sensitivity

Sensitivity of an RF receiver is defined as the minimum signal level that the system can detect with acceptable Signal to noise ratio. This can be expressed in terms of Noise figure as follows

$$Sensitivity(dBm) = NF + SNR_{min,required} + 10log_{10}(kTB) \tag{2.9}$$

where B is the Bandwidth of the channel to be received [13].

2.4 Non linearity in radio receivers

Non-linearities in a system lead to signal distortions and hence errors in detection. Non-linearity of a system manifests itself in different ways like gain compression, harmonic distortion, intermodulation distortion etc. In the case of a radio receiver, the most relevant of these are gain compression and intermodulation distortion. 1 - dB compression point (P1dB) and Input Referred Intermodulation Product - 3rd order (IIP3) are two frequently used linearity metrics to characterize systems in an RF

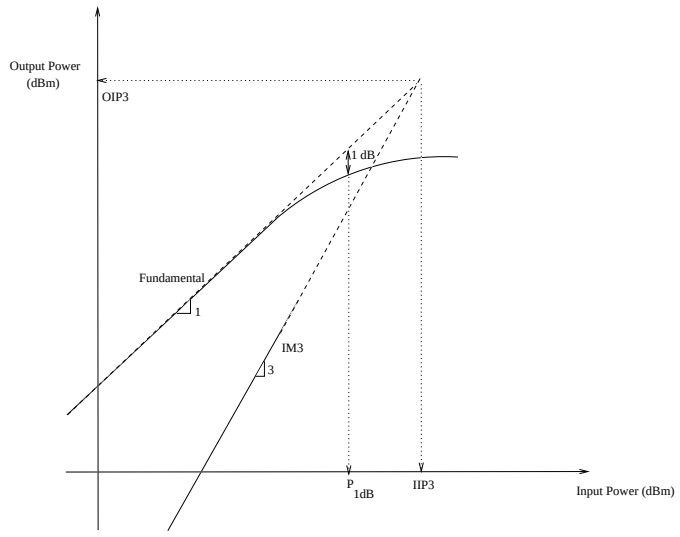


Figure 2.2: Definitions of P_{1dB} and $IIP3$ for a hypothetical non-linear system transfer function

receiver.This section briefly reviews these metrics. It should be appreciated that even an inherently non-linear system such as a mixer which performs frequency translation can be characterized by these metrics, if the definition linear behavior is modified appropriately.

2.4.1 1 - dB compression point (P_{1dB})

Gain of a system is generally reported using its small signal behavior, ie when the input signal levels are small. However when the input signal level increases non-linearities of the system begin to mainfest and the gain begin to vary. Figure 2.2 shows the input-output plots for a generic system. 1-dB compression point is defined as the input signal level at which the gain becomes 1 dB lesser than small-signal gain. Fig. 2.2, shows the P_{1dB} point for a hypothetical non-linear system.

2.4.2 Input Referred intermodulation product 3rd order (IIP3)

When the input signal to a non linear system has two frequencies f_1 and f_2, the output has components at frequencies $mf_1 + nf_2$ also. These terms are called InterModulation(IM) terms of $(m+n)^{th}$ order. In radio receivers 3rd order intermodulation are studied with great care as they fall close to the input signal frequencies. Higher order odd intermodulation terms are ususally negligible and even order intermodulation terms are cancelled in a differential structure.

Input Referred intermodulation product 3rd order(IIP3) is defined as that input signal level at which the output fundamental and third order intermodulation products have equal power. In general both the output fundamental and third order components saturate well before the IIP3 level and hence IIP3 is obtained by extrapolation of the fundamental and third order IM products amplitudes at lower signal levels.

In the case of a system in which the third order non-linearity dominates over the other non-linearites, it can be shown that IIP3 and P1dB are related [13] by the equation.

$$IIP3 = P_{1dB} + 9.6dB \tag{2.10}$$

Fig. 2.2, shows the $IIP3$ point for a hypothetical non-linear system. IIP3 of a receiver is generally chosen such that the IM3 products lie below the noise floor of the system.

2.5 Cascaded systems

When multiple systems are cascaded together as shown in Figure(2.3), the Noise factor and IIP3 of the complete system can be expressed in terms of the Noise factor, IIP3 and gain of the individual systems. Noise factor of cascaded system is given by

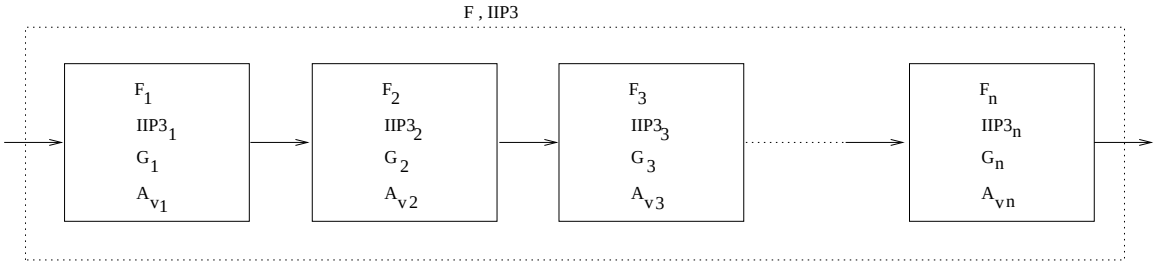


Figure 2.3: Noise figure and IIP3 of cascaded systems

the famous friss formula [14].

$$F = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 G_2 ... G_{n-1}} \tag{2.11}$$

This classical formula use the available gain of the systems, which is not very convenient to use in the case of an integrated systems, because of the lack of impedance matching between successive stages. Hence a more meaningful expression for cascaded systems has been given in sinencio by changing the definition in terms of noise/IIP3 voltages and voltage gains [7].

$$V_{ni,tot}^2 = V_{ni,1}^2 + \frac{V_{ni,2}^2}{A_{v1}^2} + \frac{V_{ni,3}^2}{A_{v1}^2 A_{v2}^2} + ... \frac{V_{ni,n}^2}{A_{v1}^2 A_{v2}^2 .. A_{v(n-1)}^2} \tag{2.12}$$

where $V_{n,i}$ is the input referred noise voltage of a system and $A_{v,i}$ is the voltage gain of the system. similarly the IIP3 of the cascaded system can be represented as

$$\frac{1}{V_{IIP3,tot}^2} = \frac{1}{V_{IIP3,1}^2} + \frac{A_{v1}^2}{V_{IIP3,2}^2} + \frac{A_{v1}^2 A_{v2}^2}{V_{IIP3,3}^2} + ... \frac{A_{v1}^2 A_{v2}^2 ... A_{v(n-1)}^2}{V_{IIP3,n}^2} \tag{2.13}$$

where V_{IP3} is the input voltage at which the output fundamental and IM3 voltages become equal (voltage counterpart of IIP3).

2.6 IEEE 802.15.4 LR-WPAN Standard - A brief overview

IEEE 802.15.4 WPAN standard [4] released a preliminary draft in 2003, targetted at low-data rate applications such as low-cost pervasive wireless sensor networks, with extremely low duty-cycle capability ($\leq$ 10 ppm). It is the first global wireless standard aimed at low-power remote monitoring and control applications.IEEE 802.15.4 operates in three unlicensed industrial, scientific and medical (ISM) bands of 868/915 MHz and 2.4 GHz with a total of 27 channels .

Of the 3 bands, 2.4 - 2.4835 GHz band is most attractive as it is the only worldwide allocation of spectrum that does not have restrictions on the application and transmit duty-cycling. The center frequencies in this band are given by

$$f_c = 2405 + 5(k - 11)\ MHz,\ k = 11, 12....26$$

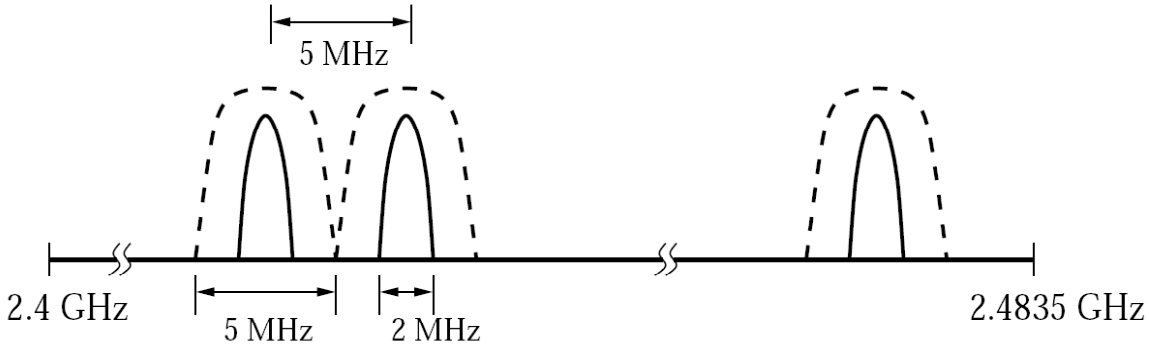


Figure 2.4: Frequency Plan of IEEE 802.15.4 standard

Figure (2.4) shows the frequency planning of ZigBee. Table 2.1 summarizes the important specifications for the receiver prescribed by the standard. Raw data at the rate of 250Kbps is modulated using DSSS-OQPSK. Spreading is done grouping four data bits and assigning a 32 length nearly orthogonal chip sequence for the 16 possible symbols. The symbols are then pulse shaped using half sine pulses and modulated in

Table 2.1: Important Specifications for a IEEE 802.15.4 Standard

Specification	Value
Maximum Data Rate	250 Kbps
Symbols	16ary Orthogonal
Modulation	OQPSK
Symbol rate	62.5 Ksps
Sensitivity	-85 dBm
Maximum Input signal level	-20dBm
Adjacent Channel Rejection	0 dB
Alternate Channel Rejection	30 dB
Transmission Range	10-100m

I & Q carriers using OQPSK modulation.

Being a relatively low data rate standard, ZigBee has relaxed performance specification compared to cellular and wireless LAN standards. So it has been used for demonstrating the low power issues being addressed in the remaining of the thesis. However it should be noted that, the techniques themselves are applicable to a wide class of radio receivers and not necessarily to ZigBee alone.

Chapter 3

Optimal Power and Noise Allocation for Analog and Digital Sections of a Low Power Radio Receiver

3.1 Introduction

The noise figure specifications for a radio receiver are typically derived based on the SNR requirements at the input of the demodulator to achieve a target BER. The usual practice is to assume that the noise contribution from the digital section (quantization noise) is minimal and allocate almost the entire noise budget to the analog front end [15]. While this practice is analytically more tractable, as well as provides for a good engineering margin, it inevitably leads to an over-design and hence excess power consumption. For applications like wireless sensor networks, which demand ultra low power consumption, there is a need to reduce the over-design margin to squeeze out as much power savings as possible. The authors in [16] show that there is a continuum of design choices for the noise figures of the analog front end as well as the resolution

and oversampling rate of the digital section, all of which meet the target BER for the 802.15.4 based radio receiver. Thus, even a 1-bit digital section will meet the target BER, provided the SNR at the input to the ADC is sufficiently high and a certain minimum oversampling rate is used for the digital processing. Hence a less noisy analog front end can use a reduced resolution digital section while a noisier analog front end, needs a higher resolution digital section. This sets up an interesting optimization problem: viz., what should the target SNR be at the analog-digital interface (SNR_{AD}), and what resolutions and oversampling rates should be used in the digital section, so that the overall power is reduced while meeting the target BER. In this work, we address this optimization problem, for a simple low-IF based 802.15.4 receiver.

A recent work by Sheng et. al. in [7] addresses the problem of optimal analog front end design. For a given SNR specification at the output of the analog front end, they determine the optimal power, noise and linearity budgets for the different components of the analog front end based on some simple analytical models for these. However they do not address the requirements of the local oscillator and digital section in their work. We will use their results for modeling the analog front end, and combine it with our analysis of the local oscillator and the digital section to obtain the optimal power and noise allocation for the overall receiver.

3.2 Optimization formulation

We consider a Low-IF 802.15.4 receiver with an IF of 3MHz for demonstrating this optimization (Figure.3.1) .The analog section of the receiver consists of the LNA, Mixer, Channel select filter and the frequency synthesizer. The digital section consists of the ADC, IF to baseband down-converter, demodulator and the digital IF oscillator with its timing recovery loop. The demodulator is a bank of coherent correlators, which correlate the incoming sampled data stream with all 16 sampled chip sequences,

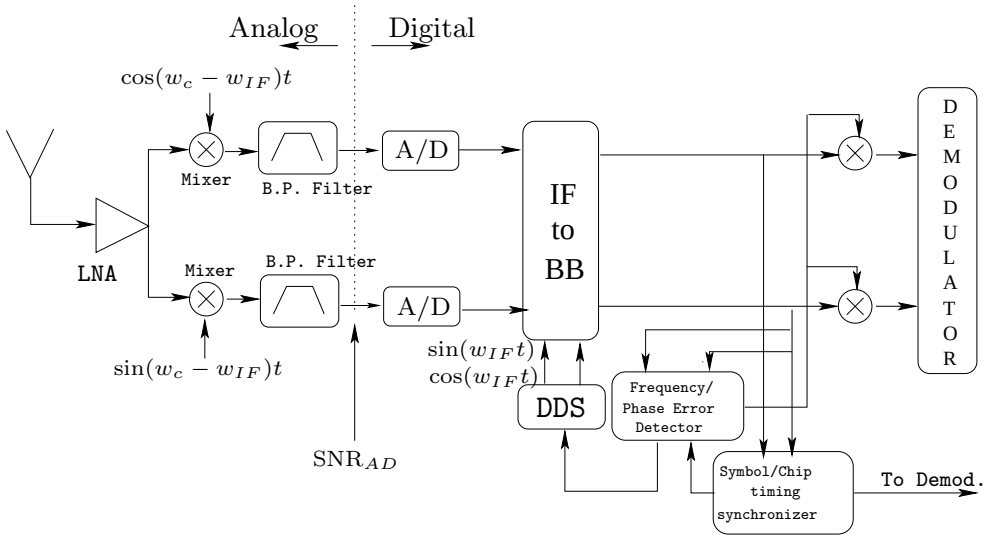


Figure 3.1: Low IF Radio Receiver

followed by a max detector. The target BER for this application is 6.25×10^{-5}, which results in a Packet Error Rate (PER) of less than one percent for a PHY service data unit (PSDU) of length 20 octets.

We will denote the SNR at the interface between the analog and digital sections (i.e the input to the ADC in Fig. 3.1) as SNR$_{AD}$. As specified by the standard, receiver should be capable of achieving a sensitivity of -85 dBm or better. The noise figure of the analog front end with 50 Ω matching at input of LNA and 2 MHz channel bandwidth, can be calculated as [13]

$$\mathrm{NF}_{analog} = -85 \text{ dBm} + 173.8 - 10\log_{10}(2 \times 10^6) - \text{ SNR}_{AD} \tag{3.1}$$

The power of the analog front end, P_{analog} is a function of NF_{analog} which in turn is dependent on SNR_{AD} through the above equation. For a given SNR$_{AD}$, the target BER can be achieved by a variety of choices of resolution and operating frequency

of the digital section as shown in [16]. The resolution of the digital section can be controlled at the three locations shown in Fig.3.3a, viz., the ADC resolution, the digital local oscillator resolution and the demodulator chip sequence resolution. For this study, we use the same resolutions for both the demodulator and the local oscillator and only consider 1-bit and 8-bit as two possible candidates. We further assume for this study that the operating frequency of the entire digital section is the same as the sampling frequency of the ADC. For a given SNR_{AD}, there can exist multiple resolution, operating frequency combinations for the digital section, which meets the target BER as shown in Fig. 3.2. These graphs have been obtained by performing BER simulations in MATLAB at the waveforms level, to consider effects of quantization.

The figure shows three graphs, one for an ideal multi-bit receiver with no quantization degradation, one for a 1-bit receiver with only the ADC restricted to one-bit and the final one for a 1-bit receiver where the ADC, the oscillator and demodulator all are 1-bit. As can be seen, the performance degrades with increasing quantization, in the sense that for a given SNR, one needs increasingly more operation frequency with increasing quantization, to meet the target BER. Also the minimum SNR required to achieve the target BER for any operating rate increases with increasing quantization. Thus an all one-bit digital section needs at least 1.3dB of SNR_{AD} at its input. We can now formulate the power optimization as follows. We first relate the SNR_{AD} to the resolution and operating frequency of the digital section as

$$\text{SNR}_{AD} = F(resolution_{ADC}, resolution_{LO/DEMO}, freq) \tag{3.2}$$

Unfortunately, we do not have a closed form analytical expression for the above function and instead we use the simulation derived relation for further analysis, an example of which is shown in Fig. 3.2. The total power for the receiver can now be

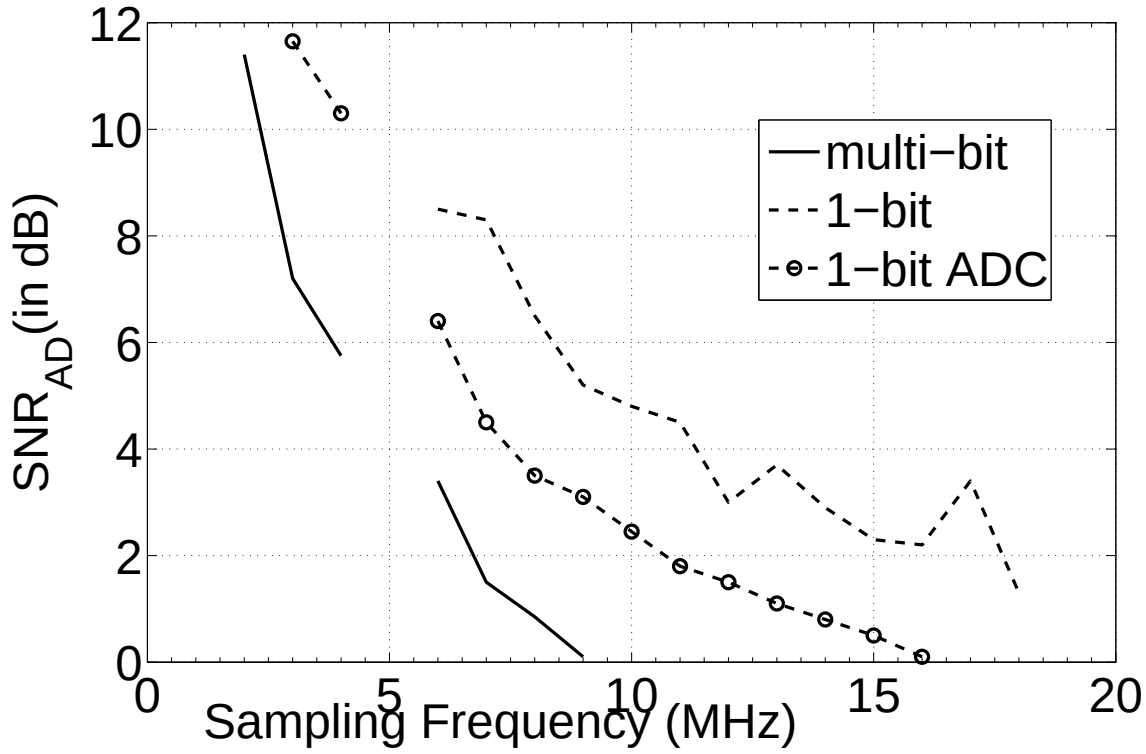


Figure 3.2: SNR_{AD} vs sampling frequency curve for low-IF receiver for BER of 6.25×10^{-5}.

written as

$$P_{total} = P_{analog}(SNR_{AD}) + P_{digital}(SNR_{AD}) \tag{3.3}$$

and the above needs to be minimized over the set of feasible values for resolution_{ADC}, $\text{resolution}_{LO/DEMO}$ and frequency.In order to carry out this optimization, we need to model the analog and digital power and we discuss this next. We have used SPICE models for an industrial 0.13um RF CMOS Process.

3.3 Power estimation of Analog Section

The analog front end consists of LNA, mixer, Local Oscillator and the channel select filter. Within the analog section of the receiver there exists an optimization problem of choosing the right set of noise - power budgets for the various analog sub-blocks, which minimizes the power consumption of the analog section. One must solve this

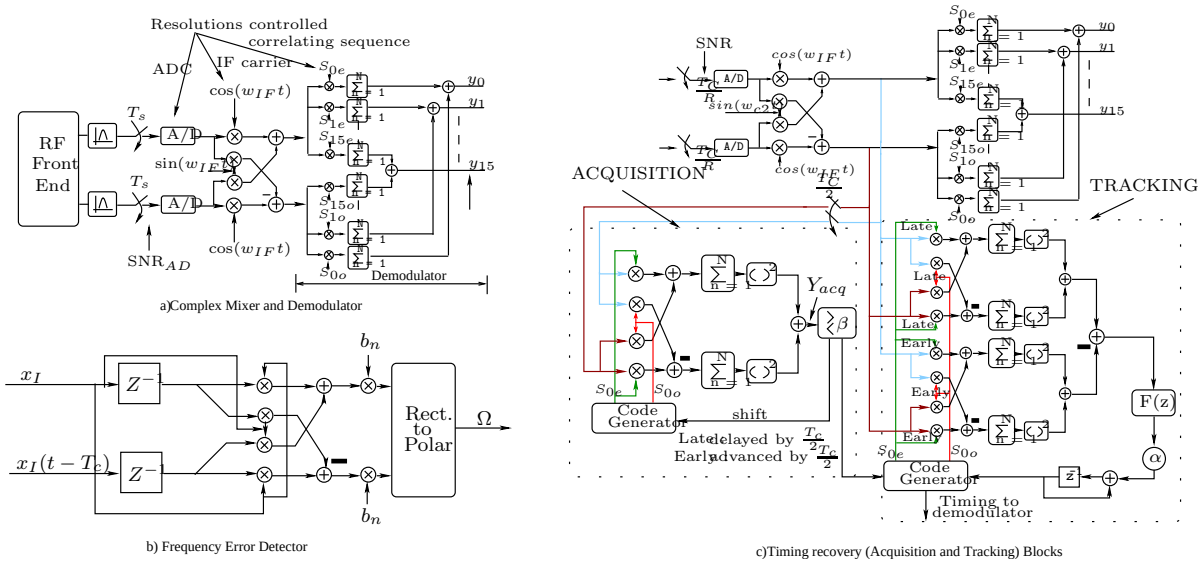


Figure 3.3: Detailed block diagram of the digital Section of the receiver

sub-optimization problem before attempting at the full receiver power minimization. Part of this problem was solved in [7] but the local oscillator was not included in the work.We extend the work in [7] by including the local oscillator in the power-optimization problem.To achieve this,we derive the effect of local oscillator on the noise figure of the analog front end. Then the optimization problem is solved using power models for the analog sub -blocks.Once the optimal noise-power budgets for all the sub-blocks are obtained, they are used to estimate the power of the analog section of the receiver.

3.3.1 Noise model of the receiver

Consider the Noise model of the receiver given in Figure. 3.4. Defining the symbols as given in Table 3.1 , the Noise power at the output of the receiver is given by

$$N_{output} = G_{LNA}G_{mix}G_{filt}N_{in} + G_{mix}G_{filt}N_{LNA} + N_{mix}G_{filt} + N_{filt} + (G_{LNA}G_{mix}P_{int}PN_{osc}B)G_{filt}$$

The last term in the expression is the noise added to the signal band due to reciprocal self mixing of interferers with the finite Phase Noise of the oscillator. This equation

Symbol	Definition
$N_{lna}, N_{mix}, N_{filt}$	Noise power added by LNA, Mixer, Filter referred to their outputs
Nin	Noise at the input of the receiver
P_{int}	Power of the dominant interference signal at the input
$G_{lna}, G_{mix}, G_{filt}$	Gain of LNA, Mixer Filter
B	Channel Bandwidth
PN_{osc}	Phase Noise of the Oscillator at a frequency offset corresponding the dominant interferer
F_{analog}	Noise factor of analog front end
F_{osc}	Noise factor contribution of Oscillator
F_{chain}	Noise factor contribution of LNA, Mixer, Filter

Table 3.1: Definitions of Symbols

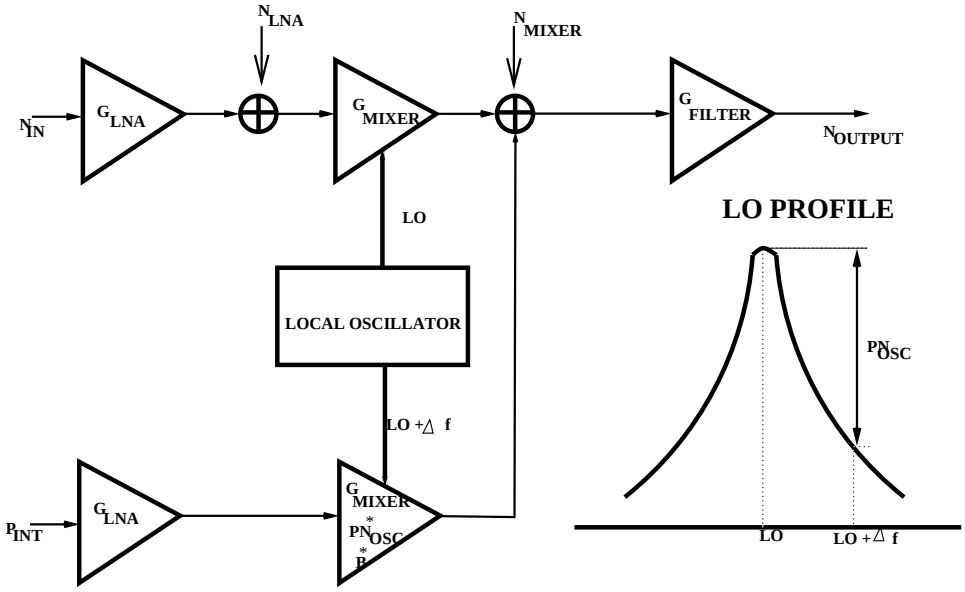


Figure 3.4: Noise Model of the Receiver

considers only one dominant interferer signal whereas in a practical case there can be many. In the case of ZigBee the interference can be either from an adjacent channel or alternate channel. Since the alternate channel interferer tolerance specification is 30dB above that of the adjacent channel[4], the noise due to reciprocal self mixing of alternate channel will be more dominant. Hence the assumption of a single dominant interferer is justified for a ZigBee receiver.Now we can write the Noise Factor of analog section as.

$$F_{analog} = \frac{N_{output}}{G_{LNA}G_{mixer}G_{filter}N_{in}} \tag{3.4}$$

$$F_{analog} = 1 + \frac{N_{LNA}}{G_{LNA}N_{in}} + \frac{N_{mixer}}{G_{LNA}G_{mixer}N_{in}} + \frac{N_{filter}}{G_{filter}G_{LNA}G_{mixer}N_{in}} + \frac{P_{int}PN_{osc}B}{N_{in}} \tag{3.5}$$

from (3.4) and (3.4)

$$F_{analog} = F_{chain} + F_{osc} \tag{3.6}$$

where

$$F_{osc} = \frac{P_{int}PN_{osc}B}{N_{in}} \tag{3.7}$$

and

$$F_{chain} = 1 + \frac{N_{LNA}}{G_{LNA}N_{in}} + \frac{N_{mix}}{G_{LNA}G_{mix}N_{in}} + \frac{N_{filt}}{G_{filt}G_{LNA}G_{mix}N_{in}} \tag{3.8}$$

So the noise due to local oscillator phase noise appears as the term F_{osc} in the noise factor of the receiver. This term is independent of the gain of the mixer and the stages before it. This is intuitively satisfying because the SNR degradation due to reciprocal self mixing is dependent on the ratio of the interferer power to the signal power which remains the same independent of the gain preceding the mixer.

3.3.2 Power model of the receiver

The power consumption of the analog front end can be written as

$$P_{analog} = P_{chain} + P_{osc} \tag{3.9}$$

where P_{chain} is the total power consumption of the blocks along the signal path(LNA, Mixer, Filter),henceforth referred to as the chain and P_{osc} is the power consumption of the local oscillator.To solve the optimization problem we need analytical expressions for P_{chain} and P_{osc}. To get the expression for P_{chain}, we use the power models developed in [7]. The power of an analog block is modelled to be proportional to its Dynamic Range(DR).

$$P_i = P_{Ci}\frac{V_{IIP3}^2}{V_{ni}^2} = P_{Ci}DR \tag{3.10}$$

where, V_{ni} is the input referred noise voltage (equivalent to Noise figure) of the block and V_{IP3} is the signal amplitude for input power equal to the IIP3(Input referred Third order Intermodulation product) of the block and P_{Ci} is the power coefficient of the analog block, a measure of the power hungriness of the circuit topology [7].Using this model, the authors in [7] derive the optimal power consumption for the LNA,mixer and filter(which is same as P_{chain} as per our definition) as a function of the noise and linearity specifications of the front end as follows

$$P_{chain} = \frac{V_{IIP3,tot}^2}{(F_{chain}-1)kTR_s}(P_{Clna}^{1/3} + P_{Cmixer}^{1/3} + P_{Cfilter}^{1/3})^3 \tag{3.11}$$

if $F_{chain} \gg 1$ then

$$P_{chain} = \frac{K_{chain}}{F_{chain}} \tag{3.12}$$

where

$$K_{chain} = \frac{V_{IIP3,tot}^2}{kTR_s}(P_{Clna}^{1/3} + P_{Cmixer}^{1/3} + P_{Cfilter}^{1/3})^3 \tag{3.13}$$

Next we proceed to develop an analytical expression for P_{osc}. The SSB Phase Noise

due to thermal noise in a ring oscillator is given by [17]

$$L(f) = \frac{2kT}{I}\{\frac{\gamma_N + \gamma_P}{V_{DD} - V_t} + \frac{1}{V_{DD}}\} \left(\frac{f_0}{f} \right)^2 \tag{3.14}$$

where I is the average current flowing through the ring oscillator if $V_{DD} \gg V_T$ then the Phase Noise of the oscillator at a given frequency offset is given by

$$PN_{osc} \propto \frac{1}{VDD.I} = \frac{\lambda}{P_{osc}} \tag{3.15}$$

where λ is the power coefficient for the oscillator. From equation (3.15) and (3.7) one can write

$$P_{osc} = \frac{K_{osc}}{F_{osc}} \tag{3.16}$$

$$K_{osc} = \frac{\lambda P_{int} B}{N_{in}} \tag{3.17}$$

Though the expression is given only for a ring oscillator, the same power-phase noise trade off is shown by LC Oscillators also.

3.3.3 Power optimization of the analog front end

Now for a given F_{analog} we can optimize P_{analog}. from (3.6) (3.9) (3.12) (3.16) we get

$$P_{analog} = \frac{K_{chain}}{F_{analog} - F_{osc}} + \frac{K_{osc}}{F_{osc}} \tag{3.18}$$

Differentiating with respect to F_{osc} and equating to zero we get

$$F_{osc} = F_{chain}\sqrt{\frac{K_{osc}}{K_{chain}}} \tag{3.19}$$

from (3.6) (3.7) and (3.19), Optimal phase noise of the oscillator is given by

$$PN_{opt} = \frac{F_{analog}\sqrt{\frac{K_{osc}}{K_{osc}+K_{chain}}}N_{in}}{P_{int}B} \tag{3.20}$$

and the optimal power consumption of the receiver is given by

$$P_{analog,opt} = \frac{(\sqrt{K_{chain}} + \sqrt{K_{osc}})^2}{F_{analog}} \tag{3.21}$$

It can be seen that the optimal power of the analog section is inversely proportional to the Noise factor required from the analog front end. The interference specification affect the power of the analog section in two ways.Since K_{osc} is a directly proportional to the interferer power, higher interference specifications increases the optimal power consumption of the receiver. Also, the IIP3 specification may depend on the interferer level making K_{chain} , a function of P_{int}. It can also be proved that as the interference increases the fraction of the oscillator power in the power consumption of the analog front end increases.

Using the result of the above optimization one can estimate the optimal power consumption of the analog front end, by just knowing the power coefficients of the LNA, Mixer, filter and oscillator. Estimation of these coefficients is described in the next sub-section.

3.3.4 Estimation of power coefficients

Estimation of power coefficients is done through preliminary simulations of the circuit topologies used.These simulations need not be very accurate and rigorous because the optimal specifications are highly insensitive to the errors in the power coefficients.[7]. This is necessary, as this kind of power estimation/optimization is done at the early stages of the design cycle when the circuit blocks would not have been completely designed/simulated.

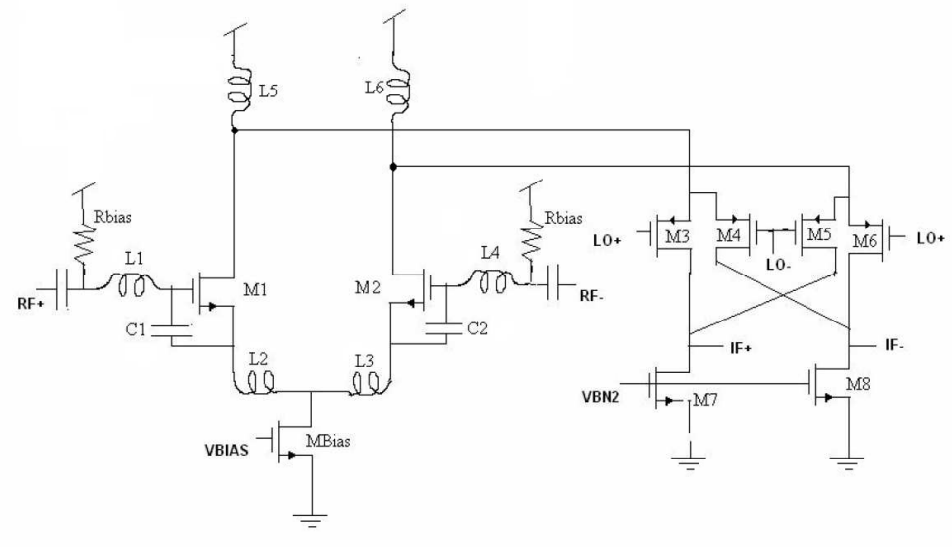


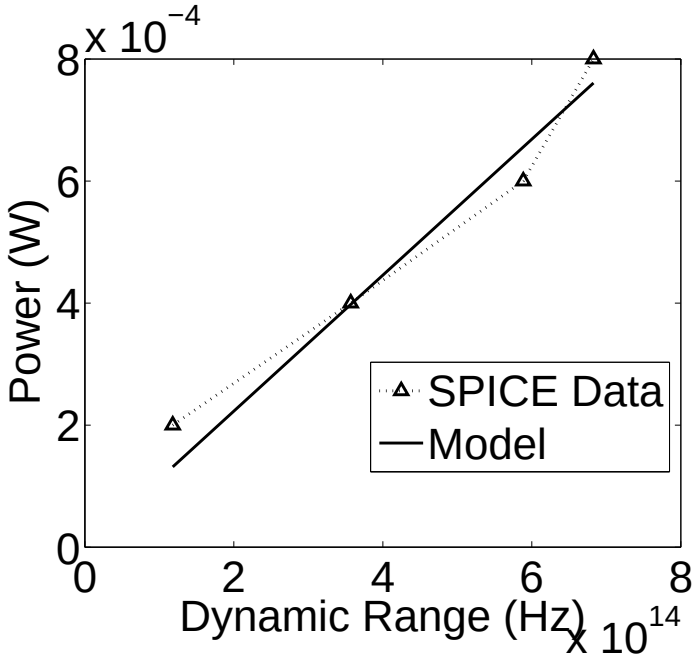
Figure 3.5: Merged LNA-Mixer topology designed for the ZigBee receiver

Variable	Value(J)
0.13um UMC Process	
P_{clnam}	1.13e-18
$P_{cfilter}$	1.43e-17
λ	7.29e-14

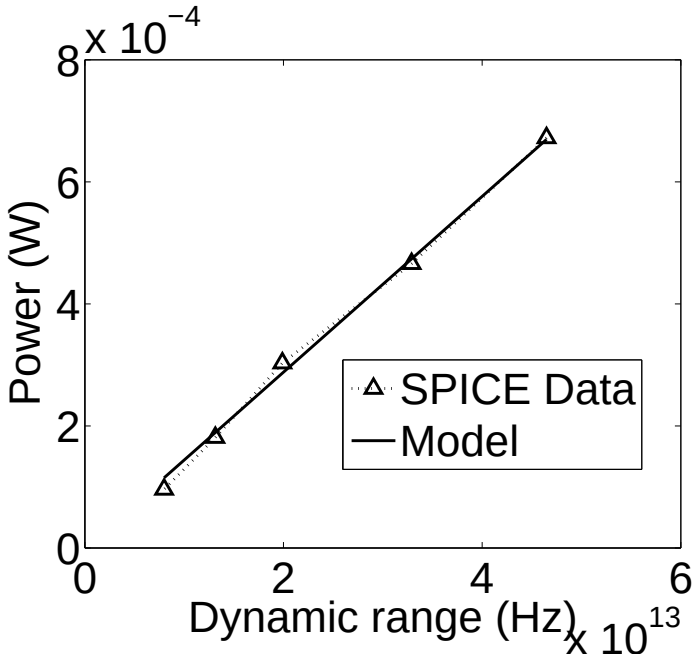
Table 3.2: Estimated Power Coefficients of different analog blocks

In the receiver design example taken, we use a folded cascode merged LNA-mixer circuit in the front end Merging the LNA and mixer helps in reducing the power consumption and the folded structure helps to achieve operations at a low supply voltage. To obtain the power coefficient of the merged LNA-Mixer (P_{Clnam}), we find the dynamic range(DR) of the circuit for different bias currents. For each value of bias current, noise figure and the IIP3 of the LNA-Mixer is measured by simulation, from which DR is computed. Cadence Spectre-RF tool is used for simulations.The plot of power vs DR for the merged LNA-Mixer(LNAM) is shown in Fig.3.6(a).The slope of the straight line approximation of points on the plot gives P_{Clnam}.

Fig.3.6(b) shows the power vs dynamic range of a second order complex bandpass Gm-C filter,[18] used as the channel select filter of the receiver. Power coefficient of filter ($P_{Cfilter}$) is computed in the same procedure used for LNA-Mixer. While



(a) LNA-Mixer



(b) Filter

Figure 3.6: Power Vs DR plots for P_{Ci} calculation.

varying bias current of the filter for obtaining $P_{Cfilter}$, the cut-off frequencies of the filter are kept constant by varying capacitors of the filter, hence preserving the filter characteristics.The filter used gives an attenuation of 26dB for the adjacent channel and 53.4dB for the alternate channel.Strictly speaking the power coefficient of the oscillator, λ should also be obtained from a power Vs Phase Noise plot of the oscillator, obtained through simulations. However in this work we have extracted λ from a single data point only[19].

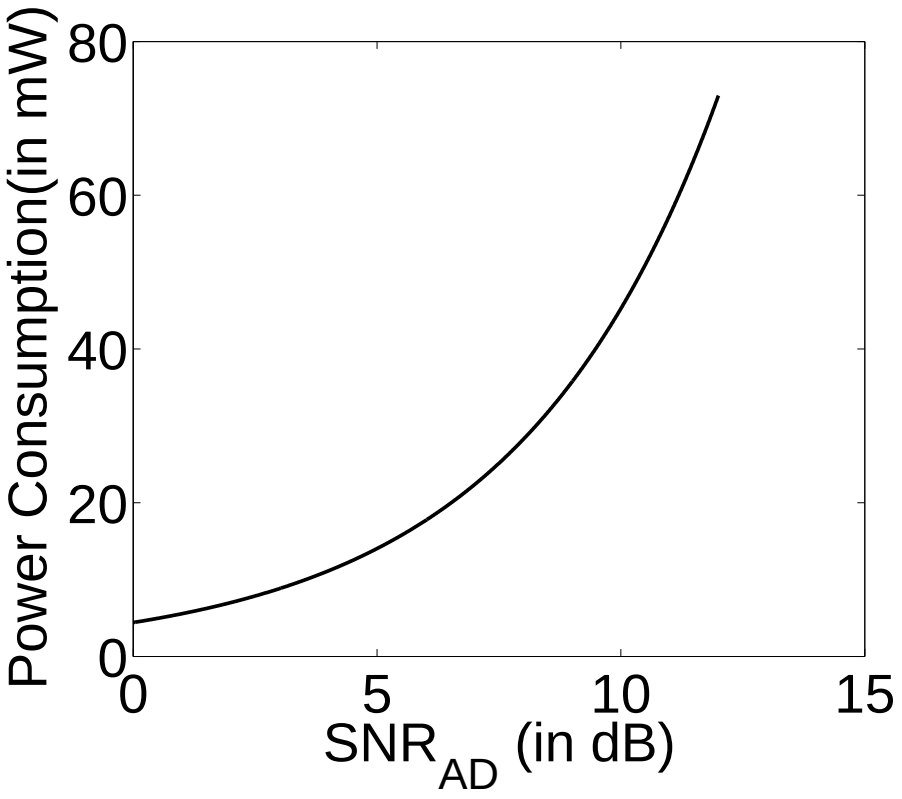


Figure 3.7: Estimated Power of the analog section vs SNR$_{AD}$of the ZigBee Receiver

Knowing the power coefficient values (refer Table.3.2), we proceed to estimate the power of the analog section of the receiver as a function of SNR_{AD}. For every value of SNR$_{AD}$, Noise figure specification is computed using Equation (3.1).The IIP3 specification is fixed at -10 dBm. Knowing the power coefficients of all subblocks, K_{osc} and K_{chain} are computed using equations (3.16) and (3.13). Then F_{osc} and F_{chain} and subsequently the optimal power-noise budgets of all the sub-blocks can be

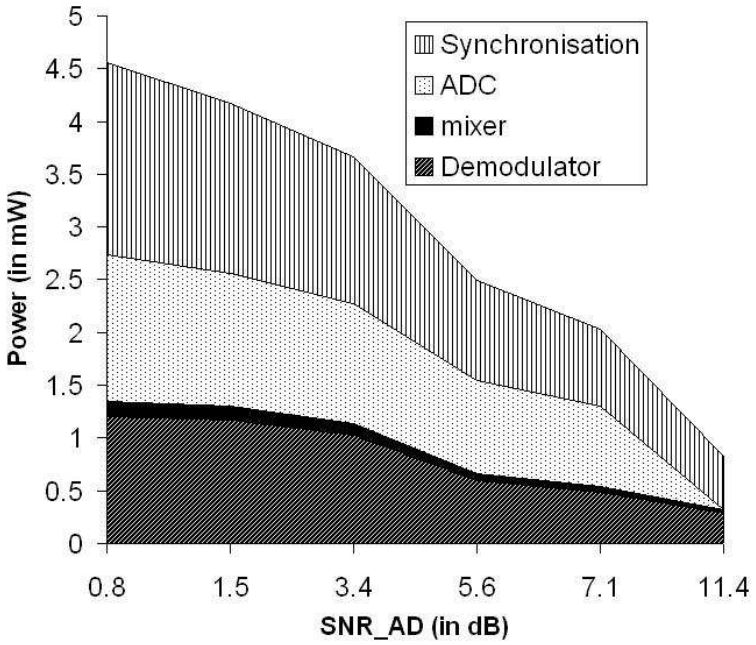


Figure 3.8: Power vs SNR_{AD} for 8-bit resolution of signals to the digital section

found. The power of the analog front end is then estimated by summing up the power consumption of all the blocks. Fig.3.7 shows the estimated power consumption of the analog section of the 802.15.4 receiver. vs SNR_{AD}.

3.4 Power estimation of digital section

Power consumption of the digital section is estimated from the Verilog HDL description of the digital blocks. The gate level netlist is synthesized using Synopsys Design Compiler tool and then power is estimated using Synopsys Prime Power. The Faraday cell library for the UMC 0.13um technology has been used for these simulations.

From Fig.3.2, for a given SNR_{AD},the operating frequency of the digital section is found for different sets of signal resolutions. The power consumption of the digital section is a function of the signal resolutions and the operating frequency and is estimated as described below.

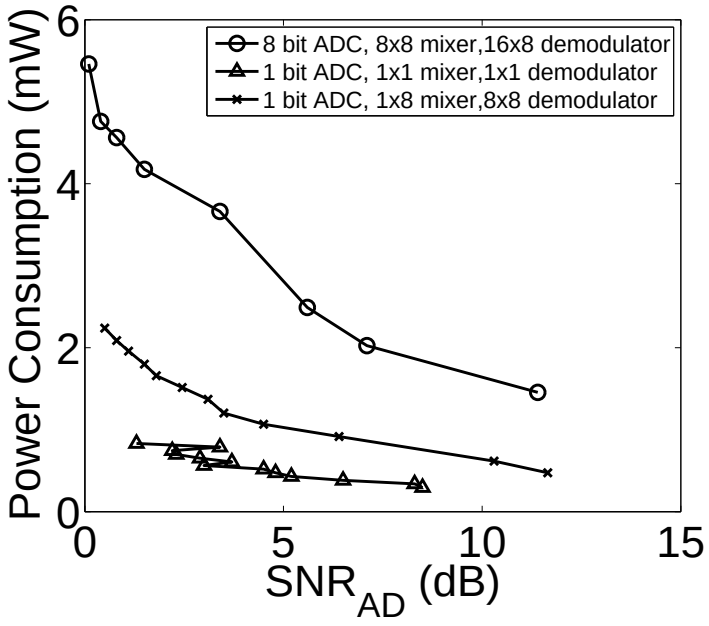


Figure 3.9: Estimated Power of the digital section vs $\text{SNR}_{AD}$of the ZigBee Receiver

3.4.1 ADC power estimation

Power consumption of Nyquist ADC can be estimated from the following expression [20]:

$$P = \frac{V_{dd}^2 L_{min}(F_{sample} + F_{signal})}{10^{(4.838-0.1525\times ENOB)}} \tag{3.22}$$

Where, V_{dd} is the power supply, L_{min} is the minimum channel length of the process used, F_{sample} is the sampling frequency of the ADC, F_{signal} is the input signal frequency, $ENOB$ is effective number of bits of ADC . For power estimation we have $V_{dd} = 1.2V$, $L_{min} = 0.13\mu m$, F_{signal} is 3 MHz and F_{sample} varies from 2 to 18 MHz and $ENOB$ varies from 1 to 8 bits.

3.4.2 Downconverter and Demodulator

Downconverter is a complex mixer(refer Fig.3.3a) which mixes the incoming IF signal with IF carriers.Complex mixer consists of four multipliers and two adders. Different structure of multipliers is considered for different resolutions of the signals. For 1bit

resolution , the multiplier reduces to an Ex-or, where as for higher resolutions, we use a carry save tree based signed multiplier. The IF carriers are generated using CORDIC algorithm[21]. Each arm of the demodulator consists of a signed tree multiplier followed by a carry save accumulator. Decision on the transmitted symbol is made by a four level tree comparator, which finds the maximum among outputs of the sixteen correlations.

3.4.3 Synchronization Units

Synchronization blocks perform symbol timing recovery, frequency error correction and phase recovery. Power dissipation and performance of synchronization units in receiver section does depend on the resolution of signals considered. Timing recovery blocks for acquisition and tracking are shown in Fig.3.3c. Acquisition is coarse timing recovery and Tracking is fine timing recovery [22]. The acquisition block as shown in the Fig.3.3c computes the metric Y_{acq} for each timing hypothesis and if it exceeds β then the current hypothesis is passed to the tracking block. Y_{acq} and β depends on ADC resolution for a given Probability of detection, P_D. To pass all possible correct hypothesis the β is chosen as:$\beta = \min_{delay}\ (\ |x_I| + |x_Q(t - T_c)|\ )^2$. Equation removed added in above matter

$$\beta = \min_{delay}\ (\ |x_I| + |x_Q(t - T_c)|\ )^2 \tag{3.23}$$

Frequency/phase error estimation is a data-aided estimation [23]. Fig.3.3b shows the structure used as frequency error detector [24]. Ω is the estimated frequency error which is further used to correct the frequency error. Acquisition block consists of a non-coherent correlator and operates at 2 MHz [22], Whereas, tracking and frequency/phase error estimators operate at sampling frequency same as of ADC. Tracking block is a non-coherent delay-lock-loop [22]. Power consumption of the synchronizer is estimated by summing up the power of the basic building blocks like

the adders, multipliers etc. and gives an upper upper bound to the actual power consumption.

3.4.4 Total Power of digital section

Total power of the digital section is given as

$$\mathrm{P}_{digital} = 2 \times P_{ADC} + P_{mixer} + P_{demod} + P_{synch} \tag{3.24}$$

$P_{digital}$ vs SNR_{AD} is shown in Fig.3.9 for different values of resolutions. From Fig.3.2 we see that, for a given SNR_{AD} lower resolution setup needs to run at higher frequency than higher resolution setup. However, lesser resolution setup has lesser switching capacitance. Decrease in power due to lesser switching capacitance overcomes the increase in power due to higher frequency of operation. Thereby, resulting in overall power reduction. Also we had noted that synchronization is the most power consuming block in the digital section accounting for 15-20% of the total power as reported in [24].

3.5 Total receiver power vs SNR_{AD}

Fig. 3.10 shows power consumption of the total receiver and power consumption in analog and digital sections for varying SNR_{AD} for 8-bit resolution of the signals to the digital section. The trends for analog and digital power is as observed previously. We can observe an optimum value of SNR_{AD}, denoted as SNR_{AD}^{opt}, at which P_{total} is minimum. In this case,SNR_{AD}^{opt} is 0.4 dB and the corresponding P_{total} is approximately 9 mW. For SNR_{AD} lesser than SNR_{AD}^{opt}, the digital section's power consumption is more prominent. Whereas, above SNR_{AD}^{opt} analog power dominates the total power consumption. At SNR_{AD}^{opt}, analog power constitutes 50% of the total power and digital the rest 50%. Fig. 3.11 shows the P_{total} for different set of resolutions. We see that

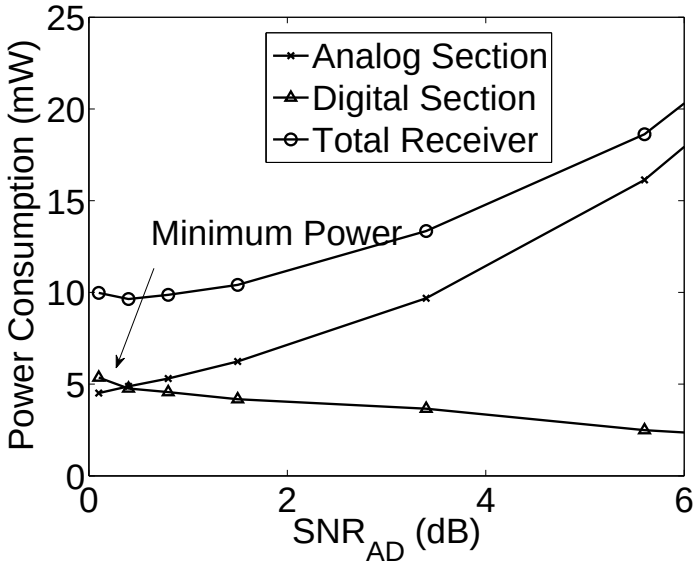


Figure 3.10: Power vs SNR_{AD} of the whole receiver for 8 bit resolutions

the high resolution case consumes more power than cases with low resolution, even though it operates at a lower frequency. As discussed before, there exists an optimum for the 8-bit case. Whereas, for other two cases power is minimized for the lowest possible SNR_{AD} for which performance is met. The least power consumption of 7 mW is achieved in 1-bit resolution case at SNR_{AD}^{opt} of 1.3 dB. We can also observe that the optimal power is almost the same for both the cases which use 1-bit ADC. Thus the extra resolution for the local oscillator and the demodulator does not have significant effect on the total power, indicating that the ADC resolution is of more significance for the optimization.

3.6 Conclusions

Existing practice in radio receiver design, allocates most of the noise budget to the analog front end. Consequently both the analog front end and the digital back end are overdesigned in terms of power. For ultra low power applications, one can judiciously apportion the noise budget amongst the two sections and achieve optimal power

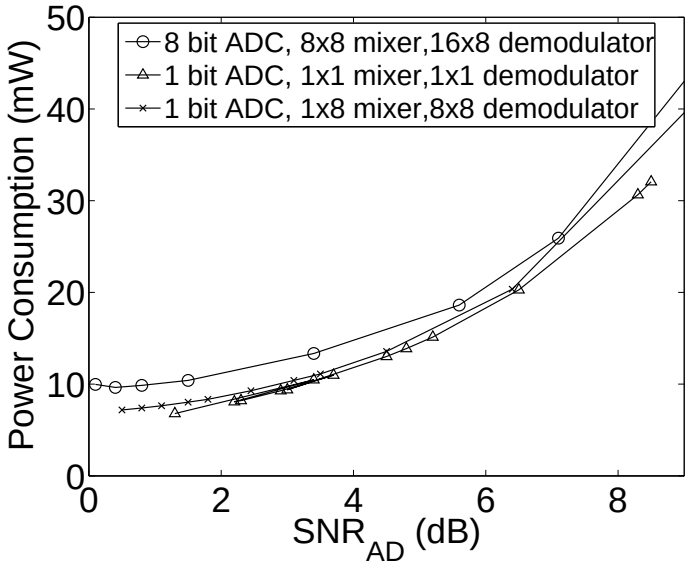


Figure 3.11: Total Power vs SNR_{AD} for different resolutions of signals to the digital section

consumption.

We show how such an optimization can be performed, by first obtaining the relationship of the SNR at the analog-digital interface, SNR_{AD}, to the digital section's resolution and operating frequency. SNR_{AD} in turn imposes a certain power dissipation of the analog front end. Using power models for the analog front end, along with power estimation of the digital backend, we can solve for the optimal SNR at the analog-digital interface, which minimizes the overall power dissipation of the receiver. For the example case of a Low-IF receiver in a 1.2V 0.13um process, we find that the lowest power is obtained for a SNR_{AD}^{opt} of 1.3dB with 1-bit digital section, consuming an overall power of 7mW. We also find that the ADC resolution has the most impact for the overall power dissipation, as compared to the resolution of the local oscillator and the demodulator.

Chapter 4

A low voltage LNA-Mixer for an adaptive ZigBee receiver

4.1 Introduction

With the advent of applications such as mobile systems and sensor networks, low power wireless receivers have become the need of the hour. Energy scalable systems which cranks down their power at lower performance modes are known to yield significant power savings.The design of several energy scalable digital systems have been discussed in [25].Extending the idea to wireless systems is natural and a few attempts have been made in the past. An energy scalable OFDM wireless transmitter is discussed in [26]. On the receiver side, [27] and [28] discuss system level architectures to control the power consumption of LNA, Mixer and Local oscillator while keeping the signal fidelity acceptable. In another work by Kim et. al.[29] a feedback mechanism to control the purity of the local oscillator based on the received interference strength is discussed. The authors in [30] discusses a energy scalable OFDM receiver in which the power of the RF front end is cranked down based on the measurement of Error Vector Magnitude(EVM). Though adaptive receivers have become an active research topic, the problem of circuit design for adaptive receivers has not been sufficiently

explored in the literature. Authors of a recent work [31], has explored the design of an oscillator for adaptive receivers.In [29], the authors propose a novel reconfigurable VCO architecture based on the LC-ring structure.In this thesis we try to address the problem of front end (LNA-Mixer) design for adaptive receivers.In this chapter, we discuss an adaptive front-end topology for an 802.15.4 ZigBee receiver.

First we derive the performance specifications required by an adaptive ZigBee receiver as a function of the channel conditions.From the receiver specifications, we derive the optimal specifications for the front end, using the power optimal design methodology discussed in chapter 3. The obtained specifications show that the front end needs independent tunability of Noise and linearity metrics. In existing literature one can find several variable gain LNAs which can potentially be converted to adaptive LNAs. The approaches to build variable gain LNA can be broadly classified into 2 types ,Bias voltage/current control of input/cascode transistors[32],Changing the strength of a feedback/feed forward path[33][34] [35]. The variable gain LNA-Mixers in these works have a single tuning knobs to vary the Gain/Noise Figure for different input signal power. However an adaptive receiver requires a front end in which Noise figure and linearity has to be set independently of one another(shown in section II), hence the need for two control knobs. The topology presented in a recent work [36] provides two such tuning knobs . In this circuit part of the signal current is dumped to a dumping path achieving high linearity while maintaining low gain/Noise figure. Wasting part of the signal current to trade-off noise figure for linearity does not look appealing. In this chapter, we propose a topology in which the effective width of the input transistor and the bias current are used as two independent tuning knobs, allowing the setting of Noise Figure and IIP3 independent of each other.

4.2 Adaptive Receiver and its Specifications

Traditionally wireless receivers are designed assuming worst case conditions ie the minimum signal strength is used for arriving at the Noise figure specification while the maximum signal/interferer level is used to arrive at the linearity specification. Thereby the dynamic range of the receiver designed, is very large because of the huge dynamic range of the input signal. However in a practical case at most times the channel may be good in the sense,signal level can be higher than the minimum specified level and interferer level less than its maximum specified level. Under such cases the receiver performance can be relaxed to the extent that just meets the required BER,thus saving power. So if we can design an intelligent receiver which measures the signal and interferer power levels and adapts its performance (while meeting the BER), based on these measurements, significant savings in power can be achieved. We call such a receiver as an adaptive receiver

Noise figure,IIP3,Gain are three important specifications of an RF receiver. For an adaptive receiver these specifications are not fixed but dynamically vary as a function of the received signal and interference strengths. In the next sub-section we derive these parameters as a function of signal and interferer levels.

4.2.1 Specifications of an adaptive Receiver as a function of Channel conditions

If SNR_{min} is the minimum required SNR at the output of the receiver to meet the BER specification, the Noise Figure can be derived as follows

$$NF = \frac{SNR_{in}}{SNR_{out}} \tag{4.1}$$

$$NF = P_{in} - 10log(kTB) - SNR_{min} - design\ margins \tag{4.2}$$

where B is channel Bandwidth of the receiver P_{in} is the received input signal power. It should be noted that a conventional receiver uses $P_{in,min}$, minimum specified input signal level whereas the adaptive receiver Noise figure equation uses P_{in}, the received input signal level . The IIP3 specification of the receiver is derived as follows. Given a signal level P_{in} and interferer level $P_{interferer}$, a two tone test with the power level level of the two tones equal to $max(P_{interferer},P_{in})$ is assumed. The IIP3 is set to make the third order IM products below the noise floor of the system[13].

$$P_{two-tone} = max(P_{interferer}, P_{in}) \tag{4.3}$$

$$IIP3 > \frac{3P_{two-tone} - P_{in} + SNR_{min} + margins}{2} \tag{4.4}$$

The 1 dB compression point of the system should be sufficient enough to avoid gain saturation effects. The 1 dB compression point is set as

$$P_{1dB} = max(P_{interferer}, P_{in}) \tag{4.5}$$

The more stringent condition of (4.4) and (4.5) should be used to set the linearity of the system. The voltage gain of the system should be sufficient enough to produce a full scale at the ADC.

$$A_v = \frac{V_{fullscale}}{V_{in}} \tag{4.6}$$

where V_{in} is the amplitude level corresponding to P_{in} in a 50Ω resistor.

Fig.4.1 shows the calculated specifications for an adaptive Low IF super heterodyne receiver for an 802.15.4 ZigBee standard.It can be seen that IIP3 curve shows two distinct region which we call as signal dominant region and the interference dominant region. In the interference dominant region the interference dominates the linearity specification. In this region as the signal level increases the acceptable noise floor of the adaptive receiver also increases thus the IIP3 specification gets relaxed. However

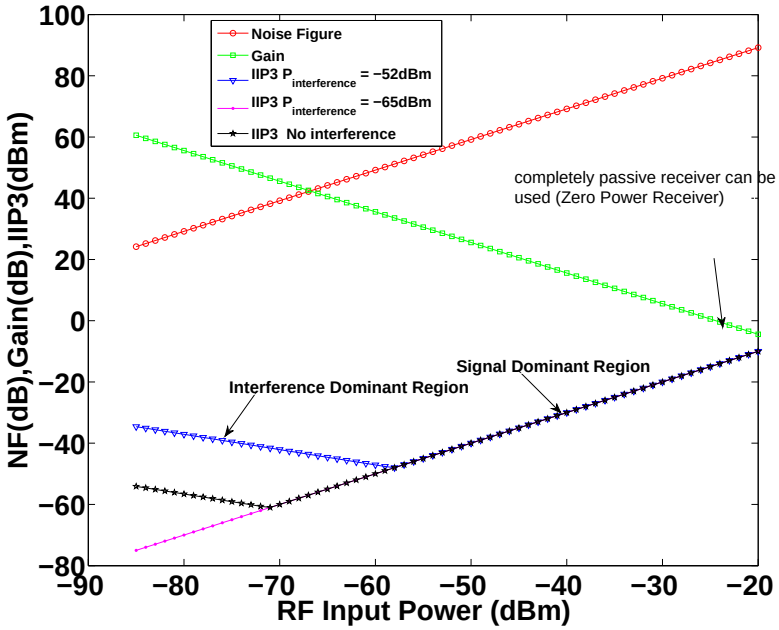


Figure 4.1: Specifications of an Adaptive receiver for ZigBee

in the signal dominant region the as the signal dominates the linearity, higher signal amplitude implies a higher linearity requirement. Hence IIP3 increases with increasing signal power. Also it should be noted that at high signal levels the gain required becomes negative (in dB). In this region a completely passive receiver can be used resulting in zero power dissipation.

4.2.2 Specifications of the sub-blocks of the adaptive receiver

The sub-blocks of a Low-IF super heterodyne receiver are the LNA,Mixer,Channel Select Filter and the local oscillator. Across channel conditions the receiver requires different NF and IIP3. The next natural question that has to be answered is how should the specifications of the various sub-blocks of the receiver vary? Authors in [7] provide a way to arrive at the optimal allocation of the specifications of the sub-blocks of the receiver. This work has been extended by including the local oscillator in the optimization by the us in [37] and the same methodology was discussed in the previos

chapter. Given a Noise Figure and IIP3 specification of a receiver the optimal specifications of the sub-blocks of the receiver which minimizes the power consumption can be found using these methodologies. However one should be careful in applying the procedure in [7] for an adaptive receiver. The power model in [7] assume saturation region operation of transistors and may not hold good for low dynamic range systems. However the authors show that the optimal set of specification derived using these models are highly insensitive to the errors in the model. So we can find the specifications of all the sub-blocks of the adaptive receiver for different channel conditions. Once the circuit topologies of the different sub-blocks are fixed one can find the power coefficients through simple simulations. Knowing the power coefficients one can find the optimal specification of all the blocks for various channel conditions. Though the power coefficients may not remain constant across different values of Dynamic ranges, the error in the optimal specifications will be acceptable as explained before. The optimal NF and IIP3 specifications of a merged LNA-Mixer,Channel select filter and the Phase Noise specifications of the local oscillator are given in figures (4.2 and 4.3). It can be seen that Optimal specifications of the LNA-Mixer look very similar to that of the receiver itself. Being the first stage on the receiver it demands more tunability. Since the gain of the LNAM tracks the variation in the signal level, input signal at the filter has a lesser dynamic range than the system dynamic range. Hence the noise figure of the filter remains constant throughout the range. (Though in a practical case the LNAM may not provide such high a tunability and the Filter required must also be tunable). Also the rejection characteristics of the filter can be relaxed at lower interference levels.Following the derivations from [37] it can be shown that at the optimal allocation of specifications the ratio $P_{lnam} : P_{filter} : P_{local-oscillator}$ will be constant for all channel conditions.

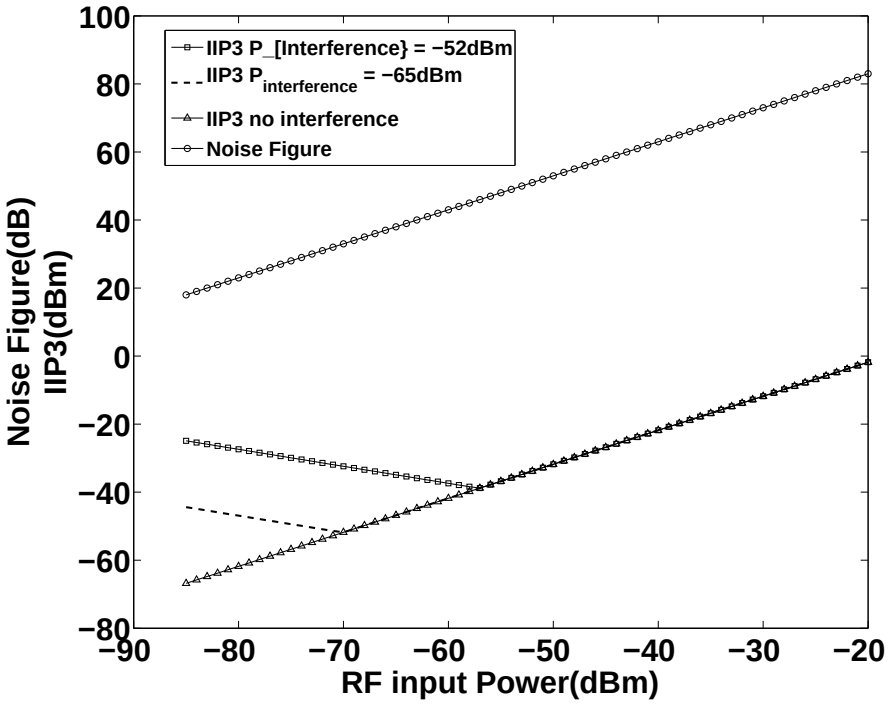
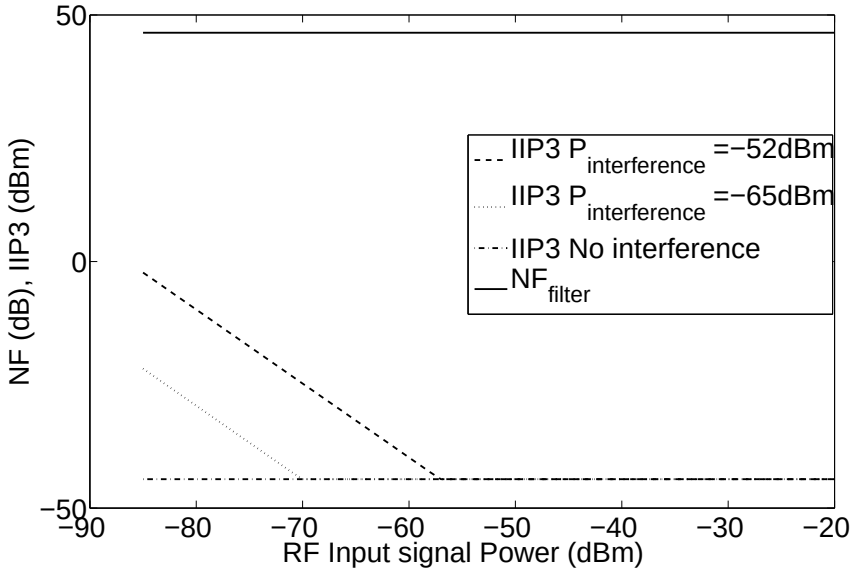


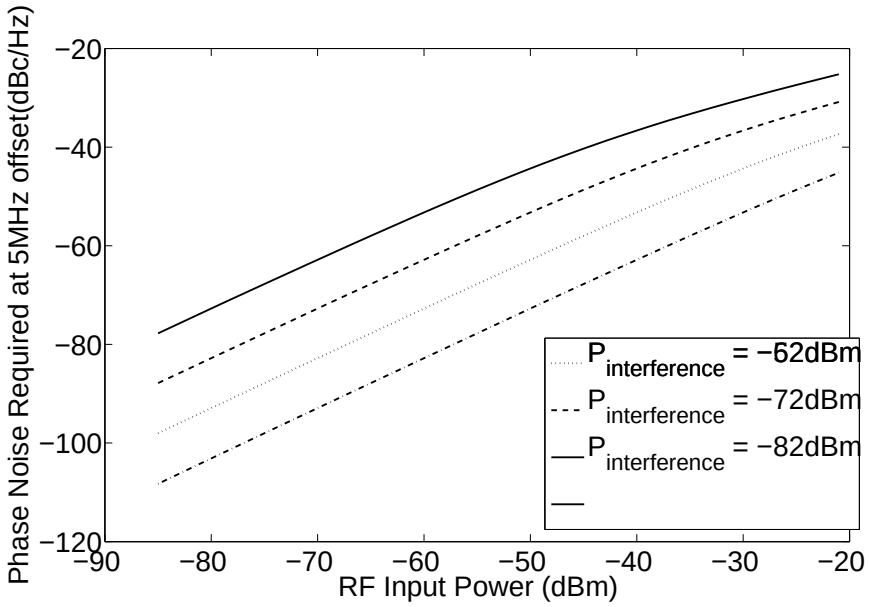
Figure 4.2: Characteristics of an merged LNA-Mixer for an adaptive ZigBee Receiver

4.2.3 Design considerations for the adaptive front end

The design challenges of an adaptive front end differs significantly from that of its non-adaptive counter part. Power consumption, noise and linearity are the performance metrics to characterize the conventional non -adaptive front ends. Apart from these metrics, an adaptive front end also should show considerable tunability of individual performance metrics i.e one must be able to set the noise figure, input matching, Linearity, gain almost independently of each other if not completely independent. So the designer of an adaptive front ends must look for tuning knobs to set these metrics.In this thesis, we propose two front ends with tuning knobs to individually set the Noise figure and linearity and input matching.



(a) Characteristics of an channel select filter for an adaptive ZigBee Receiver



(b) Required Phase noise of the local oscillator

Figure 4.3: Specifications of filter and local oscillator as a function of channel conditions

4.2.4 Identification of tuning knobs

Lets us take a single transistor and look at its linearity and noise characteristics to identify the potential tuning knobs in a bigger circuit. Assuming the sub micron transistor current equation,

$$I = \frac{W}{2L}\frac{\mu C_{ox}}{1+\theta(V_{GS}-V_T}))(V_{GS}-V_T)^2 \tag{4.7}$$

one can derive the V_{IP3} (input voltage at which the output first order and third order components become equal) of the transistor as[7],

$$V^2_{IP3,tran} = \frac{16}{3}\frac{I}{g_m\theta} \propto \frac{\sqrt{I}}{\sqrt{W}} \tag{4.8}$$

The drain current noise due to the transistor can be written as

$$V^2_{ni,tran} = \frac{4kT\gamma g_m}{\alpha} \propto \sqrt{IW} \tag{4.9}$$

Rewriting the equations in terms of drain current and width of the transistor, we can see that the V^2_{IP3} and V^2_{ni} of the transistor can be fixed independently of each other, using current and width as the tuning knobs.Now we extend the same observation to design a merged LNA-Mixer in which width of the input transistor and the bias current can be used as tuning knobs to set the Noise figure and IIP3.

4.3 A Low-Voltage Merged LNA-Mixer for an adaptive ZigBee Receiver

4.3.1 Proposed LNA-Mixer

To achieve width tunability,We propose a Merged LNA-Mixer in which the input transconductor is segmented and the appropriate number of segments are switched

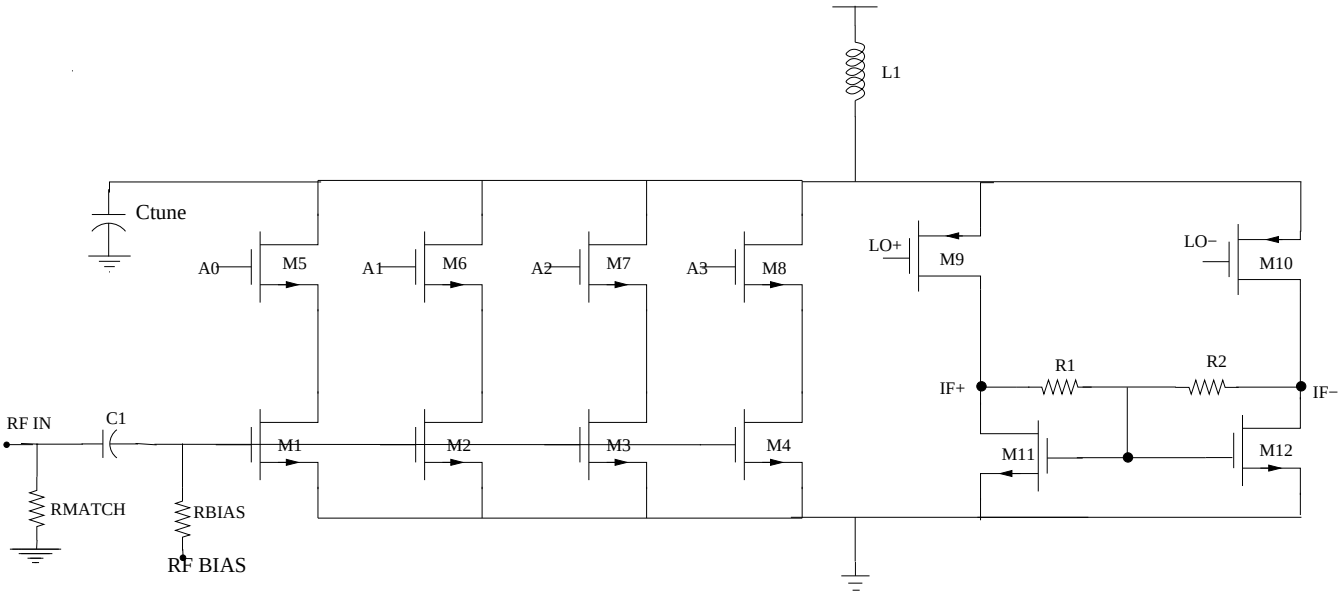


Figure 4.4: Proposed LNA-Mixer Circuit

according to the effective width required.Fig.4.4 shows the proposed circuit. The transistors M1-M4 are the segmented input transistors. The widths of M1-M4 increase gradually in a geometric fashion by a factor of 2.Transistor M5-M8 which normally act as the cascode transistors also serve the purpose of switches to control the width in this circuit. The sizes of the switches are also increase in a geometric fashion. An input digital control word ($A_3A_2A_1A_0$) controls the switches and hence fixes the effective width of the input transconductor. The effective width of the input transistor is the sum of widths of the switched ON segments. PMOS M9-M10 act as the LO transistors and M11 and M12 act as the load. The load transistors use Common mode feedback to fix the output common mode voltage. The current in the load branch is fixed by the LO transistor's bias voltage and the LO signal is capacitively coupled into the circuit. The current in the input branch is determined by the bias of the input transistors and the RF input signal is capacitively coupled to the circuit.Table 4.3.1 gives the component values used in the design.

The circuit provides two tuning knobs to vary the performance the LNA-Mixer.The

Component Name	Value
M1-M4	L=0.3u W = 7.52u,14.4u,28.8u,57.6u respectively
M5-M8	L=0.12u W = 10u,20u,40u,80u respectively
M9-M10	L=0.3u W =36u
M11-M12	L=2u W =12u
L1	10.37nH
Rmatch	50Ω
Rbias	600Ω
C1	2.5pF
R1-R2	20KΩ
Ctune	100fF

Table 4.1: Component Values used

current in the input branch, I_{bias} and the effective width, W_{eff} of the input transistors. If we assume that the Noise Figure and IIP3 of the circuit is dominated by the input transistors [7] simplified equations for input referred Noise voltageV_{ni}^2 and $V_{iip3}^2$are given by

$$V_{ni}^2 \approx \frac{2\pi^2 kT\gamma}{g_m} \tag{4.10}$$

$$V_{iip3}^2 \approx \frac{16I}{3g_m\theta} \tag{4.11}$$

Assuming a square law model for transistors and replacing g_m with $\sqrt{2IW_eff}$ we see that using these two tuning knobs one can independently fix the Noise Figure and IIP3. Since the bias current has to be kept constant across all gain modes the bias circuit has to be designed accordingly. We can introduce a tail current source which determines the bias current. However this will increase the transistor stack and decrease the voltage headroom available preventing low-voltage operation. The next subsection describes the proposed bias circuit, which enables independent control of bias current irrespective of the effective transistor width.

4.3.2 Proposed Bias Circuit

Fig.4.5 shows the bias circuitry. Transistors MB1-MB4 form the usual current mirror transistors corresponding to each of the segmented LNAM input transistors. MB4-MB8 are the switches which determine the effective width of the segmented mirror

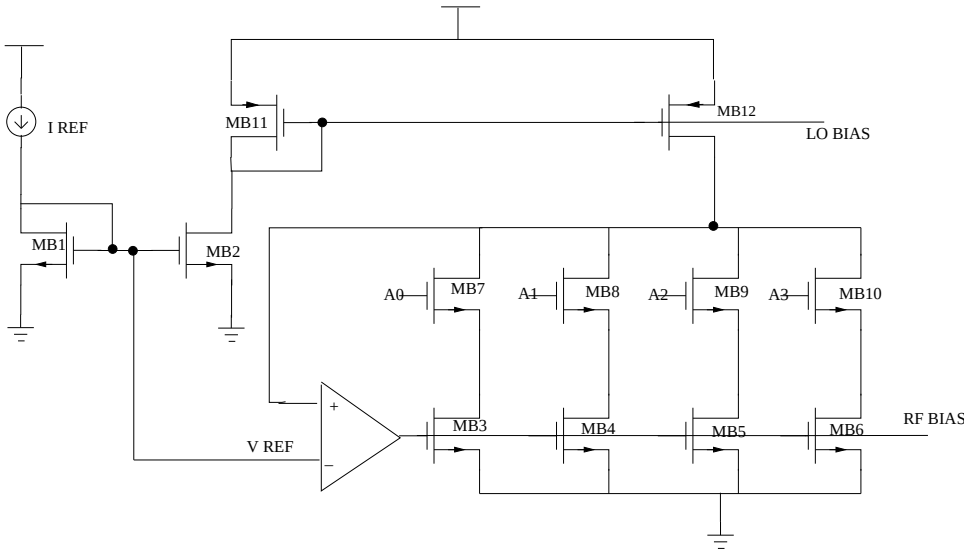


Figure 4.5: Proposed Bias Circuit

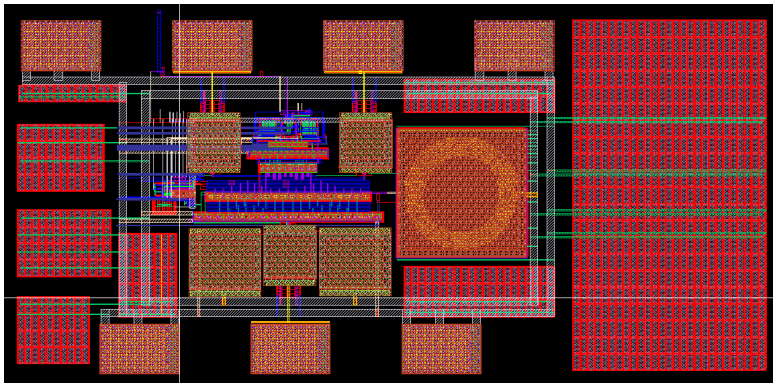


Figure 4.6: Layout snapshot of the Proposed Circuit

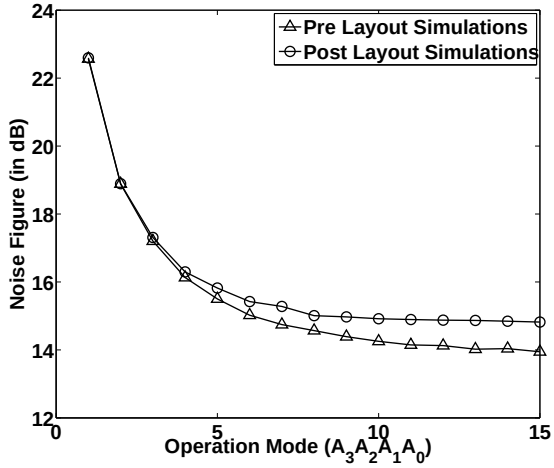
transistors. The digital control word which controls the LNAM mode also controls these switches. To reduce the variation in current in the bias circuitry across different modes , the variation in the voltage of node FB1 should be minimized thus avoiding any channel length modulation effect. A feedback loop as shown in is introduced to keep the VFB1 almost constant.

4.4 Simulated performance of the Proposed Circuit

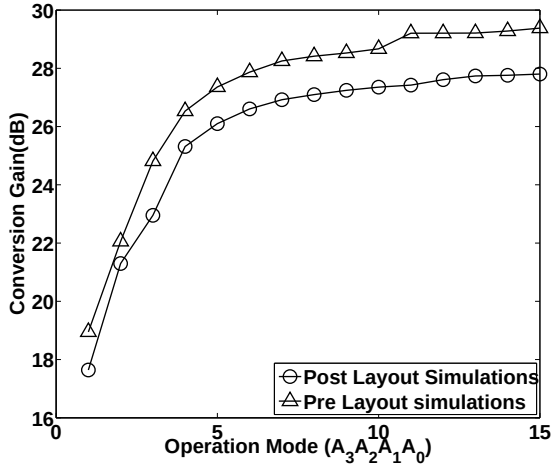
The proposed circuit was designed and its layout was drawn in UMC 0.13um Mixed-mode RFCMOS technology.The simulations were done using Cadence Spectre-RF tool.Layout of the circuit was also drawn and a test chip has been taped out. The details of the test chip are given in the next chapter. The simulated performance of the proposed circuit is given here.

4.4.1 Tunability of the proposed LNA-Mixer

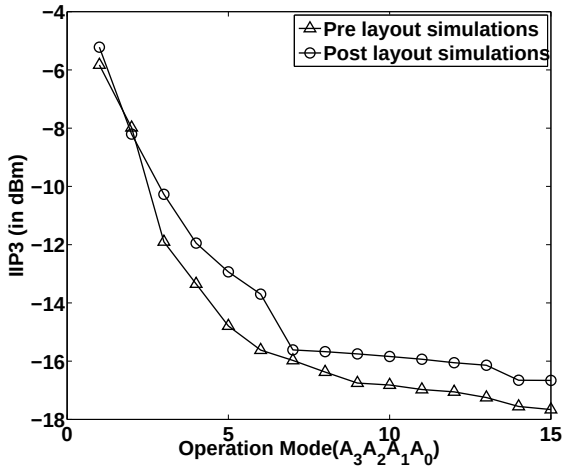
Fig.4.7 show the effect of tuning the effect width on the Noise Figure ,Gain and IIP3 of the system for a supply voltage of 1.2V and bias current of 700uA. The mode number is the decimal equivalent of the digital control word$A_3A_2A_1A_0$. As the effective width increases the gain increases and noise figure decreases while IIP3 decreases due to reduced overdrive of the input transistors. Thus by using this knob one can trade off noise figure for linearity. Fig.4.8 show the effect of bias current tuning on NF, Gain,IIP3 of the LNA-Mixer for a supply voltage of 0.8V for different modes. The Noise figure decreases and gain increases withe current consumption. But at the highest gain mode the IIP3 Vs current consumption shows a minima. This can be explained as follows. At high gain modes as the non-linearity due to the load transistors start dominating as output amplitude becomes high. So as current consumption is increased while the non-linearity due input transistors decrease, the non-linearity due to load transistors increase due to the increase in gain. This opposite trends yield a U shaped curve with a minima.



(a) Noise Figure

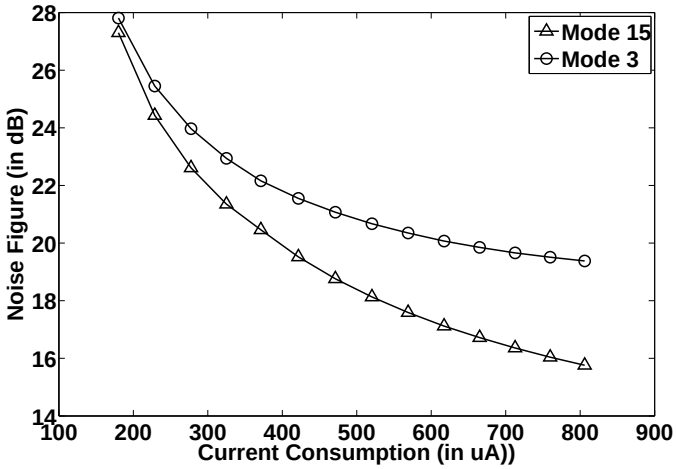


(b) Conversion Gain

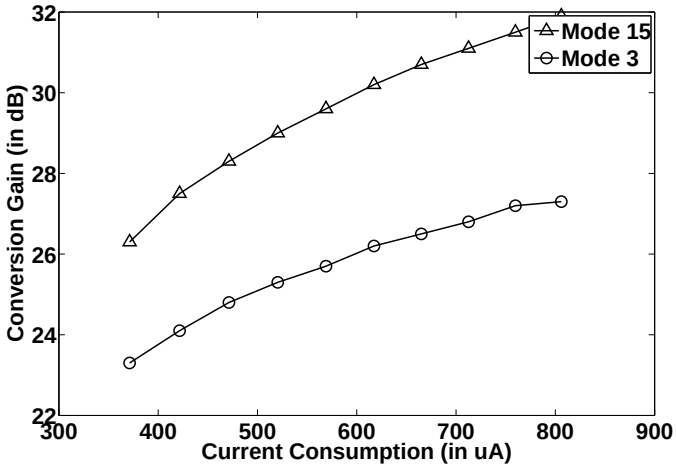


(c) IIP3

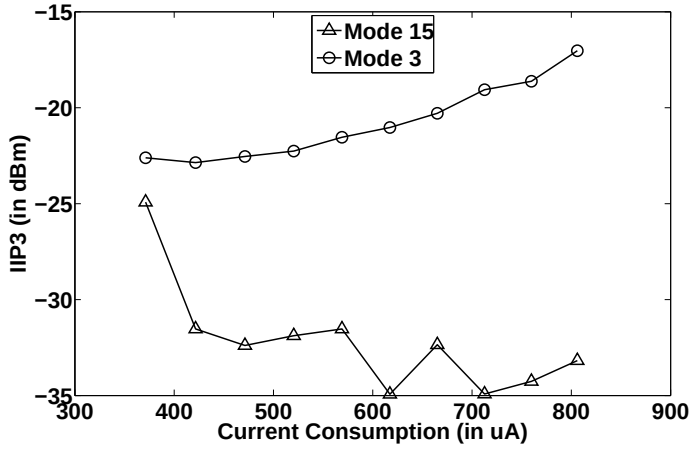
Figure 4.7: Simulated Performance of the proposed merged LNA-Mixer at I_{bias}=700uA and V_{dd} =1.2V



(a) Noise Figure Vs current consumption with $V_{dd} = 0.8$V



(b) Conversion across Vs current consumption with $V_{dd} = 0.8$V



(c) IIP3 Vs current consumption with $V_{dd} = 0.8$V

Figure 4.8: Simulated Performance of the proposed merged LNA-Mixer at $V_{dd} = 0.8$V

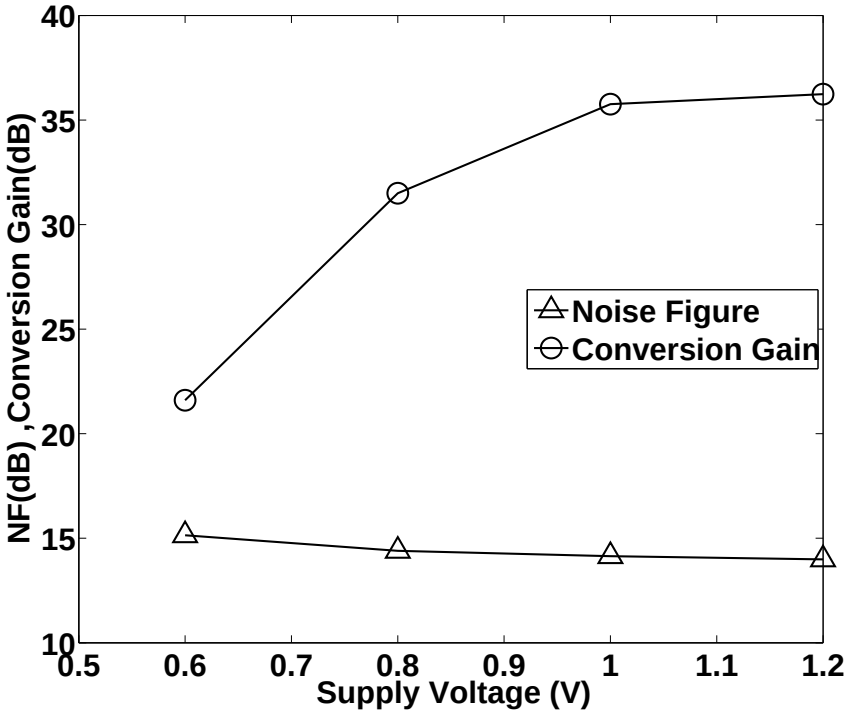


Figure 4.9: Voltage Scalability of the design

4.4.2 Voltage Scalability of the proposed merged LNA-Mixer

The proposed circuit has only two transistors in the stack and hence allow very low voltage operation the Fig4.9 shows the voltage scalability of the structure. The current through the circuit was kept constant while the supply voltage was varied. The Noise figure degrades only by a 1.5dBs.The gain reduces rapidly around 0.6V, because the transistors start operating very close to the linear region.

4.4.3 Power savings of the adaptive LNA-Mixer

To demonstrate the suitability of the proposed circuit for an adaptive receiver let us assume two cases. In the first case the input signal level remains constant and the interferer power varies. Now from Fig.4.2 we see that Noise figure must remain constant while the IIP3 has to be reduced with interference power. The LNA-Mixer was simulated across different modes and bias currents and the minimum power setup

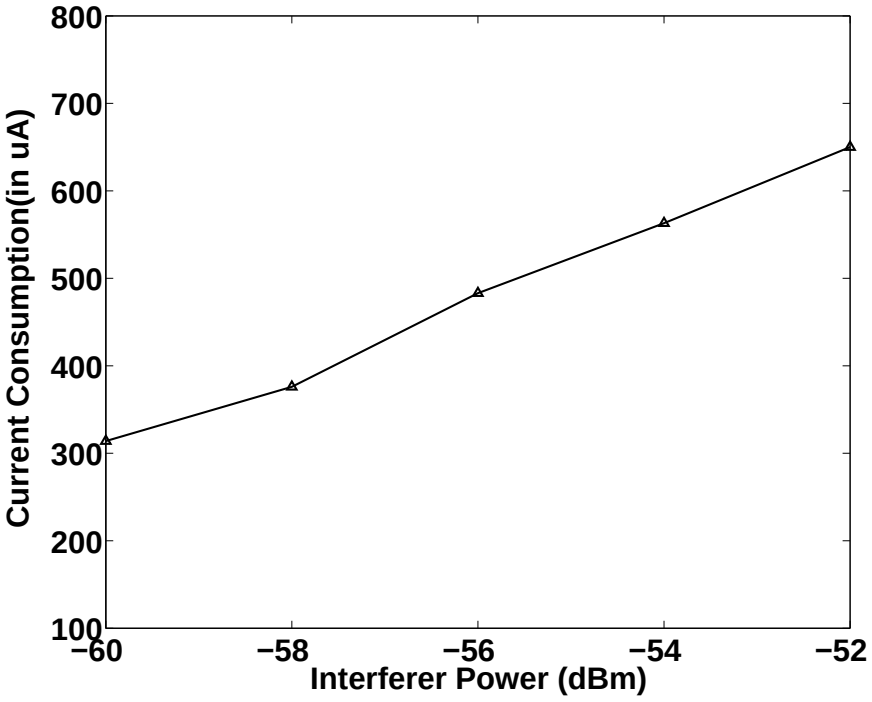


Figure 4.10: Power consumed for different interferer power levels for P_{sig}=-85dBm

which meets both Noise figure and IIP3 specifications is found out. In Fig.4.10, the power at this minimum-power setup is plotted against a range of interference power -52 dBm to -62 dBm for a constant signal level of -85dBm. The graph shows that as the interference reduces the adaptive LNAM cranks down its linearity while saving power by as much as 50%.

In the second case the interference is assumed to be constant at -52 dBm while the signal level is varied from -85dBm to -75dBm. Again the minimum power setup which meets both noise figure and IIP3 is found out and the power at this setup is plotted against the signal level. Fig.4.11 shows that the power savings of 5X is obtained while signal level increases from -85dBm to -75dBm.Thus the proposed circuit is well suitable for an adaptive ZigBee receiver.

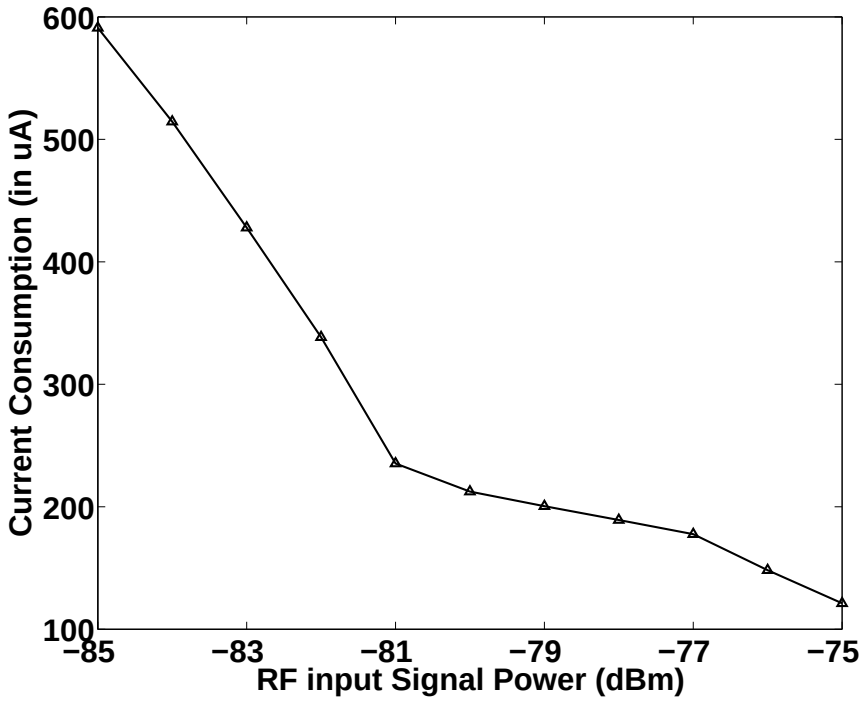


Figure 4.11: Power consumed by LNA-Mixer for different input signal level at constant $P_{interferer}$=-52dBm

4.5 Conclusions

We have derived the specifications of the adaptive receiver and its sub-blocks as a function of the channel conditions and proposed two front end topologies for an adaptive receiver. The proposed LNA-Mixer topology is well suited for an adaptive receiver in terms of tunability and power savings. In the case of the merged LNA-Mixer topology designed for a ZigBee receiver, the power savings is as much as 50% when the interference level is relaxed by 8dB from the maximum level and 5X when the signal level improves by 10dB than the minimum level specified by the ZigBee standard.

Chapter 5

Test Chip Design

5.1 Introduction

To validate the proposed adaptive merged LNA-Mixer circuit, a prototype design was implemented in UMC 130nm RFCMOS/Mixed Mode 2P8M process. This chapter gives the details of the prototype chip and the layout issues.

5.2 Prototype LNA-Mixer and Peripheral Circuitries

The block diagram of the prototype merged LNA-Mixer is given in 5.1. Since the IOs in the process offer higher capacitance, degrading the high frequency performances, all 2.4GHz band signals (input RF signal and the differential LO signals) are given through probe pads. The output buffers with low output impedance drive out the 3MHZ IF signal out of the chip.Bias generation circuitry generates the necessary bias for the LNA-Mixer core and the output buffers. The following subsections explains the peripheral circuits in detail.

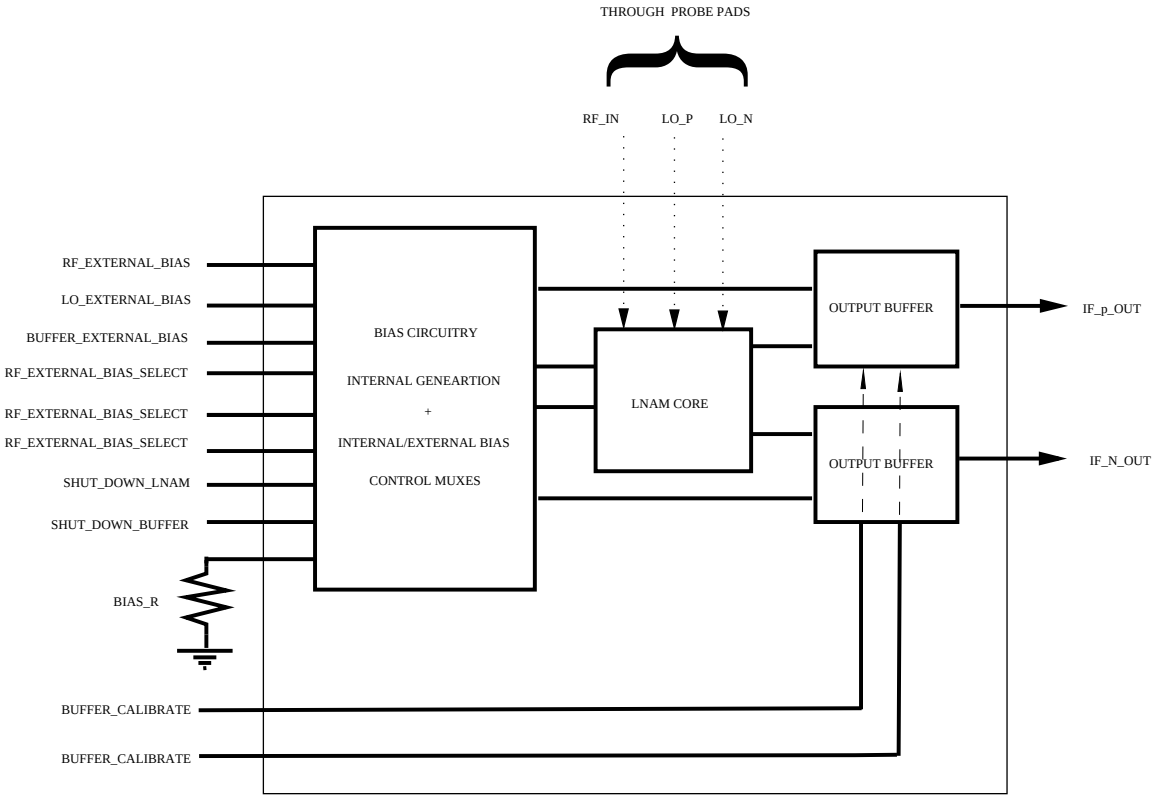


Figure 5.1: Prototype LNA-Mixer with the peripheral circuitry

5.2.1 Bias Generation

The adaptive bias generation circuitry was explained in chapter 4. This circuit takes a single reference bias current I_{ref} and generates the bias voltage for the two branches of the folded merged LNA-Mixer, namely RF_BIAS and LO_BIAS. The reference bias current is generated by the constant g_m circuit. The reference bias current is programmable via an external resistor BIAS_R, enabling an external control of the bias currents.The detailed diagram of the internal bias generation circuitry is shown in figure.5.2 To measure the power consumption of the LNA-Mixer core and the buffers separately, two digital controls SHUT_DOWN_LNAM, SHUT_DOWN_BUFFER are used. When asserted, they shut off the bias currents for the LNA-Mixer core and buffers respectively. To give more controllability of the bias in the circuitry, a provision has been made to bypass the internally generated bias voltages and feed the required bias voltages (RF_BIAS, LO_BIAS, BUFFER_BIAS)

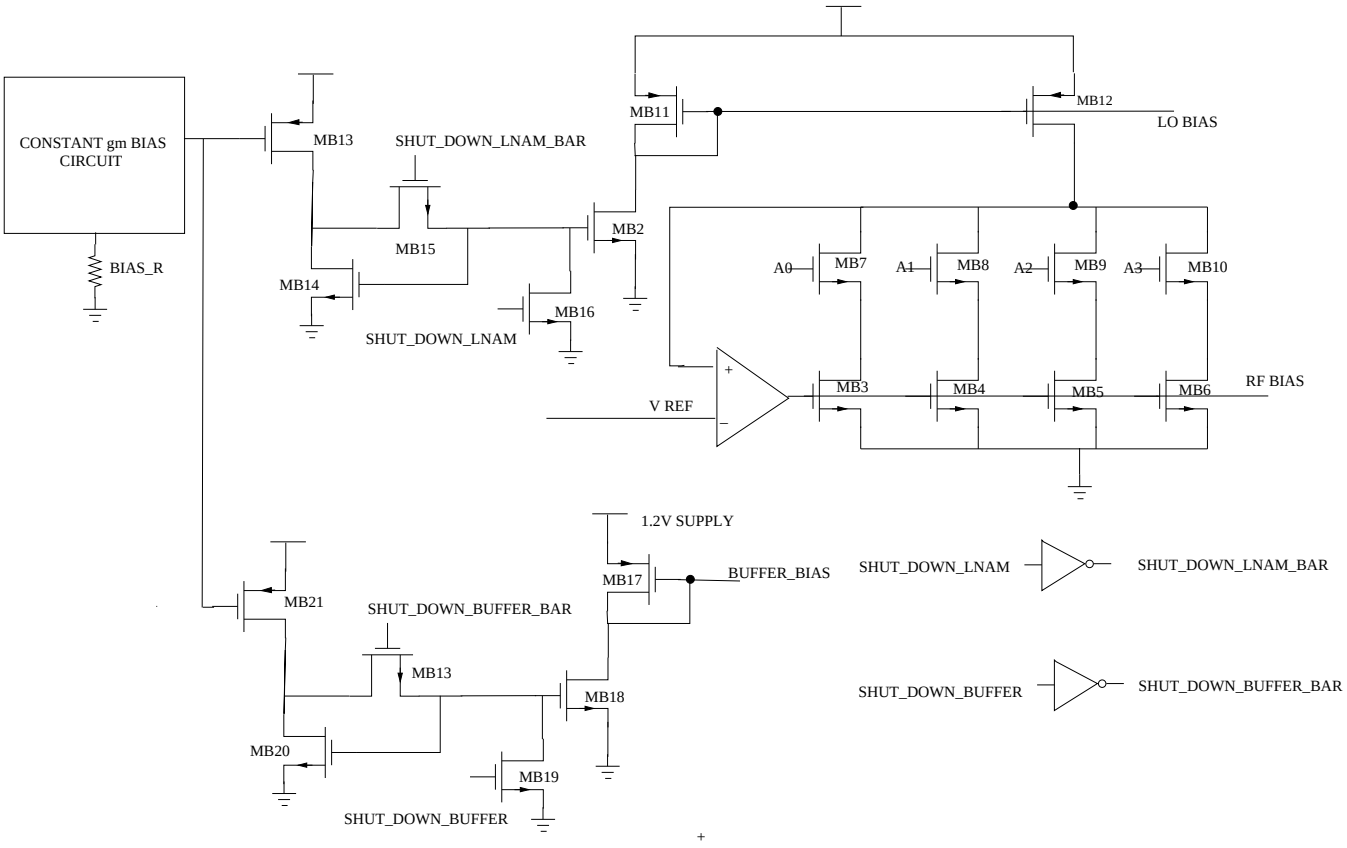


Figure 5.2: Internal Bias Generation Circuitry

through external IO pins(RF_EXTERNAL_BIAS, LO_EXTERNAL_BIAS, BUFFER _EXTERNAL _BIAS). Three control signals (RF_EXTERNAL_BIAS_SEL, LO_EXTERNAL_ BIAS_SEL, BUFFER_EXTERNAL _BIAS _SEL), are used to choose between the internal and external biases.The detailed block diagram of the bias generation block is given in figure 5.3 The MUX used to select among the internal/external biases are

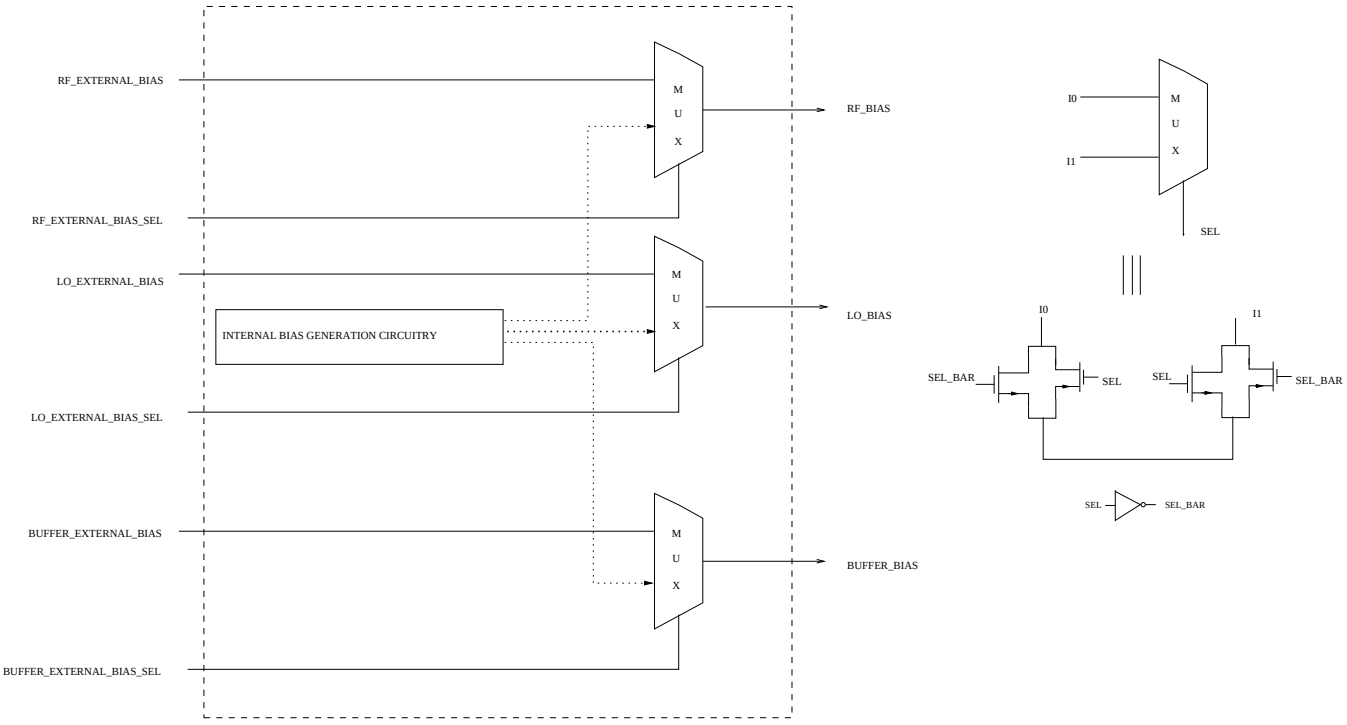


Figure 5.3: Detailed Block Diagram of Bias Generation Circuitry

made of two transmission gates and inverters as show in figure 5.3.

5.2.2 Output Buffers

Since the LNA-Mixers output impedance is high, it cannot drive out the IF signal through the IO pins which offer considerable capacitive load. So an output buffer with low output impedance is necessary to drive out the IF signals. The various design choices of buffers have been discussed in [8] and a modified super follower is found to be best suited for this application. Since the load transistors of the LNA-Mixer are NMOS the output buffer has a PMOS input for matching the common mode

values. The IO buffer attenuates the IF signal slightly and also contributes to the noise figure and non-linearity of the design. So to decouple the buffers' contribution to noise figure/linearity measurements made and to arrive at the proper performace numbers for the LNA-Mixer, a provision to calibrate the buffers is made. To calibrate

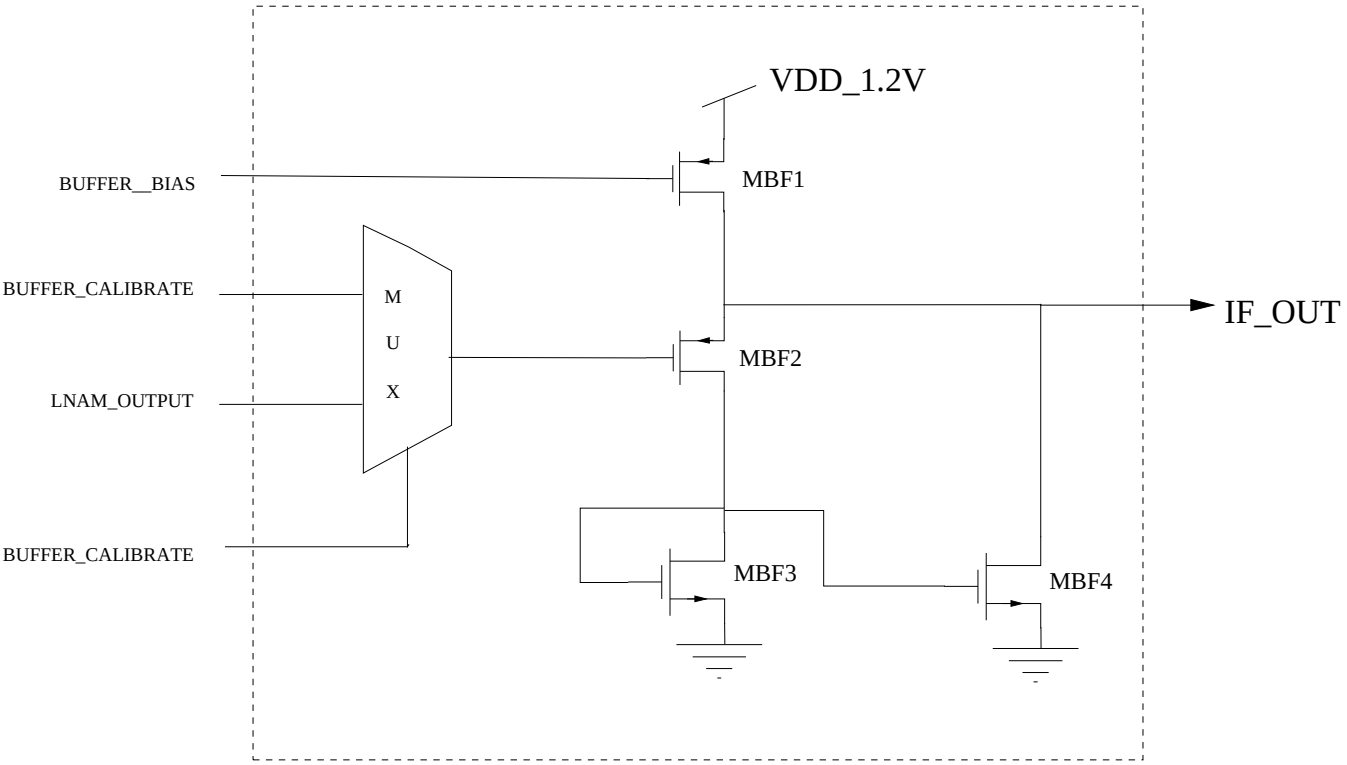


Figure 5.4: Output Buffer designed to drive the IF Signals

the buffer a 3MHZ signal is fed through BUF-calibrate-input. A digital control bit is used to select the buffer input either from the LNA-Mixer output or from the calibration input. The detailed block diagram of the output buffer is given in the figure 5.4 .The minimum supply voltage at which the buffer could operate was higher than that of the LNA-Mixer. Hence to actually evaluate the supply scaling potential of the LNA-Mixer, the buffer is operated from a separate fixed supply voltage of 1.2V

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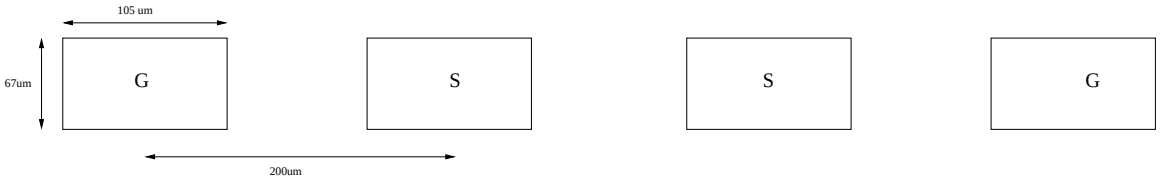

Figure 5.5: GSSG Probe pad dimensions

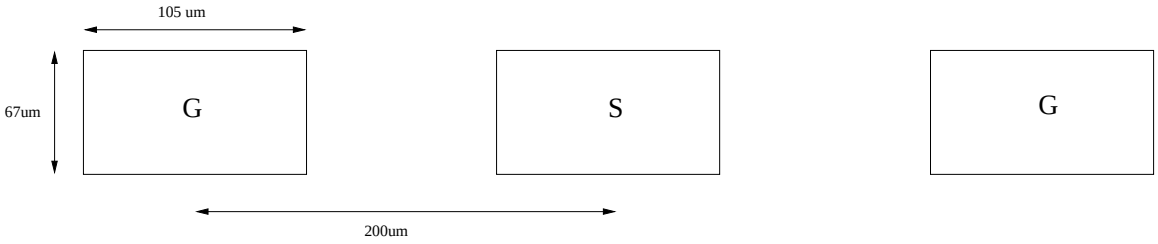

Figure 5.6: GSG Probe pad dimensions

5.2.3 Probe pads

The RF signals are to be fed into the test chip through probe pads. These pads are of dimension shown in the figure. The single ended RF signals are fed through probes of GSG(Ground-signal-Ground) configuration. The dimensions of the probe pads are shown in figure 5.5 and Figure 5.6 The differential LO signal is fed through GSSG pads. These pads occupy all the 8 metals with vias in between all successive metal layers for mechanical support. The density of the vias has to be between 20% and 30% to avoid the via form density error as specified by the UMC layout design rules.

5.3 Layout issues

a) The input transistors of the adaptive LNAM has 4 transistor segments. The transistors in each segment is twice the size of the previous one(i.e size increase geometrically). In layout the phase of the RF signal reaching the gate each segment should be made same by making the distance from the signal source(in this case the probe pads) to each segment the same. To have close matching between the different segments, each transistor is further segmented and laid out in a common centroid

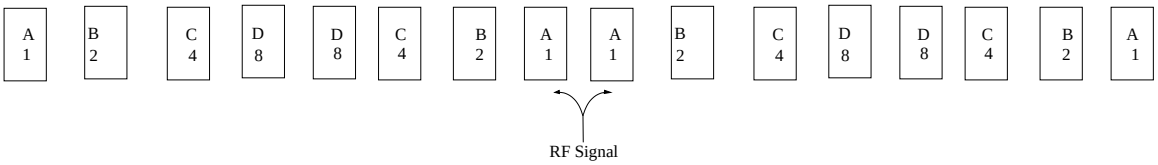

Figure 5.7: Common Centroid Layout used for Input Segmented transistors. characters A-D represent 4 different transistors and the number below the character in each block, represent the number of unit transistor the block is made of

fashion.Figure. 5.7 shows the arrangement for 4 segmented transistors. A-D represents the four segments. The numbers below represent the number of unit transistors that makes that block. It can be seen that the RF signal path length remain the same for all segments A-D. Also any linear variation in the process parameters along x direction gets cancelled out. Also dummy transistors are added on either ends for better matching. Similarly for the LO and load transistors pairs also a common centroid layout is used.

b) To avoid the substrate noise coupling,triple well transistors are used for all the NMOS transistors in the signal path(the input and cascode transistors)

c) Since the structure in the mixer branch(LO -transistors and load) is differential, mirror symmetry is maintained, to improve matching.

d)A decoupling capacitance of 10pF (MIMCAPS) is used to provide the ac current for the LNA-Mixer, reducing the effect of the supply pin inductance. All the free space available in the chip was filled with NMOS capacitances, which amount to around 500pF of capacitance, which further reduces the effect of pin inductance.

e)Separate Guard rings are placed around the input transistors, cascode transistors,LO transistors and the load transistors and the inductors. A big guard ring which surrounds the entire LNA-Mixer structure isolating it from the other designs in the chip was also placed.

5.3.1 Layout Snapshots

The test chip also had a VCO and PLL together with the LNA-Mixer. The layout of the snapshot of the test chip with the IO Pads is shown in Figure. 5.8 The total area of the LNA-Mixer without probe pads is 520um x 640um.The chip die area is around 1.5mm x 1.5mm. The details about the pins of the chip and their functionalities are given in Appendix A. Details of the board designed for the chip are given in Appendix B

5.4 conclusion

The proposed Low Voltage Merged LNA-Mixer has been prototyped in UMC 0.13um RFCMOS 2P8M Technology. Post Silicon validation of the proposed circuit has to be done.

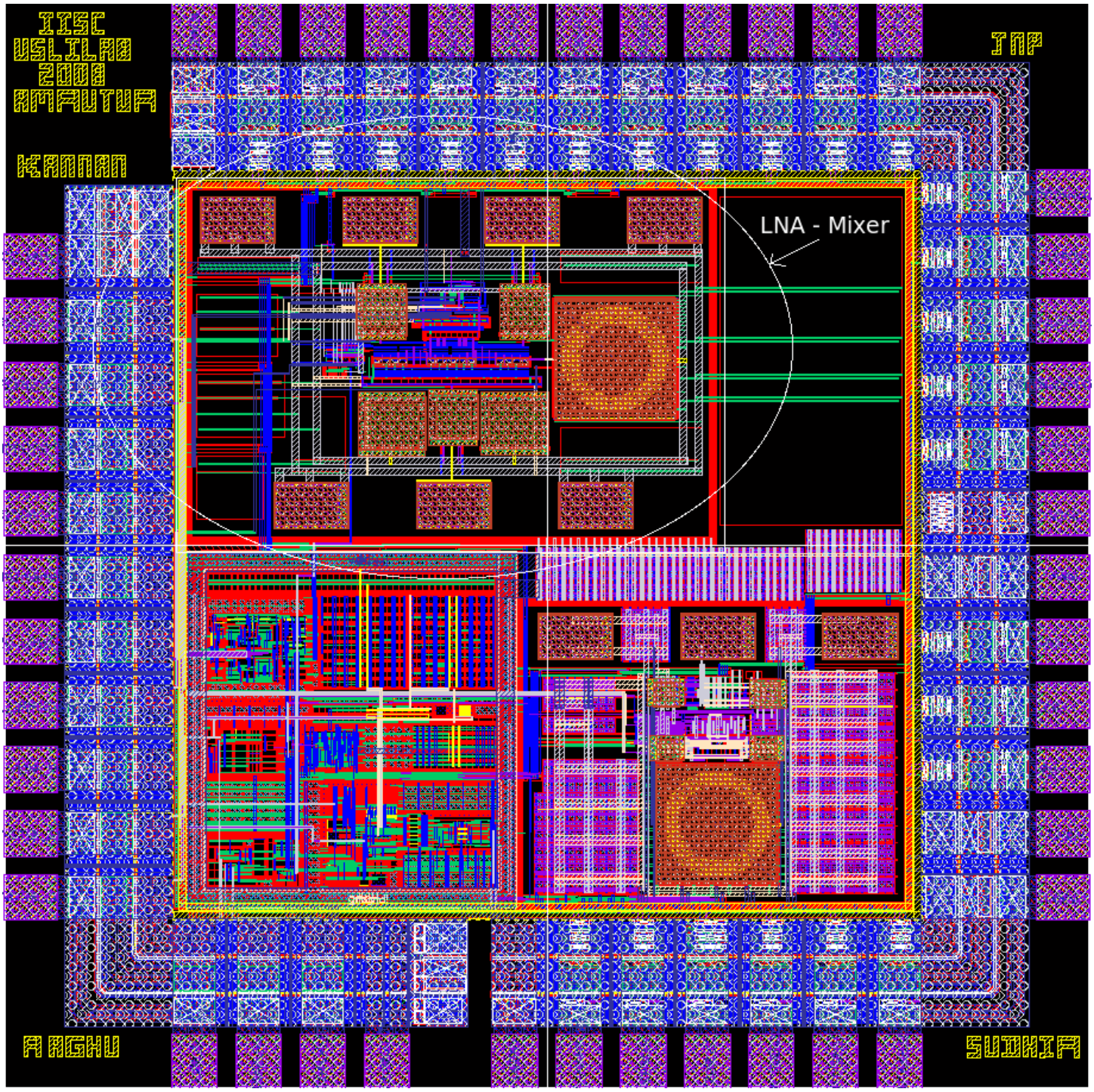

Figure 5.8: Layout Snapshot of the Full Chip

Chapter 6

An adaptive Active Inductively Degenerated Common Source LNA

6.1 Introduction

Radio for a ZigBee receiver has relaxed performance specifications compared to other mobile and wireless LAN standards, due to its relatively low data rate specifications. Table. 6.1 compares the noise figure requirement of a few standards. This was exploited to arrive at a low power adaptive LNA-Mixer topology with resistive input termination in the previous chapter. However for wireless LAN kind of applications where the noise figure requirement is $\leq$ 10dB, a resistive matched LNA will not meet the performance requirement. For such low noise figure narrow band receivers,a common source inductively degenerated LNA, shown in fig.6.1 has been the traditional

Table 6.1: Performance Specification of a few wireless IEEE standards

Standard	Frequency	Max. Data rate	Noise Figure
ZigBee	2.4GHz PHY	250 Kbps	20.5
E-GSM	900MHz	270Kbps	9
802.11g	2.4GHz	54Mbps	7.5
802.11b	2.4GHz	2Mbps	14.8

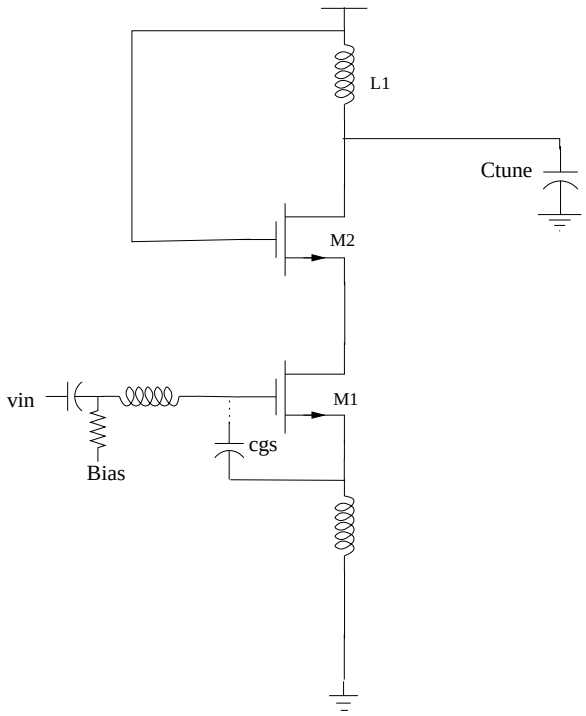

Figure 6.1: Basic Inductively degenerated LNA

choice of the designers. Being a popularly used topology, It will be beneficial to modify this topology to make it adaptive. This chapter discusses a Common source inductively degenerated adaptive LNA, suitable for very low noise figure and low power demanding receivers, like 802.11 wireless LAN receivers.

6.2 Proposed Adaptive Common Source LNA

The Common source inductively degenerated LNA circuit has been analyzed extensively in [38]. The main advantage of this topology is that there is no fundamental limitation on the achievable noise figure.As discussed in the previous chapter we plan to use the effective width of transistor M1/M2 as a tuning knob. We achieve this by segmenting transtors M1/M2 and switching on/off the appropriate number of legs.As seen in figure.6.1, the cascode transistor gate is usually connected to the supply voltage and hence the same transistor can be used for switching a leg on/off,

avoiding the need for an extra transistor in the stack.The proposed topology is shown in figure.6.2.Though the figure shows only 4 legs the number of legs can be extended are reduced suitably. Transistors M1-M4 are sized in a geometric progression, making it possible to use any effective width(W_{eff}) which is a integral multiple of the minimum width (W_{min}. Digital bits $A_3 - A_0$ are used to switch on and off the cascode transistors, thus controlling W_{eff}.A key issue in making this topology adaptive is the input matching. The real part of the input impedance depends on the transconductance of the input transistors. Hence when we vary gm to adjust the noise figure/ IIP3 the input matching may become extremely poor.One must find a way about to keep the matching (i.e) Input reflection coefficient, S11 of the LNA to an acceptable level.The Input impedance Z_{in} of the common source LNA in figure 6.1 is given by the equation.

$$\begin{aligned} Re(Z_{in}) &= \frac{g_m L_s}{C_{gs}} \\ Im(Z_{in}) &= (L_s + L_g)\omega + \frac{1}{C_c \omega} \end{aligned} \tag{6.1}$$

In the above equation, the gate capacitance C_{gs} of the segmented transistor vary very less between switched on/off modes. Figure. 6.3 shows the gate capacitance of the segmented transistor,C_gs against the number of on/off legs. It can be seen that the maximum variation is only 2.8% in a UMC 0.13um technology, with W_{min}/L = 7.1u/0.3u. When we vary W_{eff} or the bias current to tune noise figure/IIP3, $Re(Z_{in})$ varies proportional to g_m, severely affecting the input matching.For example for a 4X variation in g_m, the real part of input impedance may vary from 50Ω to 12.5Ω, making the S_{11} in the later case to be just -4dB. To keep the $Re(Z_{in})$ constant, the inductor L_s must be varied in a fashion inversely proportional to g_m. To achieve this we propose an g_m tracking active inductor configuration.This is discussed in the next sub-section.

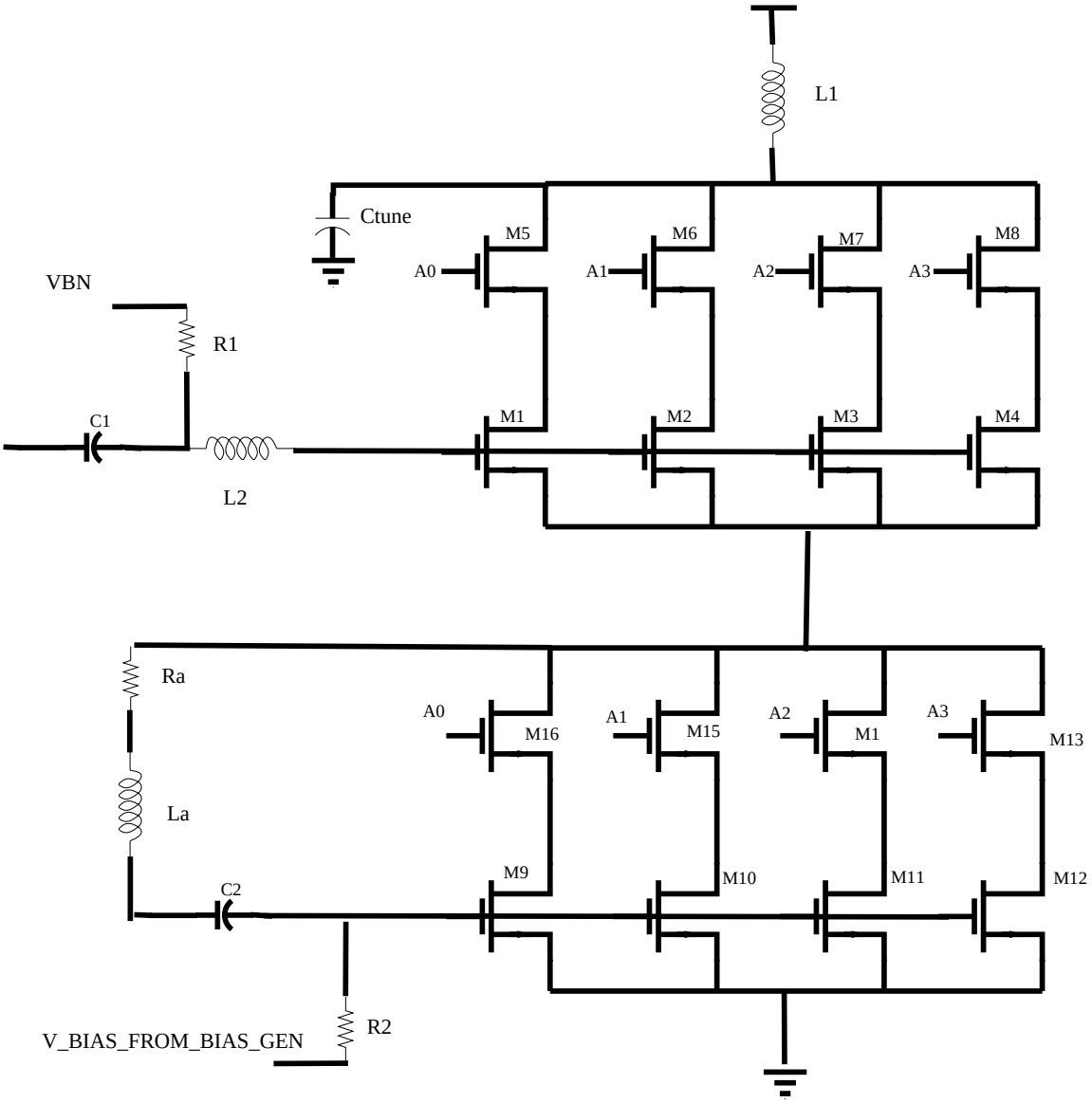

Figure 6.2: Proposed LNA Circuit

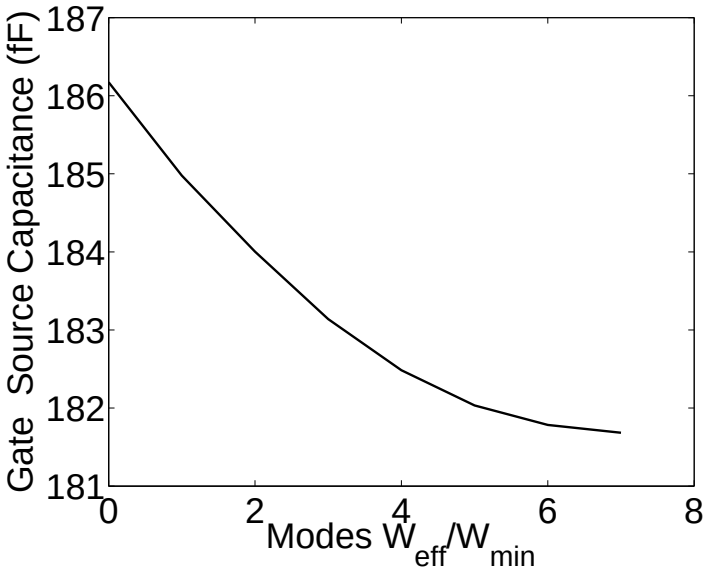

Figure 6.3: Plot showing gate-source capacitance variation across switched segment widths

6.2.1 g_m tracking Active Inductor

Active inductors realized using gyrator circuits are very popular and different gyrators have been discussed in [39]. The existing active inductor topologies are primarily used to get high Q inductors(since passive inductors in modern sub-micron processes have very low Q) or in circumstances where the process does not have inductors. However the main disadvantage of the active inductors are their higher noise and the extra power consumption to realize them. In the present situation, these two disadvantages will be deleterious to the LNA as it would degrade the noise figure and increase its power consumption. Another major requirement of the active inductor is that it should track the g_m changes as closely as possible.To achieve this we propose the topology given in figure. 6.4 Though the proposed g_m tracking active inductor topology uses another inductor for its realization, it is acceptable for RF designs, which have inductors anyway. The admittance looking into the active inductor can be computed as

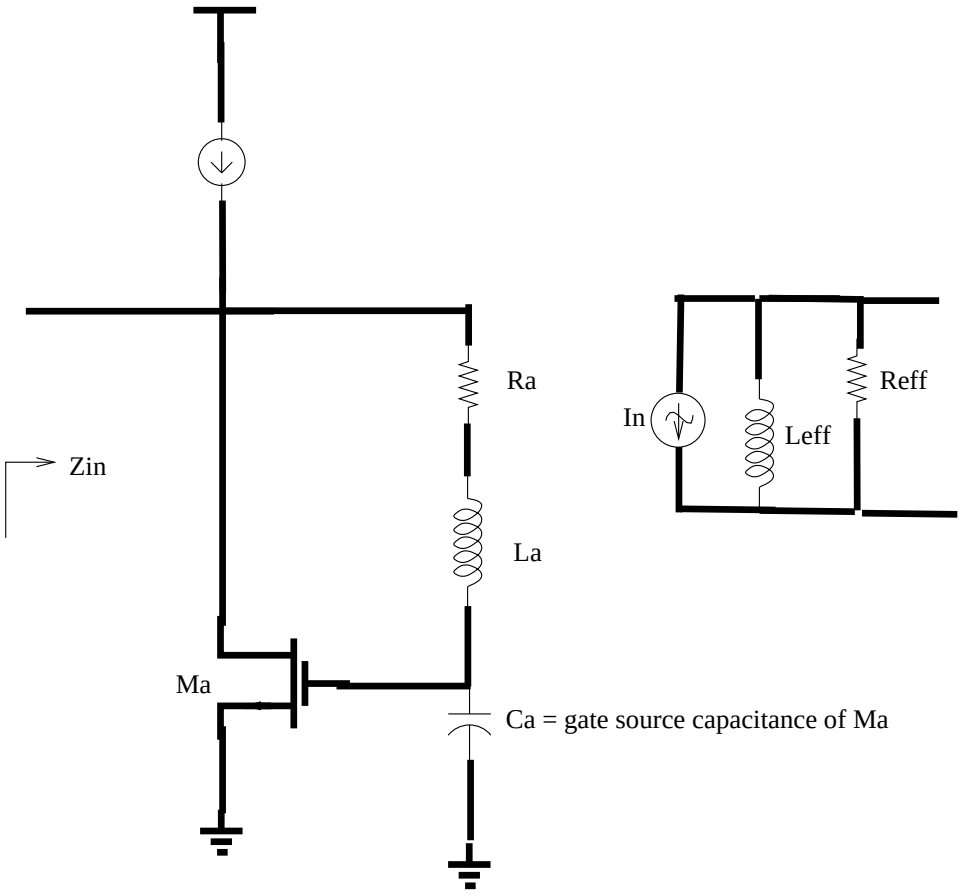

Figure 6.4: Proposed g_m tracking active inductor

$$Y_{in} = \frac{1}{R_a} + \frac{g_{m,a}}{jR_aC_{gs,a}\omega_0} + g_{ds} \tag{6.2}$$

neglecting g_{ds} and using the approximation $\omega_T/\omega_0 \gg 1$, the series inductance can be written as

$$L_{eff} = \frac{R_aC_{gs,a}}{g_{m,a}} \tag{6.3}$$

It can be seen that the Q of the inductor of the inductor will close be ω_T/ω_0, which is reasonably high. The short circuit noise current is the drain current noise of the transistor M_{active}. The equivalent circuit of the active inductor is given in figure 6.4.

6.2.2 Proposed Adaptive LNA

If we can make $g_{m,a}$ track the g_m of the input transistors of the LNA across different current and W_{eff}, then the $Re(Z_{in})$ remains constant. However in the proposed method the real part depends on R_a and $C_{gs,a}$ which may vary heavily under process conditions. To overcome this R_a and $C_{gs,a}$ can be made programmable using resistor banks and varactors. Another beneficial effect is that the since $g_{m,a}$ tracks g_m process variations in the input transistor and active inductor transistor does not affect the matching. However there is a problem with the proposed solution. since the inductance L_s vary with gm, the imaginary part starts varying with g_m. But by making the contribution of L_s to the imaginary part of the input impedance small(i.e $L_g \gg L_s$ the percentage variation in imaginary part can be made very small.Since the inductive part can now be written as $L_g\omega + \frac{R_aC_{gs,a}}{g_{m,a}}.\omega$The percentage variation in the inductive part (percentage variation in the imaginary part will not be meaningful as nominal value of imaginary part is zero) can be found as

$$\frac{\delta Z_{in,inductive}}{Z_{in,inductive}} = \frac{\frac{R_aC_{gs,a}}{g_{m,a}}}{L_g\omega + \frac{R_aC_{gs,a}}{g_{m,a}}} \frac{\delta g_m}{g_m} \tag{6.4}$$

by making L_g provide most of the inductive part needed, the variation in inductive

part can be maintained as small as needed to keep the S_{11} under acceptable levels. In many recent works an S_{11} of -10 dB is reported as acceptable, in which case 90% of the input power couples into the LNA. Hence in our design, we have made the S_{11} to be made less than -10 dB across all the different modes of operation of LNA. It should be noted if we had not chosen to make L_s to track g_m the real part would have varied. also since the real part depends only on L_s the percentage variation in g_m directly translates to variation in $Re(Z_{in})$ leading to a poorer matching across different modes. Hence the proposed method is superior in terms of matching. The proposed LNA with the adaptive input matching is shown in figure 6.2. It can be seen that current for the input transistors have been reused for the transistors of the active inductor also. Also the transistors of the active inductors are switched and controlled by the same controlling bits which control W_{eff}. Thus the effective widths of active inductor transistors and the LNA's input transistor remain in the same ratio across all modes. They also carry the same current and hence their g_m track one another excellently.Also it is shown in the next section that the noise contributed by the active inductor will be proportional to $\frac{g_{m,a}}{g_m}$, which can be made low to keep the noise degradation to a minimum level. The disadvantage of the proposed topology is the increased voltage headroom for the extra active inductor transistors in the stack. (Since the switches for the active inductor transistors are in linear region they drop only a few tens of milli Volts across them).

6.2.3 Noise Figure and Linearity of proposed LNA

Defining the symbols as shown in Table.6.2.3, Lets us analytically derive the noise figure of the proposed structure. We have already shown that the gate source capacitance remain constant independent of the number of switched legs, call this total capacitance C_t. If at a particular mode the capacitance contributed by the switched on transistors is C_{gs} the present situation is analogous to the case where an extra capacitor is added in parallel to the gate-source capacitance of the input transistor in

Symbol	Meaning
i_{no,R_s}	output noise current due to Input 50Ω source
i_{no,d_1}	output noise current due to drain noise of input transistor
i_{no,g_1}	output noise current due to gate noise of input transistor
$i_{no,activeinductor}$	output noise current due to active inductor transistor
$i_{no,corr}$	correlated component of gate noise
i_{n,R_s}	Thermal noise current density of input source resistance.
i_{n,d_1}, i_{n,g_1}	drain noise current, induced gate noise current of input transistor
$i_{activeinductor}$	noise current of active inductor
i_{no}	total output noise current
C_{gs}	Total Gate source capacitance of switched on transistor segments
C_t	Total Gate source capacitance of all transistor segments
P	$\frac{C_{gs}}{C_t}$
Q	$\frac{1}{R_s\omega_0 C_t}$
$K_1 - K_6$	Constants dependent on process and bias parameters

Table 6.2: Symbols used in the noise figure derivation

a inductively degenerated LNA. The model chosen for deriving noise figure is shown in figure.6.5 The figure also shows the various noise sources contributing to the output noise. .Define the ratio $P = \frac{C_{gs}}{C_t}$, we can see that this case is analyzed in [40] except for the active inductor's noise contribution. The output noise current due to the each of the noise sources are

$$\begin{aligned} i_{no,R_s} &= \frac{g_m}{j2\omega_0 C_t} i_{n,R_s} \\ i_{no,d_1} &= \frac{i_{n,d_1}}{2} \\ i_{no,g_1} &= \frac{g_m}{j\omega_0 C_t} \frac{jR_s w_0 C_t - 1}{2jR_s w_0 C_t} i_{n,g_1} \\ i_{no,activeinductor} &= \frac{i_{activeinductor}}{2} \end{aligned} \tag{6.5}$$

$$i_{n,o} = i_{no,R_s} + i_{no,d_1} + i_{no,g_1} + i_{no,activeinductor} \tag{6.6}$$

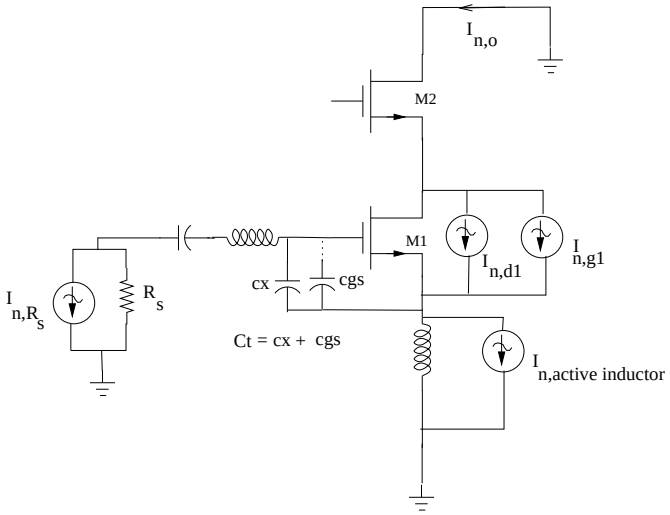

Figure 6.5: Noise model used to derive the noise figure of proposed LNA

While calculating the mean square noise current at the output, care should be taken to consider the correlation between the gate and drain noises of the input transistor.

$$i_{n,o}^2 = i_{no,R_s}^2 + i_{no,d_1}^2 + i_{no,g_1}^2 + i_{no,activeinductor}^2 + i_{n,corr}^2 \tag{6.7}$$

from the basic drain and gate noise models for the transistors as discussed in chapter 2, we can write

$$\begin{aligned} i_{no,R_s}^2 &= g_m^2 Q^2 R_s kT \\ i_{no,d_1}^2 &= \frac{kT\gamma}{\alpha} g_m \\ i_{no,g_1}^2 &= g_m P^2 (Q^2+1) \frac{kT\alpha\delta}{5} \\ i_{no,activeinductor}^2 &= \frac{kT\gamma}{\alpha} g_{ma} \\ i_{no,corr}^2 &= 2P|c|g_m kT\sqrt{\frac{\delta\alpha}{5}} \end{aligned} \tag{6.8}$$

Now the Noise factor can be written as

$$F = \frac{i_{n,o}^2}{i_{no,R_s}^2} \tag{6.9}$$

substituting from 6.8 and absorbing all the process dependent constants and the constant $\frac{g_{ma}}{g_m}$ into constants $K1$, $K2$, $K3$,

$$F = 1 + \frac{K_1}{g_m} + \frac{K_2 P}{g_m} + \frac{K_3 P^2}{g_m} \tag{6.10}$$

Since P and g_m are functions of the bias current and W_{eff} we can write

$$F = f_1(I, W_{eff}) \tag{6.11}$$

It can be seen that increasing the bias current increases g_m without changing P and hence theoretically arbitrarily low noise figure can be obtained be obtained for this structure. To intuitively analyze the effect of varying width let us assume square law for the transistor current which makes

$$g_m \alpha \sqrt{W_{eff}} \tag{6.12}$$

and noting that $P \alpha W_{eff}$, the noise figure in terms of the transistor width, for a constant bias current as

$$F = 1 + \frac{K_4}{\sqrt{W_{eff}}} + K_5 \sqrt{W_{eff}} + K_6 {W_{eff}}^{\frac{3}{2}} \tag{6.13}$$

Since there are terms proportional to and inversely proportional to W_{eff} in the expression for noise factor, there exists an optimum W_{eff} at which the noise factor is minimum. this is a traditionally reported result for inductively degenerated LNA which hold good in our present structure also.

The linearity of LNAs can be analyzed rigorously using Volterra series. However in this work we refrain from doing so and resort to a simple intuitive equation. We

assume that the linearity is predominantly determined by the input transistor. and now the linearity of the LNA can be derived as

$$V_{IP3,lna}^2 = \frac{V_{IP3,tran}^2}{\frac{V_{gs}^2}{V_{in}^2}} \tag{6.14}$$

Substituting for transistor IIP3 from equation from chapter 4, we get

$$V_{IP3,lna}^2 = \frac{16}{3}\frac{I}{Q^2 g_m \theta} = f_2(I, W_{eff})\ (say) \tag{6.15}$$

Now from equations (6.11) and (6.15) one can see that using bias current and W_{eff} we can vary IIP3 and Noise figure, each to a specified value independently. This kind of an independent tuning is possible over the range in which the assumptions we made hold true.Also it should be noted that the optimum width for noise figure need not give us the required linearity. By backing off from the optimum width we trade off noise figure for linearity as required by the adaptive receiver. The following are the steps in designing the adaptive LNA structure.

a) First design a non-segmented LNA (referred as the base design, henceforth) by constraining the power consumption, and estimating the optimum width of the input transistor which minimizes the noise factor.

b)Choose the number of control bits needed, say N. divide the width of the input transistor in the base design by $2^N - 1$ to get W_{min}.

c)Now use W_{min} as the minimum sized transistor controlled by bit A0 and make the successive transistors twice the size its preceding transistor.

d) To reduce the noise contribution due to the active inductor noise, choose the widths of the active inductor transistors smaller than the input transistors. find the ratio $\frac{g_{ma}}{g_m}$ and design R_a and C_a to make the real part of the input impedance equal to R_s.

6.2.4 Bias Circuitry for the proposed LNA

The bias current of the LNA is set by the gate voltage of the transistors M9-M12 in figure 6.2. Since we like to vary the bias current independently of the effective width of the transistors, the bias circuitry also should use the configuration bits $A_3 - A_0$ to set the appropriate gate voltage. One can use a simple current mirror with the effective width of the current mirror transistors varied according to the configuration bits. But in the short channel regime the channel length modulation is very severe thereby changing the bias current when W_{eff} is varied. since this variation is severe we provide a feedback based bias circuitry as shown in figure.6.6 This bias circuitry mimics the LNA topology except that all the transistors and bias currents are scaled down in size.A feedback is used to keep the node X at a constant voltage $V_{ref,bias}$ to avoid any channel length modulation in the PMOS across different currents.

6.2.5 Simulation results of the proposed LNA

An LNA based on the proposed topology is simulated using UMC 0.13um transistor models. The simulation results are given in Fig(6.7 - 6.9). The LNA was designed to have 8 modes controlled by bits A3-A0 .Figure. 6.7 shows the noise figure of the LNA for three diffrent bias currents for the different modes. The noise figure decreases with increasing bias and widths as expected. Similarly figures6.8,6.9 shows the IIP3 and gain of the LNA across bias currents and modes. Figure. 6.10 shows the contours of constant noise figure (NF = 2.7dB - 7dB) and contours of constant IIP3 (IIP3 = -15dBm - -23dBm). The tunability of the circuit is explicit in this figure, as we can note that the IIP3 can be varied while maintaining the same noise figure by trading off power for W_{eff} and similarly Noise figure can be varied without changing the IIP3. A 10 dB tuning range of IIP3 and around 6 dB tuning range for Noise figure has been obtained for this design.The effectiveness of the proposed g_m tracking matching method is shown by figure 6.11. The S_{11} is under -10 dB under

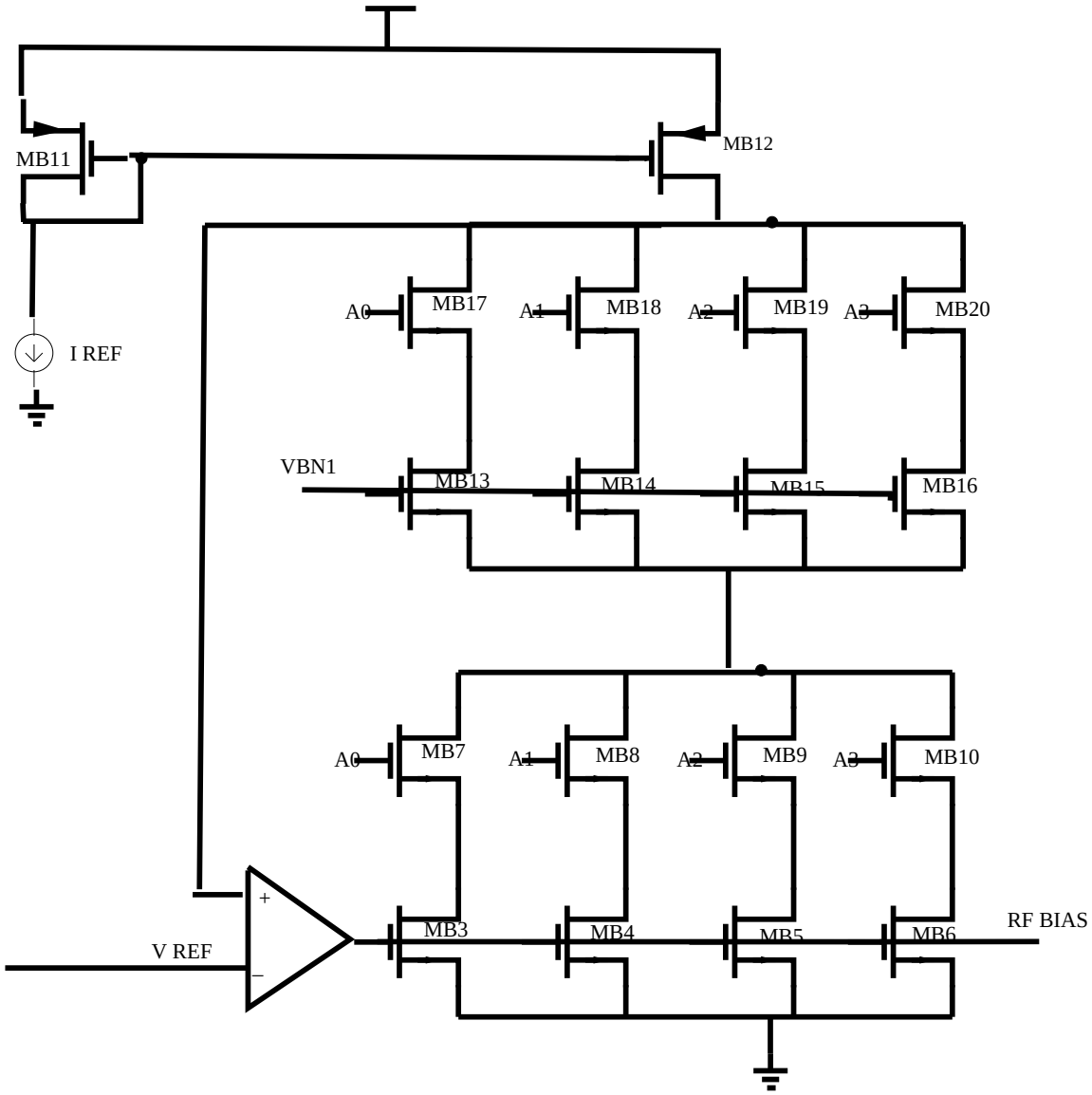

Figure 6.6: Proposed Bias circuitry for adaptive inductively degenerated LNA

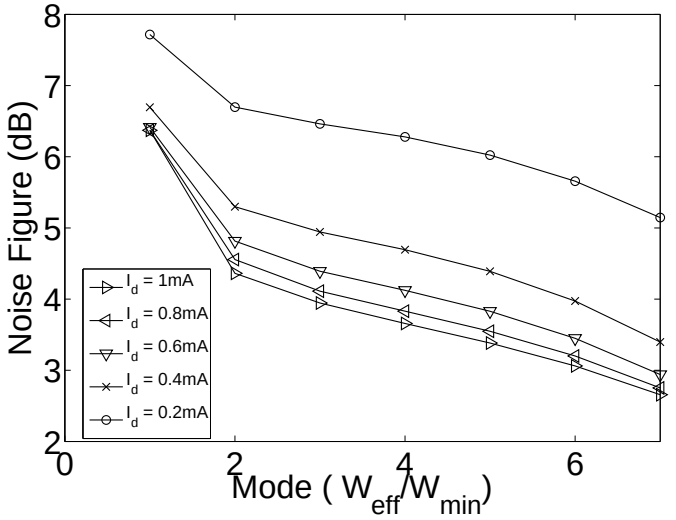

Figure 6.7: simulated Noise figure of the proposed adaptive LNA

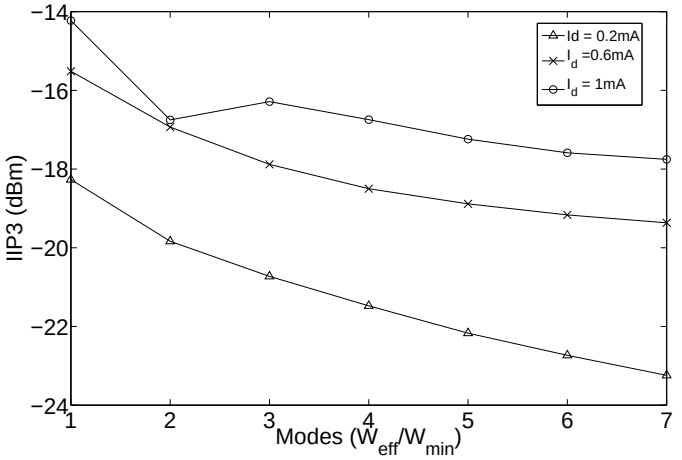

Figure 6.8: simulated IIP3 of the proposed adaptive LNA

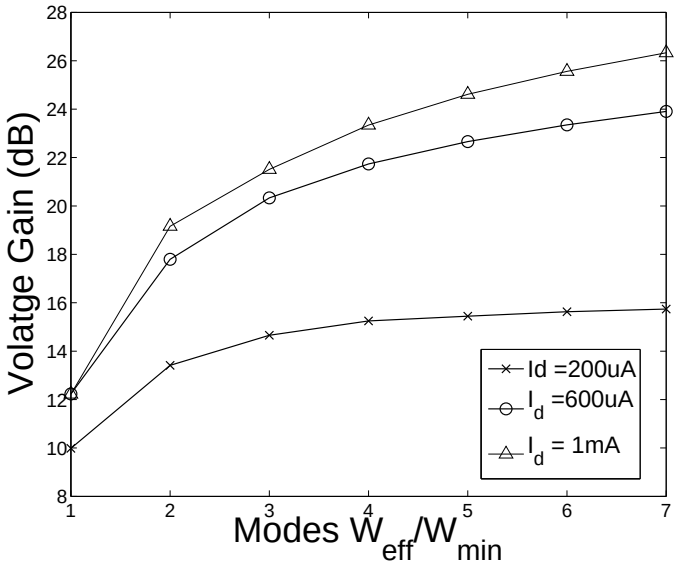

Figure 6.9: Simulated Voltage gain of the proposed adaptive LNA

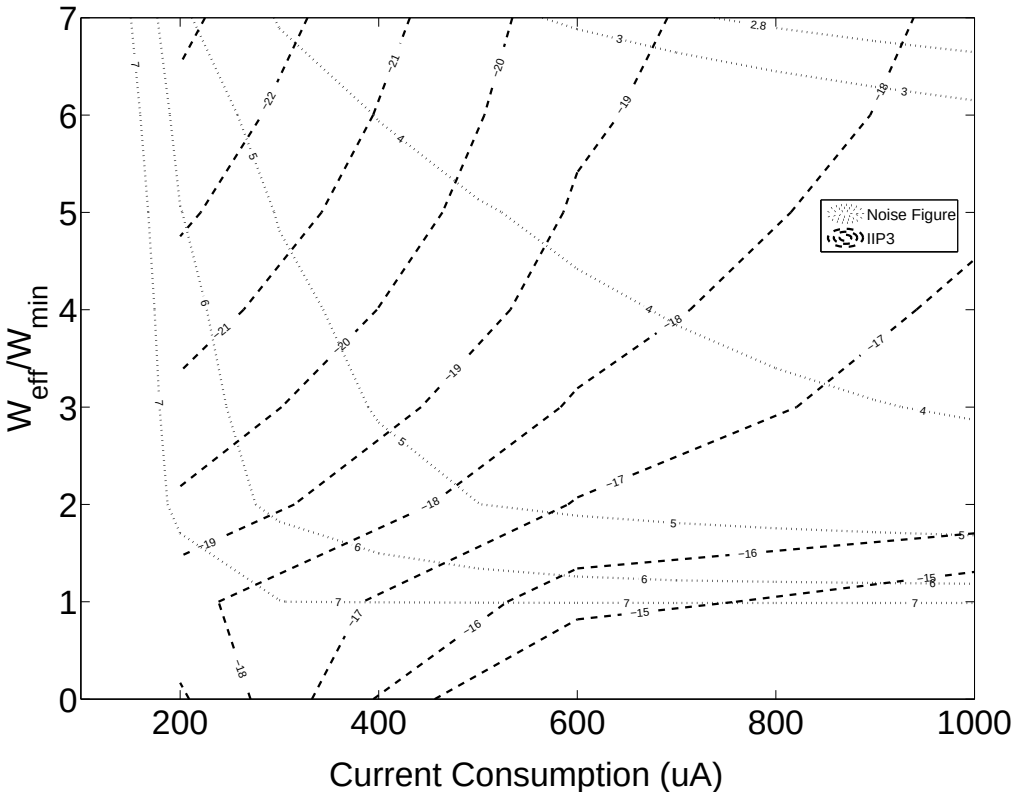

Figure 6.10: Contours of constant Noise figure and constant IIP3

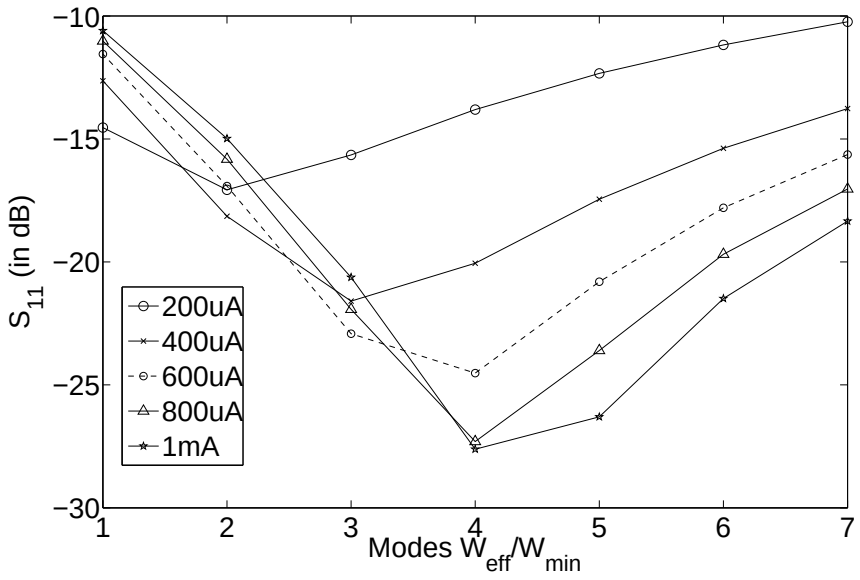

Figure 6.11: S_{11} of the proposed LNA under different modes and bias conditions, showing the effectiveness of the g_m tracking inductive matching method

any bias/width conditions.

6.3 Conclusions

In this chapter, we have discussed an adaptive common source LNA suitable for radio receivers which demand very low noise figures, such as wireless LAN receivers. The proposed LNA uses a novel g_m tracking active inductor as degeneration inductor, thereby decoupling the input matching from gain and IIP3 specifications. We have analytically shown that, noise contribution due to the active inductor can be kept as low as possible, while meeting the input matching requirements. Simulation results of the proposed topology show a noise figure tuning range from 2.7dB - 9dB and IIP3 tuning range from around -15dBm - -25dBm.

Chapter 7

Conclusion and Scope for Future Work

7.1 Conclusion

The present work proposes two low power design techniques for a radio receiver. We have proposed a unified power optimal methodology for systematic system level design of a complete RF receiver. The proposed designed methodology was applied for the design of an 802.15.4 ZigBee receiver. The minimum power consumption for the ZigBee receiver, occurs by having the analog section give an output SNR of 1.3 dB and operating the digital section at a 1 bit resolution and 18MHz sampling frequency.

We have addressed the issue of design of front end for adaptive receivers and proposed two front end topologies,one suitable for low data rate applications and another for high data rate applications. The first topology,a merged LNA-Mixer designed for an adaptive ZigBee receiver uses a resistve input matching and uses segmented transistors to provide knobs to tune the noise figure and lineaity independently. The proposed topology potentially yields 5X power savings while adapting to 10dB of input signal level and 50% power savings while adapting to 8 dB of interferer level, without considering the implementation overhead of the tuning mechanisms. The LNA-Mixer

topology also provides a low voltage operation of upto 0.6V. The second topology, is an adaptive Common source LNA, which is inductively degenerated to achieve low noise figures required by high data rate applications like wirelss LANs. The topology uses an adaptive active degeneration inductor to maitain its input matching at acceptable levels while adapting for signal and interferer levels. The proposed adaptive inductively degenerated LNA provides a tuning range of around 6 dB for noise figure and 10dB for IIP3.

The proposed low voltage merged-LNA-Mixer topology has been prototyped in a test chip fabricated in 130nm UMC RFCMOS technology. Post chip Silicon validation of the proposed circuit is to be done.

7.2 Scope for Future Work

The research in this thesis can be taken forward in the following directions discussed in the sections below

7.2.1 Power Optimal Design Methodology for adaptive Receivers

The proposed power optimal design methodology can be extended to an adaptive receiver. It will be interesting to see that if the optimal power allocation between analog and digital section varies significantly with channel conditions. Also a criteria for identifying the optimal allocation,will be useful while building the power control system for adaptive receivers. The criteria may have its parallel in the power optimal criteria in digital design , where the optimal allocation between dynamic power and leakage power occurs when they are in the ratio 2:1.

7.2.2 Adaptive front ends for other class of receivers

The two front end topologies are suitable for narrow band receivers only. One can extend the same idea and modify it suitably to arrive at adaptive front end topologies for Ultra Wide Band receivers which are gaining popularity. Multi standard adaptive topologies also deserve investigtaion.

Appendix A

Pin details of Test Chip

A.1 Introduction

This appendix gives the details of the IO pins of the test chip. The test chip fabricated in 130nm UMC technology is a multiproject chip, which had a PLL and Frequency multiplier in addition to the LNA-Mixer circuit. the IO pins were shared among all the designs to effectively use the available pinouts in a CQFP-64 package.

A.2 Pin Details

IO Cells from Faraday 130nm High Gain IO Library were used in the IO design. The IO cells operated from a dedicated 3.3V supply whereas the core circuits operated from a 1.2 V supply. Figure A.1 show the layout snapshot of the test chip with the IO Pins labelled. The analog section of the IO ring, pins 4-21, are separated from the digital section, pins 23-64, by two power cut cells - left and right power cut cells - , (pin 3 and 22). 2 Pins at each end of each edge (Pins 1-2 15-18, 31-34, 47-50 are unusable, due to lack of space in the corners of the die for placing the IO Cells. Tables A.1 and A.2 give the detailed functionality of analog and digital pins respectively. Pins shared between two designs are named after the two functionalities it provide, with

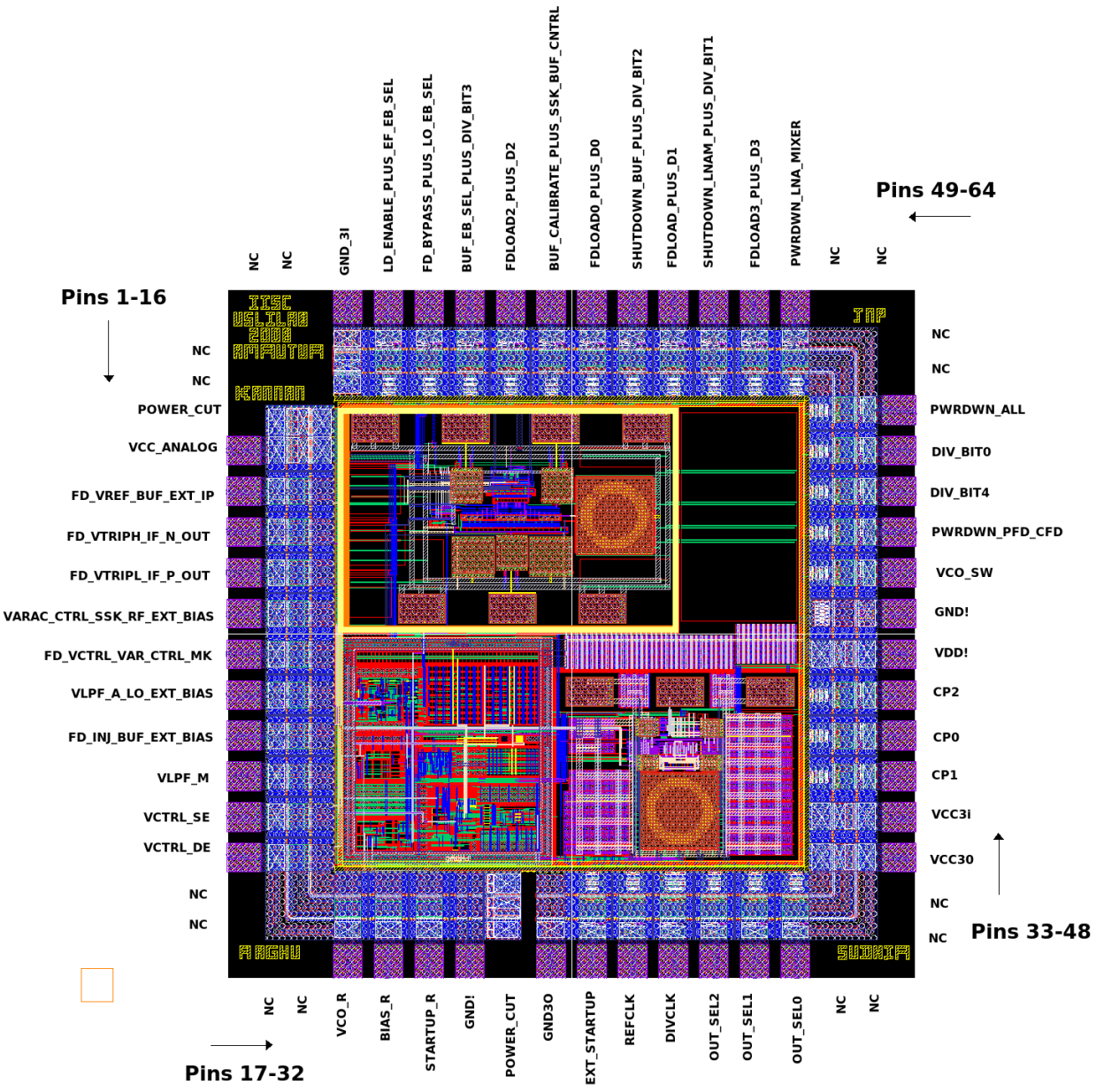

Figure A.1: Layout Snapshot of the test chip with IO Pins named

Table A.1: Functionalities of Analog IO pins

Pin	Pin Name	Pin Type	Functionality
3	POWER_CUT	NA	Left Power Cut To Separate Analog and Digital IO Cells
4	VCC_ANALOG	Power	Variable Supply Voltage for LNA-Mixer, maximum voltage-1.2v
5	FD_VREF_BUF_EXT_IP	Input	Used to calibrate the output buffer. A 3MHz(IF) signal is inputted through this pin.
6	FDVTRIPH_IF_N_OUT	Output	Negative terminal of differential IF output
7	FDVTRIPL_IF_P_OUT	Output	Positive terminal of differential IF output
8	VARAC_CONTROL _SSK_RF_EXT_BIAS	Input	External DC bias input to LNA transistor.
9	FD_VCONTROL_VAR _CTRL_MK	Input	Varctor control voltage to tune the LNA's operating band
10	VLPF_A_LO_EXT_BIAS	Input	External DC bias for the LO transistors
11	FD_INJ_BUF_EXT_BIAS	Input	External bias for Output buffer.

the word 'PLUS' in between them

Table A.2: Functionalities of Digital Pin

Pin	**Value**	**Description**
PWRDWN_LNA_MIXER	0	Normal Circuit Operation
	1	Shuts down LNA-Mixer and all its peripheral circuitry
FDLOAD3_PLUS_D3 to FD-	0	Mode Configuration bits controlling effective transistor width
LOAD0_PLUS_D0	1	no selection
SHUT_DOWN_LNAM_	0	Normal operation of LNA-Mixer
PLUS_DIV_BIT1		Continued on next page

Table A.2 – continued from previous page

Pin	Value	Description
	1	Shuts down LNA-Mixer while peripherals are working. Used to measure power of peripherals separately
SHUT_DOWN_BUF_ PLUS_DIV_BIT1	0	Normal operation of buffer
	1	Shuts down buffer without affecting LNAM. Used to measure power consumed by core LNAM circuitry
BUF_CALIBRATE PLUS SSK_BUF_CONTROL	0	LNAM Output is fed to Buffers
	1	External Input to Calibrate buffer is fed to the buffers.
BUF_EB_SEL PLUS_DIV_BIT3	0	Internal Bias is used for Buffers
	1	External Bias is used for Buffers
FD_BYPASS_ PLUS_LO_EB_SEL	0	Internal bias is used for LO branch
	1	External Bias is used for LO transistors
LO_ENABLE_ PLUS_RF_EB_SEL	0	Internal bias is used for input LNA branch of LNAM
	1	External Bias is used for input LNA branch of LNAM

A.3 Power supply and Ground Details

A separate pin VCC_{ANALOG} (pin 4) is used to supply a variable supply voltage to the LNA-Mixer.The output buffer operated from the supply marked as V_{dd}! (pin 40). A Separate 3.3V supply powers the VDD_3I and VDD_3O and these two pins are

shorted externally on the board designed to test the chip. All the Core circuits and IO Cells share the same ground. Though different ground pins are shown in the IO pin diagram, all the grounds are internally shorted.

Appendix B

Board Design for Test Chip

The fabricated design has to be tested for its functionality and performance. So a printed circuit board was designed for it along with the required interfacing circuits. The follwing are a few details about the board designed for the test chip.Figure B.1 shows the snapshot of the board schematic.

- The substrate used for the board is a 60mil FR4 board.
- All the digital configuration signals are provided with a jumper switch, which can be connected either to a 3.3V supply (Logic 1) or Ground (Logic 0).
- The 3 MHz input signal to calibrate the buffer is provided through a BNC cable.(Pin 5)
- A potentiometer is connected with the Bias_R pin so that the internal bias current is made tunable.

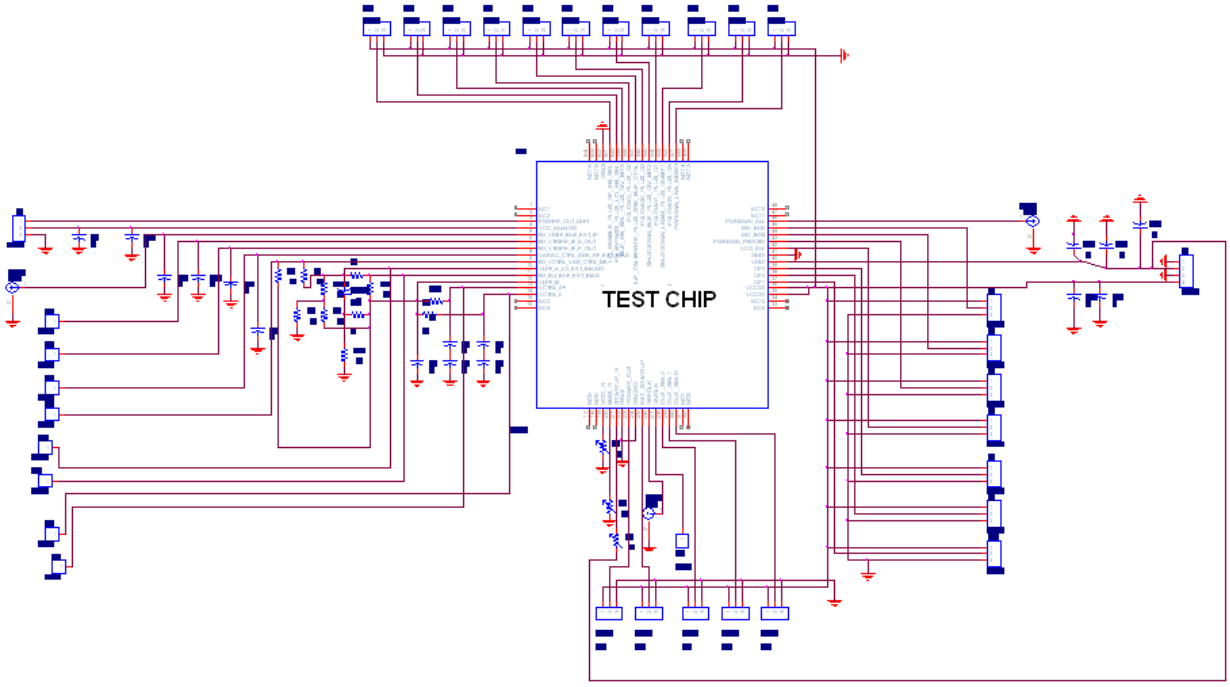

Figure B.1: Schematic of the Board for the test chip

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