ASIC Implementation of a Low Power BaseBand-Processor for UHF RFID Tag

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Abstract — **A novel digital baseband processor of an UHF RFID tag was presented based on the ISO/IEC 18000-6 type C standard. In order to enhance the signal-noise ratio in the return link, spread spectrum technique is used in addition to the FM0 encoding/Miller sub-carrier modulation. The tag supports all the 11 mandatory commands which are required by the 6C standard as well as the implementation of probabilistic/slotted anti-collision scheme and read/write operation to EEPROM. Low power techniques are adopted to reduce the instantaneous power and average power. The chip was designed and fabricated using 0.18um 6 metal layers CMOS technology. Area of the proposed baseband processor is 0.5mm^2. From the measurement result, the overall power consumption is about 16uW at the minimum voltage of 1.04V.**

Index Terms— **RFID; baseband processor; low power; spread spectrum**

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0 INTRODUCTION

Nowadays the application of Radio Frequency Identification (RFID) can be found in more and more fields, such as logistics, manufacturing and transportation, as well as tickets, mobile phones, secure access and many more[1]. To meet the sharply increasing market requirements, the preferred RFID system must exhibit features like low cost, long operation range and high data rate, requiring small and low power passive fully integrated circuits.

Tags usually work in adverse environments, so it is important to enhance their anti-disturbance capacities and reduce the Bit Error Rate (BER) of RFID communication. What's more, the mass usage of RFID has raised concerns regarding security and privacy issues [2].

In this paper, we present a high performance digital processor of passive UHF RFID tag in fully compliance with but not limited to the ISO/IEC 18000-6 type C standard which takes into account of the issues mentioned above——of low-power and low-BER, as well as the strong anti-disturbance capacities.

This paper is organized as follows. In Sect.1 and Sect.2 below, the air interface standard and system architecture are presented, while Sect.3 more specifically describes the low power strategies in the design of each sub-module. Realization of spread spectrum is presented in Sect.4. Sect.5 discusses the ASIC implementation and verification result. Further expected development and conclusions are eventually drawn in Sect.6

1. AIR INTERFACE STANDARD

In 2006, the EPC Class-1 Generation-2 UHF RFID Protocol was absorbed into the ISO/IEC18000 series of RFID standard as ISO/IEC 18000-6 Type C, accommodating the latest development of passive RFID technology in the UHF frequency band in the air interface communication [3].

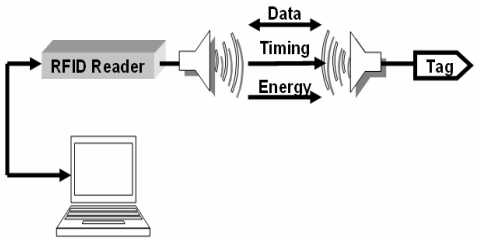

Fig.1. RFID system
图1 RFID 系统

The RFID system is shown in fig.1. Interrogators transmit information to tags by modulating RF signals in the 860 MHz to 960 MHz frequency range, the tags receive both information and operating energy from this RF signal. The interrogator receives information from a tag by transmitting an un-modulated RF signal to the tag and listening for a backscattered reply. The tag responds by modulating the reflection coefficient of its antenna, thereby backscattering an information signal to the interrogator [3]. Tags are usually passive, meaning that they receive all of their operating energy from the interrogator's RF waveform.

2. SYSTEM ARCHITECTURE AND REQUIREMENT

Baseband-processor is one of the major parts of the RFID tag, which determines the tag functions and performance.

The baseband-processor fully implements the ISO/IEC 18000-6 type C standard, which performs PIE decoding, CRC checking, probabilistic/slotted anti-collision arithmetic, memory accessing, FM0 encoding, as well as all the inventory and assess commands such as the select, query, write, read, lock, kill and so on.

Various techniques are taken to achieve high performance. Major considerations focus on the power issues especially the peak power in each sub-module design [4]. Moreover, Spread

spectrum technology is introduced into the backscattered communication link to enhance the anti-disturbance capabilities and the security level of the tag [5].

3. LOW POWER STRATEGIES IN TAG DIGITAL CORE DESIGN

3.1 Reusing of CRC Modules

CRC checking is a relatively mature technique, but the CRC process of 6C protocol is unique — the CRC check type in forward links and return link are different, and in each link exists 3 CRC types including CRC16, CRC5 and NO_CRC. Fortunately, the interrogators and tags are not required to talk simultaneously, rather, communications are half-duplex, meaning that interrogators talk and tags listen, or vice versa.

So the same CRC modules can be adopted in both the forward link and return link at different times, and the same registers are used for both CRC16 and CRC5. For realization, two parameters of "crc_type" and "isT2R" are used to control the state machine of CRC checking.

Since the CRC type can be determined only after the corresponding command is recognized, but the data transmission between the modules is serial, so we initialize the "crc_type" as "CRC_UNKNOWN" firstly, and then set as CRC16 or CRC5 after the command code is identified.

In this way, we reduce the area and lower the power of the chip by the method of reusing the CRC modules.

3.2 Idle State of Main Controller

The Main Controller is the control unit of the baseband processor which is mainly a FSM. It sends control signals to the sub-modules and receives status signals from the sub-modules.

There are four main states here —— STATE_INIT, STATE_KILLED , STATE_WORK, STATE_IDLE.

When the tag goes into the RF field, it starts the STATE_INIT state and initializes the tag. In this state, the tag should be tested if it is killed or not, and then the access password and kill password need be read out from the RESERVED Memory if it is not killed, otherwise the tag goes into the STATE_KILLED state.

If the tag is not killed, the sub-modules are waked up at different times into the STATE_WORK when needed. After the tag finishes working, it will go to STATE_IDLE, and the Tag keeps idle in this state utile next work cycle.

With the design method mentioned above, tags will not consume power in the STATE_IDLE, so both the overall power and the peak power of the processor can be reduced significantly.

3.3 Precalculation of Random Number Generator (RNG) and Slot Counter

In the state of STATE_ INIT, one more task is generating a 16-bit Pseudo random number (RNG) and a 15-bit slot counter using M sequence which based on the D flip-flop shifting and feedback logic circuits. To achieve the randomness of the Random Number, the initial value of m registers is determined by a time-variable. So an internal counter "init_data" is set up here. When the tag powers up, the "init_data" begins to work (plus one) at each rising clock edge; in this way, it can be seen as a good random number, hence can be used as the initial value of M sequence register and ensure the randomness of both the RNG and slot counter.

Such kind of calculations mentioned above are pretreated at the time of powering up before starting to receive command, when most of the modules don't work, which will reduce the peak power of the processor [6].

3.4 Special Process for Receiving the "Select" Command

For receiving the commands, tag works in state of receiving command code (RECEIVING_HEADER) and state of receiving command body (RECEIVING_SERIAL).

According to the standard, of all the command bodies, the command body of "select" contains "mask", which may need up to 255 registers for storage and is waste of resource. So here we set up three more states for the receiving of "select". The tag receives and stores the command body before "mask" in RECEIVING_SEL_1 state, and after "mask" in RECEIVING _SEL_2 state, while receiving and storing the "mask" in the RECEIVING_SEL_ MASK state, as shown in Table1.

Table1 State of Receiving

表1 命令接收状态表

Receiving_State	Symbol
RECEIVING_HEADER	0
RECEIVING_SEL_1	1
RECEIVING_SEL_MASK	2
RECEIVING_SEL_2	3
RECEIVING_SERIAL	4

While in the state of RECEIVING_SEL_MASK, two 16-bit registers (A and B) was adopted to storage the content of mask. Register A is used to receive the first 16 bit, and update the register B with the content of A when A is full. Then the tag reads the corresponding content from the EEPROM and compares them with the content of B while A is reused to receive and store the next 16 bit.

In this way, we can receive and compare up to 250 bits of the content of "mask" by using just 16 registers, which not only reduces nearly 230 registers, but also accelerates the data response rate.

3.5 Special Response Treatment for ACK and READ

As we know, the commands of READ and ACK have the variable-length response which needs to be read from the memory, but data-width of memory is 8 bit, so here we use the similar method as we deal with the receiving of the

command body of select. Two 16-bit registers of A and B are adopted here. Firstly the tag reads 16 bits of data from the memory into register A, then updates the register B with the contents of A, and outputs response serially from B; while at the same time reads the next 16 bits of data from the memory to A.

This method can lead to the reduction of power and the tag is able to deal with higher signal processing rate.

3.6 Register Reuse

According to the 6C protocol, each command has different structure, so the strategy of register reuse is proposed here. We use a relative large receiving-register (about 56 bit) to receive and store different commands at different times, and then deal with the command content after the respective command reception is completed later on. When the tag goes into the state of response, the receiving-registers are in the state of idle and therefore can be reused to store response data.

Such considerations take full account of the register's availabilities at different times and raise the utilization of resource, which also reduce the overall power consumed by the chip.

4. REALIZATION OF SPREAD SPECTRUM TECHNIQUE

As pointed out at the beginning of the paper, tags are passive and backscatter information signals to the interrogator by modulating the reflection coefficient of its antenna. Most of time, the energy is weak in the return link and the tag is vulnerable to the impact of noise and interference, which can lead to the deterioration of communication performance.

In this design, we adopt spread spectrum (SS) technique in the return link [7]. Opposed to regular narrowband communication, the SS process is a wideband technology.

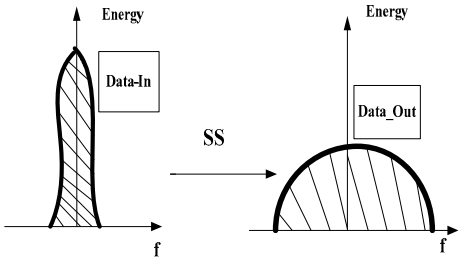

Fig.2. Spread Spectrum
图 2 扩频原理

To apply the SS technique, we simply inject a pseudo-random number (PRN) in the data level of backscattered transmitting chain before the antenna. That injection is just called the spreading operation [8]. The effect is to diffuse the information into a larger bandwidth as shown in fig.2. Conversely, we can remove the SS code at a point in the receive chain before data retrieval. So the main SS characteristic is the presence of PRN, the codes are digital sequences that must be as long and as random to appear as "noise-like". Here, we adopt a 6-bit M-Sequence based on a feedback shift register, by which the typical SS processing gain will run 63-fold increase.

Since the total energy is the same, it is widely spread in frequency after SS process, so the spectral density is very low. Application of such SS technique effectively rejects the intentional or un-intentional interference and jamming signals in the RFID return link because they do not contain the SS key; only the desired signal, which has the key, will be seen at the authorized receiver.

In a word, the application of spread spectrum greatly improves the signal-noise-ratio of the RFID communication system.

5. ASIC IMPLEMENTATION AND VERIFICATION RESULT

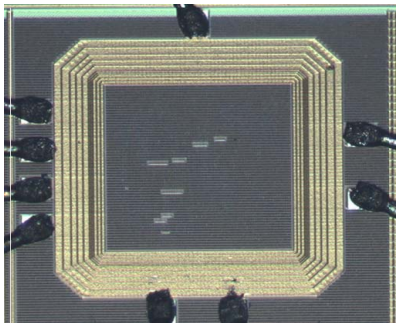

Fig 3. Photomicrograph of the chip
图 3 芯片版图

The baseband processor is designed as a full digital ASIC with Synopsys Design Complier tolls for synthesizing and Cadence SOC Encounter tools for placing and routing. Finally, the chip was fabricated using 0.18um 6 layers standard CMOS technology successfully. Fig.3. shows the photomicrograph of the developed chip, which is 0.5mm*0.5mm in size.
The chip measurement is implemented with Agilent 93000 C200e test system and Agilent Infiniium 54845 AR Oscillograph. Fig4. shows the results of the functional measurement (Clock Frequency = 2MHz), from which we can see that the tag is able to receive commands and output the corresponding responses successfully.

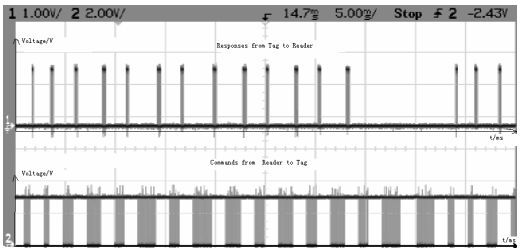

Fig.4. Command and Response Measurement
图4 命令发送和应答测试

Table 2 and Table 3 show the average power measurement (including the memory) at different voltages and

different clock frequencies. From the results, the chip is able to work at a wide voltage and clock frequency range. The minimum voltage for the chip is 1.04V. The power consummation will be minimized while the operation voltage and frequency is as low as possible, which points out the direction of future low power investigation —— low clock frequency and low voltage.

Table2 Implementation Result 1
表2 测试结果1

Voltage = 1.8V

Clock Frequency（MHz）	2 5	2	1.8	1.4	0.3
Current (uA)	68	59	52	41	9

Table3 Implementation Result 2
表3 测试结果2

Clock Frequency = 2MHz

Voltage (V)	3	2.5	1.8	1.2	1.04
Current (uA)	140	98	59	34	30

Actually, we are more concerned about the consumption of peak power (instantaneous power) rather than the average power. Fig.5 shows instantaneous power consumption of the whole baseband processor.

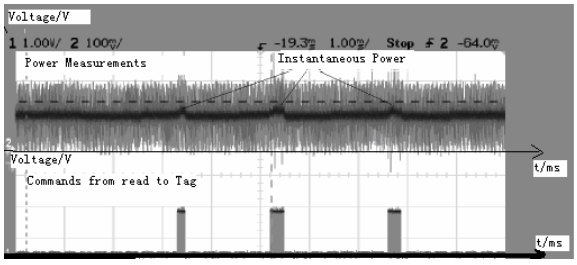

Fig.5. Peak Power Measurement
图 5 峰值功耗测试结果

It is clear that the chip has the maximum power consumption when the tag is in states of commands processing and response, especially the later. Careful analysis of peak power consumption reveals that, compared with other commands, the process of commands of ACK and READ consumes much more power, followed by commands of LOCK, WRITE and KILL. The similarity of all of these commands is that they need frequently read/write operations from/to the EEPROM. For reducing peak power consumption, it is required to keep balance of the power consumption distribution among sub-modules and at different times.

6. CONCLUSION

A baseband processor for UHF RFID tag chip is presented. In the design, several techniques are adopted to achieve lower power consumption and higher data rate; moreover, strategies such as spread spectrum technology are carried out to ensure the communication reliability. Finally, detailed chip measurements showed that the chip fulfills the design objectives.

Future works include the realization of spread spectrum receiver in the RFID reader system to reconstitute the information in its original bandwidth and researching for more strategies to further reduce the power consumption of the baseband processor.

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一种低功耗UHF RFID标签基带处理器的ASIC实现

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摘要： 设计实现了一种新颖的超高频RFID标签的基带处理器。该标签以ISO/IEC 18000-6C协议为基础，但在反向链路通信方面，在原协议FM0编码/Miller调制副载波的基础上增加了扩频编码的实现，目的是提高反向链路的通信信噪比。本设计支持协议要求的所有11条强制命令的读写操作，概率/分槽防冲突算法，以及对存储器的读写操作。设计中采用了低功耗技术，显著降低了芯片的平均功耗和峰值功耗。该芯片采用0.18um 6层金属CMOS工艺进行流片，面积为0.5mm²。测试结果表明，芯片消耗功耗约为16uW，最低工作电压为1.04V。

关键词：RFID 标签，基带处理器，低功耗，扩频

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