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High performance InP/InAlAs/GaAsSb/InP double heterojunction bipolar transistors

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Abstract

DC and RF characteristics of InP/InAlAs/GaAsSb/InP double heterojunction bipolar transistors (DHBTs) are reported. The device heterostructures include InAlAs spacer layer between InP emitter and GaAsSb base layer. The impact of thin InAlAs spacer layer was investigated by comparing the DC characteristics of large-area devices fabricated on InP/InAlAs/GaAsSb/InP and conventional InP/GaAsSb/InP heterostructures. By suppressing the base tunneling current and surface recombination current, the DHBTs with thin InAlAs spacer layer exhibited 5 decade lower crossover current of 7×10^{-11} A (collector current at unity current gain) than conventional InP/GaAsSb/InP DHBT that exhibited crossover current of 4×10^{-6} A. The current gain also improved twice by the impact of thin InAlAs layer. To investigate the high-frequency characteristics of InP/InAlAs/GaAsSb/InP DHBTs, small-area devices employing laterally etched undercut micro-airbridges were fabricated. The unity current gain cut-off frequency, f_T, of 100 GHz was obtained from a 1×30 μm^2 emitter DHBT.

Keywords: Heterojunction bipolar transistors; Spacer layer; GaAsSb; InAlAs; Compound semiconductor

1. Introduction

InP/GaAsSb/InP double heterojunction bipolar transistors (DHBTs) have drawn great attention for their potential applications in the area of ultra-high speed low power electronic circuits [1]. GaAsSb-based DHBTs have inherent advantages over InGaAs-based DHBTs such as simple heterostructures without complicated collector design, low base access resistance, and low surface recombination currents [2–4]. However, InP/GaAsSb/InP DHBTs suffer from high tunneling recombination current because of electron pile up at the InP/GaAsSb emitter–base junction [5], which results in low current gain especially under low current operating conditions. The high tunneling recombination current is due to the spatially indirect type-II transition at InP/GaAsSb interface [6]. Type-II heterostructure of InP/GaAsSb junction is beneficial at a collector side, but it is detrimental at an emitter–base junction. To overcome this shortcoming of conventional InP/GaAsSb/InP DHBTs, several emitter designs have been investigated [5,7,8]. It has been reported that high quality InAlAs/GaAsSb heterostructure can be achieved much easier than InP/GaAsSb heterostructures [8]. Elegant growth techniques have been employed to achieve nearly ideal InP/GaAsSb E–B interface by utilizing MOCVD (metal organic chemical vapor

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deposition) method [9,10]. However it is very difficult to produce high quality InP/GaAsSb heterostructures by MBE (molecular beam epitaxy) so that InAlAs is a good candidate for emitter material especially for the GaAsSb-based HBTs grown by MBE. Another concern regarding aluminum containing compound semiconductor alloys grown by MBE system is high concentration of deep traps giving rise to degradation of low-frequency noise characteristics of HBTs [11,12]. It can be circumvented by avoiding the use of full InAlAs emitter.

In this study, a thin 15 nm-thick InAlAs spacer layer was inserted between the InP emitter and GaAsSb base layer to enjoy the advantages of InAlAs/GaAsSb interface and superior carrier transport properties of InP emitters with minimal effect of deep traps in InAlAs layer. The device performances of InP/InAlAs/GaAsSb/InP and conventional InP/GaAsSb/InP DHBTs were compared to investigate the impact of InAlAs spacer layer on the DC characteristics of DHBTs. We also report the RF characteristics of small-area devices ($1 \times 30\ \mu m^2$ emitter) fabricated on InP/InAlAs/GaAsSb/InP heterostructures.

2. Experiments

The epitaxial structures for DHBTs were grown on semi-insulating InP substrates by utilizing molecular beam epitaxy (MBE) system. Two device heterostructures used in this experiment are presented in Table 1 and band diagrams of both device heterostructures are illustrated in Fig. 1. Sample A (InP/InAlAs/GaAsSb/InP) is a DHBT heterostructure which has a 15 nm-thick InAlAs spacer layer between the InP emitter and the GaAsSb base layer. Sample B (InP/GaAsSb/InP) is a conventional GaAsSb DHBT layer which has abrupt InP/GaAsSb heterointerfaces at both E–B (emitter–base) and B–C (base–collector) junctions. To investigate the effect of the thin InAlAs spacer layer on DC characteristics of DHBTs, large-area devices with emitter sizes of 80×40, 50×64 and $32 \times 100\ \mu m^2$ were fabricated on the two DHBT structures. Wet-etch and optical lithographic techniques were utilized in the fabrication of DHBTs. The InGaAs emitter cap, GaAsSb base and InGaAs collector contact layers were etched using H_3PO_4:H_2O_2:H_2O solution. The InP emitter, InAlAs spacer, InP collector and sub-collector layers were etched with HCl-based solution. Non-alloyed ohmic metallization schemes consisting of Ti/Pt/Au and Pd/Ir/Au were used for n-type and p-type ohmic contacts. Small-area DHBTs having 1×30 and $2 \times 20\ \mu m^2$ self-aligned emitters were also fabricated to investigate the high-frequency characteristics of InP/InAlAs/GaAsSb/InP DHBTs. The laterally etched undercut micro-airbridges were employed in the fabrication of small-area DHBTs to improve RF characteristics [13]. BCB layer was used for passivation and planarization prior to interconnecting emitter metal deposition.

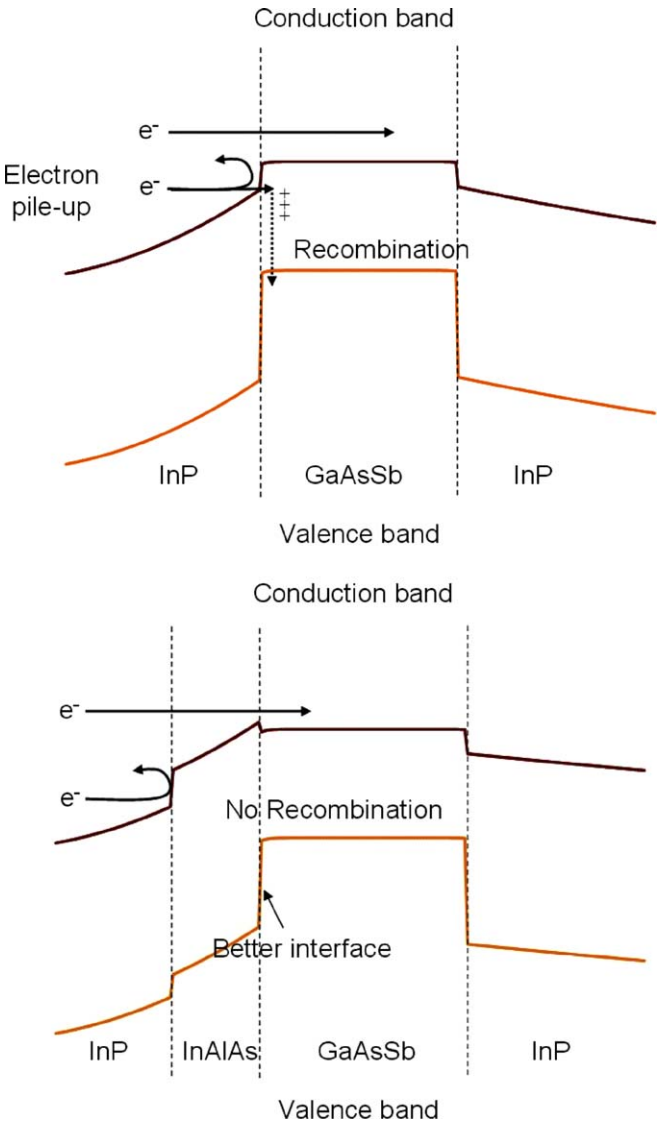

Fig. 1. The impact of InAlAs spacer layer of the InP/InAlAs/GaAsSb/InP DHBT.

Table 1
Device heterostructures of sample A (InP/InAlAs/GaAsSb/InP) and sample B (InP/GaAsSb/InP)

	Sample A	Sample B
Emitter cap $In_{0.53}Ga_{0.47}As$	200 nm, Si: 2×10^{19} cm^{-3}	50 nm, Si: 2×10^{19} cm^{-3}
Emitter InP	50 nm, Si: 5×10^{18} cm^{-3}	100 nm, Si: 4×10^{18} cm^{-3}
Emitter InP	70 nm, Si: 4×10^{17} cm^{-3}	70 nm, Si: 3×10^{17} cm^{-3}
Spacer $In_{0.52}Al_{0.48}As$	15 nm, Si: 4×10^{17} cm^{-3}	–
Base $GaAs_{0.49}Sb_{0.51}$	35 nm, C: 6×10^{19} cm^{-3}	40 nm, C: 5×10^{19} cm^{-3}
Collector InP	450 nm, Si: 1×10^{16} cm^{-3}	220 nm, Si: 3×10^{16} cm^{-3}
Collector contact $In_{0.53}Ga_{0.47}As$	30 nm, Si: 2×10^{19} cm^{-3}	20 nm, Si: 1×10^{19} cm^{-3}
Subcollector InP	550 nm, Si: 2×10^{19} cm^{-3}	470 nm, Si: 4×10^{18} cm^{-3}
S.I. InP Substrate		

3. Results and discussion

3.1. The effects of the thin InAlAs spacer layer

The DC characteristics of the large-area devices were measured by using HP 4155B semiconductor parameter analyzer. Base sheet resistances of sample A and sample B were measured by TLM (transfer length method) were 960 Ω/□ and 880 Ω/□, respectively. Fig. 2 shows the Gummel plots of the two types of DHBTs. There is a remarkable difference in the base currents of the two devices. The ideality factor of base current was reduced from 1.7 (sample B) to 1.26 (sample A) by introducing InAlAs spacer layer. From this observation, the dominant base current of sample A is determined to be diffusion current, while that of sample B is recombination current. The InAlAs spacer layer prevents electron pile up which occurs at type-II InP/GaAsSb E–B interface as shown in Fig. 1. By avoiding electron pile up at InAlAs/GaAsSb E–B junction, the tunneling recombination current from the emitter conduction band to the base valance band was suppressed. This effect resulted in five decade lower crossover current of 7×10^{-11} A (collector current at unity current gain) in comparison with that of conventional InP/GaAsSb/InP DHBT which was measured to be 4×10^{-6} A. Current gain also improved from 16 to 37 due to the suppressed base current in sample A. The almost same current gain characteristics were observed in the InP/InAlAs/GaAsSb/InP DHBTs with different emitter periphery to area ratios (80×40, 50×64 and 32×100 μm^2 emitter) as shown in Fig. 3. It indicates that the current gain is determined by the bulk characteristics rather than the surface characteristics of the base material [14]. The dominant surface recombination current in InP/GaAsSb/InP HBTs is direct electron injection from InP emitter sidewall to the extrinsic GaAsSb base [3]. This surface recombination current may be less severe compared in InAlAs emitter HBTs than InP emitter HBTs due to the stronger surface depletion in InAlAs emitter sidewall than InP emitter sidewall.

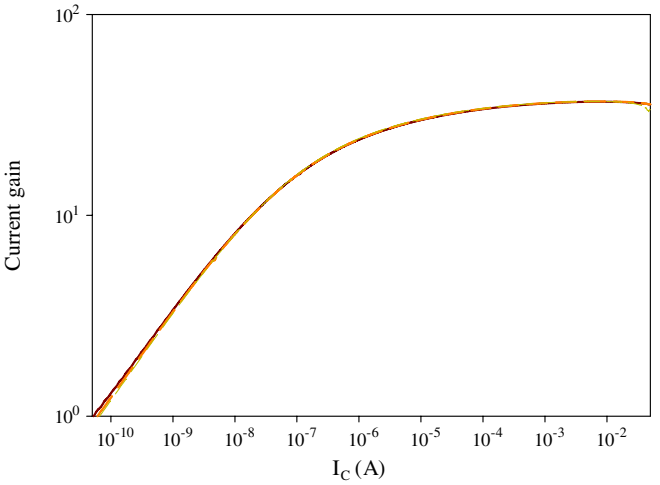

Fig. 3. The current gain as a function of collector current characteristics for sample A with various emitter periphery to area ratios (— $A_E = 80 \times 40$ μm^2, --- $A_E = 50 \times 64$ μm^2, –··– $A_E = 32 \times 100$ μm^2).

There are two current-transport mechanisms at heterojunction interface: diffusion limitation mechanism and the conduction band barrier limitation mechanism [15]. The dominant carrier injection mechanism at E–B (emitter–base) junction of the HBTs could be identified by comparing collector currents (in forward active mode) and emitter currents (in reverse active mode) of the devices. When there is a significant conduction band discontinuity, ΔE_C, at E–B junction, the carrier injection is dominated by tunneling or drift process and the ideality factor of the collector current in the forward active mode is much higher than unity value [16]. As shown in Fig. 4, the collector current of sample A has ideality factor of 1.07 that is very close to 1. It indicates that the current injection at emitter–base junction is dominated by diffusion process and the conduction band

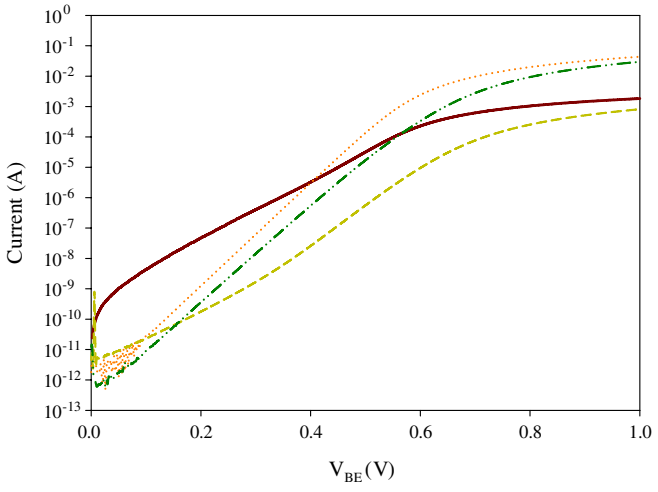

Fig. 2. Gummel plots of 80×40 μm^2 GaAsSb DHBTs (— I_B of sample B, ··· I_C of sample B, --- I_B of sample A, –··– I_C of sample A).

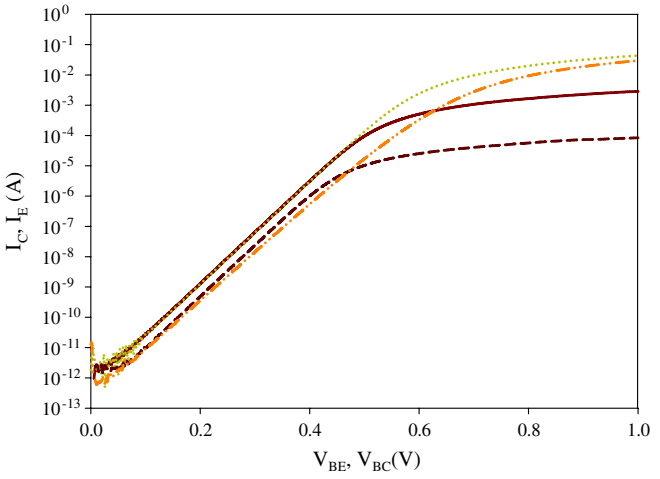

Fig. 4. I_C and I_E of 80×40 μm^2 GaAsSb DHBTs in forward and reverse active modes (— I_E of sample B, ··· I_C of sample B, --- I_E of sample A, –··– I_C of sample A).

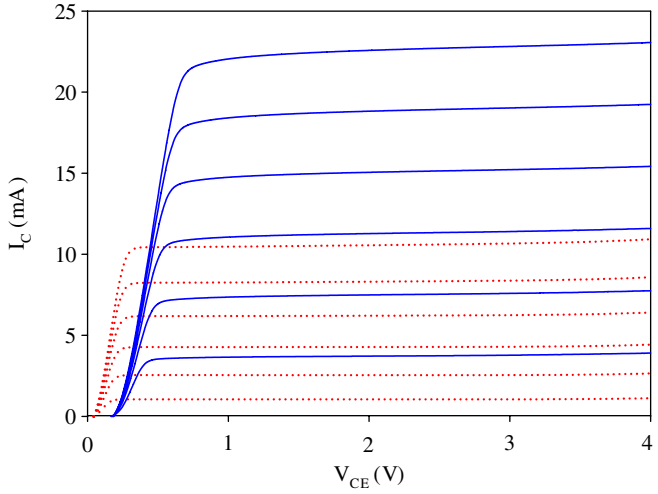

Fig. 5. Common-emitter output characteristics with base current step of 100 μA. Emitter area is 80×40 μm^2 (— Sample A; ··· Sample B).

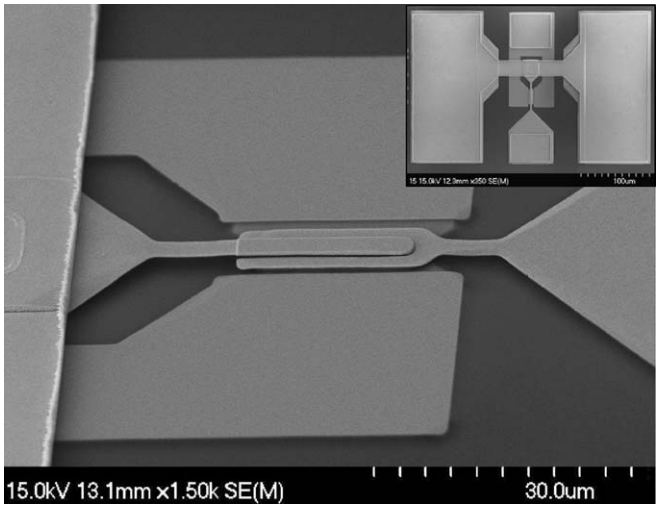

Fig. 6. SEM micrograph of the fabricated 2×20 μm^2 DHBT.

discontinuity is insignificant for InP/InAlAs/GaAsSb E–B junction design.

As shown in Fig. 5, higher current gain was obtained in sample A which includes a thin InAlAs spacer layer. Another important parameter in DHBTs is the collector–emitter offset voltage (V_{offset}). V_{offset} of sample A and B are 175 and 43 mV, respectively. The offset voltage can be written as:

$$V_{offset} = \left(1 - \frac{n_{BC}}{n_{BE}}\right) \cdot [V_{BE} - R_B I_B] + \frac{n_{BC}}{n_{BE}} R_E I_B + \frac{n_{BC} kT}{q} \cdot \ln\left(\frac{A_C J_{CS}}{A_E \alpha_N J_{ES}}\right) \quad (1)$$

where n_{BE} and n_{BC} are the ideality factors of the E–B and B–C heterojunction, J_{ES} and J_{CS} are the magnitudes of the emitter and collector saturation currents at $V_{BC} = V_{BE} = 0$, α_N is the forward current gain, R_E and R_B are emitter and base series resistances [15]. The higher V_{offset} of sample A is due to an unsymmetrical nature of the InP/InAlAs/GaAsSb/InP DHBT structure, which results in the distinct ideality factors and saturation currents in I_C and I_E. Different ideality factors and saturation currents in emitter and collector currents leads to higher V_{offset} [17,18].

3.2. Small-area InP/InAlAs/GaAsSb/InP DHBTs

To investigate the high-frequency characteristics of InP/InAlAs/GaAsSb/InP DHBTs, small-area DHBTs having emitter area of 1×30 and 2×20 μm^2 were fabricated. The SEM micrograph of the fabricated 2×20 μm^2 DHBT with laterally etched undercut micro-airbridges is presented in Fig. 6.

Fig. 7 shows the common-emitter output characteristics of a typical 1×30 μm^2 DHBT. The measured peak current gain is 32. The offset voltage and the ratio of the base–collector junction area (A_C) to the emitter–base junction area (A_E) have a logarithmic relationship as shown in Eq. (1). The small-area devices with large ratio of A_C/A_E resulted

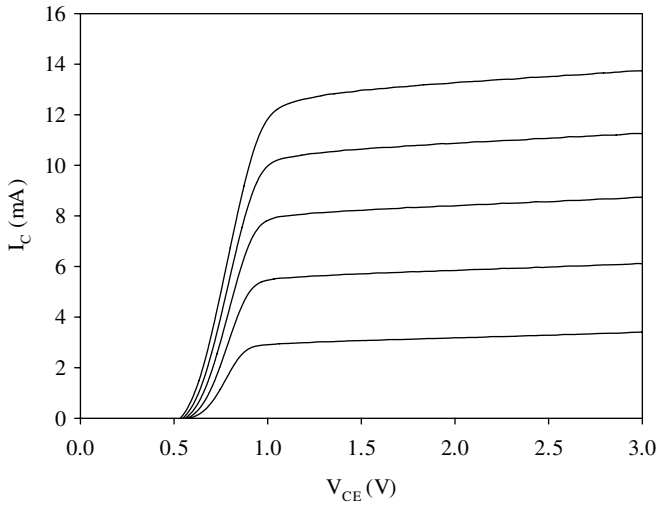

Fig. 7. Common-emitter output characteristics of 1×30 μm^2 InP/InAlAs/GaAsSb/InP DHBTs with base current step of 100 μA.

in the higher V_{offset} than the large-area devices although both devices had the same InP/InAlAs/GaAsSb/InP heterostructure. A high breakdown voltage of 6.6 V (BV_{CEO}) was measured for the 1×30 μm^2 emitter InP/InAlAs/GaAsSb/InP DHBTs whose breakdown voltage was defined at collector current of 100 μA.

On-wafer microwave *S*-parameter measurements were performed on InP/InAlAs/GaAsSb/InP DHBTs at frequencies up to 40 GHz, using an HP8510C vector network analyzer. Fig. 8 shows the common emitter short circuit current gain (h_{21}) of the typical small-area (1×30 and 2×20 μm^2) DHBTs. Current gain curves were extrapolated with a −20 dB/decade roll-off to obtain unity current gain cut-off frequency, f_T. Unity current gain cut-off frequencies were measured to be 60 and 100 GHz for 2×20 and 1×30 μm^2 emitter DHBTs, respectively. For the maximum f_T values, the transistors were biased at $V_{CE} = 2.5$ V and 2 V and $I_C = 12.2$ mA and 18.5 mA for 2×20 and

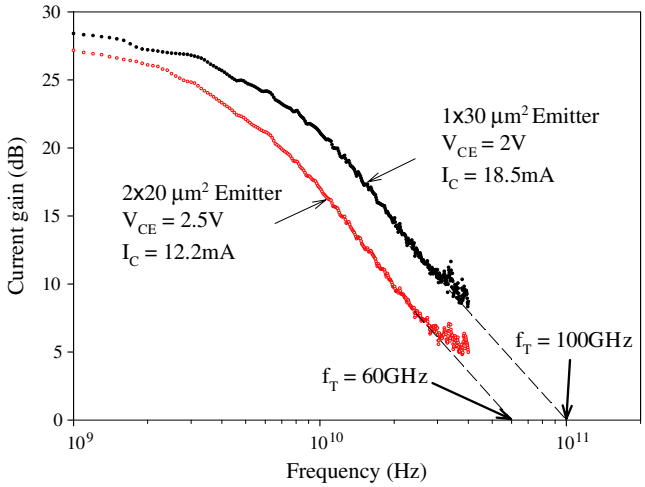

Fig. 8. Frequency dependence of h_{21} for InP/InAlAs/GaAsSb/InP DHBTs with 1×30 and 2×20 μm^2 emitter sizes.

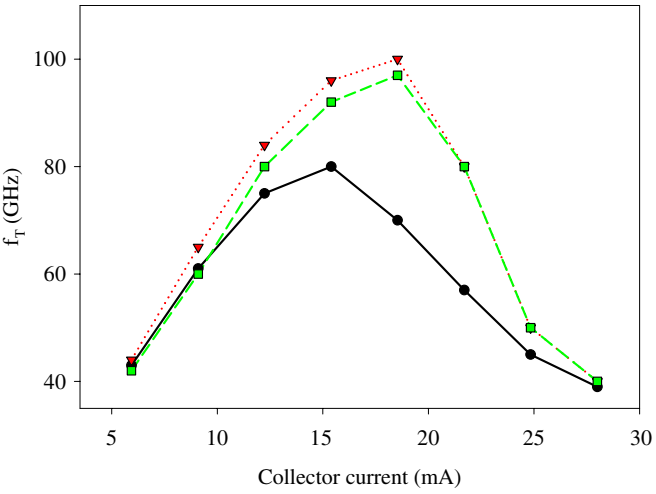

Fig. 9. Common emitter current-gain cut-off frequency (f_T) versus collect current at various V_{CE} for 1×30 μm^2 InP/InAlAs/GaAsSb/InP DHBTs. (–●– $V_{CE} = 1$ V, –▼– $V_{CE} = 2$ V, –■– $V_{CE} = 3$ V).

1×30 μm^2 emitter DHBTs, respectively. A peak maximum oscillation frequency, f_{MAX}, was also extracted from the measured S-parameter. A relatively low f_{MAX} of 62 GHz for 1×30 μm^2 emitter DHBTs may be ascribed to the large base–collector parasitic capacitance C_{BC}, which can be improved by undercut etching of collector layer and further scaling of base width.

The variation of f_T with collector current for the 1×30 μm^2 emitter InP/InAlAs/GaAsSb/InP DHBTs was measured at $V_{CE} = 1$, 2 and 3 V as shown in Fig. 9. A peak f_T of 100 GHz is obtained at collector of 18.5 mA. When the collector current was further increased beyond 18.5 mA, f_T's was degraded. The reduced f_T at high collector current can be ascribed to Kirk effect [19].

4. Conclusion

The performances of InP/InAlAs/GaAsSb/InP and InP/GaAsSb/InP DHBTs were compared and the impact of the thin InAlAs spacer layer was investigated. The InP/InAlAs/GaAsSb/InP DHBTs exhibited the improved DC characteristics by effectively suppressing tunneling recombination at E–B junction. The DC current gain of 37 and very low crossover current of 7×10^{-11} A were demonstrated. The conduction band discontinuity, ΔE_C, at InAlAs/GaAsSb interface was also found out to be negligible. The microwave performance of InP/InAlAs/GaAsSb/InP DHBTs was also characterized. The current-gain cut-off frequency of 100 GHz was obtained for 1×30 μm^2 emitter DHBTs.

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References

[1] Dvorak MW, Bolognesi CR, Pitts OJ, Watkins SP. 300 GHz InP/GaAsSb/InP double HBTs with high current capability and $BV_{CEO} \geqslant 6$ V. IEEE Electron Dev Lett 2001;22:361–3.
[2] Jang JH, Cho HK, Bae JW, Pan N, Adesida I. Low-resistance Pd/Ir/Au ohmic contacts on p-GaAsSb. Electron Lett 2004;40:1550–1.
[3] Tao N, Liu HG, Bolognesi CR. Surface recombination currents in type-II NpN InP–GaAsSb–InP self-aligned DHBTs. IEEE Trans Electron Dev 2005;52:1061–6.
[4] Bolognesi CR, Liu HG, Tao N, Zhang X, Bagheri-Najimi S, Watkins SP. Neutral base recombination in InP/GaAsSb/InP double-heterostructure bipolar transistors: Suppression of Auger recombination in p+ GaAsSb base layers. Appl Phys Lett 2005;86:253506.
[5] Oda Y, Yokoyama H, Kurishima K, Kobayashi T, Watanabe N, Uchida M. Improvement of current gain of C-doped GaAsSb-base heterojunction bipolar transistors by using an InAlP emitter. Appl Phys Lett 2005;87:023503.
[6] Yi SS, Chamberlin DR, Girolami G, Juanitas M, Bour D, Moll N, et al. Growth and properties of GaAsSb/InP and GaAsSb/InAlAs superlattices on InP. J Cryst Growth 2003;248:284–8.
[7] Zhu X, Pavlidis D, Zhao G. First high-frequency and power demonstration of InGaAlAs/GaAsSb/InP double HBTs. Int Conf on Indium Phosphide Related Materials 2003:149–52.
[8] Zhu HJ, Kuo JM, Pinsukanjana P, Jin XJ, Vargason K, Herrera M, et al. GaAsSb-based HBTs grown by production MBE system. Int Conf Indium Phosphide Related Materials 2004:338–41.
[9] Bolognesi CR, Matine N, Dvorak MW, Xu XG, Hu J, Watkins SP. Non-Blocking collector InP/GaAsSb/InP double heterojunction bipolar transistors with a staggered lineup base–collector junction. IEEE Electron Dev Lett 1999;20:155–7.
[10] Liu HG, Wu JQ, Tao N, Firth AV, Griswold EM, MacElwee TW, et al. High performance InP/GaAsSb/InP DHBTs grown by MOCVD on 100 mm InP substrates using PH3 and AsH3. J Cryst Growth 2004;267:592–7.
[11] Yamanaka K, Nartsuka S, Kanamoto K, Mihara M, Ishii M. Electron traps in AlGaAs grown by molecular-beam epitaxy. J Appl Phys 1987;161:5062–9.
[12] Costa D, Harris JS. Low-frequency noise properties of n–p–n AlGaAs/GaAs heterojunction bipolar transistors. IEEE Trans Electron Dev 1992;39(10):2383–94.
[13] Tadayon S, Metze G, Cornfeld A, Pande K, Huang H, Tadayon B. Application of micro-airbridge isolation in high speed HBT fabrication. Electron Lett 1993;29(1):26–7.

[14] Song JI, Palmstrom CJ, Van der Gaag BP, Hong WP, Hayes JR, Chough KB. High-performance InP/InGaAs heterojunction bipolar transistors with highly carbon-doped base grown by chemical beam epitaxy. Electron Lett 1993;29:666–7.
[15] Yan BP, Hsu CC, Wang XQ, Yang ES. Current transport mechanism in InGaP/GaAsSb/GaAs double-heterojunction bipolar transistors. Appl Phys Lett 2004;85(17):3884–6.
[16] Liu W, Fan SK, Kim TS, Beam III EA, Davito DB. Current transport mechanism in GaInP/GaAs heterojunction bipolar transistors. IEEE Trans Electron Dev 1993;40:1378–83.
[17] Chand N, Fischer R, Morkoc H. Collector–emitter offset voltage in AlGaAs/GaAs heterojunction bipolar transistors. Appl Phys Lett 1985;47:313–5.
[18] Hong WP, Song JI, Bhat R, Chough KB, Hayes JR, Sugeng B, et al. Microwave power InP/InGaAs/InP double-heterojunction bipolar transistors. Int Conf Indium Phosphide Related Materials 1993:21–4.
[19] Kirk CT. A theory of transistor cut-off frequency (f_T) fall off at high current densities. IRE Trans Electron Dev 1962;9:164–74.