New Floating Capacitance Multipliers

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Abstract

In this paper, a technique for realizing a floating capacitance multiplier based on the use of dual output current conveyors and grounded capacitance is proposed. Its multiplication factor can be tuned by changing the ratio of resistors. Moreover, the circuit is easily modified to electronically tunable floating capacitance multiplier by using current controlled conveyor. Simulation results are obtained to show adequate agreement with theory.

Keyword: current conveyor, capacitance multiplier

1. Introduction

One of the most limiting problems in the design of integrated circuits is constituted by the realization of silicon area. Moreover, in some sensor applications, it can be useful to deal with capacitance value higher than those normally given by capacitive sensors. In these cases, the use of capacitance multipliers can be vary important.

Presently, there has been a strong motivation to design analog circuits utilizing active circuit elements, such as current amplifiers (CAs), operational transconductance amplifiers (OTAs) and current conveyors (CCs). Several circuits of capacitance multiplier that are implemented through the used of those active circuit elements have been presented [1-4]. The circuits in [1-4] are realized to operate for a grounded capacitance multiplier. Although, a grounded capacitance multiplier a vary useful building block for many applications, but a floating capacitance multiplier can offer wider applications than a grounded capacitance multiplier, particularly; it can be employed as a floating capacitor for the active filters and oscillators. A floating capacitance multiplier realization has been proposed [4]. The circuit of [4] used two operational transconductance amplifiers (OTAs), an operational amplifier (OA), a voltage buffer and a ungrounded capacitance, which has the attractive feature of electronically tuning multiplication factor. However, this circuit suffers from the used of an excessive number of elements.

This paper introduces two new floating capacitance multipliers. The first circuit employs two dual output current conveyors and three passive elements. And the second circuit is modified from the first circuit by replacing CCII± with CCCII±, which yields the attractive feature of electronically tunable multiplication factor.

In the first section, the basic circuit of a floating capacitance multiplier is proposed and analyzed. Secondly, the implementation of the floating capacitive multiplier is given. The circuit for electronically tunable multiplication factor is also presented. The SPICE simulation results of the circuits are finally considered to show adequate agreement with theory.

2. Theoretical approach

The proposed basic circuit of a floating capacitance multiplier is shown in Fig. 1.

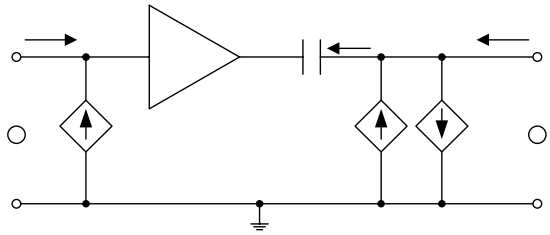

Fig. 1 The proposed basic circuit

By straightforward analysis, the short circuit admittance matrix between port *a* and *b* is found to be:

$$[Y] = sCk\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} = sC_{eq}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \quad (1)$$

This implies that, a floating capacitance between port *a* and *b* has value C_{eq}. The capacitance C_{eq} is a function of normal *C* and the current gain, k:

$$C_{eq} = kC \quad (2)$$

This indicates that, the capacitance value is tuned by changing the gain, which can be implemented with an amplifying device.

3. Circuit implementation

From the basic circuit of floating capacitance multiplier depicted in the Fig. 1, can be implemented by employing the dual output second-generation current conveyors (CCII±s). The dual output current conveyor (CCII±) can be obtain by modifying the original circuit of CCII [5] by adding additional current-mirrors and cross-coupled current-mirrors to obtain the required plus and minus type outputs as shown in Fig. 2(a), and its symbol is shown in Fig. 2(b).

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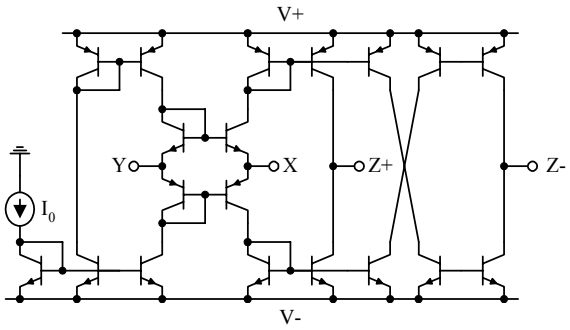
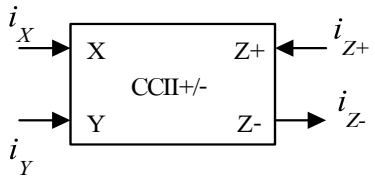


(a)



(b)

Fig. 2 (a) Schematic circuit of CCII±
(b) Symbol of CCII±

The electrical behavior of this CCII± can be described by the following matrix relationship between terminals Y, X and Z:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{3}$$

The positive sign denotes a positive type conveyor (CCII+) and the negative sign denotes a negative type conveyor (CCII-). Using characteristics of the CCII±, can be realizing the floating capacitance multiplier as shown in Fig. 3. The circuit consists of two CCII±s, two resistors and a grounded capacitor.

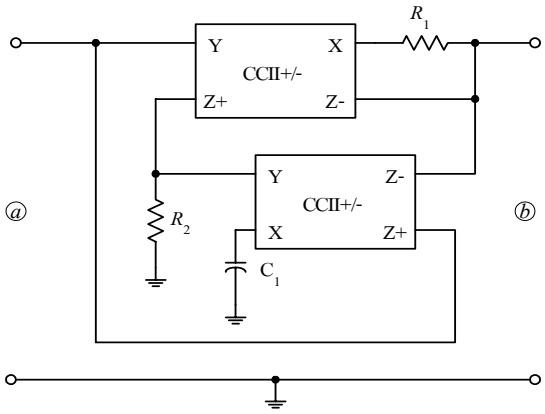


Fig. 3 CCII±s based a floating capacitance multiplier

When the CCII± is assumed to be ideal and the routine circuit analysis, the short circuit admittance matrix of Fig. 3 is found to be

$$[Y] = sC\frac{R_2}{R_1}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{4}$$

This equation shows that the floating capacitance between port *a* and *b* has value C_{eq} is given by

$$C_{eq} = \frac{R_2}{R_1}C \tag{5}$$

From this equation (5) indicates that, the capacitance C_{eq} can be tuned by controlling either the resistance R_2 or the resistance ratio R_2/R_1; however it cannot be tuned electronically. To obtain electronic tunability, the circuit is modified by employing so-called second-generation current controlled conveyor (CCCII±) [6] in place of a CCII±. The CCCII± has the properties similar to the CCII±, but the CCCII± has a finite input resistance, Rx, at the x-terminal which is controllable in the term of bias current I_0 as follows:

$$R_x = \frac{V_T}{2I_0} \tag{6}$$

where V_T is the thermal voltage which is about 26 mV at 27°C.

From the Fig. 3, by replacing the CCII± with the CCCII±, the passive lumped resistive component R_1 is replaced by the intrinsic input resistance of the CCCII±, therefore the passive lumped element R_1 can be eliminated. One can obtain a new electronically tunable floating capacitance multiplier based on current controlled conveyor is shown in Fig. 4.

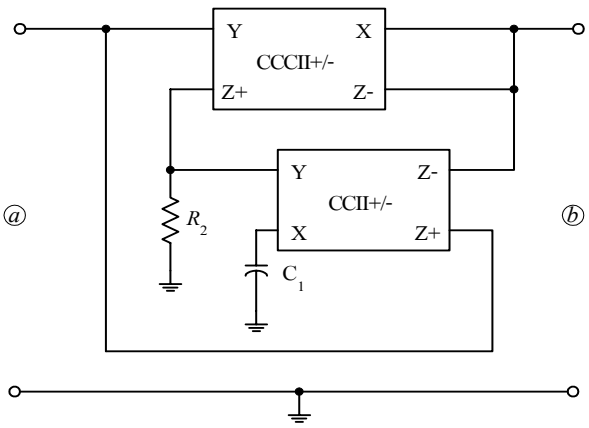


Fig. 4 The electronically tunable floating capacitance multiplier

This circuit contains only one CCII±, one CCCII± and two grounded passive elements, which is the one of the attractive features of our purposed circuit. The analysis of the circuit in Fig. 4 gives the short circuit admittance matrix as

$$[Y] = sC\frac{R_2}{R_x}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \quad (7)$$

where the value C_{eq} is given by

$$C_{eq} = \frac{R_2}{R_x}C \quad (8)$$

By substituting equation (6) into (8) yields

$$C_{eq} = \frac{2I_0R_2}{V_T}C \quad (9)$$

This equation shows that the floating capacitance between port *a* and *b*, can be tuned electronically by controlling the bias current I_0.

4. Simulation results

To verify the theoretical analysis of the proposed circuits, a number of SPICE simulations were carried out at 27°C by using the structure of CCII± and the CCCII± as described above. The p-n-p and n-p-n transistors were simulated by using complementary bipolar transistors NR100N and PR100N of the ALA400 array from AT&T [7]. The circuit of Fig. 4 was simulated using C = 1nF, R_2 = 1kΩ and ±2.5V power supplies and assuming that the CCII± are ideal. The current characteristics of the series resonance circuit in Fig. 5, when the ideal C is replaced by floating capacitance multiplier, are shown in Fig. 6. The solid curves are the results obtained from the simulation when the bias current of the CCCII± is varied from 50, 100 and 200μA. The dotted curves are the detail results corresponding to calculation when C =3.846, 7.692 and 15.385 nF.

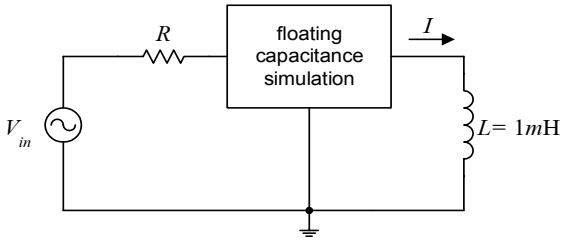


Fig. 5 Series resonance circuit

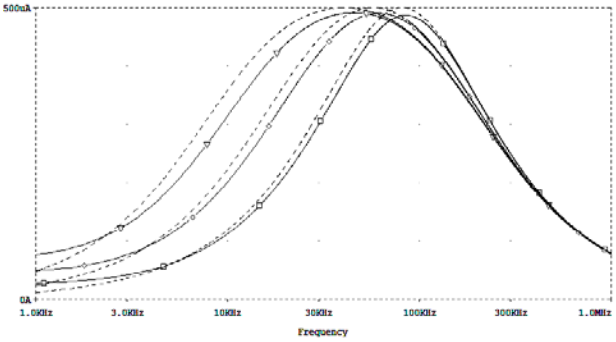


Fig. 6 Simulation results of current characteristics of the series resonance circuit when I_0 is varied
□ I at $I_0 = 50\mu$A
◊ I at $I_0 = 100\mu$A
∇ I at $I_0 = 200\mu$A

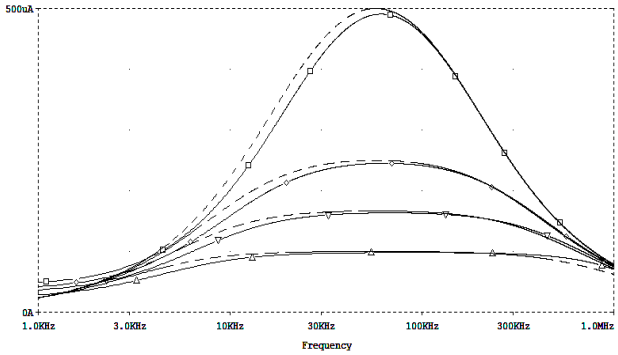


Fig. 7 Simulation results of current characteristics of the series resonance circuit when R is varied.
□ I at R = 1 kΩ
◊ I at R = 2 kΩ
∇ I at R = 3 kΩ
Δ I at R = 5 kΩ

The curves in the Fig. 7 show the current characteristics of the same resonance circuit when I_0 is kept constant at I_0 = 100μA and the resistance R is varied to be 1, 2, 3 and 5kΩ. The solid curves are the simulation results, whereas the dotted are the result of an ideal calculation.

5. Conclusions

Based current conveyors, the floating capacitance multipliers are proposed. Each circuit employs a grounded capacitance, which is easier to fabricate in IC technology. The basic circuit employs only CCII± as active components. Moreover, the circuit is easily modified to be electronically tunable floating capacitance multiplier by using current controlled conveyors; the simulation results agree well with ideal calculation results.

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