Advanced deep reactive ion etching: a versatile tool for microelectromechanical systems

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Abstract. Advanced deep reactive ion etching (ADRIE) is a new tool for the fabrication of bulk micromachined devices. Different sensors and actuators which use ADRIE alone or combined with other technologies such as surface micromachining of silicon are presented here. These examples demonstrate the potential and the design freedom of this tool, allowing a large number of different shapes to be patterned and new smart devices to be realized.

1. Introduction

The fabrication of microelectromechanical systems (MEMS) has always used a large number of very sophisticated techniques. Surface micromachining [1, 2] and bulk anisotropic silicon etching [3–5] were used to build pressure sensors, inertial sensors, micropumps, micromotors, xy-stages and other smart devices [6–10]. Both technologies suffer some limitations such as the sticking of the structures for surface micromachining and the silicon crystal orientation dependency for anisotropic etching.

Deep silicon dry etching has been investigated to extend the bulk micromachining and to fulfil some requirements like: etch depths from 20 to 300 μ m, aspect ratio greater than 30 [11–14] and more freedom in the design.

First trials with deep reactive ion processes have shown that by extending the etching time, the photoresist mask layer deteriorates faster due to the increasing temperature of the substrate [11]. Thick photoresist, multi-layer mask or low-temperature wafer stage have been investigated [12, 13]. In both cases, trade-off between the etching rate and the etching selectivity to the mask has been observed. Therefore advanced deep reactive ion etching (ADRIE) tools have been proposed [15]. There are currently two ADRIE systems available on the market. One system is manufactured by Alcatel [16] and the other by STS [17]. For these new tools, silicon etch rates up to several microns per minute, with geometrical aspect ratios of at least 15:1, even at depths up to 300 μ m are obtained. Different microstructures have been fabricated successfully with both pieces of equipment [18, 19]. Thanks to the difference between the etching rate of the silicon and the silicon dioxide, silicon dioxide layers are often used as etch stop layers.

In this paper, several MEMS devices realized at the Institute of Microtechnology of the University of Neuchâtel are presented. They were fabricated using the commercial ADRIE etcher from STS Ltd, Gwent, UK.

2. Micro-opto-mechanical 2 \times 2 switch for single mode fibers

The high precision ADRIE technique can be used to microfabricate integrated actuators [20, 21]. Electrostatic actuation is of particular interest because no additional actuator material has to be added, i.e. when using the etched surfaces as the capacitor electrodes the actuator can be fabricated directly in the etching step. But the force generated by electrostatic actuators is rather small, which limits their application range. Nevertheless a very promising application can be found in the field of micro-optics. To redirect a light beam principally no force is necessary and an actuator of reduced power is already sufficient. A fiber optic 2×2 switching device was successfully demonstrated [22]. It is based on the ADRIE technique [23], where the switching mirror, its electrostatic actuator and the alignment grooves for the passive alignment of the fibers are all fabricated in one etching step.

Figure 1 shows the operation principle of the 2×2 micromechanical switch. Four single mode (SM) fibers with tapered ends are placed into alignment grooves at 90° to each other. The fibers are tapered to be able to bring them closer together than their 125 μ m diameter in order to keep light losses small. In the bar state the light from the two pairs of fibers goes in a straight path; in the cross state the vertical mirror reflects the two light beams



Figure 1. Operation principle of 2×2 fiber optic switch in (a) bar and (b) cross state.



Figure 2. Actuator-mirror structure fabricated in one ADRIE etching step on an SOI substrate. The mirror-actuator structure becomes moveable after partially dissolving the buried oxide.

by 90° in order to couple the light into the output fibers normal to the input fibers. The quality of the vertical mirror is of primary importance in order to keep the light loss minimal also in the cross state. The mirror should be as flat, vertical and thin as possible. Figure 2 shows an SEM micrograph of the ADRIE etched vertical mirror, together with the electrostatic actuator and the alignment grooves for single mode fibers. The etching depth was 75 μ m. A minimal beam thickness of 2.3 μ m for the mirror and the spring structures was obtained. The surface roughness was evaluated by atomic force microscopy to be around 36 nm (rms) [23].

This one-mask fabrication process needs the use of special silicon-on-insulator (SOI) substrates. The buried oxide serves to stop the etching at a uniform thickness and allows us to release the thin mechanical structures in a time stopped sacrificial layer etching.

The switching time of a completed switch was about 0.2 ms, which is about a factor of 10 to 50 times faster than conventional mechanical switches, with driving voltage between 40 and 50 V. The light loss is below 1 dB in the bar state, whereas in the cross state the loss was close to 2 dB. This points out the high quality of the vertical walls obtained by ADRIE.



Figure 3. SEM micrograph of fabricated monocrystalline silicon membrane resonator. The outer diameter of the free standing membrane is 3.4 mm. Thickness of the membrane is 20 μ m.

3. Surface micromachined membrane resonators in view of their application in micromotors

A porous silicon layer has successfully been demonstrated as a valuable sacrificial layer [24–27] to form free-standing micromechanical structures. The fabrication process developed here uses ADRIE and selective porosification of silicon [24]. It is suitable for the fabrication of structures ranging from μ m to mm size. It is fully compatible with standard CMOS processes when a non-contaminating etchant such as TMAH is used for the etching of the sacrificial layer. Among various applications, a millimeter size resonator activated by piezoelectric layers will be used as a component of miniaturized ultrasonic motors for wristwatch applications.

An n-type epitaxial layer grown over a p-type silicon wafer is patterned with ADRIE using photoresist as a mask. Vertical wall profiles of complex shaped structures with thicknesses in the several tenths of micrometers range are obtained with a high precision.

Subsequent porosification of the p-type bulk silicon forms a well controlled porous silicon sacrificial layer underneath the n-type epitaxial layer. Details of this process have been discussed in [24].

Figure 3 demonstrates that 19 μ m thick very wide freestanding membranes can be fabricated. Up to 1.2 mm overhanging diameters have been achieved by using a 200 μ m × 200 μ m square grid of 4 μ m × 4 μ m etching holes. The membrane is attached to the substrate by a central hub of 160 μ m diameter. Figure 4 shows the air gap between the n-type silicon and the p-type substrate near the free-standing edge of the membrane. Height to width aspect ratio over 25:1 has been obtained for the vertical walls of the resonator edges as well as for the etching holes. Note the high precision of the free-standing silicon side walls obtained by ADRIE.

The combination of a porous silicon sacrificial layer with ADRIE of silicon has pointed out the high potential of these techniques to be applied in the processing of various complex actuator designs.



Figure 4. Close-up of the air gap profile near the external edge of the resonator. The holes in the membrane are used to underetch large areas.



Figure 5. Patterned thick photoresist mask for ADRIE.

4. Thick photoresist layers applied for the protection of protruding structures during deep reactive ion etching processes

ADRIE needs sometimes to be performed after the formation of protruding delicate parts of a device (for example silicon tips on cantilevers for atomic force microscopy [28, 29] or tips on porous membranes for electro-physiological studies [30]).

Thick photoresist (about 40 μ m) was patterned and used as a protective layer for protruding structures (sharp, high aspect ratio atomic force microscope (AFM) tips) in ADRIE etching (figure 5).

Figure 6 shows a 15 μ m high sharp tip on a 65 μ m high pedestal. As can be seen on the inset, the tip was perfectly protected during the etching. On other structures, 25 μ m wide and 300 μ m deep trenches were etched without blunting the tip demonstrating the interest of this technique [31].

5. Double octupole deflector for use in an electron microcolumn

The fabrication of a double octupole deflector is part of a project to fabricate a micromachined, low-energy electron column for lithography applications [32–34]. The advantages of such a column are the reduction of the proximity effect by using low energy beams and also that the miniaturization allows for the columns to be arrayed to increase throughput. By applying suitable voltages to each



Figure 6. Sharp silicon tip on 65 μ m high pedestal. The inset shows a close-up view of the apex: scale bar is 400 nm and curvature radius is estimated to be about 10 nm.



Figure 7. SEM micrograph of the STS etched deflector structure.

of the eight electrodes the deflectors can be used to raster the electron beam and also to correct astigmatism.

The device is etched by ADRIE to produce the 200 μ m high silicon electrodes (figure 7). The final structure consists of two of these deflector chips anodically bonded to a Pyrex[®] spacer with a bore hole drilled into it. Finally the chips are mechanically lapped to thin the silicon until the trenches are reached, using the Pyrex[®] as a support (figure 8). Small etch pits were formed at the bottom of the trench at the corners of features; however these were of no concern as they were removed during lapping. The sidewalls of the trench showed layers arising from zones of different microroughness (figure 7). This roughness was acceptable for our application although further optimization of the ADRIE to reduce this roughness would be desirable.

Preliminary measurements obtained from a single deflector, using a standard power supply with an applied deflection voltage of ± 20 V gave deflection angles along the *x* and *y* axis of $\pm 2.1^{\circ}$ and $\pm 2.4^{\circ}$ respectively for an electron energy of 150 eV. For an electron energy of 300 eV



Figure 8. Cross-section of the final device.



Figure 9. Schematic representation of the device.

the x and y deflection angles were ± 1.05 and $\pm 1.15^{\circ}$ respectively. Hence ADRIE has been successfully used to fabricate double octupole deflectors for use in electron microcolumns.

6. Electro-physiological monitoring of cells on perforated substrates

Microelectrode arrays for monitoring of extracellular electrical activity of nerve cells *in vitro* have numerous potential applications ranging from fundamental neural network research to practical applications in e.g. drug screening. Integrated usually on a solid silicon or glass substrate, these devices have proven their suitability for electrophysiological monitoring. For some recent cell culture techniques, microelectrode arrays on a perforated substrate are required.

As shown in figure 9, an array of Pt microelectrodes consisting of 30 electrodes (diameter of the active area: 10 μ m) is realized on a micromachined silicon chip perforated in its central region (3 mm × 4 mm). This area (figure 10) is formed by an array of via holes spaced by 25 μ m and of which the diameter is 35 μ m. The resulting porosity is about 25%.

In previously available technology, these holes were obtained using a C_2ClF_5 -SF₆ plasma [11] on a 15 μ m thick silicon membrane made by wet anisotropic etching. This substrate was mechanically too fragile to allow the tissue slice manipulations.

As shown in figure 10, the ADRIE gives the possibility to etch 35 μ m diameter holes through the 390 mm thickness of a 4 in wafer.

Such devices were successfully used for stimulating and recording experiments on organotypic cultures [30] and point out the possibility of building small holes through silicon wafers.



Figure 10. SEM micrograph of a 390 μm thick silicon chip perforated by ADRIE.

7. Processing of ultra-thin plates with arbitrary geometric shapes

In most applications involving membrane processing technology, the silicon areas on the wafer back side are chemically wet etched in a solution of potassium hydroxide (KOH). This relatively simple method allows the microfabrication of high quality residual membranes with well controlled thickness. Howewer, three major disadvantages are encountered. First, many layers are not compatible with KOH and must be protected during this step. This is dramatically the case when a ferroelectric thin film like lead zirconate titanate (PZT) is present on the top side of the wafer [35]. A mechanical protection chuck is then required. Secondly, with the chuck protection, very thin membranes (less than two micrometers thick) having large areas are difficult to fabricate, due to residual pressure between the membrane and the mechanical protection. In particular, multilayered membranes composed of layers subjected to in-plane tension such as silicon nitride, platinum and PZT thin film are very sensitive to any small stress gradient between the chuck and the silicon frame. KOH contamination of the whole wafer due to one membrane break increases the difficulty of this process. Thirdly, as already explained in the introduction, only simple geometrical shapes (square or rectangle) are generally processed with bulk micromachining. Polygonal, elliptical or arbitrary shapes are not easily feasible.

Here we present the possibility of using STS technology to process very thin composite plates with large areas over a 400 μ m thick wafer. 0.45 μ m thick silicon dioxide (SiO₂) is first thermally grown on both sides of the four inch wafer, followed by the plasma-enhanced chemical vapour deposition (PECVD) of 0.6 μ m thick low stress silicon nitride (Si_xN_y) on one side. A Ta/Pt (10 nm/150 nm) metal ground plane is then evaporated over the Si_xN_y layer. The membrane pattern is defined by a photolithography step with an 8 μ m thick positive resist. The silicon nitride is etched by dry etching while the silicon oxide is removed by wet chemical etching in a solution of buffered hydrofluoric acid (BHF). In our case, only rectangular membranes (figure 11) were tested with two different sizes: 1 × 8 mm² and 2 × 8 mm².



Figure 11. Photograph of four multilayer membranes (silicon nitride and platinum). Overall dimensions are 2 mm by 8 mm, while the thickness is 0.76 μ m.



Figure 12. SEM close up of the vertical walls. The depth of the cavity is 400 μ m. The arrow shows remaining parts of a broken plate.

After 88 min mean time of silicon etching by the ADRIE technique, a selective etch stop is provided by the SiO₂ underlying layer which is then wet etched. Figure 11 shows final composite suspended membranes having only 0.76 μ m thickness. On the left part, two of them are broken. In figure 12, a closer view of one broken membrane with right angle profile emphasizes the potential of this technology. Other membrane profiles are currently under study.

8. Torque measurement microsystem

The realization of a torque measurement system is presented in the following section. This system allows the friction of the small size bearings and gears used in wrist watches to be measured. It is also very accurate to characterize the output torque of micromotors [36].

The microsystem is composed of two piezoresistive force sensors of 6 mm by 6 mm and of an interface micromechanical unit which insures the transmission of the torque to the sensors. Each strength sensor consists of a



Figure 13. Picture of two sensors.



Figure 14. SEM of the force sensor back side, illustrating its design freedom.

circular membrane and of a central bump on which the force is applied (figure 13). The latter serves also as the overrange protection of the system. The piezoresistive sensing resistors are placed on the top side of the membrane in high stress locations. To obtain a sensitive system particular attention has been given to their positioning and orientation. This has been done by simulating the sensors on a finite element modeling tool (ANSYSTM) [37, 38].

This device is a good example of the design freedom which is given by the new ADRIE processes which do not suffer the crystal orientation limitation of standard anisotropic silicon etching [3]. ADRIE combined with the use of silicon on insulator (SOI) wafers allows a selective etch stop and very accurate membrane thickness to be defined (figure 14). A structured glass [39] is then bonded to the bottom side of the chip limiting the movement of the central bump in the vertical direction and increasing the stiffness of the whole chip.

9. Silicon micromachined angular rate sensor

Low cost gyroscopes (angular rate sensors) are promising devices for automotive applications [40–43]. In this paper, a new silicon angular rate sensor is presented. Its design



Figure 15. Micrograph of a silicon prototype gyroscope.



Figure 16. SEM picture of a suspension beam: 2000 μm long, 40 μm wide and 377 μm thick.

benefits from the conclusion of previous work [42] and includes enhanced mode separation [43] to reduce cross-axis sensitivity.

This new gyroscope is based on the tuning fork principle [42]. Compared to the previous concept, this design shows two major improvements: first, the inertial centers of the masses are aligned with the suspensions allowing pure in plane antiphase excitation; second, the high aspect ratio of the suspensions prevents parasitic mode coupling between the excitation and the detection. To define both frequencies, the suspensions are fixed to the frame by thin shells.

Double side polished, 4 inch, n-type, SOI wafers (380 μ m thick) are used for the fabrication of these gyroscopes. A combination of two ADRIE steps allows this design to be realized, while the buried silicon dioxide is removed by wet etching. Figure 15 shows a vibrating prototype gyroscope integrated with these new concepts. Figure 16 illustrates the high aspect ratio (about 10) of the beams.

10. Conclusion

This contribution discusses different projects realized with the ADRIE process of STS. It points out the design freedom allowed by this new tool which allows 400 μ m thick silicon wafers to be etched with aspect ratio up to 15.

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