Reordering Algorithm for Minimizing Test Power in VLSI Circuits

K.Paramasivam *Member, IAENG,* Dr.K.Gunavathi

Abstract— **Power consumption has become a crucial concern in Built In Self Test (BIST) due to the switching activity in the circuit under test(CUT). In this paper we present a novel method which aims at minimizing the total power consumption during testing. This is achieved by minimizing the switching activity in the circuit by reducing the Hamming Distance between successive test vectors. In this method the test vectors are reordered for minimum total hamming distance and the same vector set is used for testing. Experimental results with ISCAS benchmark circuits show that the switching activity can be reduced up to 21 % in comparison with conventional ATPG Algorithms like DEFGEN. The Switching activity is reduced significantly when compared with existing methods.**

***Index Terms*— ATPG, Hamming Distance, Power Consumption, Reordering Algorithm, Switching Activity.**

I. INTRODUCTION

Very Large Scale Integration (VLSI) design plays a significant role in the fabrication of modern Integrated Circuits(ICs) with smaller in size and with more features for any electronics systems. Energy consumption and power dissipation are the major concern in the VLSI design. Several factors have contributed to this trend. With the advent of portable devices, for example low energy consumption has become one of the major design goals in order to prolong battery life. Moreover the amount of energy a circuit consumes is directly reflected in its heat dissipation, however requires expensive packaging and cooling techniques which in turn increases system cost [1]. In addition, as power consumption increases, circuit reliability gets affected adversely due to electro-migration. This is applicable for both Design power and testing power.

Testing [2, 3, 4] is a process of checking the fabricated IC's for any incorrect behavior due to faults like logical fault, delay fault, fabrication faults[2], etc. Testing is done by generating and applying a set of binary vectors called test vectors to the input of the circuit. Fault is detected by verifying the output for the given test vector with stored responses. Testing has to be done for all possible faults in the circuit. Hence more test vectors may be required to test all the faults in complete circuit. Single test vector may detect more than one fault and more than one test vectors can be generated for a single fault. A set of test vectors[4] must be generated such that more faults are covered with minimum number of test vectors.

Testing is not only done after the fabrication of IC's but also required when IC's are in usage. This is called periodic testing which is required for all type of systems like PC, Laptop, cell phones etc. The main problem under testing environment is that it results in considerably higher circuit activity rate compared to normal mode operation, hence causing above normal power dissipation. However if test vector sets are not optimized for power[10], low power circuits dissipate two fold power under test as they do at normal operating condition[2]. When the circuit is tested with pseudo-random patterns, consecutive input test vectors are statistically independent which results in increased switching activity in the circuit under test. Since in CMOS circuits energy is primarily consumed by signal transition, the average power consumption during testing is significantly higher than normal mode of operation. The Relationship between hamming distance [6] and the average power of a circuit plays a significant role to optimize the test power. In order to optimize, the hamming distance between successive test vectors is used to arrange the test vectors in specific order so that Total Hamming Distance(THD) is minimum. A test vector set with least hamming distance is obtained by optimization technique. The test power obtained by applying test patterns in the optimal order is regarded as the optimized test power. In order to guarantee the proper operating conditions during test, the total power consumption must not exceed the maximum power allowance for the circuit under test[2]. Another problem is that even if the average power dissipation over a sequence of test vectors is small, the peak (or instantaneous) power dissipation may be sufficiently high to destroy the CUT. In practice, destruction really occurs when the instantaneous power exceeds the maximum power allowance during several successive test vectors. For this reason, it is essential to take care of both average and peak power dissipation during test application.

Many low power design techniques have been proposed at all levels of the design hierarchy. However, all these techniques focus on low power dissipation during system mode or standby

Manuscript received June 6, 2006.

Mr. K. Paramasivam (Research Scholar at PSG College of Technology, Coimbatore under Anna University, Chennai), Assistant Professor is with Department of Electronics and Communication Engineering, Bannari Amman Institute of Technology, Sathyamangalam, Tamilnadu, India 638 401.(Corresponding Author: e-mail: kp_sivam@yahoo.com)

Dr. K.Gunavathi, Professor is with Department of Electronics and Communication Engineering, PSG College of Technology, Coimbatore, Tamilnadu, India. e-mail: kgunavathi2000@yahoo.com

mode, and during test mode. The simplest way to ensure non-destructive testing of a CUT is to use ordering of test vectors, which causes switching activity that is comparable to that during normal circuit operation. Several categories of techniques can be found in the literature related to the low power testing. The first category consists of ATPG (Automatic Test Pattern Generator) techniques[5], in which new ATPGs are proposed with the intent of generating test patterns that can reduce the power dissipated during test application in addition to the normal ATPG objectives. The second category consists of ordering techniques [1,6, 7, 8, 9], in which the switching activity is reduced by modifying the order in which test vectors of a given test sequence are applied to the CUT. The paper [14] discussed about two methods used for reordering of test vectors in order to reduce the dynamic power dissipation during testing of combinational circuits. Two search methods 2-opt heuristic and a genetic algorithm based approach have applied and results obtained for combinational circuits. These techniques can be applied during external testing or deterministic BIST (Built-In Self Test). In this paper we present a novel method, which aims at minimizing switching activity during testing of combinational circuit. The test vectors are reordered based on the hamming distance between successive test vectors. Graph theory based reordering algorithm is proposed to solve the problem. Since this problem is NP complete, the algorithm is developed through heuristic approach which gives better optimum solution for such problems. Random heuristics are used in previous approaches that may or may not give better solution. In this proposed algorithm structured heuristic is used to obtain better results than random heuristics.

The remaining part of the paper is organized as follows. Chapter discusses about power dissipation in CMOS ICs. The problem definition and proposed algorithm are given in the chapter3. Implementation and results are discussed in chapter 4. Paper is concluded in chapter 5 and references are listed in chapter 6.

II. POWER DISSIPATION IN CMOS TECHNOLOGY

Unlike bipolar technologies, where a majority of power dissipation is static, the bulk of power dissipation in properly-designed CMOS circuits is due to dynamic power dissipation caused by charging and discharging of capacitances. Thus, a majority of the low power design methodology is dedicated to reducing this predominant factor of power dissipation. However, there are also other components of power dissipation in CMOS circuits like short circuit current power, leakage current power, and static biasing power. These are negligible when compared with the dynamic power dissipation.

A. Sources of Power Dissipation

There are four main source of power dissipation: dynamic switching power due to the charging and discharging circuit capacitances, leakage current power from reverse-biased diodes and sub-threshold conduction, short-circuit current power due to finite signal rise/fall times, and static biasing power found in some types of logic styles (i.e. pseudo-NMOS). Here the dominant term is discussed as follows.

B. Dynamic Switching Power

When CMOS circuits switch, the output is either charged up to V, or discharged down to ground. In static logic design, the output only transitions on an input transition, while in dynamic logic, the output is precharged during half the clock cycle, and transitions can only occur in the second clock phase, depending upon the input values. In both cases, the power dissipated during switching is proportional to the capacitive load; however, they have different transition frequencies. For the simple inverter gate, it can be shown that a low-to-high output transition draws CV Joules (energy) from the power supply V. The high-to-low output transition dissipates the energy stored on the capacitor into the NMOS device. Given a frequency *f* of low-to-high output transitions, the power drawn from the supply is CVf. This simple equation holds for more complex gates and other logic styles as well, given a periodic input. Accurate calculations for C can be done. The net loading capacitance C, consists of gate capacitance of subsequent gate inputs attached to the inverter output, interconnect capacitance, and the diffusion capacitance on the drains of the inverter transistors. Test chips have shown that for 1.2m ICs, the total capacitance is split roughly equally between these three types. As the minimum gate length scales down, though, interconnect capacitance will become dominant.

Usually, the value of *f* is a difficult number to quantify, as it is most likely not periodic, and is correlated with the input test vectors into the circuit. Without doing a switched-level circuit simulation, the best way to calculate *f* is to perform statistical analysis on the circuit to determine a mean value. Since dynamic switching power is the major component of overall power dissipation, the low-power design methodology concentrates on minimizing total capacitance, supply voltage, and frequency of transitions.

III. PROBLEM FORMULATION

The power dissipation during testing [2] is minimized by reducing the number of transition in the circuit. This is achieved by reducing the hamming distance between successive test vectors. Usually test vectors are in random and hence it is necessary to rearrange the order of occurrence of test vectors so that the hamming distance between successive test vectors is minimum. In general the total switching power in the whole circuit is proportional to the hamming distance of input test vectors. Therefore the reordered test vector set with minimum hamming distance is used for testing the CUT to reduce the switching power. The problem of minimizing switching power is solved by graph theory using Hamiltonian path [3] technique. Graph G(V,E) is defined with V nodes and E edges. The problem is formulated by considering the test vector as node and hamming distance between them as edge cost of the graph. Here the Hamiltonian path is a path with all nodes and minimum total edge cost. Graph Theory based Reordering algorithm[12] is used to construct the Hamiltonian

path, which is resultant reordered test vector set whose total hamming distance is minimum. Now the path developed by the algorithm is reordered test vector sequence which offers less number of transitions at the input which in turn results in reduced power dissipation in the circuit under test during testing [3]. Heuristic approach is used in the algorithm to find more suboptimal sequences.

Total Hamming Distance(THD): Total hamming distance is defined as Sum of hamming distance between successive test vectors in the sequence.

Let hamming distance $d[t_i, t_j]$ be the total number of changes between i^{th} and j^{th} test vector. The Total Hamming Distance(THD) for the whole test vector set is calculated by the following relation.

$THD = \sum_{i=1}^{n-1} d[t_i, t_{i+1}]$

where n represents total number of test vectors in the whole set.

The overall procedure to minimize the switching activity during testing is as follows.

1. Consider a digital circuit with p inputs and q outputs.
2. Generate all the test vectors to detect all the single stuck at faults[4] of the circuit. Let the number of test vectors be n.
3. Find the hamming distance between each and every test vector and load the same in array *hd* of size *n x n*. Let hd[i][j] be the array elements which gives hamming distance between i^{th} and j^{th} test vectors.
4. Apply reordering algorithm to find the reordered test vector sequence with minimum total hamming distance.
5. Perform fault simulation[4] with reordered test vector set which gives minimum number of transition and hence less power dissipation.
6. Since Heuristic based algorithm generates more sub-optional sequences, select the best sequence with least total switch activity.

The reordering algorithm used in step 4 is discussed in the next sub-section.

A. Reordering Algorithm:

The various parameters used in the algorithms are as follows:

$t_1, t_2, \ldots t_n$ be n test vectors with m bits each.

T={1,2,… k … n} where k represents k^{th} position in the vector set generated by ATPG.

R is a set to store ordered test vector sequence.

Q is a set to store T-R.

Step 1: Select a test vector x such that swa_init[x] is minimum in the array swa_init[ ]. Add x to set R.

Step 2: Select a test vector y_{min} such that $hd[x][y_{min}]$ is minimum in the array.

Step 3: Add y_{min} to R; Q← T-R; $x_{min} \leftarrow y_{min}$.

Step 4: From the array $hd[x_{min}][j]$ when j varies as in Q, find y_{min} so that $hd[x_{min}][y_{min}]$ is the smallest value. Go to step 3.

Step 5: In the step 4, if $hd[x_{min}][j]$ has more than one smallest value, then such number of reordered sequence will be generated for every x_{min}. These sequences are called as sub-optimal sequences.

Finally the set R will have reordered test vector sequence with minimum hamming distance which results in minimum switching activity during testing.

The above procedure is illustrated with simple full adder circuit with 3 inputs and 2 outputs. The test vector set that used to detect the entire single stuck at faults is given in Table I. The set consists of 7 vectors with total hamming distance as 15 . The vectors are represented by the order of occurrence for the sake of convenience. The hamming distance array hd[ ][ ] of order n x n is constructed. This is given as in (2). It is known that the number of bit changes between t1 and t2 test vectors in the table is three. Similarly between t2 and t3 test vectors is two. This is shown in the array as hd[1][2]=3 and hd[2][3]=2 respectively. The hamming distance array hd[][] is developed in this method.

Test vector set (n=7)	No.
000	t_1
111	t_2
001	t_3
010	t_4
101	t_5
011	t_6
100	t_7

Table.I Test vectors for full adder circuit

$$hd[i][j] = \begin{pmatrix} 0 & 3 & 1 & 1 & 2 & 2 & 1 \\ 3 & 0 & 2 & 2 & 1 & 1 & 2 \\ 1 & 2 & 0 & 2 & 2 & 1 & 2 \\ 1 & 2 & 2 & 0 & 3 & 1 & 2 \\ 2 & 1 & 2 & 3 & 0 & 2 & 1 \\ 2 & 1 & 1 & 1 & 2 & 0 & 3 \\ 1 & 2 & 2 & 2 & 1 & 3 & 0 \end{pmatrix} \quad \ldots. (2)$$

On application of reordering algorithm to this matrix hd[ ] [ ], the reordered test vectors are generated with minimum hamming distance.

The solution and the THD are given as follows:

Unordered sequence : t1 – t2 – t3 – t4 – t5 – t6- t7 THD : 15

Ordered sequence : t3 – t1 – t4 – t6 – t2 – t5– t7 THD : 6

The total hamming distance for the resultant ordered sequence is 6 which shows that 60 % of total hamming distance is reduced when compared with that of unordered sequence. This reduces the switching activity and hence the power dissipation in the circuit. The above approach is experimented with various benchmark circuits and results are appreciable and improvement was achieved when compared to existing

methods.

IV. Implementation Results and Discussions

The proposed low power testing algorithm is implemented using C Language and tested with benchmark circuits ISCAS 85[13]. Each circuit is implemented using VHDL to satisfying the following conditions:

(i) Realization of the logic with zero delay model

(ii) Single stuck-at fault condition

(iii) Under the above condition the total switching activity of the circuit is calculated during testing

Fault simulation for unordered and ordered test set is carried out to find the total switching activity for the each case. Results show that switching activity of ordered test set is always less than that of unordered test set.

The reordering algorithm is applied and tested with ISCAS 85 benchmark circuits. The results are shown in the Table II for various benchmark circuits. For each circuit, a set of test vectors to detect single stuck at faults are generated using the ATPG DEFGEN. Total hamming distance is calculated for the set generated from DEFGEN and is represented as HD_{DEF} . Then the total number of switching activities of the circuit is calculated by applying the same test vector. This is represented by SW_{DEF}.

Then the hamming distance array hd[][] is obtained from the vector set and Reordering algorithm is applied to find the reordered test vector set with minimum hamming distance HD_{prop}. The reordered set is applied to the same circuit to find the total number of switching activities which is represented by SW_{prop}.

In this way $HD_{DEF,}$ $SW_{DEF,}$ HD_{prop} and SW_{prop} are obtained for the various benchmark circuits and the results are tabulated in Table II. When compared with DEFGEN algorithm, the proposed algorithm reduces the hamming distance up to 63% and reduces the switching activities of the circuit up to 53%. The ratio of % reduction in SW_{prop} and % reduction in HD_{prop} (S/H) is used to represent how much amount of switching activities reduced when compared with hamming distance reduction. This is shown in the Table II for the bench mark circuits.

If S/H <1, it means that Percentage reduction of switching activity is lesser than that of hamming distance and if S/H >1, then the percentage reduction of switching activity is more than that of hamming distance. Dependency nature between hamming distance at the input and switching activity of the circuit can be studied using this parameter S/H. When the value is high, the dependency is more and less dependent when the value is low. Based on the analysis the circuits can be classified into three cases namely Less dependent, Dependent, More dependent.

Case1. Less Dependent: In this case the value of S/H is very small and the switching activity of the circuit is more or less independent with hamming distance at the input of the circuit. Circuit c1908 comes in to this category whose S/H value is 0.068.

Case2. Dependent: In this case the value of S/H is less than 1 and the switching activity of the circuit is dependent with hamming distance at the input of the circuit. This means that the transition occurred in the internal circuit lines is depending on that of input lines. This is because of logic for which the circuit is implemented. Circuits c17, c499, c880, c1355, c5315, and c6288 are falling in to this category whose S/H values are given in the Table2. For example, in C499, only 15 % of switching activity is reduced while 30 % reduction is attained in hamming distance.

Case3. More dependent: In this case the value of S/H is more than 1 and hence the switching activity of the circuit is more dependent with hamming distance at the input of the circuit. This means that the more number of transitions are occurred in the internal circuit lines for one transition in the input line. Circuits c432, c2670 and c3540 are falling in to this category whose S/H values are 2.9, 2.2 and 2.7 respectively.

Based on the above analysis, most of the circuits fall in the case2 and case3 where dependency is more. Hence the reduction in hamming distance reduces the switching activity of the circuit which reduces power dissipation of the circuit during transitions.

The proposed work is compared with two previous works GA1[6] and GA2[7]. Both the approaches are Genetic Algorithm based and don't care bit of the test vector set is used for reordering. The Benchmark comparison results are shown in the Table III which depicts that both Hamming Distance and switching activity are reduced by average value of 89% when compared with GA1 [6] and switching activity is reduced by 71% when compared with GA2[7] .

V. Conclusion

In this paper we presented a method for reducing the power dissipation during testing of combinational circuit. Since the 80% of the total power dissipation in CMOS circuits is due to the switching activity, the proposed algorithm reduces the switching activity by minimizing the hamming distance between successive test vectors. The algorithm is designed using graph theory model and implemented by C language and Hardware Description Language (HDL) simulation tools. The performance of the algorithm is tested with ISCAS bench mark circuits. Experimental results show that our approach can reduce switching activity up to average of 12.83 % when the test vectors generated by the proposed algorithm are applied during test phase. Hence there was reduction in power dissipation during test phase. The low power design in VLSI Circuits make real needs for the test power optimization approaches of time saving and better optimization effect.

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K.Paramasivam was born in Erode, Tamilnadu, India, on 23rd April, 1973. He earned his Bachelor degree in Electronics and Communication Engineering from Bharathiar University, Coimbatore, Tamilnadu during 1995. He received his Master degree in Applied Electronics from Bharathiar University, Coimbatore, Tamilnadu during 1997. Currently he is pursuing his Ph.D. in the area of "Low Power VLSI Testing" under the guidance of **Dr.K.Gunavathi**, PSG College of Technology, Coimbatore, under the regulations of Anna University, Chennai, Tamilnadu.

He was worked as faculty in ECE Department, Amrita Institute of Technology. Presently he is with Bannari Amman Institute of Technology, Erode as Assistant Professor, in the Department of ECE. He is having 10 years of teaching and 4 years of Research experience. He has published 3 research papers in Journals and 19 papers in both International and National Conferences conducted in India and abroad. His areas of interest are VLSI design and low power testing.

Mr. K. Paramasivam is life member of Indian Society for Technical Education(ISTE), Institution of Electronics and Telecommunication Engineers(IETE). His Bio-data has been published in **Marquis Who'swho in Science and Engineering** (2006-2007 edition), USA. He received three best paper awards in Conferences and Best Youth Red Cross program officer award from Tamilnadu state of India.

Dr. K. Gunavathi completed Undergraduate, Post graduate and Doctoral program from PSG College of Technology in the years 1985, 1989 and 2000 respectively. Currently working as Professor in ECE Department, PSG College of Technology, Coimbatore.

She has 20 publications and two books to her credit. She involved in a R &D work of All India Council of Technical Education and received best project award. Her areas of interest are VLSI design and testing and digital communications.

Table II Bench mark results

Circuits	**Fault Coverage %**	**Hamming Distance**			**Switching Activity**			**S/H**
		Defgen HD_{DEF}	**Proposed Algorithm HD_{PROP}**	**% in Reduction (H)**	**Defgen SW_{DEF}**	**Proposed Algorithm SW_{PROP}**	**% in Reduction (S)**	
C17	100	26	14	46	57	49	14	0.3
C432	96.98	455	422	7.2	8284	6514	21	2.9
C499	100	473	332	30	4373	3704	15	0.5
C880	96.98	571	434	24	6362	5864	8	0.33
C1355	72.68	653	362	45	15017	11944	21	0.46
C2670	88.57	1023	970	5	5714	5100	11	2.2
C6288	70.22	144	54	63	154231	131238	15	0.84
C1908	73.58	122	99	19	2086	2059	1.3	0.068
C3540	91.14	487	422	7	7430	5999	19	2.7
C5315	96.04	1633	1380	15	17776	17158	3	0.2
Average				26.12 %	Average		12.83 %	

Table III Comparison with previous work

Circuit	Hamming Distance			Switching Activity				
	GA1 [6]	**Proposed algorithm**	**% in reduction**	**GA1 [6]**	**Proposed algorithm**	**% reduction**	**GA2 [7]**	**% reduction**
C1908	1537	99	94	36887	2059	94	9129	77.4
C2670	7827	970	88	20345	5100	75	15357	66.79
C3540	3019	422	86	33419	5999	82	38642	84.5
C5315	9901	1380	86	54554	17158	69	36519	53
	Average		89 %	Average		80 %	Average	71 %