UNIVERSITÉ DE GRENOBLE

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ DE GRENOBLE

Spécialité : **Micro et Nano Electronique**

Arrêté ministérial : 7 août 2006

Et de :

DOCTEUR DE L'INSITUTO TECNOLÓGICO Y DE ESTUDIOS SUPERIORES DE MONTERREY

Spécialité : **Technologies de l'Information et Communications**

Présentée par

José I. GÓMEZ-QUIÑONES

Thèse dirigée par **Olivier ROSSETTO** et **Sergio O. Martínez Chapa**

préparée au sein **Laboratoire de Physique Subatomique et de Cosmologie** de **L'École Doctorale d'Electronique, Electrotechnique, Automatique et Traitement du Signal** et du **Département de Génie Electrique et Informatique** de **l'Instituto Tecnológico y de Estudios Superiores de Monterrey**

Conception et Implémentation d'un Stimulateur Multi-Canal pour les Dispositifs Microfluidiques

Thèse soutenue publiquement le **10 octobre 2011**,
devant le jury composé de :

Dr. , Skandar, BASROUR
Professeur, Université de Grenoble, Président
Dr. , Bruno, ALLARD
Chercheur et Professeur, Institut National des Sciences Appliquées , Rapporteur
Dr. , Jesús, SANTANA-SOLANO
Chercheur et Professeur, CINVESTAV Unidad Monterrey, Rapporteur
Dr. , Graciano, DIECK-ASSAD
Chercheur et Professeur, ITESM Campus Monterrey , Examinateur
Dr. , Olivier, ROSSETTO
Maître de conferences à l'Université de Grenoble, LPSC, Directeur de thèse
Dr. , Sergio O., MARTÍNEZ-CHAPA
Chercheur et Professeur, ITESM Campus Monterrey, Directeur de thèse

Dedicatoria

Con todo mi amor para Bernarda, Ivette e Isabella Sue

⋆ ⋆ ⋆

A Jesús, con todo mi respeto, cariño y amor, te extraño mucho papá...

Agradecimientos

- A Dios, rector de mi vida, mi luz y mi salvación.
- Al Dr. Álvaro y Sra. Dorita por tratarme como a un hijo en todo momento, los quiero mucho. Gracias por apoyarme siempre.
- Mi mas sincero agradecimiento para mi asesor, Dr. Sergio O. Martínez Ch. por su grán apoyo, por su motivación y su guía. Gracias por confiar en mi. Gracias porque en muchas ocasiones tuvo más fé en mi que la que yo tenía en mi mismo.
- Al Dr. Graciano Dieck Assad por sus consejos y su grán ayuda en la revisión y corrección de este documento.
- A la Dra. Blanca Lapizco por su participación en el comité de tésis y por la excelente revisión que realizo a esta disertación
- Al Dr. Hugo Terashima y Dr. José Luis Gordillo por su apoyo durante mi estancia en el programa doctoral
- Al Dr. Farid Bautista D. por sus consejos, su apoyo y ayuda incondicional en todo momento.
- A la Dra. Martha Salomé por su apoyo por sus consejos y por escucharme
- A Víctor Hugo Perez por su grán ayuda en muchos de los análisis contenidos en éste documento y a Hector Moncada, es un placer trabajar con ustedes.
- A mi tía Fanny Huffmann, a Cynthia y Christine por hacer muy placentera mi estancia en Europa, mi agradecimiento eterno
- A mi padrino Pepe y mi tía Isabel por apoyarme y darme ánimos siempre. Usted sabe padrino, verdad que si?
- A mis hermanos, Maricruz, José Francisco y América, los quiero mucho.

Remerciements

Je voudrais vivement remercier tous ceux qui m'ont aidé á mener á bien mes travaux de recherche, et tout particuliérement:

- Le Professeur ROSSETO, Olivier pour sa grande aide et ses conseils précieux qu'il a eu pour moi, non seulement pour en tant qu'élève, mais aussi en tant qu'ami. En ce sens, j'aimerais lui exprimer ma reconnaissance éternelle.
- Les Professeurs BASROUR, Skandar et ALLARD, Bruno pour leur participation au jury et leur contribution très précieuse dans la correction de cette thèse.
- Mon ami et professeur, M. MICHEL, Guillaume de m'avoir ouvert les portes de la langue française et pour son grand soutien.
- M. Raymond et Mme. Nanou de m'avoir accueilli et considéré comme un membre de leur famille.
- Mon ami MARCOTTE, Galdric, pour ses grandes expressions d'amitié pendant mon séjour en France.
- Mon ami YAMOUNI, Mahfoud pour ses conseils, son soutien et son amitié.
- M. BOUVIER, Joel et RARBI, Fatah pour leur aide très précieuse dans la réalisation du prototype.
- Mes collègues du service électronique au Laboratoire de Physique Subatomique et de Cosmologie: messieurs BOULY, Jean-Luc, BOURRION, Olivier, BOSSON, Germain, SCORDILIS ,Jean-Pierre, MUGGEO, Savino, FOGLIO, Robert, RICHER, Jean-Pierre et LAGORIO, Eric, pour leur aide pendant la réalisation de mon projet.
- M. KOX, Serge pour son sutien pendant mon séjour au LPSC.
- Merci aussi Ludovic pour ton amitié!
- Et pour finir, M. PETRONE, Charles et Alain pour leur soutien inconditionnel.

Design and Implementation of an Application Specific Multi-Channel Stimulator for Electrokinetically-Driven Microfluidic Devices

by

José I. Gómez Quiñones

Abstract

This dissertation presents the design and implementation of a 16-channel sinusoidal generator to stimulate microfluidic devices that use electrokinetic forces to manipulate particles. The generator has both, independent frequency and independent amplitude control for each channel. The stimulation system is based upon a CMOS application specific (ASIC) device developed using 0.35µm technology. Several generator techniques were compared based on frequency range, total harmonic distortion (THD), and on-chip area. The best alternative for the microfluidic applications is based in a triangle-to-sine converter and presents a frequency range of 8kHz to 21MHz, an output voltage range of 0V to 3.1V_{PP}, and a maximum THD of 5.11%. The fabricated device, has a footprint of 1560µm×2030µm. The amplitude of the outputs is extended using an interface card, achieving voltages of 0V to 15V_{PP}. The generator functionality was tested by performing an experimental set-up with particle trapping. The set-up consisted of a micromachined channel with embedded electrodes configured as two electrical ports located at different positions along the channel. By choosing specific amplitude and frequency values from the generator, different particles suspended in a fluid were simultaneously trapped at different ports. The multichannel stimulator presented here can be used in many microfluidic experiments and devices where particle trapping, separation and characterization is desired.

List of Figures

List of Tables

Contents

Chapter 1

Introduction

1.1 Lab On a Chip concept

In recent years we have seen an entire new generation of devices aiming to perform bio/chemical analysis at microscale: the concept of a Lab-on-a-chip (LOC). Advances of micro and nano devices have been reported in applications like biosensors, micro-actuators, micro-fluidics, micro-valves, micro-pumps, intelligent surgical tools, therapeutic systems and MEMS for biomolecular recognition [3].

The ultimate goal of miniaturized devices who interact with biological molecules is to transport, mix, detect and characterize a raw sample. Among the fundamental attributes of a LOC are:

- To have smaller sample volumes.
- To reduce the number of sample handling steps.
- In certain processes, to reduce the sample size leads to a reduction in the processing time or preparation of the sample.
- To decrease the human involvement in the processing of complex protocols.
- To allow the development of portable systems.

The lab on a chip or Micro-Total analysis systems (µTAS) [4] require miniaturized devices such as separators and bioreactors which cover an abundant field of study including air and water quality analyzers, medical diagnostics, DNA amplification, protein labeling etc.

One of the most promising applications of LOC's is clinical diagnostics. The LOC's with capability to deal with live cells which integrate mechanical, optical and electronic components are are known as BioMEMS. The main objective in clinical diagnostic BioMEMS devices is to develop devices capable to provide a rapid analysis of organic samples offering reliable results.

BioMEMS devices should posses the following characteristics:

Small. The size reduction gives freedom of action, avoiding the confinement of physician and/or patient to medical facilities.

Fast. One of the main goals is to have accurate results as soon as possible.

Disposable. At least the contact region with the organic samples should be easily disposable, avoiding bio-contamination.

Inexpensive. Even when we are talking about state of the art systems, their cost should not represent a major issue.

Mass production. The production process must assume that a considerable amount of devices reach the market in a short period of time.

Integration. The chip must be a collection of mechanic, electronic, optic systems capable of offering the complete diagnosis without the need of extra components.

Nowadays LOC devices have already been commercialized accomplishing a small number of functions, very often they require supplementary support equipment such as computers, microscopes, signal generators etc. For example, to detect three myocardial proteins produced in abnormal quantities once a hearth attack has taken place, Biosite presented a solution (Biosite chip)[5] allowing the portability and rapidity of results (15 mins while traditional systems need hours). The results of the analysis are given in a small diagnostic device (Figure 1.1a).

Another good example is the DNA LabChip of Agilent[6] capable of perform genotyping (the identification of an object from characteristics sequences of genes). This chip can also identify RNA and proteins although a fully integrated and miniaturized system is not available yet. The device must be used along with the Agilent 2100 Bioanalyzer to deliver results(Figure 1.1b).

The next step in LOC's evolution is their integration with intelligent systems. Even though several appliances perform several automatic tasks. In the near future LOC's will require essays of greater technical complexity integrating disposable microelectronic and microfluidic components, and also to be programmable, reconfigurable and reusable. In many ways, the LOC's are natural fit for a point-of-care (POC) diagnostics device[1]. The rapid POC testing could lead to fast intervention and its market is estimated to be over $10 billion with important growth in cardiac and infectious diseases. POC diagnostic systems need to be simple devices with minimal or no ancillary equipment. Hence the need to provide intelligence to LOC instruments.

[1] A diagnostic test performed near the patient without the need of a clinical lab [7]

(a) **Biosite chip.** A droplet of blood is placed in a special platform on the chip, the results of the analysis are given on an special appliance in just 15 mins. The diagnostic can determine whether or not a hearth attack has taken place.

(b) **Agilent.** This device permits the identification of specific genetic sequences, the process takes 10 mins and the results are given in a microcomputer.

Figure 1.1: **Examples of Lab-on-a-chip devices.**

1.2 Microfluidics

In the 1990's MEMS and miniaturization opened the door to a new discipline: Microfluidics. Microfluidics can be defined as the study of flows that are simple or complex, mono or multi phasic, which are circulating in artificial microsystems [8]. The advantages of miniaturization allowed that many different microfluidic systems were fabricated, from electrophoretic separation systems to electro-osmotic pumping systems, micromixers, DNA amplifiers, cytometers and chemical microrreactors.

Microfluidics constitutes the real core of most labs-on-a-chip and has enabled the generation of new commercially successful products ranging from portable insulin delivery devices to high speed inkjet printers. Also, microfluidics represents the platform that has catapulted µTAS to be considered as one of the most promising research technologies for biology, chemistry and bioengineering.

Electrokinetics (EK) is rapidly gaining preferences as a microfluidic actuation mechanism, due to the fact that in many ways EK devices offer advantages over pumps and actuators with valves, gears and mechanical elements involving moving parts. EK induces micro-fluid or particle movements within a microchannel driven by an electric field. Moreover, using microdevices allows the generation of large electric field gradients using few volts to polarize closely-spaced electrodes.

1.3 Justification

LOC platforms still have a long way to go for increasing speed and throughput in the delivery of results to allow practical implementations in health care institutions. The vast majority of current microfluidic platforms take use of conventional signal generator, such instruments must be stacked when more than one signal is desired. The broader impact of LOC's will come to the scene with the arrival of low power, small, cheap devices capable of offering cell/particle manipulation used in portable systems.

The objective of this research work is to design, fabricate and implement a device capable of generating a large number of independent sine signals with amplitude, frequency and THD (Total Harmonic Distortion) control at each port (output). The use of this microelectronic system will help in electrokinetic tasks providing of multiple independent signals without the need of further equipment. The fact of having multiple stimulation ports offers the possibility of the implementation of a wide range of protocols for particle separation and characterization. The device will be programmable via a serial port and will be fabricated in a standard CMOS 0.35µm process having specifications such as low power and small on-chip area to be included in a portable platform.

1.4 Thesis organization

Chapter 2 reviews the state of the art in devices for separation of particles. Chapter 3 examines the theoretical frame of digital and analog oscillator. While Chapter 4 reviews the corresponding electrokinetic theory. The design of the device as well as the analysis of the digital and analog prototypes and the evaluation that led us to choose the final prototype are discussed in Chapter 5. The implementation of the prototype and the details of the integrated circuit and its electric characteristics are reviewed in Chapter 6. Chapter 7 reviews the results obtained from the measurements to the outputs of the device and the outcome of an experiment of particle separation in which our integrated circuit delivered the required stimulation signals. Chapter 8 describes the conclusions of this dissertation project.

Chapter 2

State of the art in stimulation systems for electrokinetically-driven microfluidic devices

The use of electric fields to achieve transport, separation and analysis in microfluidic devices has been demonstrated in many applications. This chapter reviews the state of the art on devices that perform electrokinetic tasks making use of multiple excitation stimulus or perform manipulation of frequency and/or amplitude in their output signals.

Woolley et al.[9] demonstrated that high-speed DNA separations can be performed on microfabricated capillary electrophoresis (CE) channels arrays, establishing the feasibility of integrated devices for electrophoretic DNA analysis. In a later design[10], they improve the speed and throughput allowing analysis of 12 parallel samples in less than 160s. The first stage of the process is the injection phase performed by applying +80V. Immediately following injection, the separation phase was carried out by applying +1200V.

Wang et al.[11] demonstrated the manipulation of living cells including isolation, concentration of cells, trapping and positioning, levitation, linear motion and circulation of individual cells for characterization using dielectrophoresis. They used *Friend murine erythroleukemia* DS19 cells. Voltage signals between 1kHz and 100MHz were used and the cell levitation appeared at frequencies below 120kHz. The levitation height was found to depend on the frequency and magnitude of the applied voltages. The maximum levitation was 26µm at frequencies 1-60 kHz with an applied voltage of 1.75V. The cells exhibited antifield and cofield rotation occurred at frequencies of 160kHz and 50MHz. The cell entrapment occurred at frequencies above 140 kHz.

Youlan Li and Karan V.I.S Kaler[12] proposed a planar microelectrode array fabricated on a glass substrate to fractionate cells into purer subpopulations. They investigated the dielectrophoretic response of viable and nonviable canola cells. They performed variations in the applied voltage of $9V_{PP}$ to $16V_{PP}$ leaving the frequency fixed, and manipulations in frequency going from 10Hz to 10MHz.

Esther G. Cen et al.[13] designed and implemented a microchip with three types of microelectrodes of similar layouts but different functions. They implemented a system called Leviator-Rotator in which, different kinds of electrodes were excited to perform conveyance and electrorotation. The electrodes received stimulus of $5V_{PP}$ to 15 V_{PP} with a frequency from 1kHz to 10MHz, injected with a Sin-Cos modulator and an amplifier controlled by a PC. They have confirmed and validated the theoretical predictions demonstrating the manipulation and polarization using a single microchip.

Manaresi et al.[14] presented an 8×8 mm^2 chip implemented in a 0.25µm CMOS technology featuring 102,400 actuation electrodes in an array of 320×320. The system included an embedded memory for electrode programming and an optical sensor. The huge amount of electrodes permitted a displacement controlled by software of more than 10,000 individual living cells. Each electrode was energized by either an in-phase or counter-phase sinusoidal voltage signal according to programmed patterns. The electric field is modified according to the defined pattern producing dielectrophoresis (DEP) cages. The manipulation was tested using 50µm polystyrene beads. The actuation voltages where 3.3V with a frequency range from 100kHz to 10MHz.

Il Doh et al.[15] designed a high-throughput continuous cell separation chip using switched ac signals. They proposed a three electrode system in which sinusoidal electric fields of 5MHz and $8V_{PP}$ are applied generating a non-uniform electric field. They reported ranges of purity of 95.9% $\sim$ 97.3% in the separation of viable and non-viable yeast cells.

A. Enteshari et al. [16] proposed a system to perform DEP analysis with programmable planar arrays called Lexel™. Their architecture is configurable via software and is adapted to implement various AC electrokinetic techniques with a two dimensional randomly addressable electrode array driven by one of four sinusoidal analog signals. The objective of this approach was to have a flexible microelectrode structure to be used as bio-analysis sensor for a low-power SoC. The chip has an array of 120×120 electrodes in a 1.6×1.6 mm^2 die, using a 0.18µm technology (TSMC CMOS process). The stimulating voltage is 3.3V with a frequency range of 1kHz to 5MHz generated with phases of 0, $\pi/2$, π, $3/2\pi$, 2π rad/sec.

Byoung-Gyun Kim et al.[17] presented a chip with a 2×2 micro-well array using silicon substrate and PDMS[1] channel structures for high-throughput biochemical cell-based assay applications. They propose a scheme for active positioning control of a single cell using DEP, applying signals of $10V_{PP}$ at a frequency of 200Hz. They demonstrated the successful capture of 15μm polystyrene beads applying negative DEP in the two-dimension micro well array. They performed accurate control of positioning/capturing cells one by one actively. With the proposed scheme, individual cell/microbead can be positioned and captured in each selected micro-well, and the total number of cells/microbeads in each micro-well can be easily controlled.

K. Wayne Current et al.[18] developed a high voltage integrated circuit to transport droplets on programmable paths. The chip creates DEP forces that move the droplets,

[1]Polydimethylsiloxane

it has an array of nominally 100V electrode drivers and a maximum power of 1.87W. The operating power is a changing parameter because it is related to the electrokinetic force involved in the cell manipulation, the used structure, the shape of the channel, the electrode geometry etc. However, we will take this number as a power reference in our prototype. The programmable fluidic processor (PFP) of Wayne Current et al. can use both low and high voltage excitation. Since the volumes and masses of biological cells require various DEP forces, the PFP can control them by having variable electrode excitation, voltage amplitude, phase and frequency. They used square waves an all digital electronics to drive the electrodes. Analog circuitry for generating sinusoidal electrode excitations has been included in the same device.

Bang-Chih-Liu et al.[19] have incorporated a filtering microstructure and a dielectrophoresis force device. They applied individual input voltage with different frequency on the various rows of the microchip. The separation function could be achieved by attracting the target particles and releasing the unwanted ones. The circuit was designed to generate 16 output signals adopting crystal oscillators with ripple counter acting as frequency dividers to make it an adjustable and multi-output circuit. They reported their obtained results in the separation of glass beads from latex beads.

James T. Y. Lin et al.[20] designed a DEP microchip using standard one-layer metal process capable to perform cell concentration, transportation and separation, the chip's waveforms were composed of sinusoidal voltages of $6V_{PP}$ and 1MHz. The excitation was controlled with a DAC card. This DEP microchip demonstrated that collection, transportation and separation of a variety of particles on the same parallel electrode array was possible.

Ting-Chen Shih et al.[21] proposed and demonstrated a biochip integrating DEP traps and a programmable DEP array for the multisorting applications of biomolecules. The voltage on each individual electrode was preprogrammed and controlled in real time using LabView. With fluorescence labeling/detection and this chip, is possible to address sorting applications in a low concentration sample with better selectivity and robustness. Having programmed the potentials, a mobile probe bead can migrate to the desired outlet channel. The device was micromachined on a silicon wafer with micropyramid DEP traps and a 5×5 DEP sorting array bonded with a PDMS lid.

Rodrigo Martinez-Duarte et al.[2] presented a multi-stage, multi-frequency carbon DEP device for filtering and separation with high throughput. The voltage and frequency of one of the four ports for CarbonDEP arrays can be controlled. The excitation module can deliver a signal amplitude of $1V_{PP}$ to $13V_{PP}$ with a resolution of 0.05V at frequencies up to 12.5MHz, having frequency resolution of 2.98Hz[22]. The sinusoidal signals are generated with a strategy called Direct Digital Frequency Synthesis (DDFS). They reported the separation of three different particles with no throughput degradation under an increment in the flow rate.

Honghua Liao et al. [23] proposed a system to perform traveling wave DEP based on SOPC (System on Programmable Chip). Four outputs with independent control of phase are available in the prototype. The traveling wave DEP electric field is created by the four outputs and is capable to drive biological particles to achieve separation in

a microchannel. The feasibility of the results is demonstrated by simulation results.

Maziyar Khorasani et al. [24] presented a high-voltage CMOS controller for microfluidics. This system is used to perform capillary electrophoresis on a 2cm.×1cm. glass chip. The controller offers four high-voltage output drivers capable to switch 300V, and its dc-dc converter can generate up to 68V using external passive components.

Heather Wake and Martin Brooke [25] performed low voltage electrophoresis (EP) on a CMOS chip. Their architecture operates with only a 5V power supply. They use 100 individually addressable electrodes to move the electric field with the sample as it travels along the separation area. Voltages ranging from 0.01V to 5V can be used over distances of 36µm to 1.8 mm, yielding the ability to generate electric fields from 0.05V/cm to 1389V/cm.

A microfluidic-driving manipulation array was presented by Tzu-Yu Chao and Cheng-Hsien Liu [26] for the manipulation of microscale biological samples based on Alternating Current Electro-Osmosis Flow (ACEOF). Controlling the voltage and frequency the actuator can not only orient the microscale objects but also convey them. The controller of the array is set-up using a manual switch circuit board to operate the particle manipulation.

A fully integrated CMOS interface for cell manipulation and separation in LOC devices is proposed by Mohamed Amine Miled and Mohamad Sawan in [27]. Their interface includes all microelectronics circuitry for dielectrophoretic manipulation and capacitive detection. An embedded microcontroller to command frequency and phase is included. The device can perform rotation, translation and separation of cells. The circuit provides four different AC voltage signals with a maximum amplitude of 3.3V and a frequency range of 10MHz.

As we have seen, electrokinetic tasks rely on signal generators, most of the devices summarized in Table 2.1 are stimulated using external generators. From the dedicated stimulators we may note a great need of multiple and independent signals with control of amplitude and frequency. The incorporation of such stimulators to microfluidic devices can contribute in the integration of better diagnostic and portable appliances. Also the embedded circuitry reduces considerably the overall cost and power consumption of the equipment.

Currently none of the existing prototypes described in the bibliography present a compact design, low power and a large of stimulator ports allowing the manipulation of a large variety of cells/particles all those characteristics integrated in the same chip. The challenges at this point will be to have a device capable to offer multiple stimulation ports, with a wide range of frequencies to manipulate a large number of particles/cells. The invention must count on low power consumption and small size (in order to be portable), with the possibility of being mass produced. The research and prototype presented in this work addresses these features.

Table 2.1: **Summary of advances in Electrokinetic-driven devices**

EK force	Voltage(V)	Frequency	Reference	Tested on	ASIC	Year
CE	+80, +1200	DC	Wolley et al. [9], [10]	pBR322 *MspIDNA*	No	1997
DEP	1-4	1KHz-10MHz	Xiao-Bo et al. [11]	*DS19*	No	1997
DEP	16	10Hz-10MHz	Youlan Li et al.[12]	Viable and non-viable canola cells	No	2002
DEP	1-10	10kHz-30MHz	Lifeng Zheng et al. [28]	Latex beads, Fluorescently labeled λ phage DNA	No	2003
DEP	5-15	1KHz-10MHz	Esther G. Cen et al. [13]	Canola protoplast	Yes	2003
DEP	3.3, 6.6, 9.9	100KHz-10MHz	Nicolo Manaresi et al. [14]	*Eukaryotic* cells[1]	Yes	2003
DEP	8	5MHz	Il Doh et al. [15]	Viable and non-viable yeast cells (*Saccharomyces cerevisiae*)	No	2004
DEP	3	1KHz-5MHz	A. Enteshari et al. [16]	Polystyrene microbeads	Yes	2005
DEP	10	1MHz	Byoung-Gyun Kim et al. [17]	Polystyrene microbeads	No	2005
DEP	10	200Hz	K. Wayne Current et al. [18]	PBS[2] droplets	Yes	2005
DEP	4, 8	100Hz-370KHz	Bang-Chih Liu et al. [19]	Separation of latex from glass beads	No	2005
DEP	6	1MHz	James T. Y. Lin et al. [20]	Polystyrene microbeads, *Pichia* yeast cells, *HeLa* cells	No	2007
DEP	8	1MHz	Ting-Chen Shuh et al. [21]	p50, conjugate *I-kappa-B-alpha* proteins	No	2007
DEP	1-13	3Hz-12.5MHz	R. Martinez-Duarte et.al. [2]	*S. cerevisae*	No	2008
DEP	N/A, Four phases 0°, 90°, 180° and 270°	N/A	Honghua Liao et al. [23]	No test	Yes	2008
CE	0-68	DC	M. Khorazani et.al. [24]	DNA sizer	Yes	2009
EP	0.01-5	DC	Heather Wake and Martin Brooke [25]	No test	Yes	2009
EO	2-10	1kHz, 10kHz, 50kHz, 100kHz	Tzu-Yu Chao and Cheng-Hsien Liu [26]	Latex beads	No	2009
DEP	0-3.3	1Hz-10MHz	Mohamed Amine Miled and Mohamad Sawan in [27]	Microspheres	Yes	2010

Chapter 3

Theoretical Background on Analog and Digital Oscillators

This chapter provides a brief introduction to the theory of analog and digital oscillations, describing their main characteristics and operation principles.

From the State of the Art chapter we have seen that the global objective of the cited inventions is the integration of a Lab-on-a-Chip device. Many of them center their study in the creation of the microfluidic platform leaving the stimulation to external sources. A multi-stimulation device will offer the capability to perform different and new research protocols providing of independent signals to characterize, filter and displace cell populations simultaneously. Several alternatives were analyzed to implement the multi-signal generator IC to stimulate electrokinetic platforms. Those alternatives cover digital and analog schemes. The digital strategies are:

- Delta Dirac Unstable Oscillator (DDUO)
- Direct Digital Frequency Synthesizer (DDFS)

The analog implementations are:

- Operational Transconductance Amplifiers and Capacitors (OTA-C)
- Triangle to Sine Converter (TSC)

3.1 Digital approach

The digital sinusoidal oscillators are basic circuits in communications, music/voice synthesis, control, radar and digital signal processing systems. These oscillators exhibit the advantages of many digital systems:

- Flexibility
- High Stability
- Low cost
- Programmability

The control of sine waveforms can be a difficult task in analog systems, because they need to include discrete components such as resistors, capacitors or inductors to control waveform specs. Adding those elements increases the on-chip or physical area, limits IC performance to a range of frequencies. On the other side oscillators based on digital techniques allow a good control over the frequency, phase and even amplitude of generated sine waves.

Among the preferred implementations of digital sine waves by the designers are:

ROM Look-Up Table A ROM is used to store the samples of the sinusoid and later the data is presented at specific-time intervals to produce the sinusoidal signal (we will reach to this specific approach later in this chapter).

Cordic-Algorithm based Similar to the ROM look-up table technique but the samples of the sinusoid are generated interactively without being stored in a ROM.

Digital feedback with poles in the unit circle Typically they offer simple hardware but they may also present long-term stability problems; in this chapter we analyzed an algorithm based on this method.

Numeric errors (e.g. truncation) lead to high THD, therefore to lower the distortion by increasing the number of bits can be increased in the system causing an upsurge in the space and consequently in power consumption. The dependence in the word size, the need of further circuitry (like DAC and post-filtering stages) and the computational power represent the major drawbacks of the digital sinusoidal oscillators.

3.1.1 Delta Dirac Unstable Oscillator (DDUO)

One efficient method to generate digital sinusoidal waveforms is the Delta Dirac Unstable Oscillator which is also called *Multiple-output direct-form digital oscillator* [29, 30]. This approach generates the sinusoidal signal in recursive fashion without the need of a ROM and is based in a second-order recursive digital filter with poles located over the z-plane's unit circle.

The oscillator presents very good high-frequency resolution and a large number of samples per cycle, with the advantage of approximately uniform frequency spacing between the generated samples. This is an essential characteristic in communication system applications such as frequency shift keying (FSK) and frequency division multiplexing (FDM).

In its simple form this digital oscillator is characterized by :

$$y(n) = \alpha \cdot y(n-1) - y(n-2) \quad n \geq 0 \tag{3.1}$$

The output sample at time $t = Tn$ is $y(n)$ being T the sampling interval. The ideal discrete output $y(n)$, and its angle θ are:

$$y(n) = \sin(n\theta) \tag{3.2}$$

$$\theta = 2\pi fT \tag{3.3}$$

The number of samples in a complete sinusoidal waveform is:

$$N = \frac{2\pi}{\theta} \tag{3.4}$$

The ideal model of the oscillator is shown in Figure 3.1.

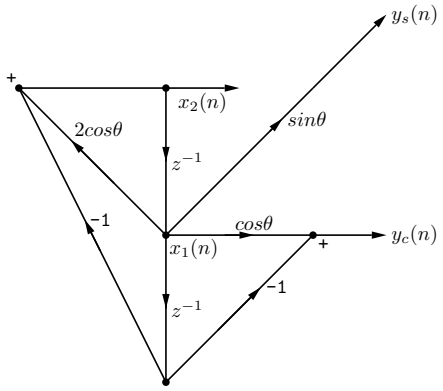


Figure 3.1: **Multiple-output direct-form digital oscillator**

The difference equations for the diagram of Figure 3.1 are:

$$x_2(n) = 2\cos\theta \cdot x_2(n-1) - x_2(n-2) \tag{3.5}$$

$$x_1(n) = x_2(n-1) \tag{3.6}$$

The $\mathcal{Z}$-transform of Equation 3.6 is:

$$X_1(Z) = z^{-1}X_2(Z) + x_2(-1) \tag{3.7}$$

we can see that the $\mathcal{Z}$-transform of $x_2(n-2)$ is:

$$\mathcal{Z}\Big\{x_2(n-2)\Big\} = z^{-1}X_1(Z) + x_2(-2)$$

being $x_2(-1)$ and $x_2(-2)$ the initial conditions.

The $\mathcal{Z}$-transform of Equation 3.5 is:

$$X_2(Z) = \frac{x_2(-1)(z^{-1}) - x_2(-2)}{1 - 2\cos\theta \cdot z^{-1} + z^{-2}} \tag{3.8}$$

From the diagram of Figure 3.1 we could see that the $\mathcal{Z}$-transform of the output signals $y_s(n)$ and $y_c(n)$ can be written as:

$$Y_s(Z) = \sin\theta \cdot X_1(Z) \tag{3.9}$$

$$Y_c(Z) = (\cos\theta - z^{-1})X_1(Z) \tag{3.10}$$

Let $x_2(-1) = 0$ and $x_2(-2) = -1$ and substituting Equations 3.7 and 3.8 in eqns. 3.9 and 3.10 we get:

$$Y_s(Z) = \frac{z^{-1}\sin\theta}{1 - 2cos\theta \cdot z^{-1} + z^{-2}} \tag{3.11}$$

$$Y_c(Z) = \frac{z^{-1}(\cos\theta - z^{-1})}{1 - 2\cos\theta \cdot z^{-1} + z^{-2}} \tag{3.12}$$

The inverse $\mathcal{Z}$-transform of Equations 3.11 and 3.12 are:

$$y_s(n) = \sin(n\theta) \tag{3.13}$$

$$y_c(n) = \cos(n\theta) \tag{3.14}$$

Note that this oscillator generates two components of a complex sinusoidal signal $y_s(n)$ and $y_c(n)$.

3.1.2 Direct Digital Frequency Synthesis (DDFS)

DDFS achieves fast frequency switching with very small steps, over a very wide band, linear phase and frequency shifting. In a Direct Digital Synthesizer (DDS), the output frequency, phase and amplitude can be easily, precisely and rapidly manipulated under digital control. Another advantage of DDFS is linear phase switching [31]. The DDS has the following basic blocks: a phase accumulator, a phase to amplitude converter (a sine ROM), a digital to analog converter and an output filter.

Phase accumulator. This structure consists of a j-bit frequency register which stores a phase increment word, followed by a j-bit full-adder and a phase register. The digital phase word is entered in the frequency register. At each clock pulse this data is added to the data previously stored in the register. The phase increment word is a phase angle step that is added to the previous value at each $1/f_{CLK}$ to produce a linear increasing digital value.

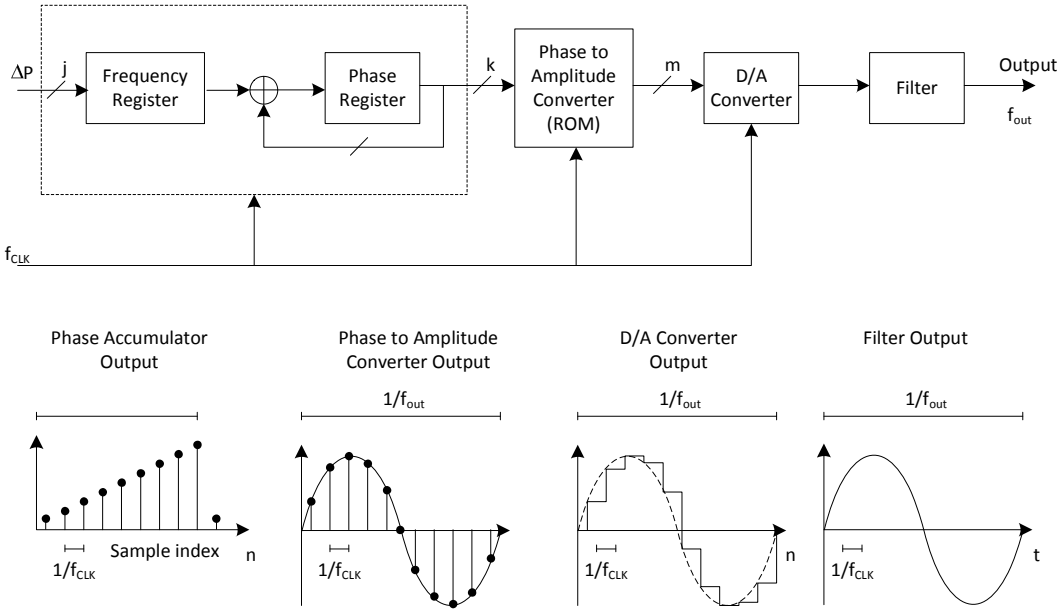


Figure 3.2: **Simplified diagram of DDFS and signal flow as shown in [1].**

Phase to Amplitude Converter. It is implemented in a Read Only Memory (ROM) as a sine look up table which converts the digital phase information into the values of a sine wave. The numerical period of the sequenced samples called from the sine ROM will have the same value as the numerical period of the sequence generated by the phase accumulator. If the phase increment is large, the phase accumulator will step quickly through the sine look-up table to generate a high frequency sine wave. If the phase increment is small, the phase accumulator will take many more steps, generating a slower waveform [32]. The main problem with the DDFS approach is the power budget. One way of minimizing this parameter is to reduce the size of the ROM. Some implementations report the development of low power schemes with consumptions of 35mW [33], and 45mW at 55MHz [34]. Reference [22] implements a ROM stage inside a FPGA system rather than recording the complete set of coefficients of the sine wave. This takes advantage of the symmetry of the sine wave using only values from 0 to $\pi/2$.

Digital to Analog Converter (DAC). The resultant data is then passed through a DAC in order to develop a quantized analog sine wave in voltage or current. In DDS the DAC subsystem is very important. In wide output bandwidth DDSs, most spurs are generated less by digital errors (truncation or quantization errors) and more by analog errors in the D/A-converter such as clock feedthrough, intermodulation and glitch energy [1]. There are some ROM-less schemes that eliminates the power consumption due to memory. The DAC must be fast enough to generate high frequency sine waves. A DAC consumes a great amount of space and power in order to be fast enough to meet the requirements of conversion speed.

Low Pass Filter. The output is also exposed to sampling harmonics of the generated frequency. A final smoothing filter is needed to interpolate the samples. It is possible to reduce switching effects in both amplitude and phase responses while still having a sharp cutoff using an elliptic filter [35].

3.1.3 Total Harmonic Distortion (THD)

A sinusoid generated by a digital synthesizer will produce samples with quantization and other errors inevitably. Therefore the generated waveform will approximate the real sine wave incorporating a certain amount of power falling into other frequencies. This spurious power cause disturbances in the shape of the sine signal referred as harmonic distortion. The main causes of harmonic distortion in the digital domain are:

1. Sample quantization.
2. Non-uniform sampling.
3. Interpolation error.
4. Calculations round-off.

An expression to measure the THD is proposed by [36], and it considers a quantized model of a zero-order filter and relates the THD with the number of discrete points in the generated wave (N). This expression is:

$$THD = \sqrt{\frac{\left(\frac{\pi}{N}\right)^2}{\sin^2\left(\frac{\pi}{N}\right)} - 1} \approx \frac{\pi}{\sqrt{3}N} \tag{3.15}$$

Another approach cited by [37] relates the number of points and quantized steps q:

$$THD = \sqrt{\left[1 + \frac{q^2}{6}\right]\left[\frac{\pi/N}{\sin(\pi/N)}\right]^2 - 1} \tag{3.16}$$

Shanerberger and Awad[38] in the early efforts of implementation of digital oscillators proposed the following expression to calculate the THD:

$$THD = \frac{E_T - E(f_0)}{E_T} \cdot 100\% \tag{3.17}$$

Where the energy of the signal can be computed as follows:

Table 3.1: **THD values for expressions 3.15 and 3.16**

N[a]	THD % [b]		THD % 8 bits [c]	THD % 12 bits[d]
4	48.342585		48.50844577	48.35296774
5	37.772219		37.96865952	37.78452656
6	31.084194		31.31303329	31.09854572
7	26.445004		26.70710892	26.46146163
8	23.028089		23.32389749	23.04668811
9	20.402184		20.7319059	20.42294725
11	16.624785		17.02246084	16.64991771
12	15.219369		15.65093037	15.24669931
13	14.034305		14.49962091	14.06383815
25	7.266674		8.117520673	7.322748934
26	6.986353		7.867242976	7.044636211
48	3.780368		5.227870007	3.88666287
94	1.929789		4.092648205	2.130303282
126	1.439613		3.885359301	1.698957257

[a]With a small N, the signal will present a high THD, the results were obtained with a zero order sample and hold register; the THD level can be improved if a high order filter is included in the design. A big N will demand a high frequency and consequently requires a clock speed at least equals to $N \cdot freq$.

[b]Values calculated with eqn. 3.15

[c]Values calculated with eqn. 3.16

[d]A small q number demands a big number of bits requiring a larger on-chip area

$$E_T = \frac{1}{N}\sum_{k=0}^{N-1}|X(k)|^2 \tag{3.18}$$

and the energy of the fundamental component is given by:

$$E(f_0) = \frac{2}{N}|X(f_0)|^2 \tag{3.19}$$

3.2 Analog Approach

The sinusoidal oscillators are present in most electronic applications. They are widely used in control systems, telecommunications systems, signal sources, music synthesis, measurement systems, digital AC bridges etc. Some of the advantages of analog implementation are:

- Low Total Harmonic Distortion (THD)
- Small on-chip space
- High stability

Two analog selections: OTA-C and triangle-to-sine converter were analyzed. Options that need several capacitors to make oscillations were discarded as they need more on chip space. Oscillators based on LC filters were discarded due to the difficulty in the implementation of on-chip inductors. The obtained results are discussed in this section.

3.2.1 OTA-C

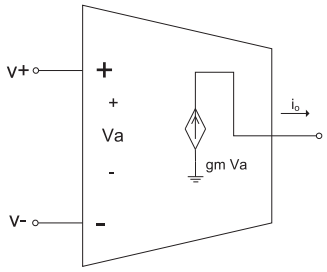


Figure 3.3: **Ideal model for an OTA**

The oscillators using Operational Transconductance Amplifiers (OTA) (Figure 3.3) and capacitors (OTA-C) have been shown to be very well suited for the generation of sinusoidal voltages. OTA based circuits have inherent programmability due to the fact that its transconductance gain can be electrically changed. OTA-C oscillators overcome the limitations in frequency and tunability of conventional opamp based oscillators

Among the advantages of OTA-C's we can find [39]:

- No additional constraints have to be imposed on their frequency response to compensate for local feedback-induced pole displacement.
- The transconductance can be electrically tuned with just varying the polarization current I_{POL} of the transistor
- It is possible to change the frequency in a continuous way
- Low harmonic distortion

It is possible to combine OTA's with capacitors to reach a second order characteristic equation:

$$s^2 - bs + \Omega_o^2 = 0 \tag{3.20}$$

The main design goal is to achieve a separate control of b and Ω. Having independent control on those variables provides a control over the frequency of operation without affecting the oscillation condition[1].

[1] A number of topologies have been studied and their advantages/disadvantages presented in [40]

To achieve free running oscillation, the parameter b must be zero. However, in practical oscillators due to parasitic effects, the poles are displaced from the nominal positions, $s_p = \pm j\Omega_o$, to either the right or left side of the complex planes. For this reason, the oscillator must have its poles initially located inside the right-half complex frequency plane in order to get a self starting oscillation. Figure 3.4 presents the simplest structure to have independent control of b and Ω.

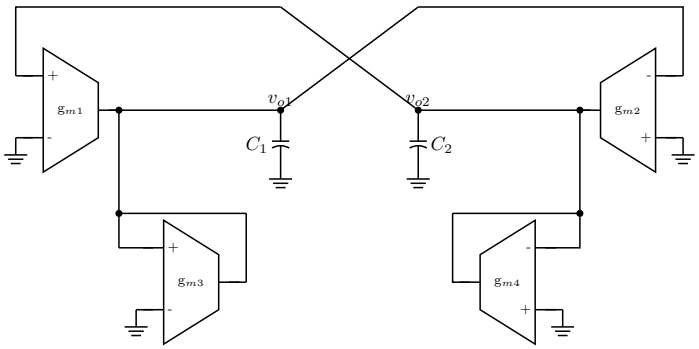


Figure 3.4: **4OTA2C oscillator structure**

The parameters for this structure are:

$$b = \frac{g_{m3}}{C_1} - \frac{g_{m4}}{C_2} \tag{3.21}$$

$$\Omega_o^2 = \frac{g_{m1}g_{m2} - g_{m3}g_{m4}}{C_1C_2} \tag{3.22}$$

There is a coupling between Ω_o^2 and b through $g_{m3}g_{m4}$. The solution to this inconvenience is to connect g_{m4} to the same node as g_{m3} in the called OTA-C quadrature oscillator[41]. Figure 3.5 illustrates this topology which is the selected structure for the analog oscillators developed in this dissertation.

Now, the parameters are:

$$b = \frac{g_{m3} - g_{m4}}{C_1} \tag{3.23}$$

$$\Omega_o^2 = \frac{g_{m1}g_{m2}}{C_1C_2} \tag{3.24}$$

In the VCO's based in OTA-C configuration, the element responsible for the change in the oscillation frequency is the transconductance of every OTA's related to the Ω_o^2 variable. The transconductance can be modified with a simple change in the polarization current I_{POL} of the sink transistor.

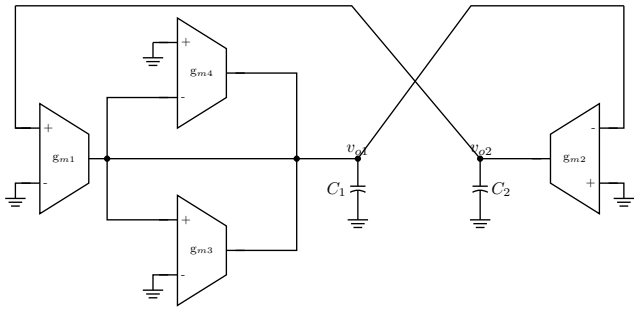
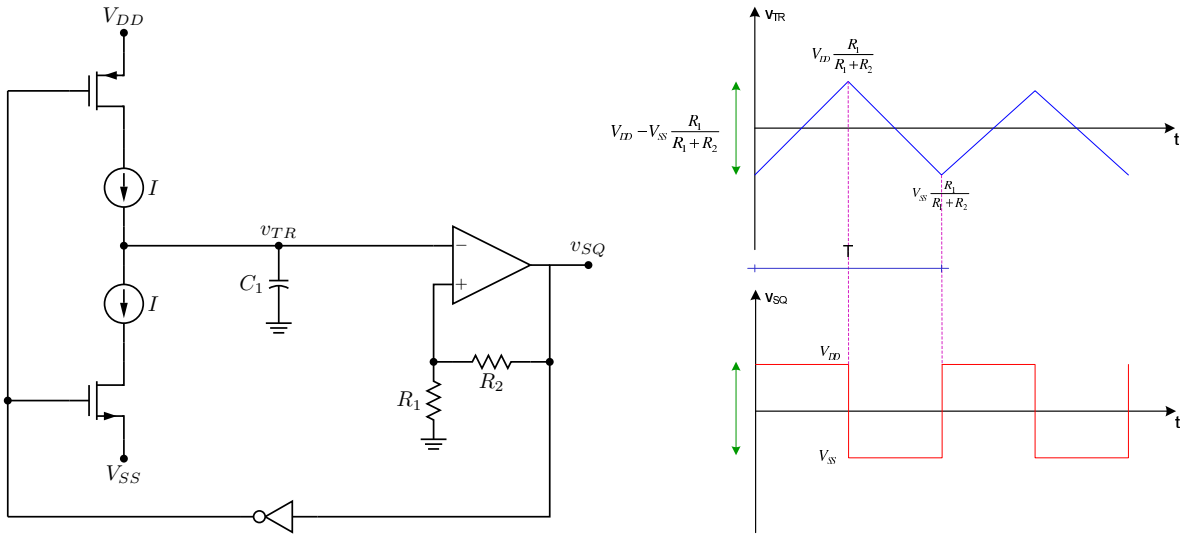


Figure 3.5: **4OTA2C quadrature oscillator**

3.3 Triangle to Sine Converters

In many communications systems, phase locked loops (PLL) and function generators the conversion of triangle signals to sine waves represent a basic signal processing operation. A very precise triangle waveform can be generated using relaxation oscillators; the relaxation oscillator is constructed with current sources, a capacitor and a Schmitt Trigger Comparator, then the sinusoidal wave can be generated through a triangle-to-sine converter (TSC) [42]-[45].

3.3.1 Relaxation oscillator



(a) Relaxation oscillator (b) Obtained waveforms

Figure 3.6: **Relaxation oscillator**

The Schmitt Trigger will commute in its upper limit V_{UL}, given by:

$$V_{UL} = V_{DD} \cdot \frac{R_1}{R_1 + R_2} \tag{3.25}$$

and the lower limit V_{LL} will be in:

$$V_{LL} = V_{SS} \cdot \frac{R_1}{R_1 + R_2} \tag{3.26}$$

The amplitude range at the output of the triangle generator is [46]:

$$\triangle v = (V_{DD} - V_{SS}) \cdot \frac{R_1}{R_1 + R_2} \tag{3.27}$$

We have the relation between voltage and current in a capacitor:

$$i = C\frac{\triangle v}{\triangle t} \tag{3.28}$$

Then, the time needed to go from V_{LL} to V_{UL} will be:

$$\triangle t = \frac{C}{i} \cdot (V_{DD} - V_{SS}) \cdot \frac{R_1}{R_1 + R_2} \tag{3.29}$$

3.3.2 Triangle to Sine Converter in strong inversion (TSC-SI)

The triangle to sine conversion can be implemented using a non-linear block; this structure can be implemented using the non-linear characteristic of a MOS transistor. Depending on the biasing current, the MOS transistor will operate in strong or weak inversion. The operation of the strong inversion approach is described next.

Once we have the relaxation oscillator it is necessary to design the Triangle to Sine converter, depicted in Figure 3.7. The triangle signal enters at the positive terminal of the differential pair; I_O controls the level of saturation needed to perform the conversion. The gain of the pair exhibits an approximately linear characteristic near the zero crossing of the input signal. However in the verge of either peak one of the transistors is driven to saturation voltage and its characteristic becomes quadratic producing a gradual rounding of the triangular wave, the triangular wave must be properly scaled to fit the requirements of the converter (static characteristic of the differential pair, Figure 3.8a).

The differential output is obtained from the v_{o1} and v_{o2} thus, further conditioning is needed to obtain the final signal. The differential pair along an OpAmp with high Slew Rate and a Comparator conform the whole circuit.

Even when the TSC oscillator is simple, its use in a VCO adds a new set of complexities due to the static and dynamic characteristics of the conversion stage. For a given frequency a certain level of distortion is present, the amount of this distortion

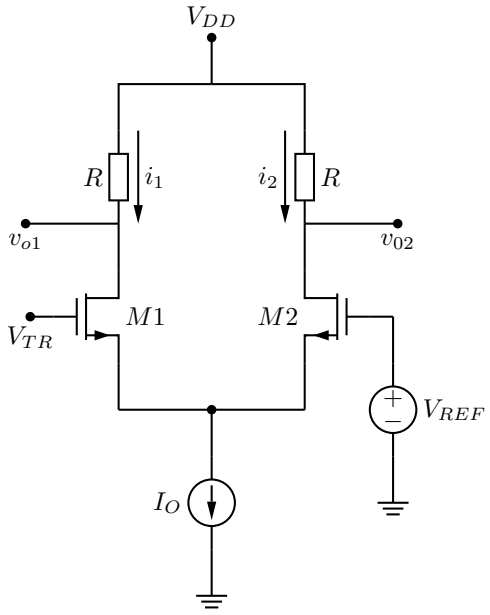


Figure 3.7: **Triangle to Sine Converter in Strong Inversion (TSC-SI)**

may change dynamically as the frequency changes increasing the complexity of the THD control.

The behavior depicted in Figure 3.8 apply to Triangle to Sine Converters working in strong inversion or in weak inversion, as the name says the only difference between them is the amount of current in the polarization stage.

The bias current controls the THD as reflected in Figures 3.8b and 3.8c; the major drawback is that if we choose a very low current to obtain low distortion the output amplitude is also reduced. The current in each MOS transistor differential pair in strong inversion can written as:

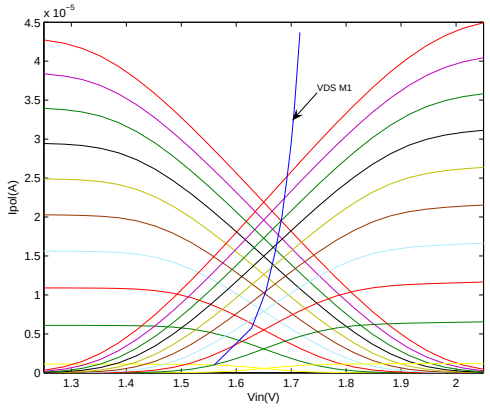
$$I_{D1} = \frac{K'}{2}\frac{W}{L}(V_{GS1} - V_T)^2 \tag{3.30}$$

$$I_{D2} = \frac{K'}{2}\frac{W}{L}(V_{GS2} - V_T)^2 \tag{3.31}$$

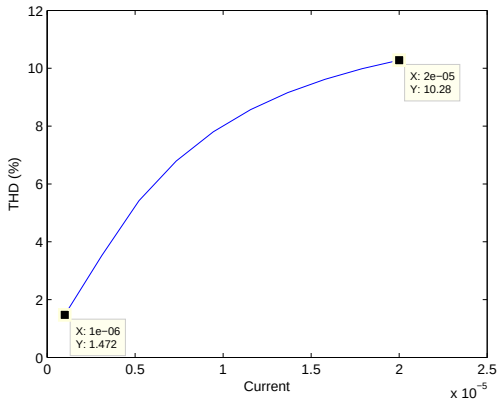
Where the I_D is the current passing through one branch of the differential pair, K' the device transconductance parameter and $(V_{GS1} - V_T)$ and $(V_{GS1} - V_T)$ the input voltages. The output voltages v_{o1} and v_{o2} will be:

$$v_{o1} - v_{o2} = RI_{D2} - RI_{D1} = R(I_{D2} - I_{D1}) \tag{3.32}$$

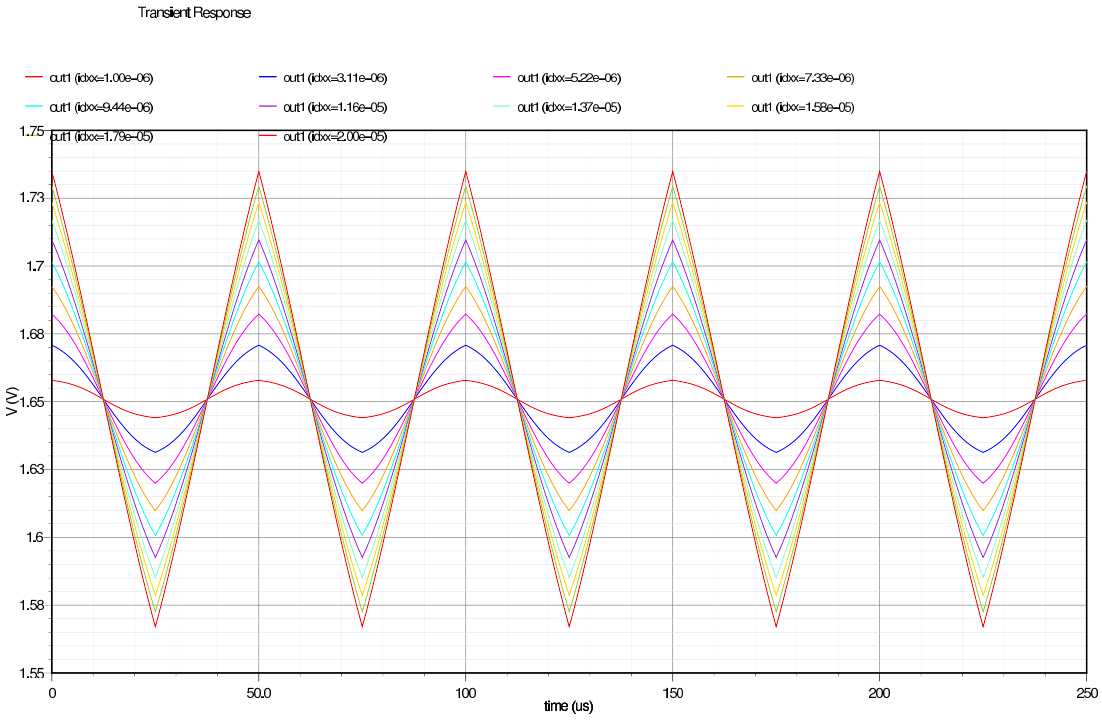
Then:



(a) Static characteristic of differential pair



(b) Dependence of THD against bias current



(c) Obtained waveforms with I_O variation

Figure 3.8: **Characteristics of Triangle to Sine Converter**

$$v_o = \frac{1}{2}K'\frac{W}{L}(v_{in1} - v_{in2})R\sqrt{\frac{4I_O}{K\frac{W}{L}} - (v_{in1} - v_{in2})^2} \tag{3.33}$$

3.3.3 Triangle to Sine Converter in weak inversion (TSC-WI)

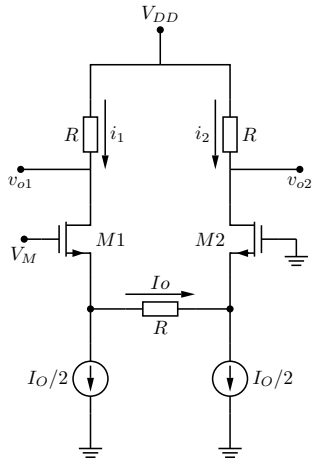


Figure 3.9: **Triangle to Sine Converter in Weak Inversion (TSC-WI)**

Another approach of the Triangle to Sine converter describes its operation when it's working at very low currents. The design exploits the fact that while in subthreshold region, the drain-to-source current I_{DS} depends exponentially on the gate to source voltage v_{GS}, the source to bulk voltage v_{SB}, and the drain to bulk voltage v_{DB}, [47], hence:

$$I_{DS} = I_o \frac{W}{L} e^{\kappa(v_{GB}/U_T)} \left(e^{(v_{SB}/U_T)} - e^{(v_{DB}/U_T)}\right) \tag{3.34}$$

Where the I_o is the subthreshold current-scaling parameter, κ the subthreshold exponential coefficient and $U_T = kT/q$ is the thermal voltage (29.5mV at room temperature). If the transistor is in saturation ($V_{DS} > 5U_T$) the I_{DS} is given by:

$$I_{DS} = I_o \frac{W}{L} e^{(\kappa(v_{GB} - v_{SB})/U_T)} \tag{3.35}$$

The differential output current written as a function of the differential input voltage is[48]:

$$I_{D1} - I_{D2} = I_O \tanh\left(\frac{\kappa(v_{in1} - v_{in2})}{2U_T}\right) \tag{3.36}$$

The output voltage will be given using Equation 3.32.

For a perfect sine wave output when triangle wave has a voltage peak of V_M we have [44]:

$$\frac{V_M}{U_T} = 1.57 \frac{I_0 R}{U_T} + 3.14 \tag{3.37}$$

We can see from Equation 3.30 and Equation 3.31 that the $I_{out}(v_{in})$ function of the differential pair in strong inversion has a quadratic characteristic while the differential pair in weak inversion presents an exponential characteristic, as shown in Equation 3.36. The difference of both characteristics can be translated in differences in the amount of distortion of the produced sine signal; further differences in both approaches appear also in the amount of dissipated power and occupation area.

The analog and digital oscillators were examined in order to choose the best option to conform the final VCO. The aspects taken into account to make the final selection were: achieved frequency, power consumption, performance working under worst power conditions, worst speed, achieved amplitude and on-chip area. The results will be reviewed in Chapter 5.

Chapter 4

Theoretical Background on Electrokinetic Phenomena

This chapter overviews the basic concepts of the electrokinetic theory.

4.1 Electrokinetic Forces

Electrokinetics is the family of different effects occurring in fluids containing particles when electric fields are applied. These forces scale down favorably and the use of microfabrication technologies allows the creation of large electric fields by using only few volts to polarize closely spaced electrodes. The main electrokinetic phenomena are electrophoresis, electro-osmosis and dielectrophoresis [8].

4.2 Movement of charged particles in an insulating fluid, submitted to an electric field

An isolated charged particle in a medium where no mobile charges exist and under the influence of an electric field $\vec{\mathbf{E}}$ experiments a force defined by:

$$\vec{\mathbf{F}} = q\vec{\mathbf{E}} \tag{4.1}$$

where q is the electric charge. In absence of brownian motion the particle obeys the following equation:

$$q\vec{\mathbf{E}} - \vec{\mathbf{F}_v} = m\frac{d\vec{\mathbf{V}}}{dt} \approx 0 \tag{4.2}$$

where $\mathbf{F}_v$ is the viscous friction force applied on the moving particle and is given by Stoke's law:

$$\vec{\mathbf{F}_v} = 6\pi r\eta\vec{\mathbf{V}} \tag{4.3}$$

where r is the radius of the particle, η is the viscosity of the fluid and $\vec{\mathbf{V}}$ is the velocity of the particle. From Equation 4.2 and Equation 4.3 we can deduce the migration velocity of the particle:

$$\vec{\mathbf{V}} \approx \frac{q\vec{\mathbf{E}}}{6\pi r\eta} \tag{4.4}$$

rewriting the equation we have:

$$\vec{\mathbf{V}} = \mu_e\vec{\mathbf{E}} \tag{4.5}$$

then, for an isolating charge the electrophoretic mobility equals:

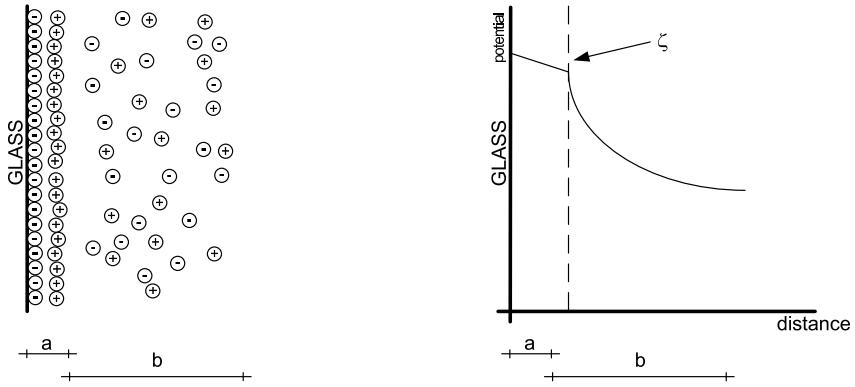
$$\mu_e = \frac{q}{6\pi r\eta} \tag{4.6}$$

4.3 The electrical double layer

When a dielectric is immersed in an electrolyte, a surface charge appears, for example a plate of glass immersed in an aqueous solution becomes negatively charged. The silane terminals Si-O-H localized on the glass surface lose hydrogen ions in the presence of the aqueous solution. The protonation leaves Si-O^- terminals on the surface causing the glass in contact with the aqueous solution to become negatively charged. The surface charges are equilibrated in the fluid by a double layer of counter-ions as shown in Figure 4.1.

The first layer is a molecular film of counter-ions fixed in the solid/liquid interface and is associated with the solid by an electrostatic interaction. This first layer is called the Stern-Layer. The second layer is diffused, not connected to the crystalline network of the solid . Its structure results from a statistical equilibrium between thermal agitation and electric forces. The thermal agitation tends to homogenize the charge distribution while the electric forces tend to displace charges of the same sign towards the surface. This diffused layer is called the Gouy-Chapmann layer. The double layer is the origin of electrostatic forces.

The potential at the shear plane between the fixed Stern layer and the diffuse Gouy-Chapmann layer is called the zeta potential. This zeta potential (ζ) is strongly dependent on the chemical composition of the wall, the chemical composition of the solution and the temperature.



(a) Fixed Layer (Stern Layer)

(b) Diffuse Layer

Figure 4.1: **Schematic diagram of the electrical double-layer.**

Model of dielectric and electrolyte. Solid line in Figure 4.1b) represents the potential.

4.4 Electro-osmosis

If an external voltage across the buffer solution is applied in axial direction, a bulk flow of the entire buffer is induced. As an electric field is applied, the charged carriers are displaced by electrophoretic forces towards the respective positive or negative electrodes. However since the negative charges from the deprotonated silanol groups are immobilized at the wall, a surplus of mobile positive charges in the solution exists and drag the entire liquid column towards the cathode. The resulting flow is called electro-osmotic flow (EOF). The electro-osmotic mobility can be defined as:

$$\mu_{eo} = \frac{\zeta_0 \epsilon}{4\pi\eta} \tag{4.7}$$

where ζ_0 is the zeta potential, ϵ the dielectric constant and η the viscosity. When an electric field $\mathbf{E}$ is applied, the electro-osmotic velocity is:

$$\vec{v_{eo}} = \mu_{eo}\vec{\mathbf{E}} \tag{4.8}$$

The main advantage of the electroosmotic flow is that it is possible to create a flow by filling a microchannnel with a buffer solution and applying a suitable voltage at the channel ends. Another advantage is the resulting flow profile, the electro-osmotic flow is generated closed to the wall and therefore produces a plug-like profile with uniform velocity distribution across the entire cross section of the channel, contrary to the hydrodynamic flows where a parabolic distribution is present.

A disadvantage of electro-osmotic flow is its strong dependence on the chemistry of the system. This dependence makes the flow very hard to control; every change in pH, dielectric constant, concentration etc. has an immediate effect on its magnitude.

On the other hand this strong dependency opens the door for many parameters to be exploited to control and manipulate the electro-osmotic flow.

4.5 Electrophoresis

Electrophoresis is the motion of ions, particles, bacteria, macromolecules or charged objects distributed in a solution in presence of an imposed electric field.

When a charged particle is immersed in an electrolyte it can no longer be considered as an isolated charge. The particle develops a local electric field and reorganizes mobile ions around itself establishing a double layer. Every charged molecule can be characterized by electrophoretic mobility (Equation 4.6). If the sample is submitted to an electric field we can thus obtain a separation effect on the charged components contained in the sample.

Most often electro-osmosis occurs as well and the final velocity is the vector sum of electrophoretic velocity v_{ep} and electro-osmotic velocity v_{eo}.

4.5.1 Capillary electrophoresis CE

If an electric field is imposed to ions confined in a capillary or in a microchannel, then an electroosmotic flow is induced displacing the whole fluid at the same velocity and separating charged particles that migrate at different velocities. This kind of separation is called capillary electrophoresis (CE) and is governed by the charge-to-mass ratio of the particles. The first to migrate through the channel are the small highly charged cations followed by larger less charged cations, then the uncharged molecules and finally the larger less charged anions.

CE is one of the most powerful methods for DNA sequencing, forensic analysis, PCR product analysis and restriction fragment sizing. This separation technique provides fast and high-resolution separations and it is used in clinical diagnostics for the detection of pathogens and diagnosis of human gene abnormalities. Capillary electrophoresis arrays to increase the speed and throughput of results have been fabricated using microfabrication methods from the electronics industry [9], [10]. Microchip electrophoresis is a rapidly growing field (refer to Agilent divide cited in Chapter 1), successful devices that perform miniaturized capillary electrophoresis are remarked in [49].

4.5.2 Gel Electrophoresis

When we have larger molecules the charge-to-mass ratio differences tend to become smaller. To separate those molecules (i.e. DNA fragments) the capillaries or channels are filled with a polymer gel that acts as a sieving matrix providing a molecular obstacle to bigger molecules. The polymerization of gels permits the adjust the pore size according to the dimension of the particle to be separated. The analyses move depending on

the charge to mass ratio, in the particular case of DNA, the charge to mass ratio is constant, the difference in DNA sizes make separation possible. Gel acts as a sieving matrix making DNA separations possible.

4.6 Dielectrophoresis

Dielectrophoresis (DEP) has been used widely to study, manipulate and separate micro/nano/bio particles. First defined by Pohl[50] this principle has proven its feasibility in a growing number of applications in the medical and biological fields, providing an increased precision of measurement and sensitivity in the detection of particles of different dielectric properties.

When a neutral particle is suspended in a medium and is submitted to a spatially non-uniform electric field, charges are induced at the interfaces resulting in electrical polarization along the direction of the electric field. The forces in either side of the particle will be different, and the net DEP force can induce translational movement of particles.

The time averaged DEP force on a particle resulting from an AC electric field $\vec{E}(\omega)$ is approximated as:

$$\vec{F}(t) = 2\pi\epsilon r^3 \mathbf{Re}(f_{CM})\nabla E^2_{RMS} + 2\pi\epsilon r^3 \mathbf{Im}(f_{CM})(E^2_{x0}\nabla\varphi x + E^2_{y0}\nabla\varphi y + E^2_{z0}\nabla\varphi z) \quad (4.9)$$

where E_{RMS} is the RMS value of the electric field strength E_{i0} and $\varphi' i(i = x, y, z)$ are the magnitude and phase of the field components in the principal axis; r represents the particle radius, f_{CM} the polarization factor (*Claussius-Mossotti factor*) Equation 4.10.

The real component is proportional to the force of the induced polarization in the particle and also to the spatial nonuniformity of the electric field ∇E^2_{RMS}. The real component causes particles to move toward strong or weak field regions according to the sign (positive or negative) of $\mathbf{Re}(f_{CM})$. The particles are reflected if they are more or less polarizable than their suspending medium in presence of the electric field. The imaginary part is a force proportional to the particle polarization and to the speed of the distribution of the electric field as reflected by the electric field phase gradients ($\nabla\varphi x$, $\nabla\varphi y$ and $\nabla\varphi z$). This force is responsible to move with or against the direction of the field travel depending on the sign positive or negative of $\mathbf{Im}(f_{CM})$. The two DEP force components ac independently and can be exploited alone or in combination.

The dielectric properties of a particle reflect aspects of its composition and structure and can be addressed making a change in the field frequency when using DEP. It is possible to manage different forces on different particle types within a mixture; particles can be concentrated to a focal point using negative DEP or trapped using positive DEP.

The element that determines the DEP responses of a particles is the Claussius-Mossotti factor expressed as:

$$f_{CM} = (\epsilon_p^*, \epsilon_m^*, \omega) = \frac{\epsilon_p^*(\omega) - \epsilon_m^*(\omega)}{\epsilon_p^* + 2(\omega)\epsilon_m^*(\omega)} \tag{4.10}$$

The ϵ_p^* and ϵ_m^* factors, represent the complex permittivities of the particle and its suspending medium; the subscripts p and m mean particles and medium respectively, σ is the conductivity; the electric polarization of a particle is not instantaneous, then, the complex permittivities of the particle and medium depend on the frequency of the electric field $f = \omega/2\pi$, hence, any DEP effect can be taken away by making a change in the frequency.

$$\epsilon^* = \epsilon - j\sigma/\omega \tag{4.11}$$

Many biological entities are encapsulated by protein coats or membranes comprising aqueous electrolytes that support life activities; these aqueous phases tend to move under the influence of an electric field. In the frequency range of 5kHz-200MHz the dielectric properties of cells are dominated by polarization at membrane interfaces.

If the conductivity in the electrolyte outside a cell differs from that within, the characteristics for polarizing the inside and outside surfaces of the membrane will differ, it is the said that the cell has acquire a dielectric signature enabling one type of cells to be discriminated from another.

The different cell types can be seen as the dielectrophoretic properties of molecules, inert particles, entities with a single membrane and more complex cells that can be modeled by equivalent dielectric shell models (Figure 4.2) according to [51]. Each spectrum shows that the determinant of the particle AC electrokinetic response is the frequency of the applied electric field. The morphological differences of cells give them distinct dielectric phenotypes making DEP an attractive method for cell manipulation and discrimination.

The frequency dependency results from time required for the electrical polarization to build up in various structures of particle (look at the different fingerprints of cellular structures with encapsulating membranes and structures that lack membrane encapsulation). Note that at certain frequencies, the DEP force transverses the zero level, they are called crossover frequencies and define the frequency at which DEP trapping ceases and repulsion begins as seen in Figure 4.3. Several DEP crossover frequencies for different cell types have been reported in [51], [52], [53] .

The complex permittivities of the cell membrane has four control parameters:

Membrane thickness: Can change 10% depending on the lipid composition

Effective area: As determined by surface morphology including folding, ruffling and microvilly; it can vary over a 20-fold range for different cell types.

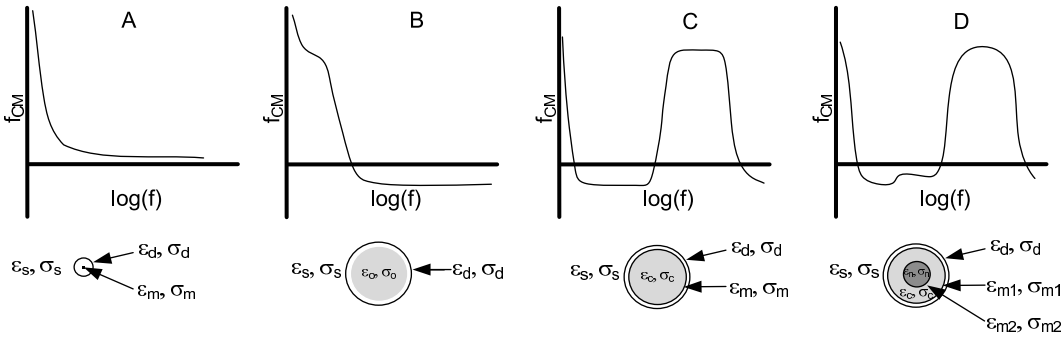


Figure 4.2: **Shell models for simulated dielectrophoretic properties**

a) Point particles; b) solid particles; c) particles with a single compartment surrounded by a thin envelope; d) particles with two concentric compartments surrounded by thin envelopes (from [52])

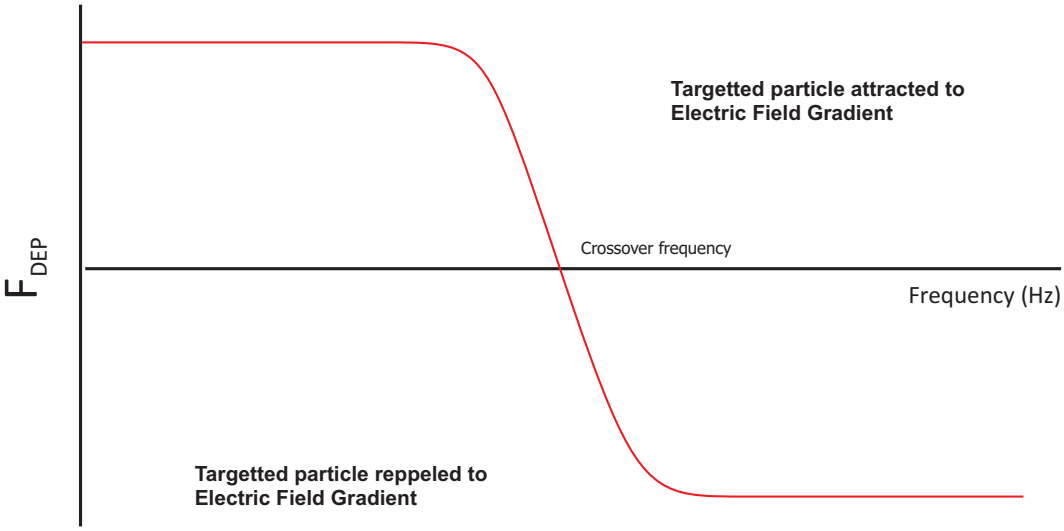


Figure 4.3: **Behavior of a particle under DEP force [2]**

Dielectric constant: remain constant within a few percent area even for widely range of protein/lipid ratios. The membrane's capacitance of a smooth biological membrane ranges from 0.8µF/cm^2 for smooth cells up to 15µF/cm^2 in the case of highly convoluted hepatocyte membranes, most mammalian cells have membranes from 1.2 to 4µF/cm^2.

Electrical conductivity: The plasma membrane conductivity of healthy cells is usually negligible, though this is not true for diseased cells.

Some advantages of DEP are the followings[54]

- It is possible to move uncharged particles without a significant movement of the fluid
- Does not require of expensive equipment or high cost optics to perform the separation
- There is no need of a clear line of sight between the laser and the particle as in optical tweezers
- Can be done in small, inexpensive micro-electrode structures
- The objects manipulated with dielectrophoresis doesn't need to be optical transparent

DEP presents a very good separation efficiency when particle compositions, cell sizes or morphologies are clearly distinct and it's used in:

- Beneficiation of ores
- Dewatering of aqueous dispersions of clays
- Separation of bacteria from mammalian cells
- Separation of live cells from dead/ debris cells

When DEP is going to be used in the continuous separation of living cells, an affinity test must be carried out. A very important parameter is the conductivity medium, a very high conductivity medium can lead to heating effects that can cause damage to cells and also cause additional fluid flow due to electro dynamic effects that can disrupt dielectrophoretic collection [15].

The DEP can employ AC or DC electric fields, the fields can be produced either by microelectrode arrays or by using insulating structures.

4.6.1 Electrode-based DEP

The advances in microfabrication have made possible the construction of micro and nano electrode structures capable to generating very high electric fields needed for DEP. a variety of electrode configurations have been studied, testing their effectiveness in the manipulation of particles, however, many approaches have been discarded because of manufacturing impracticalities.

With Electrode-based DEP is possible to:

- perform a large number of experiments on individual cells, without the use of markers and labels

- implement different analytical protocols by changing the excitation to each individual electrodes
- carry out accurate control of positioning/capturing cells/particles

The most important effects evoked with Electrode-based DEP are:

Levitation The cells/particles are levitated above the electrode plane to an equilibrium position. The height depends on the magnitude of applied voltage.

Linear motion The cells/particles can be moved in the direction opposite to the traveling electric potential wave, and can be reversed with an inversion in the phase sequence of the applied voltage signals.

Trapping at certain frequencies is possible to trap cells/particles at the edges of electrode strips.

Transitional effects In a range of frequencies a cell/particle can change its behavior from linear motion to entrapment and in certain cases rotation.

Early studies of cell dielectrophoretic responses employed electrode structures made of thin electrical wires, included cone-plate electrodes, pin-plate electrodes and four pole electrode, but advances in microfabrication processes motivated the exploration of new electrode geometries. The most important geometries in Electrode-based DEP are:

Planar electrodes. Exploit batch fabrication and MEMS technologies to yield reliable and cost effective particle manipulators. Traditionally the microfabrication techniques leads to have planar electrodes; although planar electrodes have proven to be successful in the separation of various particles they have a big drawback: the dielectrophoretic force (proportional to ∇E^2) rapidly decays as the distance from the planar arrays increases, preventing the DEP techniques from its use in high volume applications[55].

Parallel electrodes. This kind of electrodes are capable of exerting levitation and entrapment. The electrodes are parallel strips fabricated mainly composed of gold.

Interdigitated electrodes. The influence of different signal excitation over interdigitated electrodes produce cell aggregation patterns in addition to levitation and concentration.

Polynomial electrodes. Depending on the amplitudes and frequencies, it is possible to elicit circular motions along the edges of the electrodes and also it is possible to notice some transitional effects.

3D microstructures and *micropyramid quadrupole structures* have shown a remarkable capability of positioning and registration of cell trapping [21], [56]. With 3D microstructures it is possible to trap cells and keep them stationary for long periods without applying DEP AC power. The micropyramid structures exhibit higher trapping forces than planar electrodes.

The appropriate choice of the electrode designs must consider aspects like free circulation of cells/particles, best concentration, and good evacuation, and mass fabrication feasibility.

4.6.2 iDEP

An alternative to electrode-based DEP is iDEP (Insulator-based Dielectrophoresis). In iDEP devices, an array of spatially insulating structures produce electric field non-uniformities that are created by energized remote electrodes. Only two electrodes are necessary in iDEP.

Some advantages of iDEP [57] are:

- Host substrate can be any insulating and impermeable material (glass, silica, plastic, ceramic)
- Ease of replication through injection molding and hot embossing

The iDEP systems can be made purely from insulating materials (e.g. plastics) which can be replicated for high-volume applications, those structures produce no electrolytic effect and can be contoured to be gentle on cells [58].

In order to perform the trapping its necessary to have a DC electric field and the two electrodes. The insulating posts create electric field intensity gradients. While micro electrode array-based DEP face performance-limiting issues due to electrode fouling, iDEP can be less sensitive to this problem.

Lapizco-Encinas et al. [59], demonstrate the application of iDEP in the separation of live bacteria using only DC fields. Their proposed microchip was fabricated using standard photolithography, wet etch and bonding techniques. The microchip contains wight independent micro-channels, straddled each by two liquid reservoirs. There is an insulating post area in the middle of the micro-channel, the posts transverse the entire depth of the micro-channel.

Cummings and Sigh [60], performed dielectrophoretic manipulation and trapping of 200nm fluorescent latex spheres applying a DC electric field of 80V/mm to a microchip containing an array of diamond shapes posts. McGraw et al. [61], demonstrated the effectiveness of polymeric based devices and proposed a methodology to determine the concentration factors obtained in these devices.

Since iDEP uses only a couple of electrodes, the control over the complete system is traditionally an On-Off scheme, with practically no electronics are involved in the process, centering the attention in the micro-fabrication process. However, a novel method called contactless-DEP requires the use of more sophisticated electronics in the detection of living cancer cells [62].

Chapter 5

Comparison of Oscillator Approaches

We have analyzed several projects that perform electrokinetic tasks aiming to achieve the concept of a Lab-on-a-Chip. In the accomplishment of such tasks most of the reviewed devices rely on signals from external waveform generators (except those presented by Enteshari et al. [16] and Wayne C. et al. [18]).

This chapter evaluates two digital and two analog prototypes proposed as the oscillation source to implement the VCO[1] that will be the core of our solution model.

5.1 Solution model

With the newer advances in separation and isolation of particles, new challenges and needs arise constantly. This is the case of dielectric characterization. A common problem found in laboratory is that sometimes the dielectric properties of the interest particles are unknown or their behavior is not in agreement with experimental results. A better knowledge of those properties will help in the prediction of electrokinetic phenomena reducing the time needed to perform an experiment.

A similar situation exist in separation technology. Frequently a sample is composed of particles with similar dielectric properties where the frequency window for separation is very small, making difficult the separation process.

The multi-channel sinusoidal generator aims to become a central part in a LOC enabling multiprocessing tasks. This way permits a number of ports to perform separation, another group to make filtering and several ports to make characterization (Figure 5.1).

[1] Voltage Controlled Oscillator

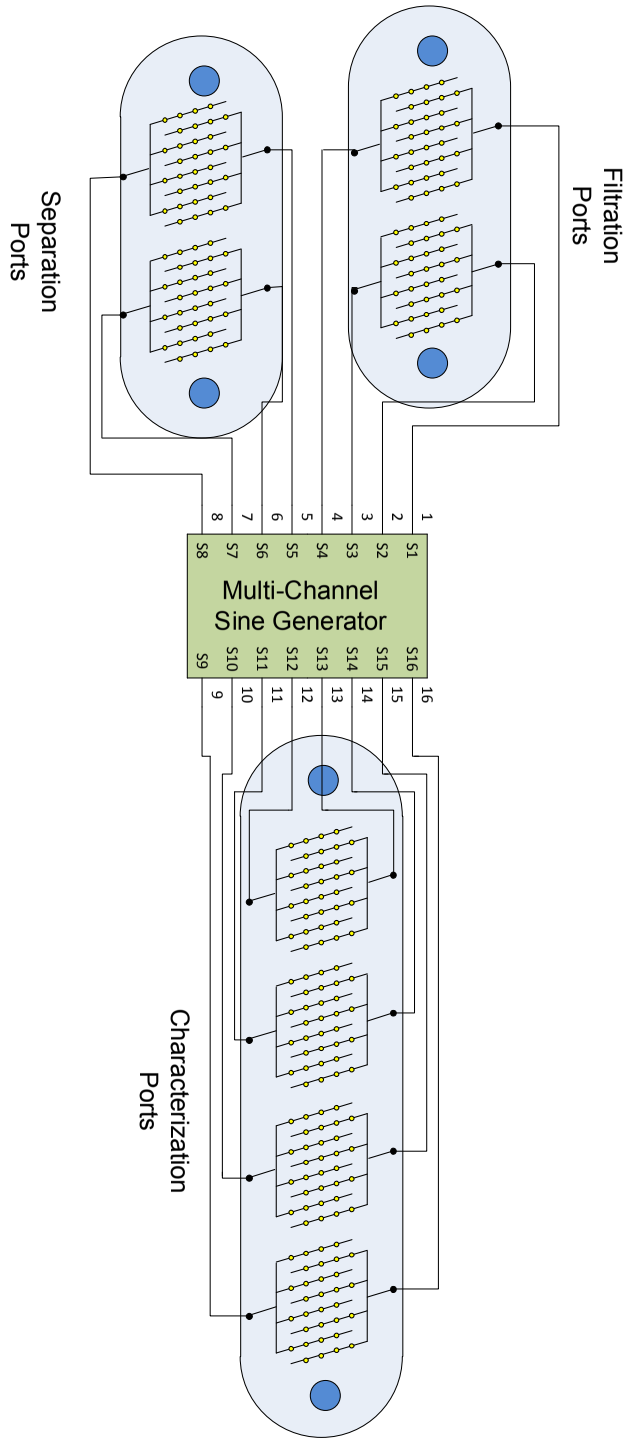


Figure 5.1: **Parallel processing of electrokinetic tasks**

The following characteristics and specifications are required for a stimulator of electrokinetic devices:

- **Multiple output ports.** It is necessary to have multiple signals generators working independently with full control of voltage, frequency and THD, so that we may count of several outputs devoted to perform different electrokinetic tasks. Our first proposed prototype will have 16 independent outputs.

- **Voltage range.** Most of the applications use voltages from mV to 100V; a range of 0V to $10V_{PP}$ is suitable to exert DEP forces on a vast number of biological cells [18]. The devices must allows the independent control of the voltage level at the output for each port.

- **Frequency range.** Our device must offer a wide frequency range in order to observe the DEP effects as levitation, rotation and conveyance, but also to perform separations and conduct experiments on a broad number of particles/cells [19], [63]. Typically a frequency range from 20kHz to 20MHz is necessary for our application. Also, the frequency at each independent output must be controllable. Figure 5.2 shows the the proposed multi-channel system. The limiting factor of frequency is the speed requirements of slew rate in the analog domain and clock speed in the digital domain.

- **Size.** Since our device aims to be a small, cheap, portable, small size platform, to give the option of carry out analysis out of lab in a simple manner, the size is a very important aspect to have in mind, also the fact of having a small device will keep low the fabrication costs.

- **Power.** It is intended to include our device in a portable appliance, the power consumption must be kept low if we want that our device work with energy supplied from batteries, an excellent reference point is that of [18] that presents a device consuming 1.87W. An integrated system will contribute to lower the global power consumption since all the modules can be included in a single integrated circuit.

- **Cheap.** In order to represent an option to be included in massive projects our design must have low fabrication costs, our device was implemented using a standard CMOS technology (AMS 0.35µm) representing the better option in cost and functionality

The digital and analog alternatives were tested to select the best oscillator that integrates the multi-channel generator.

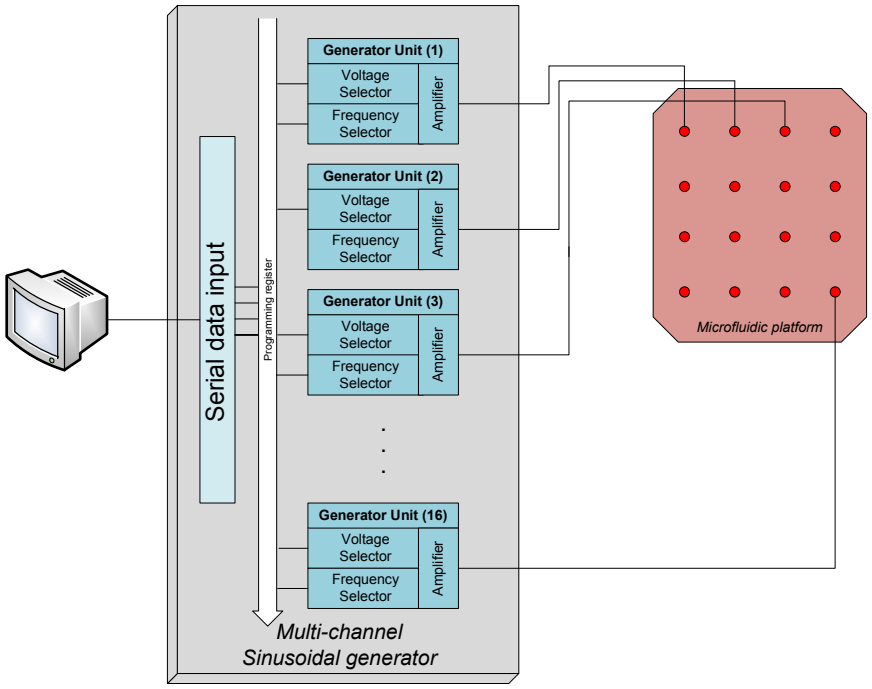


Figure 5.2: **Proposed multi-channel oscillator system**

5.2 Digital solution evaluation

The analysis of different digital solutions was made using three strategies (Figure 5.3):

System level evaluation. Since the oscillator's behavior can be modeled with VHDL it is possible to compile it and then run a simulation that show the waveform characteristics such as amplitude, frequency, linearity, and their behavior concerning the THD. The obtained data is saved to text files and analyzed using MATLAB. The clock signal for all the run-out tests was set at 40ns (25MHz), and was chose only to have a numeric reference, the maximum frequency was given as a result of the synthesis process.

IC level evaluation. One of the main objectives of this work is to implement the oscillator on an integrated circuit. The physical synthesis represents a key piece in the whole design process yielding to an estimation in the total area occupied by the oscillator and it allows additional simulation taking into account routing, timing and parasitic conditions. All those parameters serve as reference comparison versus the analog approach.

In order to achieve the physical synthesis, the VHDL code is compiled and synthesized in LeonardoSpectrum[2] [64] from AMS CMOS 0.35µm standard cell library.

[2]Both tools LeonardoSpectrum and ICStation were used in the preliminary analysis, for the synthesis

The partial product at this level is a verilog file, this HDL code is read in ICStation [65] to make the system's layout. The final product of this whole process would be a GDSII file (after parasitic extraction and verification) necessary for the IC fabrication. It is worth to mention that this analysis is fully dependent of the standard technology used in the implementation. A different technology will give as results different limits in clock frequency and on-chip areas.

Fast prototyping evaluation. A very important part of the analysis is the implementation over a developer platform. The oscillator was implemented using a Xilinx Spartan 3 FPGA aiming to obtain performance measurements such as the number of used gates and maximum clock delay. Programming the VHDL code in a developer board allows the visualization of the physical characteristics of the obtained waveforms. The selected board was the Xilinx Spartan-3 Starter Kit that includes a 3s200ft256-5 FPGA.

It was necessary to build a data acquisition board in order to convert the digital data, this board was built in the laboratories of the Electric and Computer Department at ITESM. The data acquisition board includes a Digital to Analog Converter DAC and two operational amplifiers. The selected DAC is the Burr Brown's DAC902 [66] that is a 12-bits 165MSPS converter used in medical/ultrasound applications, high speed instrumentation, video and digital TV. The chosen operational amplifier was the AD811 [67], this high speed OpAmp features a 140 MHz bandwidth, 2500 V/µs slew rate and used in medical, HDTV systems, video line drivers etc. (see Figure 5.4).

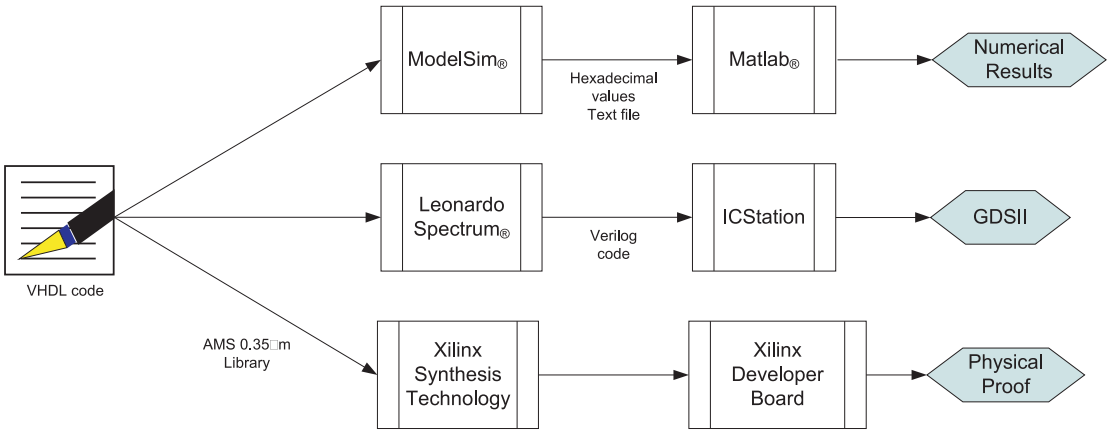


Figure 5.3: **Proposed strategy for the digital approach**

Depending parameters such as maximum clock frequency, number of used gates, and on-chip area were evaluated and the results are shown later in this chapter.

of the digital module incorporated to the integrated circuit, Encounter RTL Compiler and Simulation Analysis Environment (Simvision) of Cadence were used.

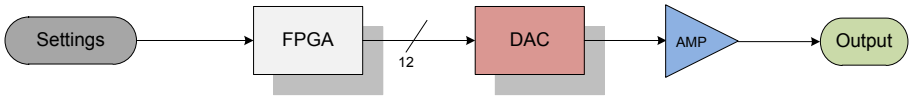


Figure 5.4: **Block diagram of the data acquisition board**

5.2.1 Analysis of the Delta Dirac Unstable Oscillator (DDUO)

The original algorithm of the oscillator uses two multipliers for an equal number of outputs [30]. However we only are interested in one output of the oscillator of Figure 3.1 is modified to a system depicted in Figure 5.5.

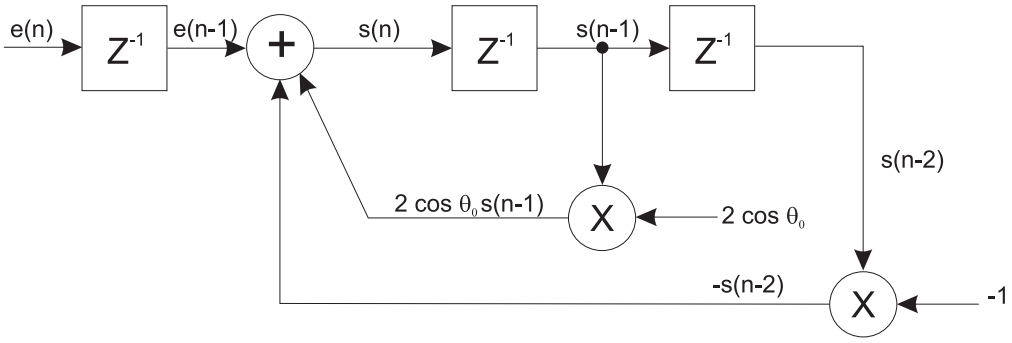


Figure 5.5: **Block diagram of the DDUO**

The DDUO can be defined with the following difference equation:

$$s(n) = e(n-1) + 2cos(\theta_0)s(n-1) - s(n-2)$$

Note that an initial input is defined $e(n)$ in order to start up the oscillator. According to the mathematical demonstration, we should see that the frequency control variable depends on $\cos\theta$, defining $K = 2\cos\theta$ we find its sensitivity (Figure 5.6).

Looking at Table 5.1 we may note that the maximum frequency of the oscillator at 25MHz is 6.25MHz. Therefore, for a sinusoid frequency of 20MHz a clock of at least 80MHz is necessary. Also the control of frequency presents a quasi-linear performance until $K = 0.6$ approximately. From this value the frequency decays rapidly as K approaches to 1.

In the first analysis of the *Unstable Delta Dirac Oscillator* all the used variables were declared to have 12 bits causing the synthesis of a 24 bits multiplier. Figure 5.7 illustrates that the oscillator performs better at low frequencies. Using Equation 3.17, THD measurements were obtained and plotted in Figure 5.8. This shows that at frequencies below 4MHz the THD decreases below 4%.

Other implementation based on 8-bit registers is proposed to save on-chip space.

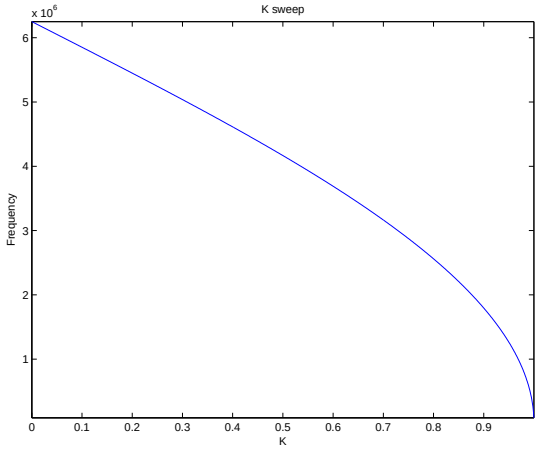
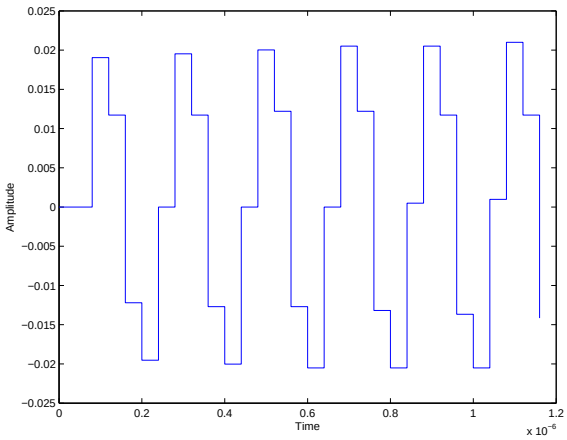


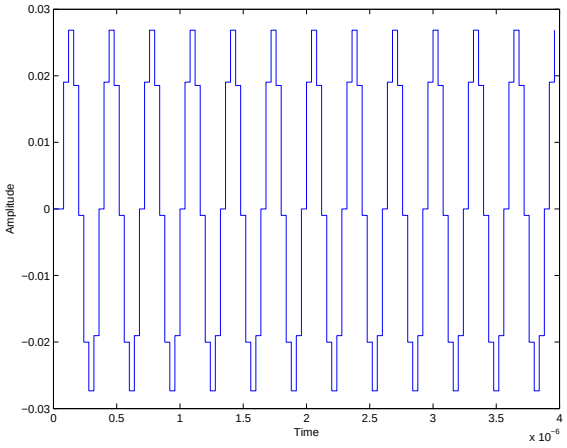
Figure 5.6: **K values sweep**

Table 5.1: **Different K-values and their frequencies, 12-bits system**

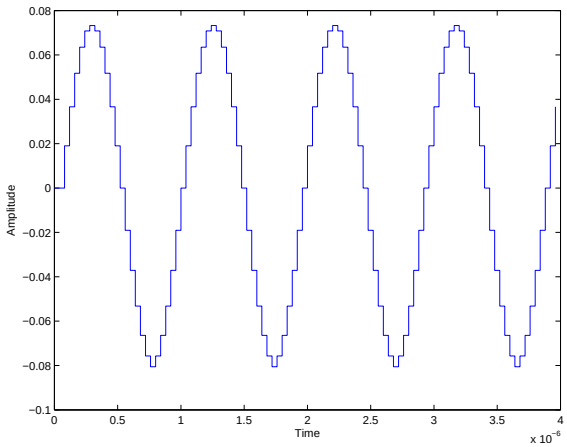
Frequency	θ	N	K HEX
6250000	1.570796327	4	0
5000000	1.256637061	5	279
3571428	0.897597901	7	4FD
3125000	0.785398163	8	5A8
2500000	0.628318531	10	679
1000000	0.251327412	25	7C0
500000	0.125663706	50	7F0
250000	0.062831853	100	7FC
195312	0.049087385	128	7FE



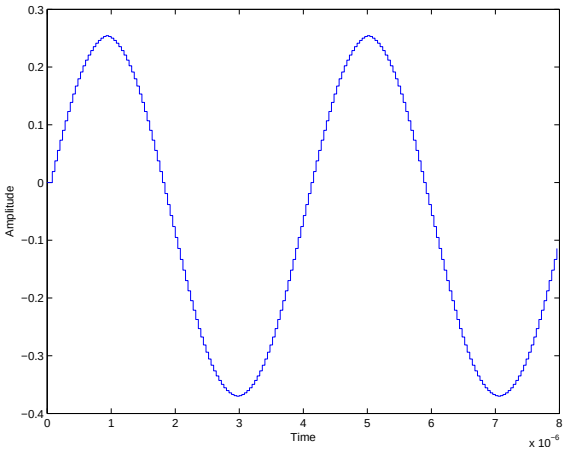
(a) Signal at 5MHz



(b) Signal at 3.125MHz



(c) Signal at 500kHz



(d) Signal at 250kHz

Figure 5.7: **12-bit system oscillator output at different frequencies**

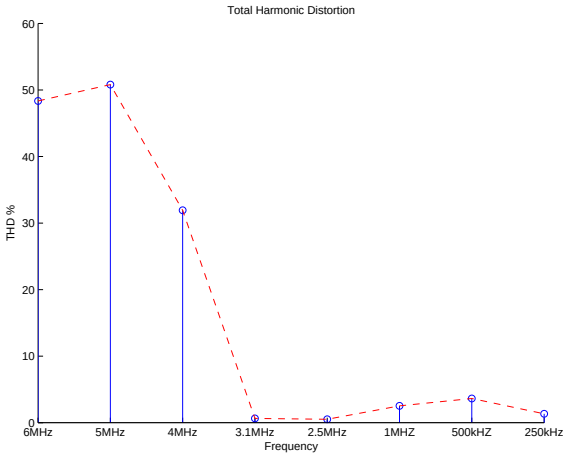


Figure 5.8: **THD measurements for a system of 12 bits**

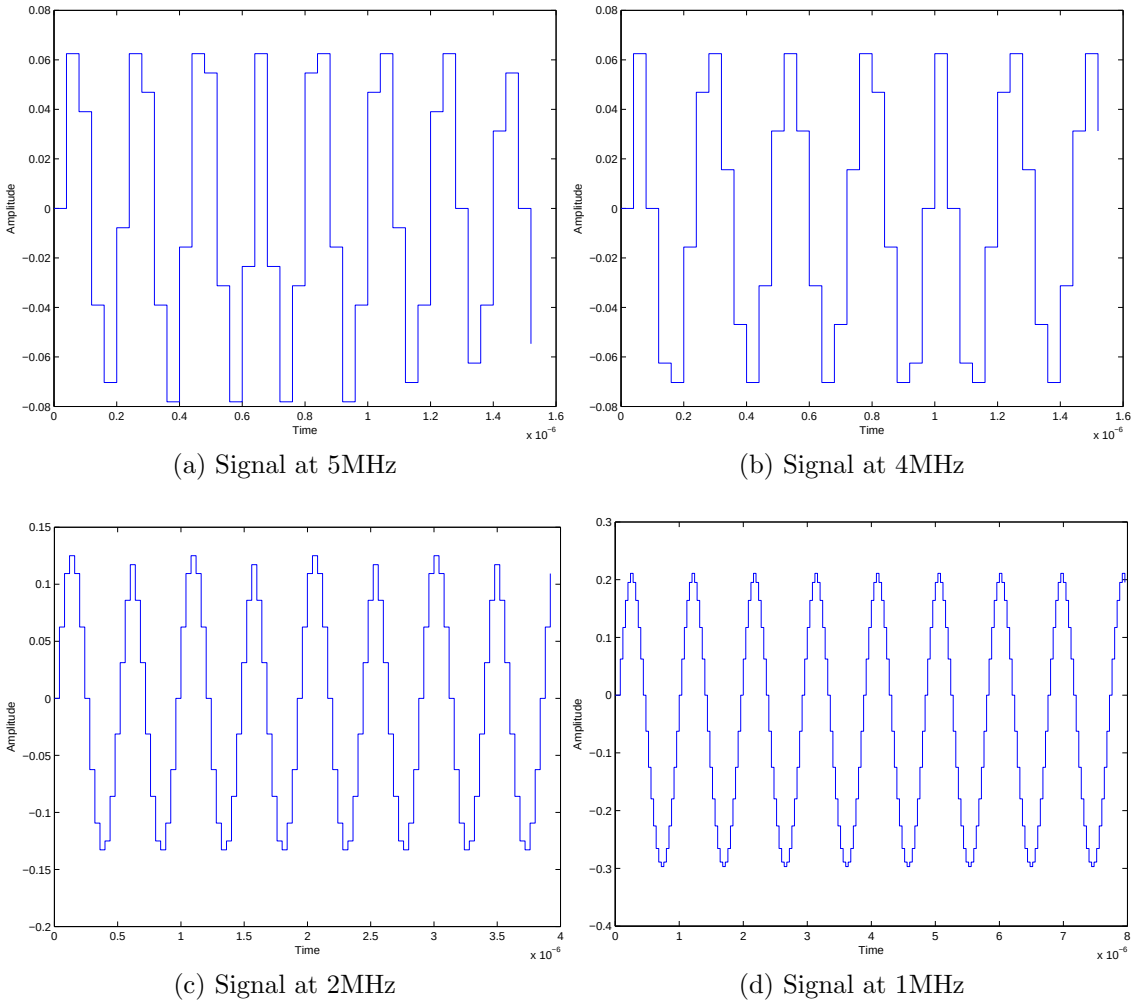
The obtained waveforms and THD are illustrated in Figure 5.9 and Figure 5.10 respectively.

5.2.1.1 Remarks on the DDUO analysis

Table 5.3: **Implementation and physical synthesis, Unstable Delta Dirac Algorithm**

	12-bit registers	**8-bit registers**
Number of Slices:	31	29
Number of Slice Flip Flops:	40	39
Number of 4 input LUTs:	47	41
Number of Ios:	24	19
Number of bonded IOBs:	16	11
Number of MULT18X18s:	2	1
Number of GCLKs:	3	2
Maximum frequency:	98.991MHz	110.832MHz
Minimum period:	10.102ns	9.023ns
Minimum input arrival time before clock:	4.335ns	4.355ns
Maximum output required time after clock:	15.580ns	6.306ns
Physical synthesis		
Number of used gates:	65884	36928
Total area:	295μm $\times$ 295μm	173μm $\times$ 173μm
Max. clock frequency:	50.1MHz	72.1MHz

1. Table 5.3 shows the characteristics of the implemented algorithms including amount of gates, area, and maximum clock frequency and others. The presented systems exhibits scalability, if the clock speed can be increased the THD measurements can be displaced to lower values. The increment in the clock speed will depend directly on the architecture synthesis. Still this sinusoid generator is capable to cover a great range of frequencies, lower frequencies could be achieved by providing slow clock signals extending the number of decades that the oscillator can sweep.



(a) Signal at 5MHz

(b) Signal at 4MHz

(c) Signal at 2MHz

(d) Signal at 1MHz

Figure 5.9: **8-bit oscillator outputs at different frequencies**

2. The signals obtained for high frequencies exhibit a great amount of distortion due to an asynchronic sampling, the zero order hold causes the sample to remain in the same level until the arrive of the next value. Remember that the approximated values have sometimes large error rates resulting in high THD numbers.

3. In the case of the 8-bit system, a bad selection of the $e(n)$ parameter can lead to instability, specially for frequencies below of 700kHz, the poles of the system may not be in the unitary circle due to rounding and/or saturation problems. The 12-bit system can deal with this problematic at the cost of a greater occupied area.

4. For several frequencies (multiples of the main clock frequency) the exhibited low THD values show that it's possible the implementation without an output filter saving space and power consumption, this condition is exclusive to those frequencies.

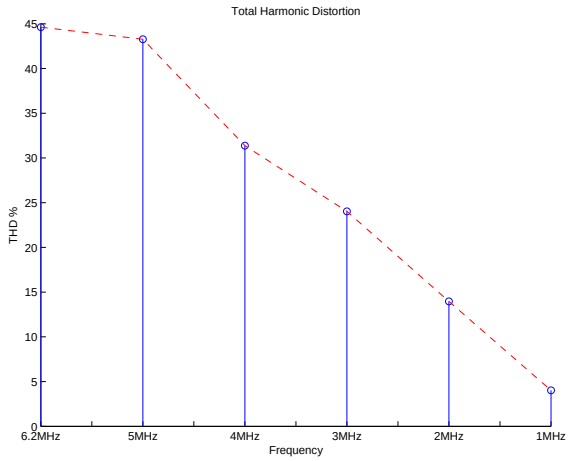


Figure 5.10: **THD measurements for a system of 8 bits**

Table 5.2: **Different K-values and their frequencies, 8-bits system**

Frequency	θ	**N**	**K HEX**
6000000	1.507964474	4.167	8
5000000	1.256637061	5	28
4000000	1.005309649	6.25	45
3000000	0.753982237	8.333	5D
2000000	0.502654825	12.5	70
1000000	0.251327412	25	7C
500000	0.125663706	50	7F
250000	0.062831853	100	80

5. We can see from the summary that the device utilization does not represent a major obstacle for its implementation over the FPGA, in fact, it is possible to include more than one oscillator in the same system. The timing summary indicates that the oscillator could reach output signals of 20MHz, bigger efforts in the VHDL stage (proposing faster architectures) can be made in order to get a better timing response whenever a higher frequency is required.

6. The results of the Xilinx synthesis show that there is no significative difference between the 12 and 8 bits system in the number of used slices to implement the algorithms, not even the clock speed represents a major drawback for the systems; the existent problems with the instability of the 8-bit system and the number of available output pins would make the difference.

7. As we can see in Figure 5.7 and Figure 5.9 the amplitude of the output signal varies as frequency changes representing a big drawback for the algorithm.

8. Even with 12-bit registers we can see that the systems based on the Unstable Delta Dirac algorithm need to include a filter stage, to deal with the high THD numbers at higher frequencies, the integration of that component and its performance were not evaluated in this study (performance, improvement in the THD, surface and consummation).

5.2.2 Analysis of the Direct Digital Frequency Synthesis algorithm

In order to change the frequency, a 12-bits word must be fed at the adder's input. The last output is then added to the current input at the leading edge of the clock and the result is sent to a 17 bit signal where the 5 most significative bits address to 1 of 32 available positions in the ROM. The ROM stores 32 8-bits values of a sine wave (Figure 5.11).

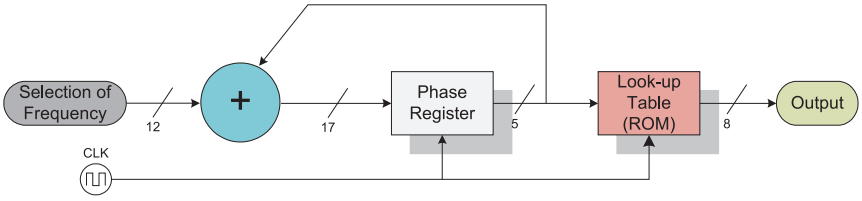


Figure 5.11: **DDFS Block Diagram**

Note that if the ROM size is big, the THD will decrease because there is a large amount of points describing the sinusoidal waveform but as a consequence the f_{OUT} will decrease ($f_{MAX} = f_{CLK}/RS$) and the on-chip area will increase.

On the other side, if the ROM size is small, the THD will increase due to a low number of points composing the sine, with less points the on-chip area will decrease. The choice of the ROM size is a big concern in the implementation of the DDFS algorithm. In principle the size can be set keeping the amount of THD low (refer to Equation 3.15 and Equation 3.16) but if the size of the register represent a constraint, different techniques (as those described in [22] and [1]) can be used.

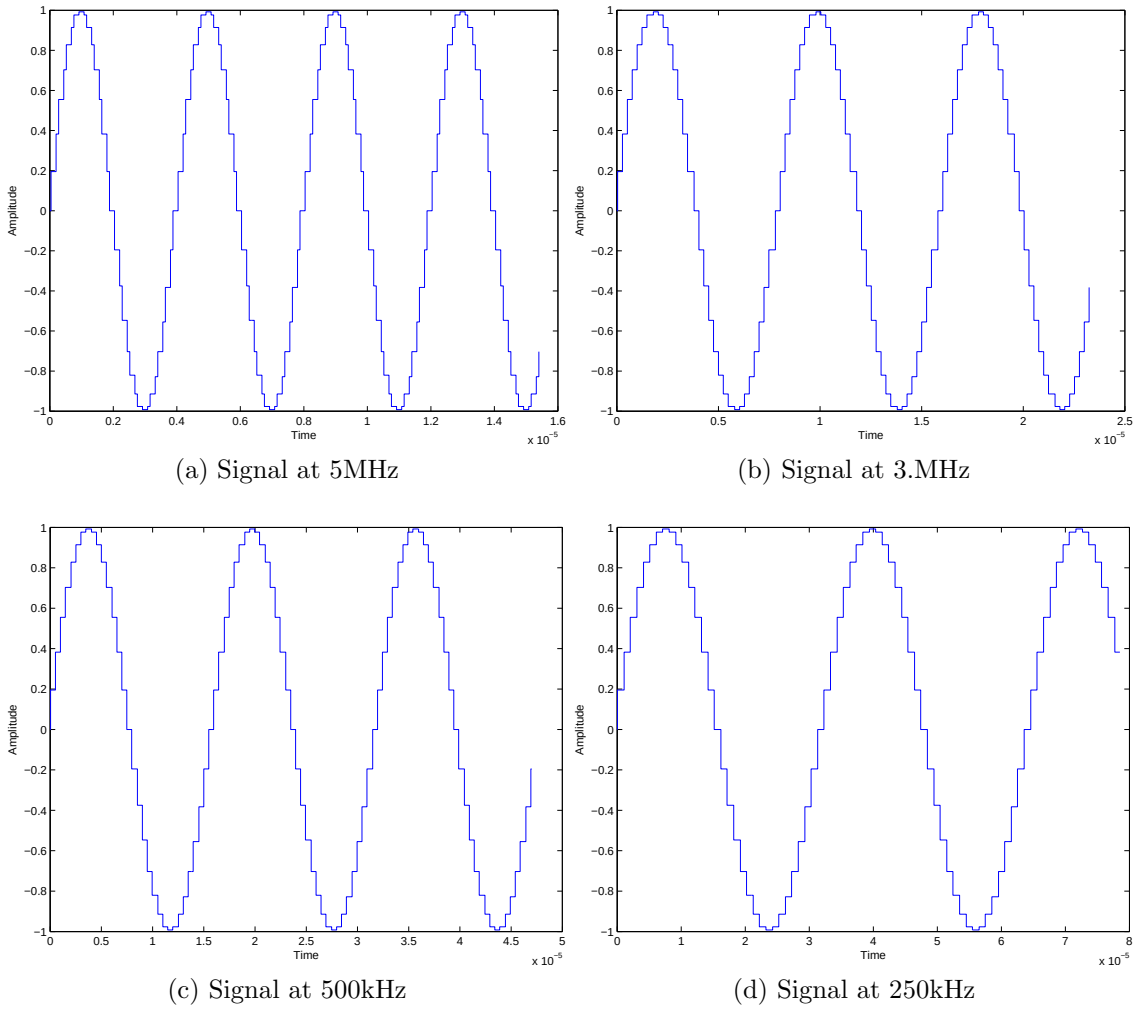
The relationship between the tuning word and the frequency output for such system will be:

$$f_{OUT} = \frac{M_X \cdot f_{CLOCK}}{LM_X \cdot RS} \tag{5.1}$$

Where M_X is the 12-bit input tuning word, taking values from 000_{H} to $\mathrm{FFF}_{\mathrm{H}}$, f_{CLOCK} the main clock frequency (50MHz). The LM_X is the length of the tuning word (2^{12}) and RS the ROM size (32).

Now, we proceed the simulation using ModelSim, the results for selected frequencies are depicted in Figure 5.12 and the calculated THD for the DDFS waveforms in Figure 5.13. See that THD was located in ranges from 5.9% to 6.5%, as a result of the digitalization of 32 values for the sine waveform. Those numbers can be lowered as more poin integrate the output sine signal or with the aid of a filtration stage.

When the algorithm was implemented using the Xilinx and physical synthesis tools we obtain the results shown in Table 5.4 and the resultant waveforms of this algorithm



(a) Signal at 5MHz

(b) Signal at 3.MHz

(c) Signal at 500kHz

(d) Signal at 250kHz

Figure 5.12: **Obtained signals with DDFS**

obtained with an oscilloscope in Figure 5.14.

5.2.2.1 Remarks on the DDFS analysis

1. Evidently the DDFS offers the best option among the analyzed to generate a sinusoidal waveform by digital means, with just 8 bits for the output signal it's capable to give low THD, excellent resolution and wide selection range.

2. In order to reduce the ROM size further efforts (like the strategy proposed in [22]) must be done in order to achieve low numbers n terms of device utilization and hence lower implementation area for an IC.

3. In a FPGA implementation the number of oscillators will be limited for the amount of available output pins.

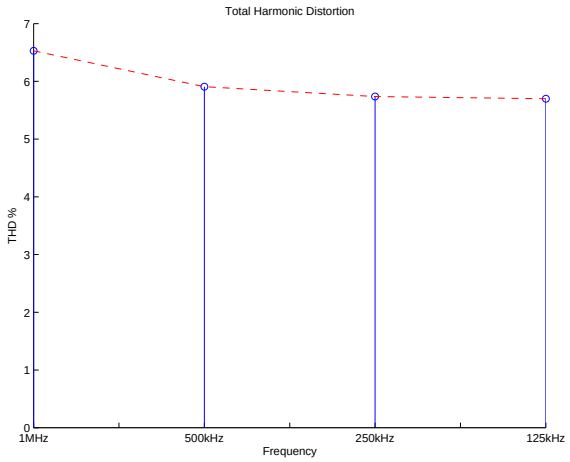
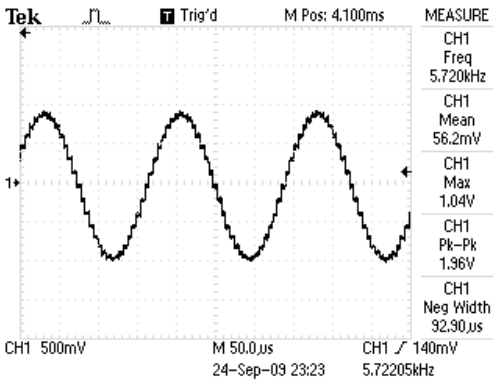


Figure 5.13: **THD for DDFS waveforms**

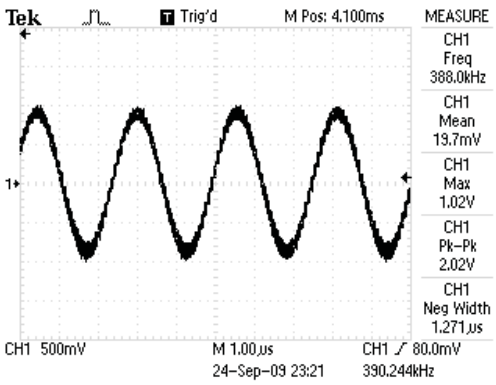
Table 5.4: **Implementation and physical synthesis for the DDS Algorithm**

Number of Slices:	18
Number of Slice Flip Flops:	17
Number of 4 input LUTs:	34
Number of Ios:	24
Number of bonded IOBs:	24
Number of GCLKs:	1
Maximum frequency:	249.044MHz
Minimum period:	4.015ns
Minimum input arrival time before clock:	4.242ns
Maximum output required time after clock:	8.313ns
Physical synthesis	
Number of used gates:	19075
Total area:	127μm $\times$ 127μm
Max. clock frequency:	124 MHz

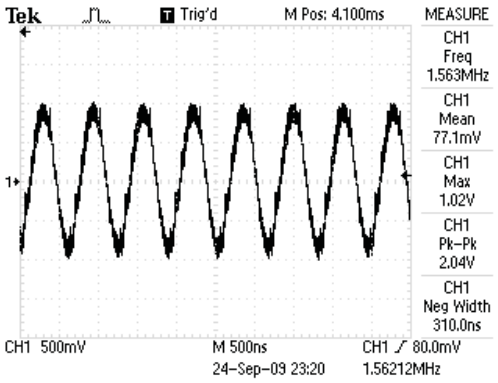
4. In an on-chip implementation the number of oscillators will be limited by the amount of area required for each oscillator, besides, each oscillator needs a fast Digital to Analog converter and conditioning circuitry, these facts discarded all possibility to implement a digital algorithm. The DDFS algorithm was the best option in occupied space and speed among the digital algorithms.



(a) Frequency=5.7kHz



(b) Frequency=388kHz



(c) Frequency=1.5MHz

Figure 5.14: **Oscilloscope waveforms**

5.3 Analog Solutions Evaluation

A review of CMOS circuits and resulting waveforms are presented now. The solutions to achieve the sinusoid waveform were designed according to the proposed specifications for the multi-oscillator:

- Frequency range 20kHz - 20MHz.
- A total area for the capacitor of 110µm×110µm which corresponds approximately to a total capacitance of 10pF using the AMS 0.35µm technology.

5.3.1 Selection criteria

Several tests were carried out to compare and select the best alternative. The following characteristics were evaluated in detail:

Frequency. Obviously all the oscillators must fulfill the frequency range. The lower frequency specification was specially difficult to accomplish due to its requirement of large capacitances and very low currents

Power. All the designs must operate with low power dissipation.

Corner Analysis. As a part of the Hit-Kit of austriamicrosystems [68], the corner analysis considers variations of range in currents, voltages and environment variables to perform a simulation having in mind the *Design For Manufacturing* (DFM) concept. The corners defined for this analysis where:

tm. Typical model, functioning at room temperature. We are going to see the information in column graphics, the results corresponding to the typical model (tm) are shown in the column marked as **corner1**.

tmmins. Typical model minimum supply voltage, shown in graphics as **corner2**.

tmmaxs. Typical model maximum supply voltage, depicted as **corner3**.

wp. Worst power maximum temperature, shown as **corner4**.

ws. Worst speed minimum temperature, indicated in graphics as **corner5**.

The most sensitive variable was the lower frequency achieved by the oscillator. This frequency should not be off by 15% of 20kHz range for each analog prototype. Also the lower frequency shall never reach a 0 (DC) level. The values of temperature and supply voltage considered for the corner analysis are shown in Table 5.5.

Montecarlo Analysis. This analysis submits the included models to random variations [69]. The designs were submitted to three types of Monte Carlo Analysis:

Process analysis. Includes the manufacturing process parameters and their statistical variations

Table 5.5: **Limits for Corner Analysis**

	Min.	Typ.	Max.
Temperature	0°	25°	85°
Voltage(1)	1.48V	1.65V	1.81V
Voltage(2)	3.0V	3.3V	3.6V

Mismatch analysis. Analyze the variations due to mismatch in the device characteristics, larger geometry devices tend to exhibit better matching characteristics than small geometry devices.

Process and Mismatch Analysis. Exhibits the combined effect of both variations.

A set of 100 runs were carried out for each type of Monte Carlo. The results are histograms of 25 bins that include mean and standard deviation. A special instruction was included in order to emphasize a frequency = 0 Hz(DC) which would represents a failure condition. One of the most stringent conditions was to guarantee that all the proposed models were out of failure in the 100 runs.

Area. An estimation of the occupied area for the oscillator and associated circuitry using the Cadence Layout XL tools. The limit in the space occupied for the oscillator will be the size of one CarbonDEP stage (525µm×1,355µm)[2].

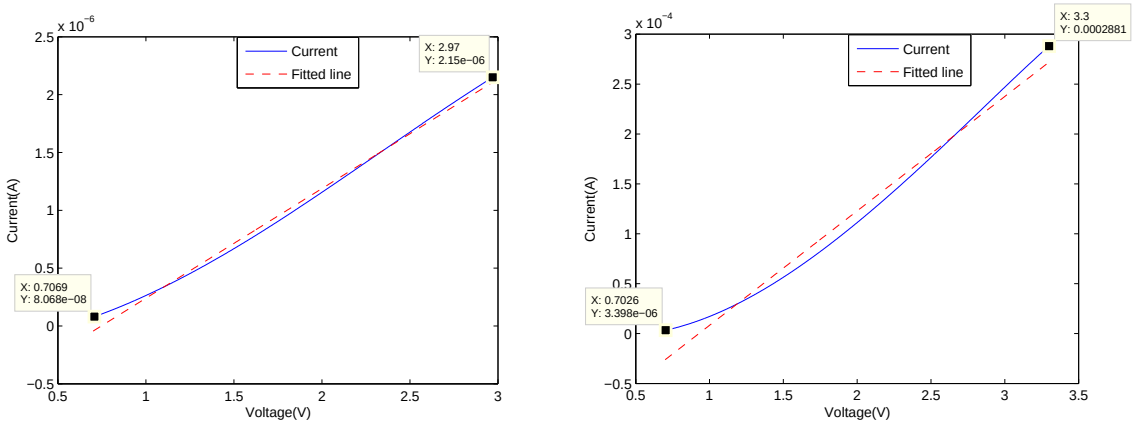
THD. Calculated from the analysis of the obtained waveform.

5.3.2 VCO-OTA alpha

This was the first analog model proposed to accomplish with the design requirements. The VCO was implemented using the diagram of Figure 3.4. The required frequency range is so wide that very different relations g_mC are needed. For example to obtain the frequency of 20kHz it is necessary to have a current around of 100nA with a capacitor of 5pF, while the 20MHz signal is obtained having a large transconductance, with a current below 300µA and a capacitor of 1pF.

A couple of voltage controlled current sources (VCCS) were designed to serve as the V/I converters, one controlled source operates from 0.8µA to 2.15µA, the other offers an output current from 3µA to 288µA. Both of them are controlled by voltages going from 0.7V to 3V. The sources exhibit a 99.7% linearity as shown in Figure 5.15 for the source with lower currents, and a linearity of 99.24% for the source with higher currents. Both sources were submitted also to a corner and Monte Carlo analysis to guarantee their operation.

A voltage change in the V/I converter will produce the correspondent (I_O) reflected in the sink transistors of the OTA_3 (controlling g_{m3}) and OTA_4 (changing g_{m4}) producing a change in the frequency (refer to Equation 3.24 in the last chapter) of the output sinusoidal signal with a fixed capacitor, see Figure 5.16.



(a) Weak inversion current source (b) Strong inversion current source

Figure 5.15: **V vs. I responses of current sources**

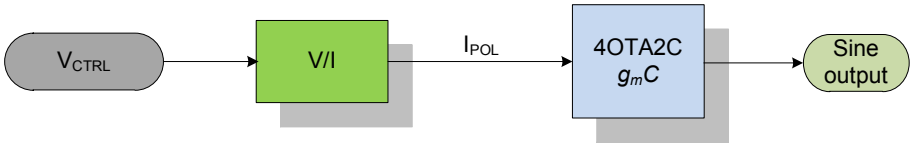


Figure 5.16: **Change of *gm* in VCO-OTA alpha oscillator**

The classic OTA circuit shown in Figure 5.17 was used for the implementation of the VCO-OTA alpha.

A switch based system connects or disconnects sources and capacitors in order to cover the whole frequency range (Figure 5.18). The operation modes are described in Table 5.6 indicating which elements (sources and capacitors) are connected. There is also a restart mode that allows both capacitors to be charged to an initial state.

Table 5.6: **Operation modes for VCO-OTA alpha**

	Capacitance	Source	Freq. Range
Mode 0	5pF	Low	8.26kHz - 203.9kHz
Mode 1	5pF	High	286kHz - 2.66MHz
Mode 2	1pF	Low	29.91kHz - 500kHz
Mode 3	1pF	High	863kHz - 21.06MHz
Restart	5pF	-	-

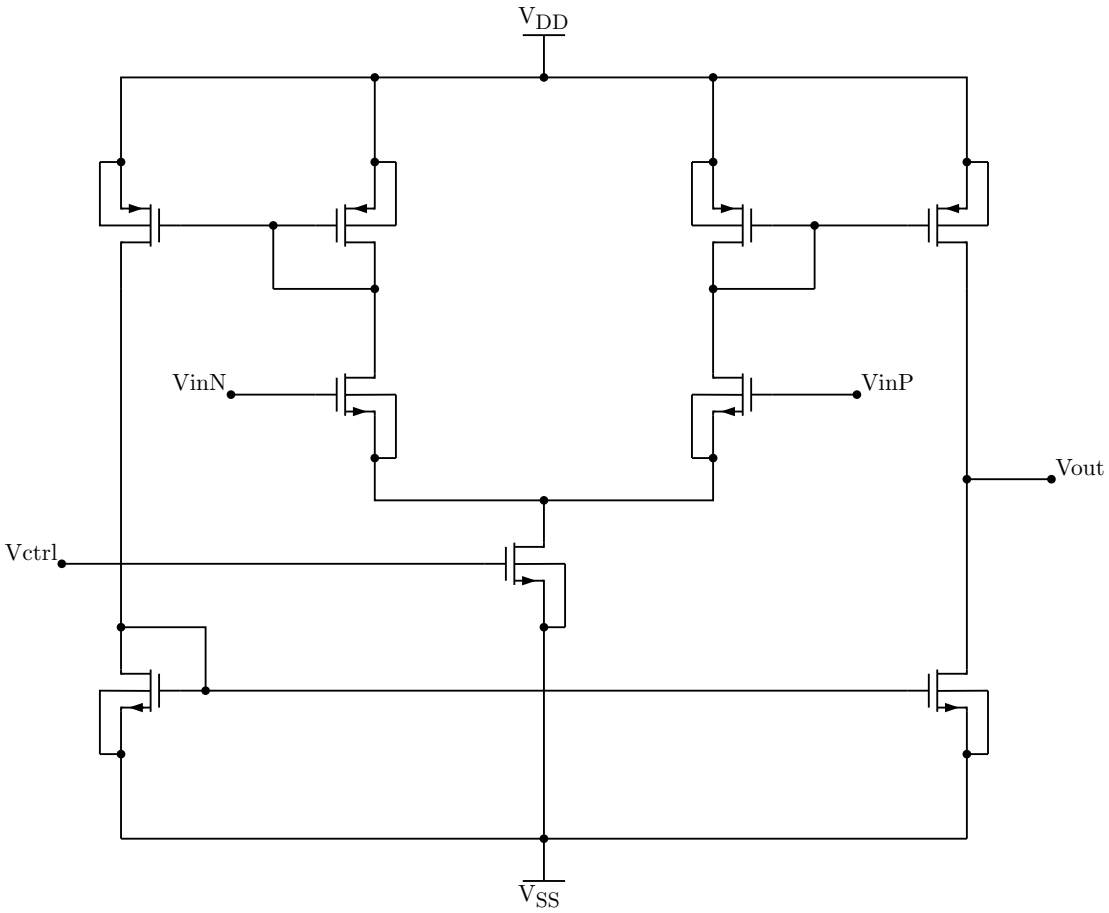


Figure 5.17: **Designed OTA for VCO-OTA alpha oscillator**

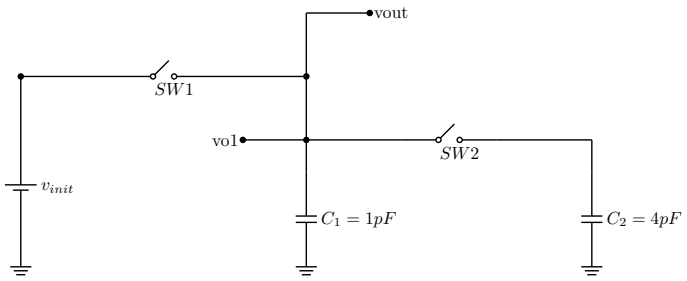
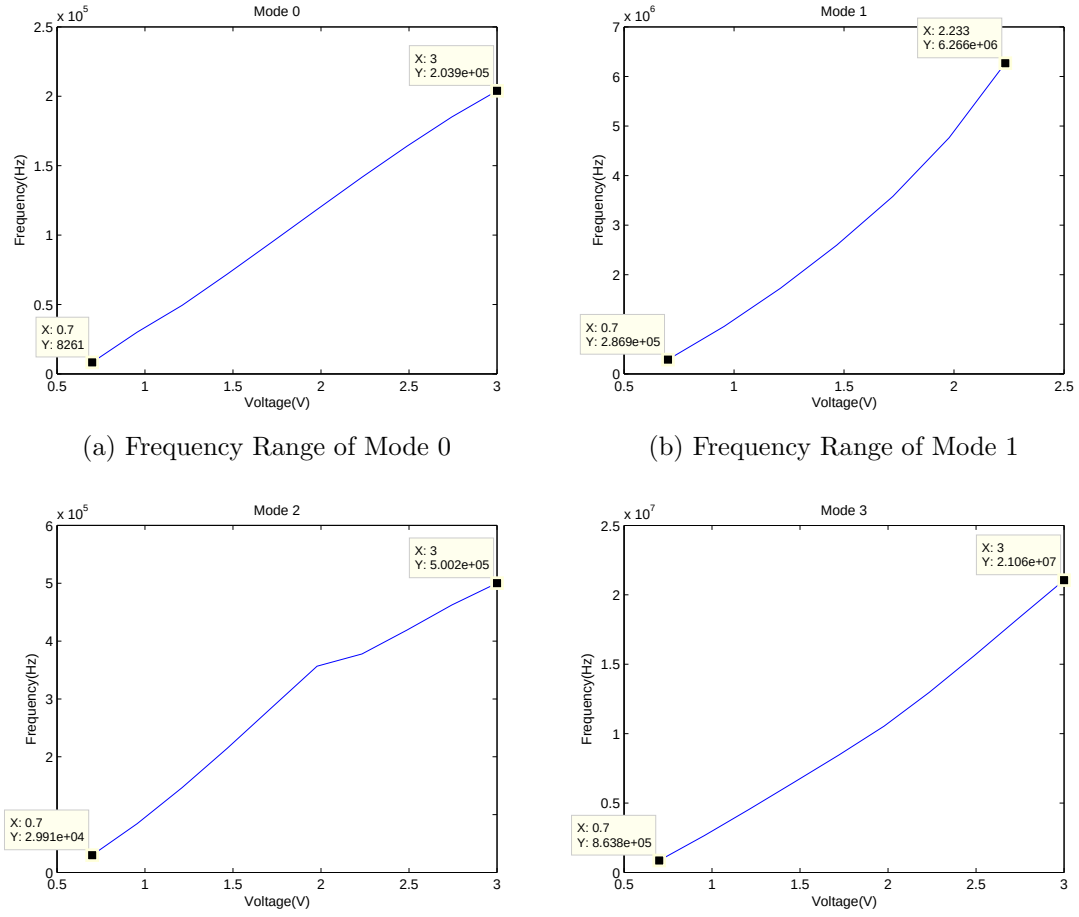


Figure 5.18: **Switched capacitors system**

5.3.2.1 Results

Figure 5.19 illustrates several modes that overlap frequency values. The repetition of the frequency band is another operation characteristic with different amplitude and/or THD (as an example see the *c)* plot in this figure where it can be seen that a instability condition exists for the Mode 2 when the input voltage exceeds 1.07V). The most important aspect at this point is that the whole range of frequencies is covered as shown in Figure 5.19.



(a) Frequency Range of Mode 0

(b) Frequency Range of Mode 1

(c) Frequency Range of Mode 2

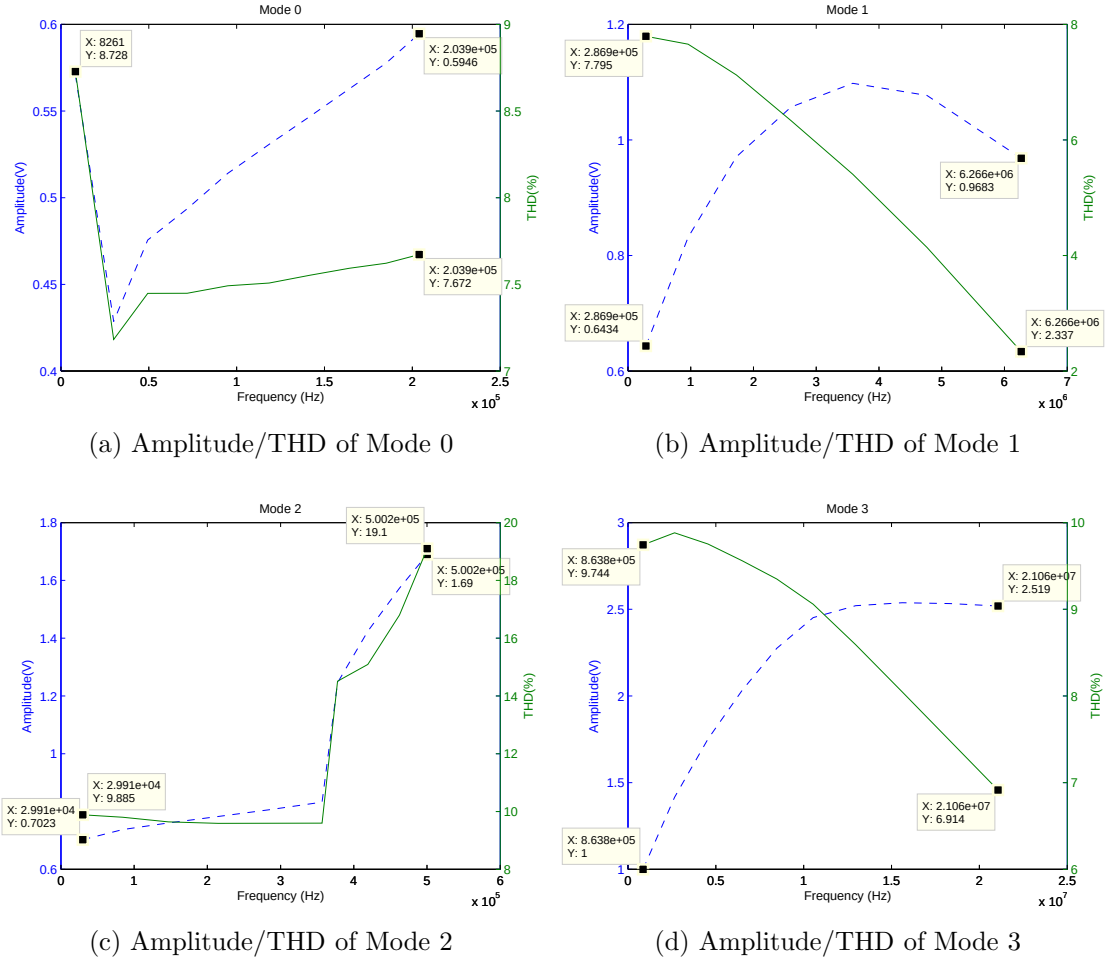
(d) Frequency Range of Mode 3

Figure 5.19: **Frequency ranges for the four operation modes of VCO-OTA-alpha**

(Plots obtained from the simulation of the OTA-C circuit)

Figure 5.20 shows the output characteristics of amplitude and THD against frequency variations for each operation mode. Note that the amplitude and THD change as frequency increases. There are important amplitude variations between modes. In an IC implementation an amplitude control would be necessary. The amount of THD represent a drawback of this oscillator since the additional circuitry to minimize this effect

cover a large amount of on-chip space. Additional details such as power consumption, THD and occupied area for this VCO will be discussed in section 5.3.5.



(a) Amplitude/THD of Mode 0

(b) Amplitude/THD of Mode 1

(c) Amplitude/THD of Mode 2

(d) Amplitude/THD of Mode 3

Figure 5.20: **Output characteristics for each operation mode of VCO-OTA-alpha**

(Amplitude plotted with dotted line with scale axis at left)

The frequency change is performed by changing the input voltage that in turn will make a change in the I_{POL} varying the gm parameter. The results in Mode 1 show that the amplitude falls from 1 to 0V when the input surpasses 2.2V. Figure 5.20b[3] illustrates this effect when a sudden interrupt reveals that the oscillation condition of the second order system are not met for the whole input signal range. this fact lead us to see that the major difficulty in the implementation of the VCO's based in OTA-C is the existence of transconductance values that can result in no oscillation conditions. A better view of this problem is shown in Figure 5.21 showing that the oscillation is interrupted when the input voltage goes above 2.5V.

[3]The whole range was not shown before in the characteristics graphs due to problems in the plotting of variables against frequency.

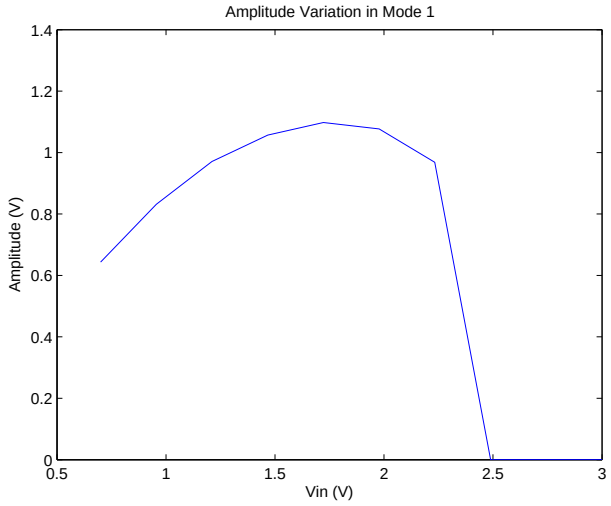
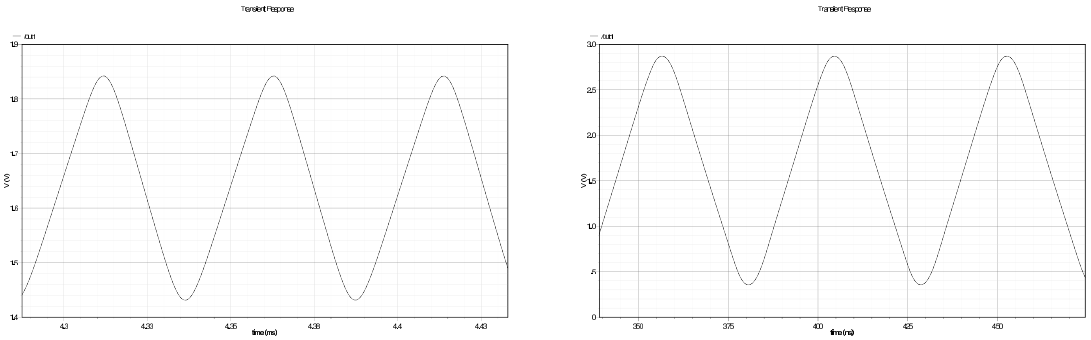


Figure 5.21: **Variation of amplitude for Mode 1**

The output waveforms of the VCO-OTA alpha at 20kHz and 20MHz are shown in Figure 5.22.



(a) Output waveform 20kHz (b) Output waveform 20MHz

Figure 5.22: **Output waveforms of VCO-OTA alpha**

Monte Carlo Analysis

The results of Monte Carlo analysis are summarized in Table 5.7 for low and high frequencies. The nominal value at low frequency was 19.3kHz and for high frequency 20.86MHz. We can see the obtained histograms in Figure 5.23

Table 5.7: **Monte Carlo Results for Low and High Frequencies of VCO-OTA alpha**

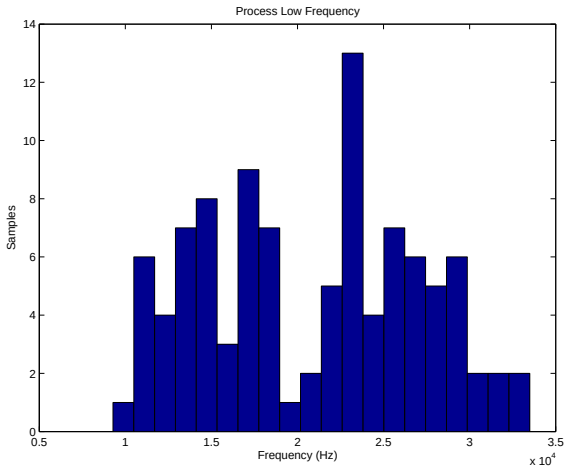
	Low Frequency (kHz)				High Frequency (MHz)		
Measurement	P&M[a]	Mismatch	Process		P&M	Mismatch	Process
Media	19.66	18.83	20.89		20.67	20.83	20.96
SD[b]	7.36	3.78	6.18		1.47	0.192	1.63
Range	6 - 52	10.6 - 26.8	8 - 32		17.4 - 24.6	20.35 - 21.2	17.8 - 24.6
Mode[c]	20(15)	19.6(10)	22(18)		20.4(6)	20.82(8)	20.6(8)

[a] Process and Mismatch

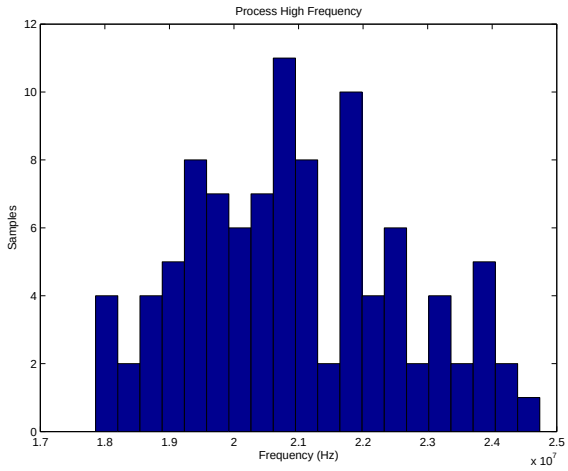
[b] Standard deviation

[c] Most repeated value, occurrences in parenthesis

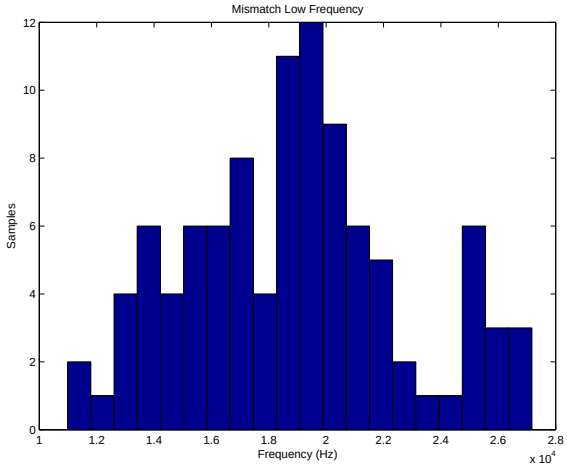
In all cases the mean values for the low frequency were around the 20 kHz specification. If the prototype presented lower frequencies, it is always possible to increase the input voltage to get to the lowest nominal limit. On the other hand if a displacement offset would have to be introduced, the highest limit (20MHz) could also be achieved. From Figure 5.19 we can see that the frequency range presents flexibilities in lower and upper limits. Even though the Monte Carlo analysis throws a minimum possible output frequency of 6kHz, not a single case (in 100 runs) presents a 0Hz failure condition. The proposed prototype works without failure for both extremes of the required frequency.



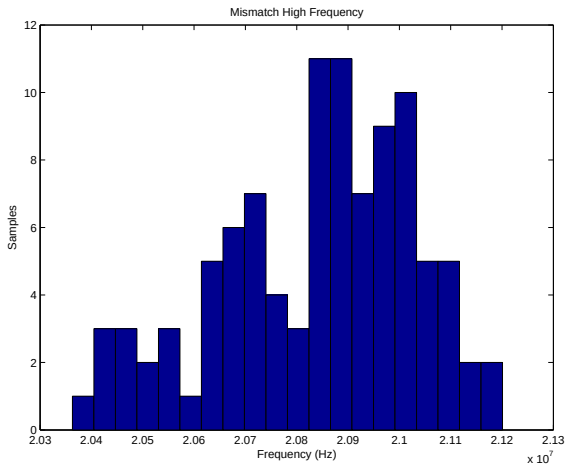
(a) Process L.F.



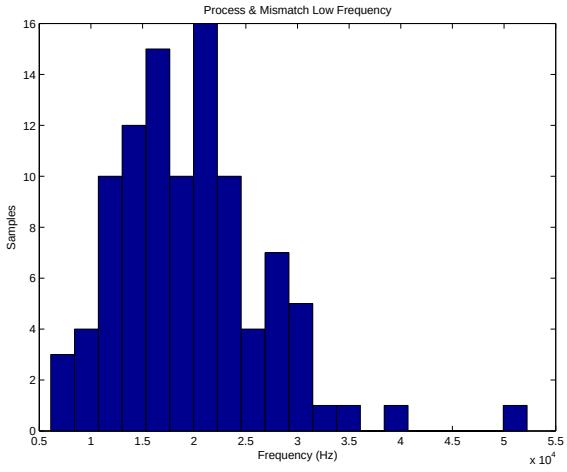
(b) Process H.F.



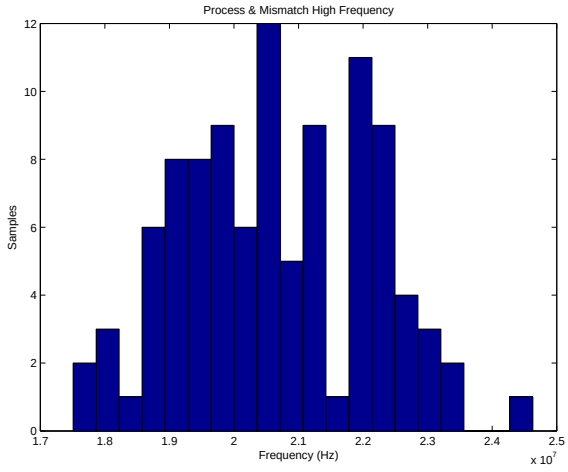
(c) Mismatch L.F.



(d) Mismatch H.F.



(e) Process & Mismatch L.F.



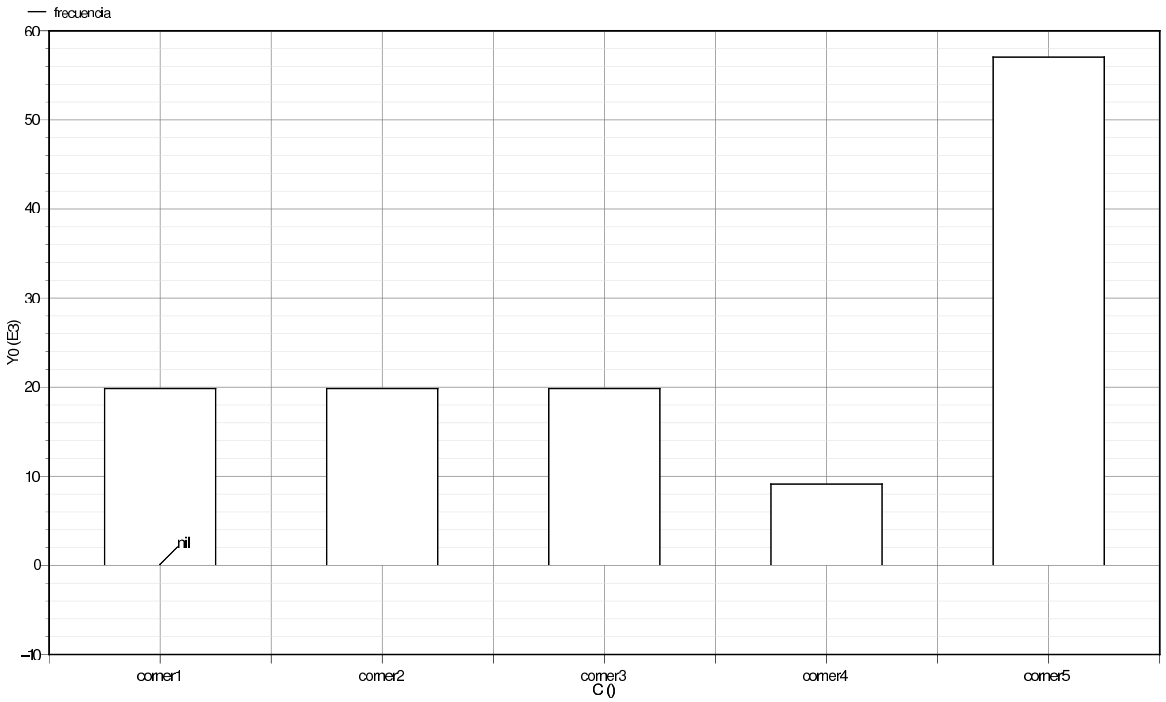
(f) Process & Mismatch H.F.

Figure 5.23: **Monte Carlo Results in Low and High Frequency for VCO-OTA-alpha**

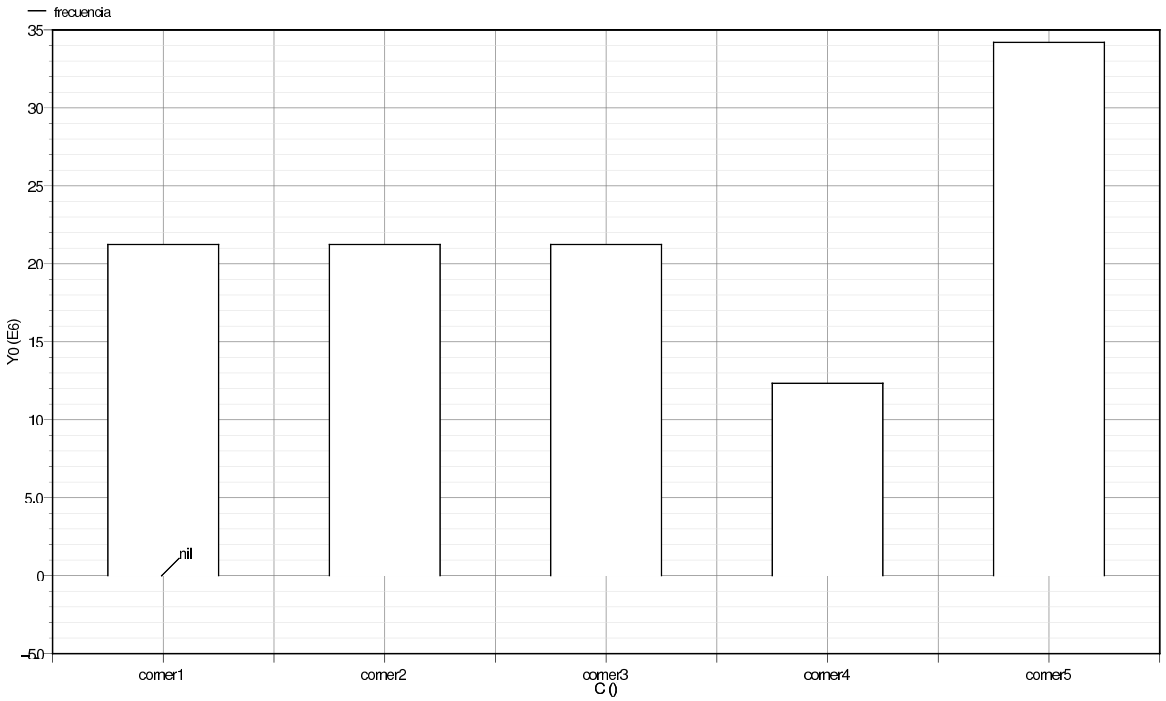
Corner Analysis

In the corner analysis the most important parameter was the frequency. The results of this analysis for low and high frequencies are depicted in Figure 5.24. The x axis show the configured corner analysis (corner1 to corner5) configured as mentioned before, the y axis show the frequency of the obtained sine signal under corner conditions.

The results for this prototype reflect almost no dependence against radical changes in supply voltage, the corner1 to corner3 columns, show that the VCO keeps oscillating at 20kHz (same behavior for the first three columns in high frequencies). The lower frequency reported when the prototype is working at worst speed maximum temperature condition (corner4 @ 8kHz) does not represent a major issue. When the design is submitted to a worst power minimum temperature (corner5) the system presents a frequency high above the nominal frequency. This is one of the major drawbacks of this oscillator. In order to carry out the test an input voltage of 0.823V is used to give a nominal output frequency of 19.3kHz, even though it can operates with a lower voltage voltage (0.7V) concluding that frequencies below 20kHz can be achieved with this model. In high frequencies, the result of corner4 presents a frequency lower than the nominal (12MHz), this outcome reflects that VCO-OTA alpha does not performs well while working in bad power conditions and high temperatures. The addition of circuitry (references) with low sensitivity could help in the solution of this problem.



(a) Corner analysis at low frequency (20kHz)



(b) Corner analysis at high frequency (20MHz)

Figure 5.24: **Corner Analysis results**

5.3.3 VCO-OTA beta

The second proposed model (Figure 5.25) was conceived to have more linearity. The OTA was designed according to Nedungadi and Viswanathan [70]. The OTA-C oscillator scheme was used (refer to Figure 3.5), having the same structure and support circuitry than VCO-OTA alpha prototype. Minor changes to sources were made in order to adjust the output currents for each operation mode.

5.3.3.1 Results

Figure 5.26 illustrates a wider voltage vs. frequency ranges at the cost of higher THD values. This VCO uses capacitances of 2 and 3pF, but the area used by each OTA is higher. Figure 5.27 shows that this prototype exhibits output signal amplitudes of 1V, while VCO-OTA alpha operates at variable amplitudes. No spikes or jumps were present in the whole frequency range and in the four modes a decrease in THD percentage was observed as frequency increases.

Even though, this prototype achieves larger frequency ranges, the implementation of the oscillator using a single capacitor for the entire frequency range, would require a huge area. Therefore no benefit is obtained in this case. The modes of operation and frequency ranges are shown in Table 5.8.

Table 5.8: **Operation modes for VCO-OTA beta**

	Capacitance	Source	Freq. Range
Mode 0	5pF	Low	13.7kHz - 267kHz
Mode 1	5pF	High	186kHz - 12.54MHz
Mode 2	1pF	Low	26.7kHz - 519kHz
Mode 3	1pF	High	361MHz - 21.37MHz
Restart	5pF	-	-

Figure 5.28 shows the output waveforms at low and high frequencies it is possible to correct the distortion but at discrete intervals of frequency, therefore no THD control was integrated in the design. This approach is more consistent when it comes to output amplitudes using its low current source. The system operates with up to 0.5V variability using the low source current. This is having the higher frequencies presenting lower amplitudes.

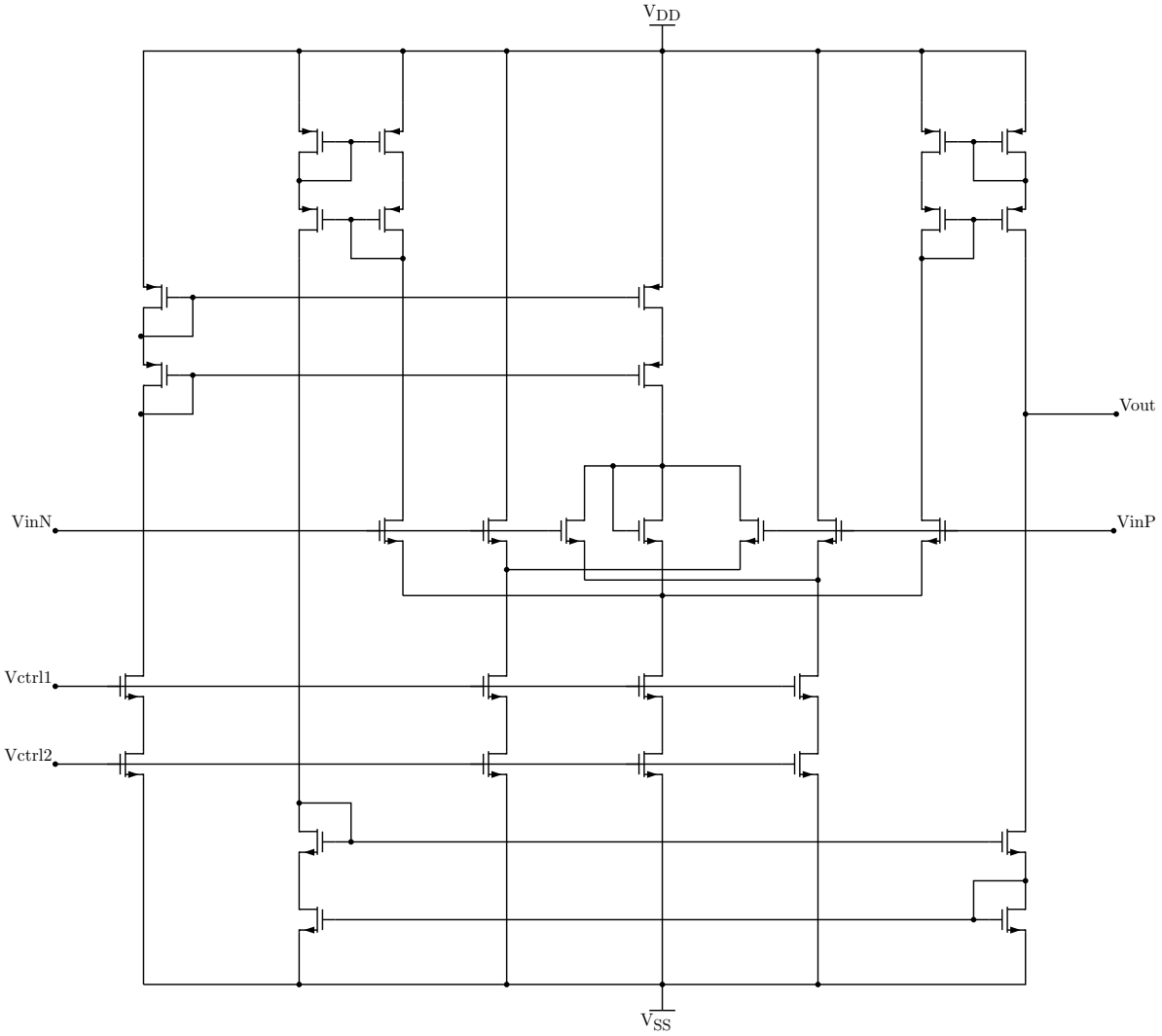
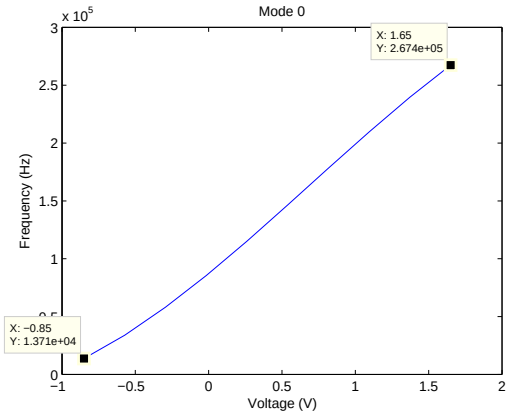
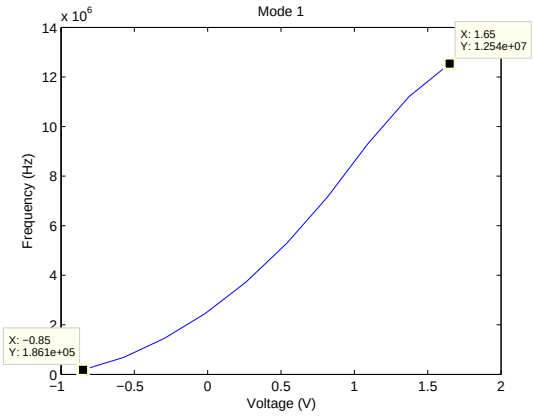


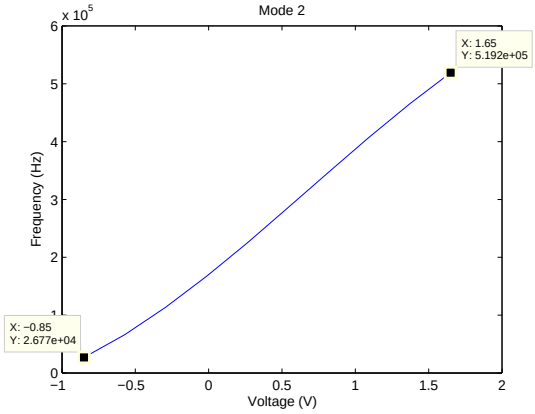
Figure 5.25: **Designed OTA for VCO-OTA beta oscillator**



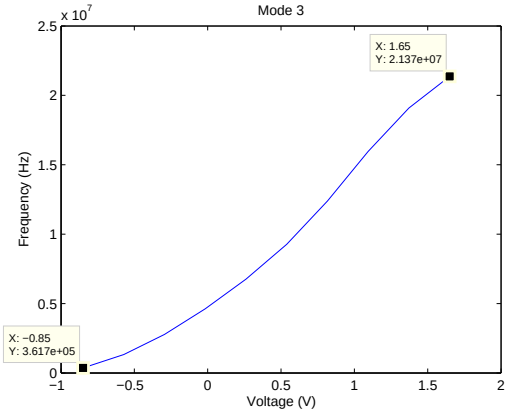
(a) Frequency Range of Mode 0



(b) Frequency Range of Mode 1

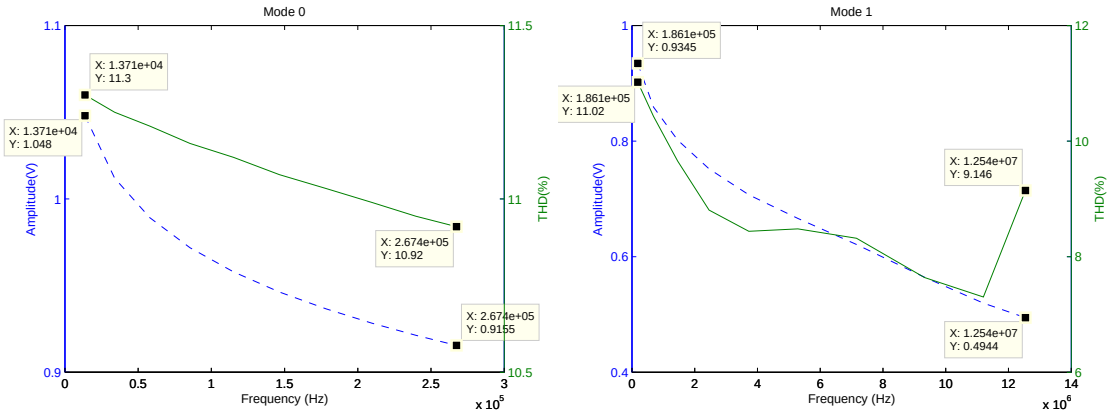


(c) Frequency Range of Mode 2



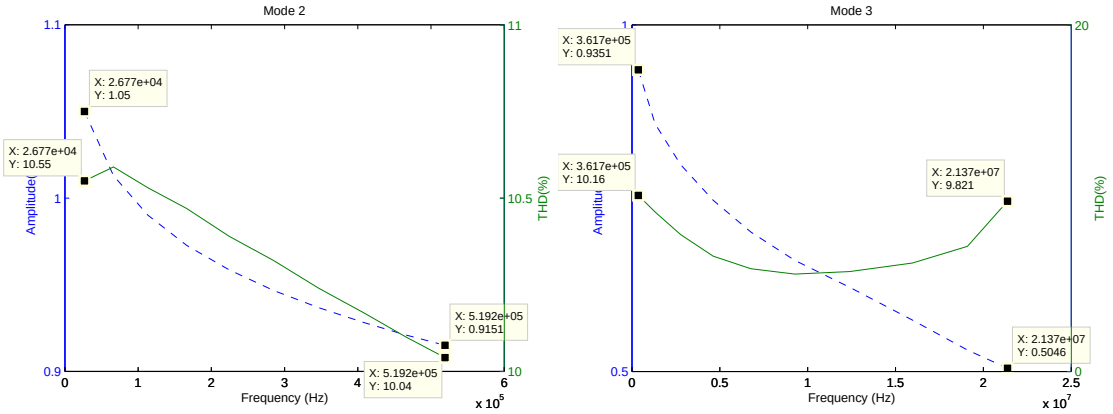
(d) Frequency Range of Mode 3

Figure 5.26: **Frequency ranges for the four operation modes of VCO-OTA-beta**



(a) Amplitude/THD of Mode 0

(b) Amplitude/THD of Mode 1

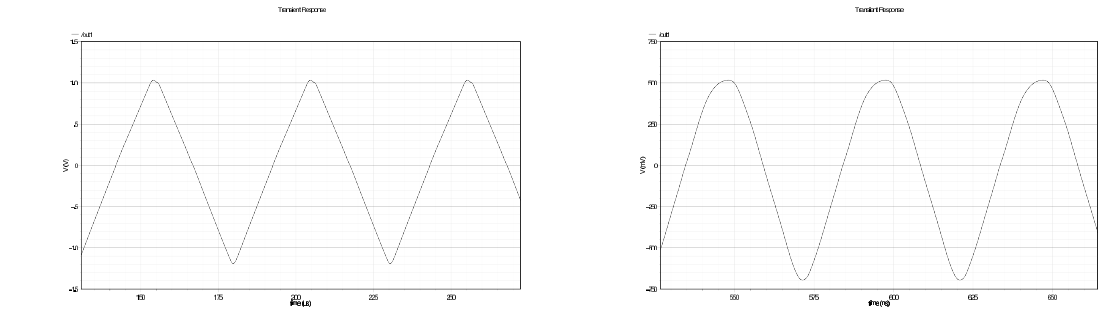


(c) Amplitude/THD of Mode 2

(d) Amplitude/THD of Mode 3

Figure 5.27: **Output characteristics for each operation mode of VCO-OTA beta**

(Amplitude plotted with dotted line with scale axis at left)



(a) Output waveform at 20kHz

(b) Output waveform at 20MHz

Figure 5.28: **Output waveforms of VCO-OTA beta**

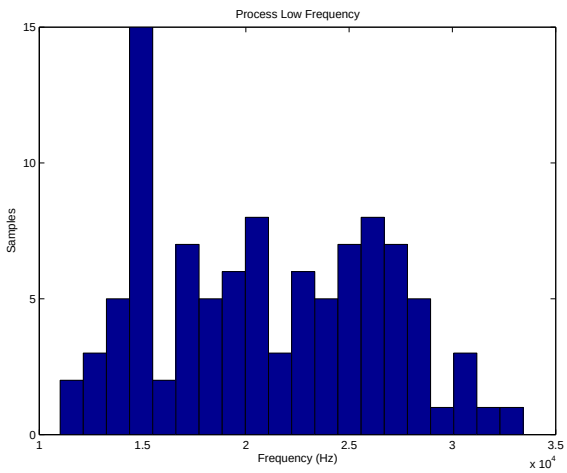
Monte Carlo Analysis

Table 5.9 summarizes the results of the Monte Carlo analysis. The nominal value at low frequency was 20.02kHz and for high frequency 20.41MHz. We can see the obtained histograms in Figure 5.29. It can be seen that smaller ranges of frequency are present for the output signal, while mean values in low frequency were farther than nominal frequency, the reduction in the dispersion of values leads us to think that this design performs better while working at low frequency. No DC conditions appeared neither during the Monte Carlo analysis nor in the frequency range plot[4].

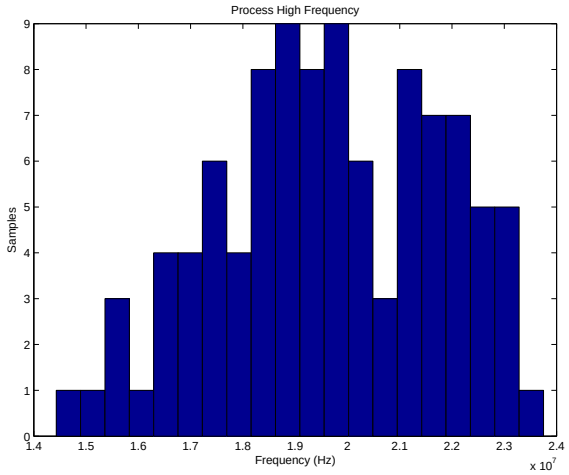
Table 5.9: **Monte Carlo Results for Low and High Frequencies of VCO-OTA beta**

	Low Frequency (kHz)				High Frequency (MHz)		
Measurement	P&M	Mismatch	Process		P&M	Mismatch	Process
Media	27.78	25.45	20.97		19.09	20.24	19.63
SD	17.43	14.32	5.45		1.8	0.160	2.11
Range	9.3 - 100	10 - 98	11 - 33		15.6 - 22.6	19.6 - 20.6	14.6 - 23.56
Mode	12(16), 18(16)	14(30)	14(15)		19.8(9)	20(15)	16(9)

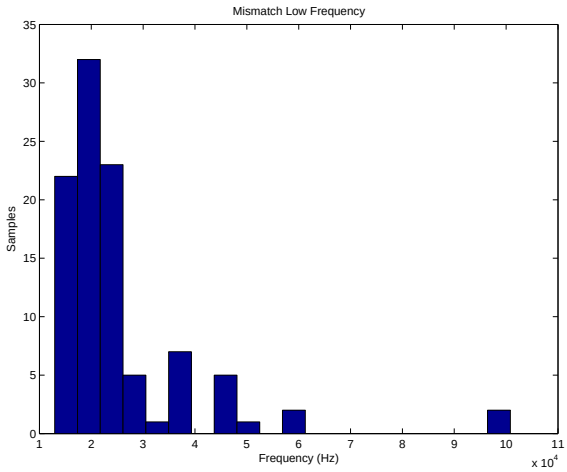
[4]As in the case of the VCO-OTA alpha.



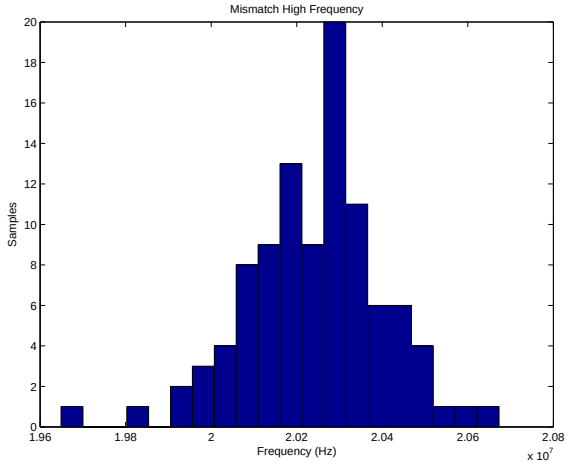
(a) Process L.F.



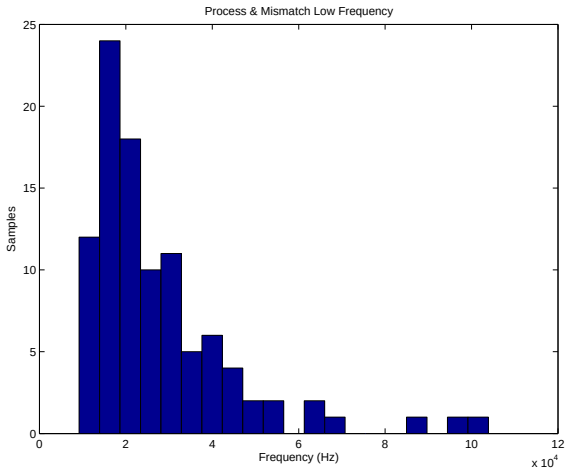
(b) Process H.F.



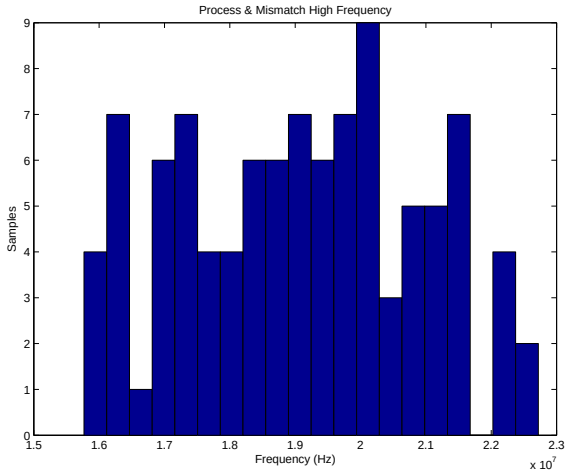
(c) Mismatch L.F.



(d) Mismatch H.F.



(e) Process & Mismatch L.F.

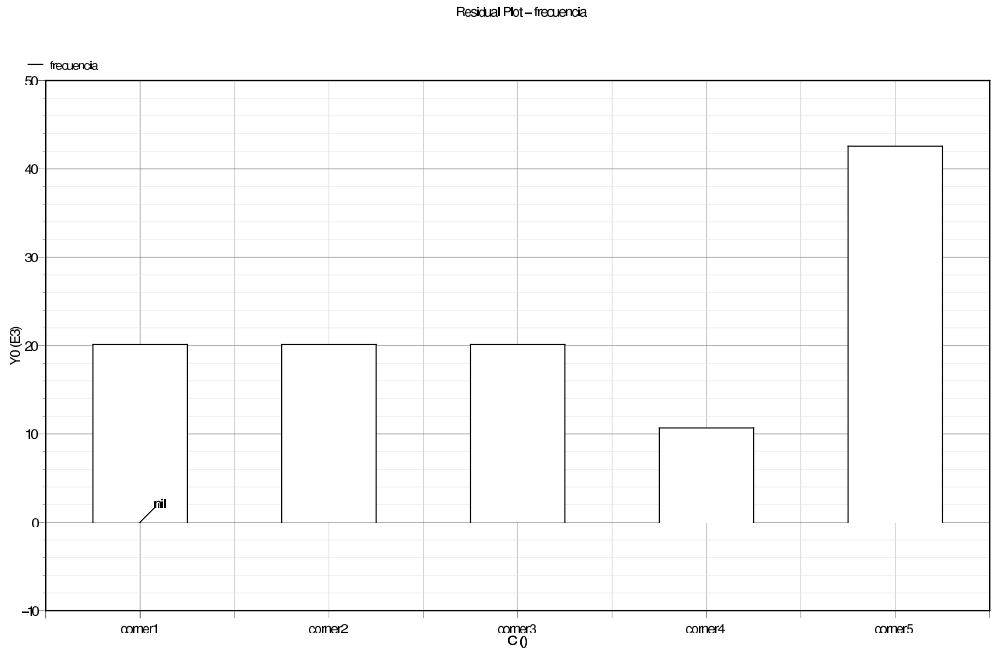


(f) Process & Mismatch H.F.

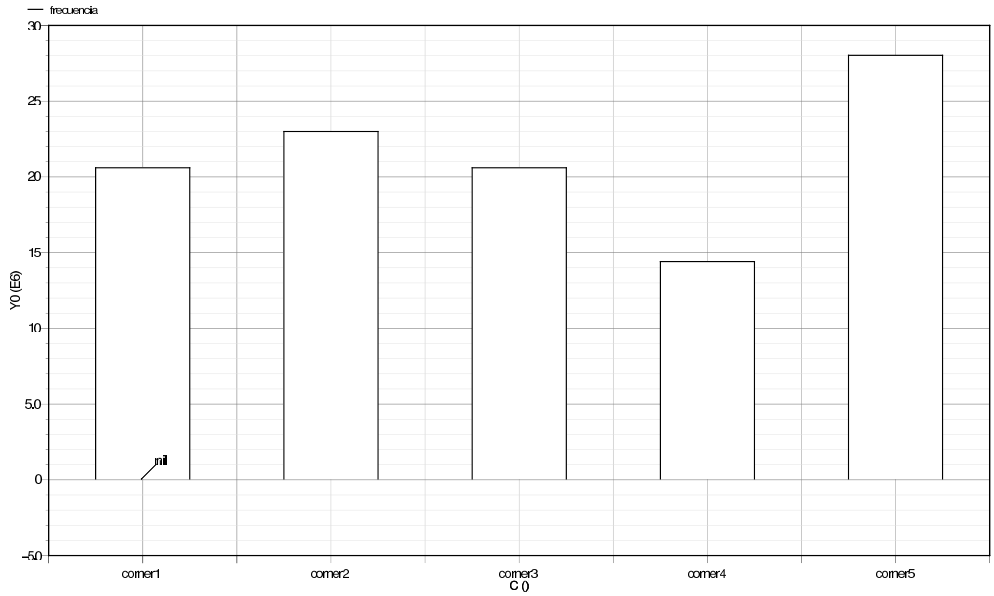
Figure 5.29: **Monte Carlo Results in Low and High Frequency for VCO-OTA-beta**

Corner Analysis

Again at low frequency a jump is observed when the design was operating at the worst power minimum temperature test. If a growing high above the nominal 20kHz is present in a real scenario, this design will behave better than its predecessor due to the fact that it has an output frequency of 19.7kHz at -0.76V (it would be possible to decrease the input voltage to -0.86V without compromising the oscillator performance). Also at low frequency this scheme presented small sensitivity to changes in supply voltage. At high frequency the difference between the maximum nominal frequency and the obtained for the worst power minimum temperature (corner5) test, shows also a reduction, while the sensitivity to the power supply exhibits an increase in nominal frequency when operating with an input voltage of 1.48V.



(a) Corner analysis at low frequency (20kHz)



(b) Corner analysis at high frequency (20MHz)

Figure 5.30: **Corner Analysis results for VCO-OTA beta**

5.3.4 Triangle to Sine Converter

This oscillator operates with only three operation modes and uses only one capacitor (546fF)[5] is needed to sustain oscillations. Two prototypes were proposed using this architecture: a Triangle to Sine Converter in Strong Inversion, and a Triangle to Sine Converter in Weak Inversion, their performances are examined in the next sections.

5.3.4.1 Relaxation oscillator

The triangle signal is obtained from a relaxation oscillator, this component is used to evaluate both approaches (triangle-to-sine converter in strong inversion and triangle-to-sine converter in weak inversion). The two current sources were substituted for one current source controlled by voltage and a directional module (to drive current towards the capacitor or from the capacitor). The comparator used by the relaxation oscillator is guaranteed to work at 25MHz and was implemented following the diagram of Figure 3.6. Circuitry to charge the capacitor to an initial value was also included.

5.3.4.2 THD control

Normally for a given amplitude, the triangle-to-sine converter (TSC) allows to have a sine signal with a small amount of distortion, this THD is very low if the TSC block is biased in weak inversion [44]. The main problem here is that the conversion from triangle to sine is done thanks to a static non-linear characteristic of the MOS transistor[6].To this static distortion a dynamic component is added (Slew Rate) given that the oscillator works at high frequencies where these dynamic aspects are noticeable. The combination of the static and dynamic non-linearities lead to a complex phenomena where according to the frequency different amount of distortion appears. In order to minimize this side effects, the TSC block was optimized with a set of different current bias which vary as a function of the signal's frequency[7]. The implemented THD control keeps distortion lower than that of a triangle wave[8].

5.3.4.3 Triangle to sine converter in Strong Inversion (TSC-SI)

A current source for charging of the capacitor was designed with three ranges of operation. Those three stages were chosen to offer a coverage of at least a decade in frequency. The current sources operate above 0.7V and below 3V, providing a frequency range from 11.94kHz (Mode 0) to 21.5MHz (Mode 2) Table 5.10 and Figure 5.31 illustrates the frequency ranges for each mode operation

[5]This capacitor takes a minimum area of 25µm×25µm (as implemented using standard technology AMS 0.35μ).

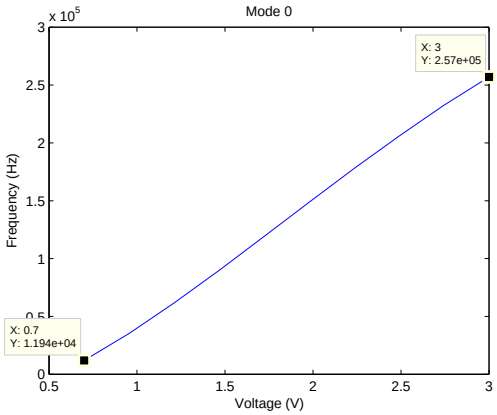
[6]This characteristic could be quadratic or exponential depending on the operation region of the MOS transistor.

[7]The details of this optimization block are given in the next chapter

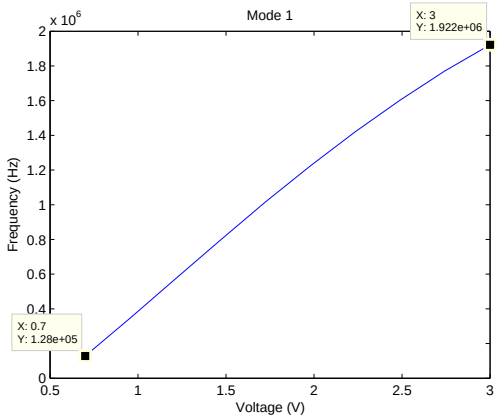
[8]The THD for a triangle waveform is 12%.

Table 5.10: **Operation modes for TSC-SI**

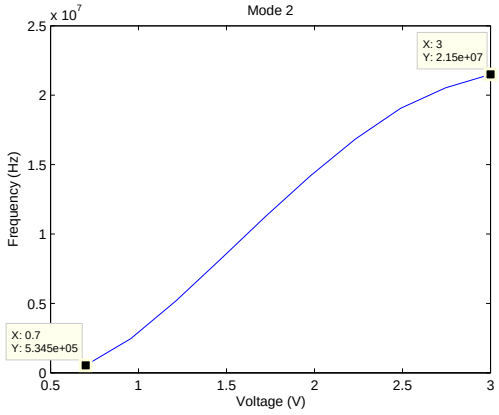
	Freq. Range
Mode 0	11.94kHz - 257kHz
Mode 1	131kHz - 1.92MHz
Mode 2	534kHz - 21.5MHz
Restart	-



(a) Frequency Range of Mode 0



(b) Frequency Range of Mode 1

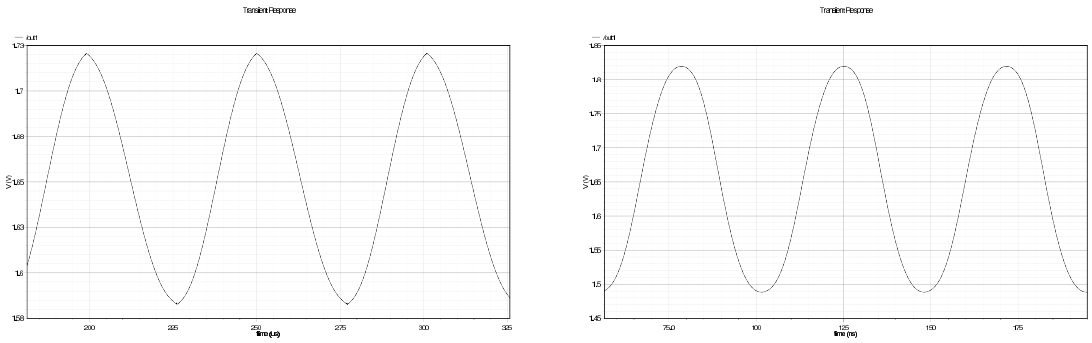


(c) Frequency Range of Mode 2

Figure 5.31: **Frequency ranges for the three operation modes of TSC-SI**

5.3.4.4 Results

Figure 5.32 illustrates the amplitude and THD levels obtained from simulations. Figure 5.33 shows the output waveforms at 20kHz, respectively. This VCO prototype maintains a THD of less than 7.8% with constant amplitudes at output signal. Moreover, the chip area used by the capacitor is relatively small but the comparator/OpAmp circuits take a larger space. Power dissipation is maintained at similar levels as previous prototypes as shown in Table 5.14.



(a) Output waveform at 20kHz (b) Output waveform at 20MHz

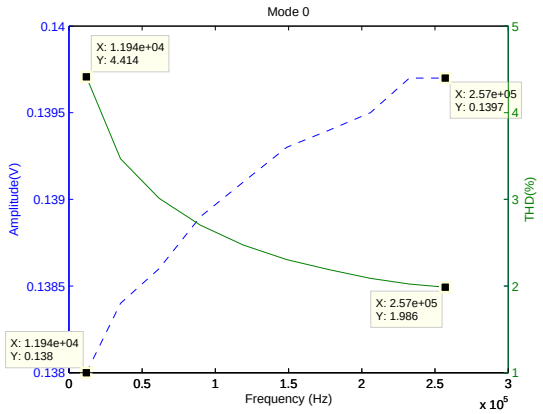
Figure 5.32: **Output waveforms of VCO TSC-SI**

Monte Carlo Analysis

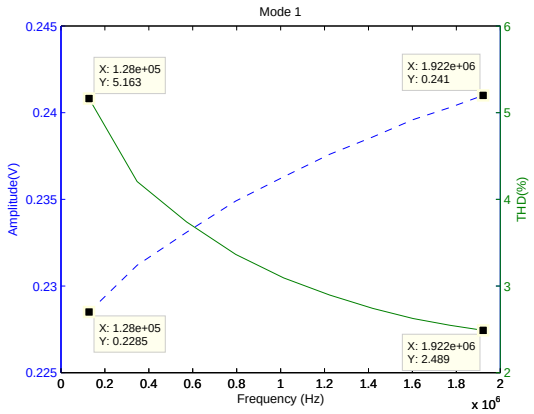
Table 5.11: **Monte Carlo Results for Low and High Frequencies of TSC-SI**

	Low Frequency (kHz)				High Frequency (MHz)		
Measurement	P&M	Mismatch	Process		P&M	Mismatch	Process
Media	21.79	20.92	21.45		21.47	21.42	21.59
SD	12.02	8.08	7.68		1.86	0.278	1.99
Range	2 - 74	7.5 - 51	7.5 - 40.5		15.75 - 26	20.68 - 22	17 - 27
Mode	12(11), 18(11)	16.5(10)	12(10)		19.25(13)	21.2(8)	22(12)

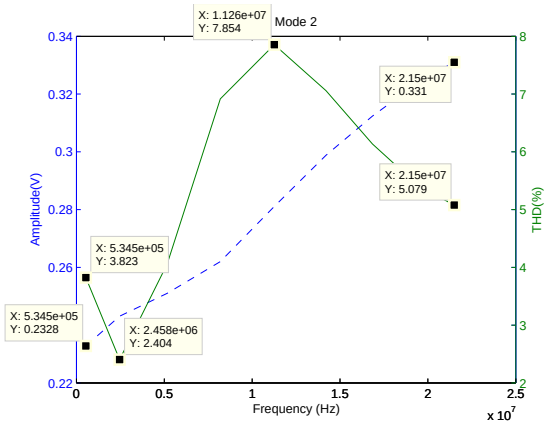
Table 5.11 presents the Monte Carlo test results for the TSC-SI oscillator. Also, Figure 5.34 shows the results at low and high frequencies using histograms. The results present consistent medias with low standard deviations. At low frequency the operation modes appear at frequency values lower than 20kHz which indicates a wider (than nominal) operation range. At high frequency the medias were above 20MHz with lowest ranges around 17MHz.



(a) Amplitude/THD of Mode 0



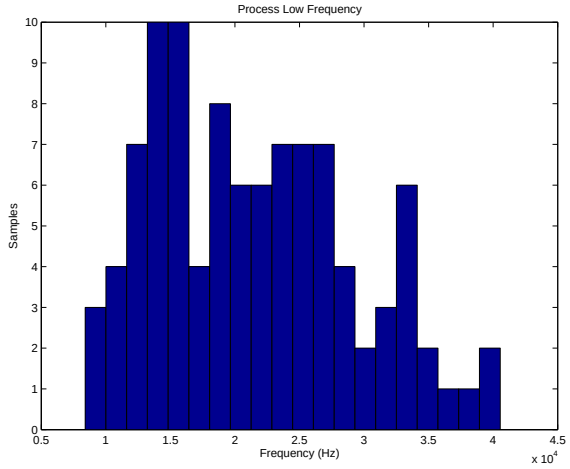
(b) Amplitude/THD of Mode 1



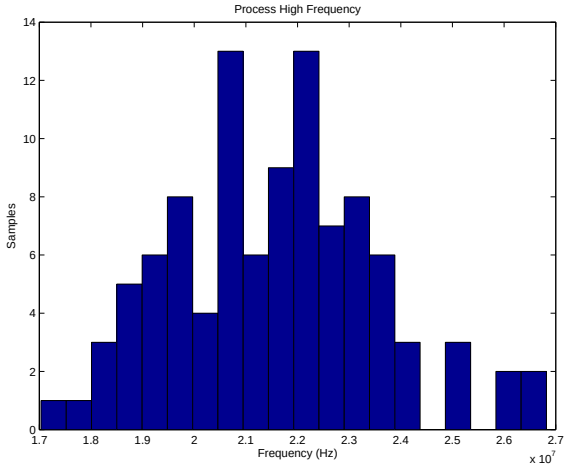
(c) Amplitude/THD of Mode 2

Figure 5.33: **Output characteristics for each operation mode of TSC-SI**

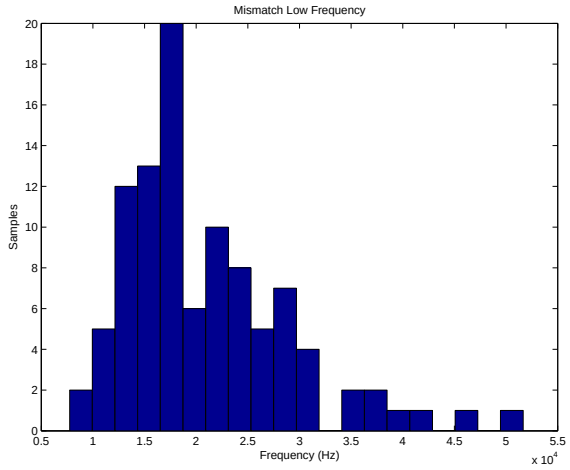
(Amplitude plotted with dotted line with scale axis at left)



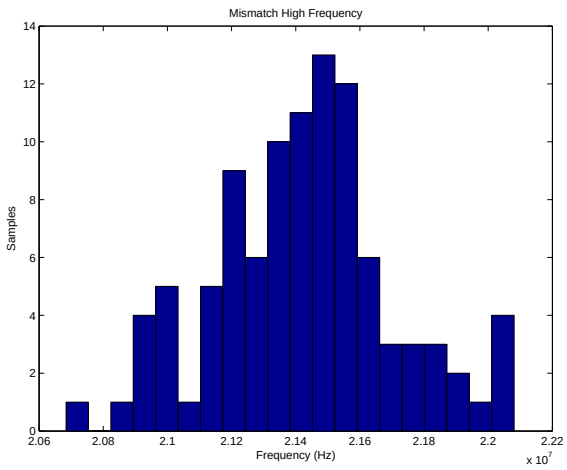
(a) Process L.F.



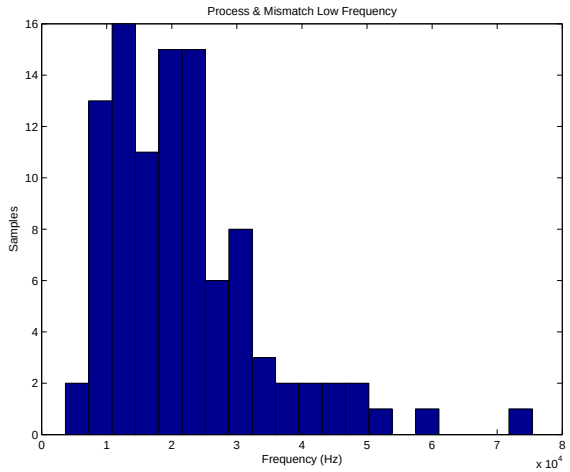
(b) Process H.F.



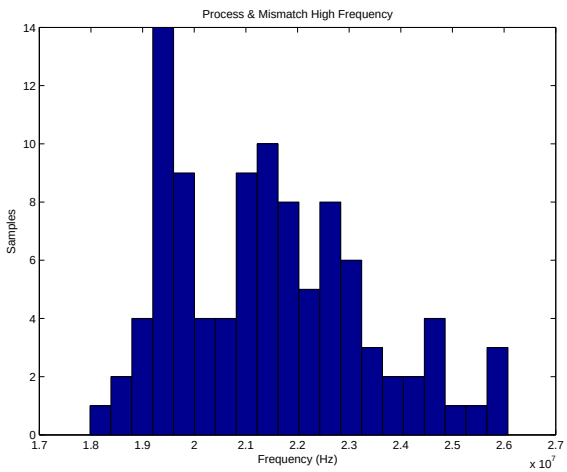
(c) Mismatch L.F.



(d) Mismatch H.F.



(e) Process & Mismatch L.F.

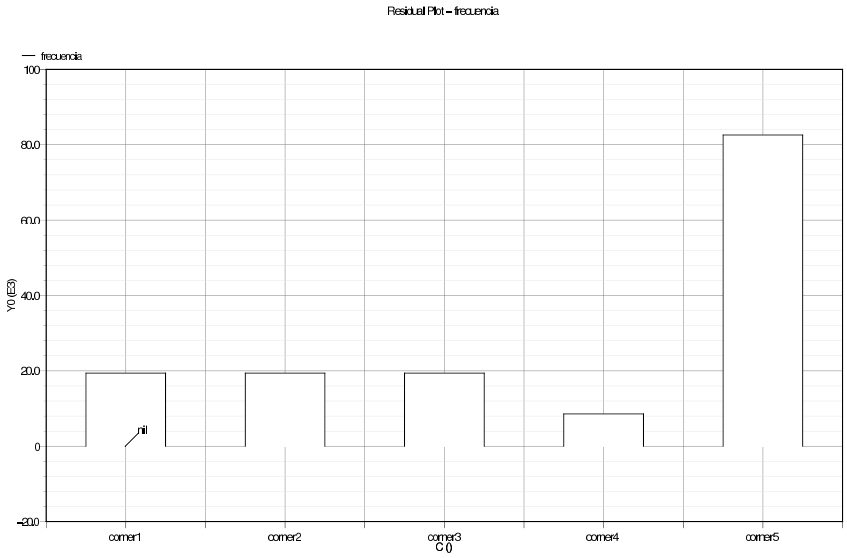


(f) Process & Mismatch H.F.

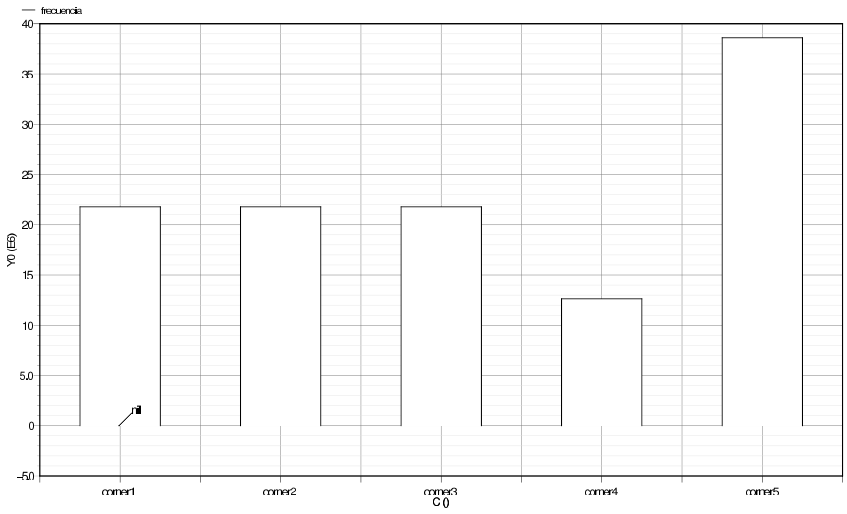
Figure 5.34: **Monte Carlo Results in Low and High Frequency for TSC-SI**

Corner Analysis

Figure 5.35 shows the results of the corner simulations. Again some problems may arise when subject to worst power condition and the output frequency of 82 kHz (corner5) may represent a drawback. However there is a small flexibility at this point due to the possibility of lowering the input voltage to 0.7V (nominal frequency of 11.94kHz). In high frequencies bad power conditions and high temperatures may decrease the output frequency, still it is possible to get higher frequencies in the conditions of corner4 increasing the input voltage above 3V thus maintaining acceptable operation levels.



(a) Corner analysis in low frequency (20kHz)



(b) Corner analysis in high frequency (20MHz)

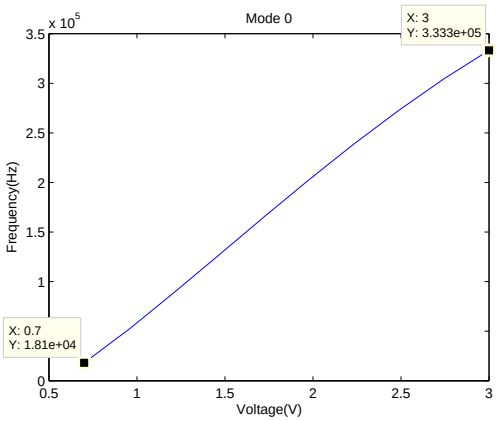
Figure 5.35: **Corner Analysis results for VCO-TSC-SI**

5.3.4.5 Triangle to Sine Converter in Weak Inversion (TSC-WI)

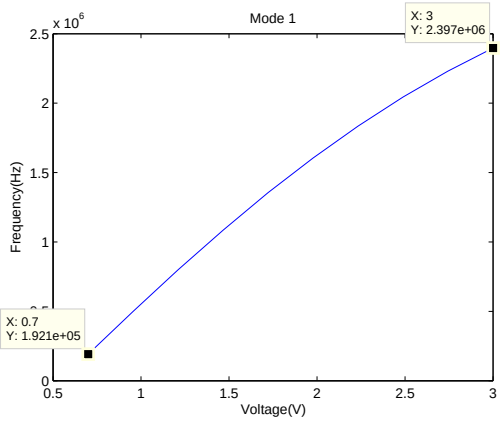
To test this circuit, the same design for the TSC-SI was used the differential pair was modified according to Figure 3.9 using resistors of 10kΩ. Using this circuit we could expect small size implementations with low consumption values; the three operation modes for this VCO are described in Table 5.12. This circuit uses the same design as the TSC-SI, but with slight modifications in the differential pair according to Figure 3.9.

Table 5.12: **Operation modes for TSC-WI**

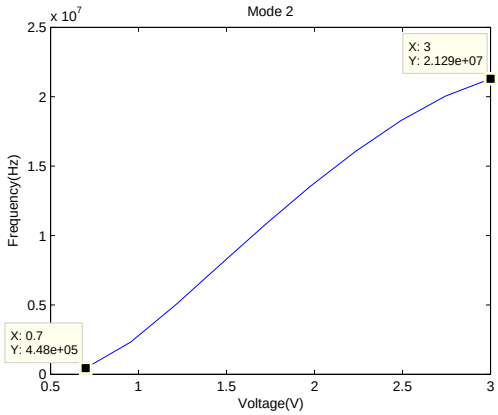
	Freq. Range
Mode 0	18.1kHz - 333.3kHz
Mode 1	192kHz - 2.397MHz
Mode 2	448kHz - 21.29MHz
Restart	-



(a) Frequency Range of Mode 0



(b) Frequency Range of Mode 1

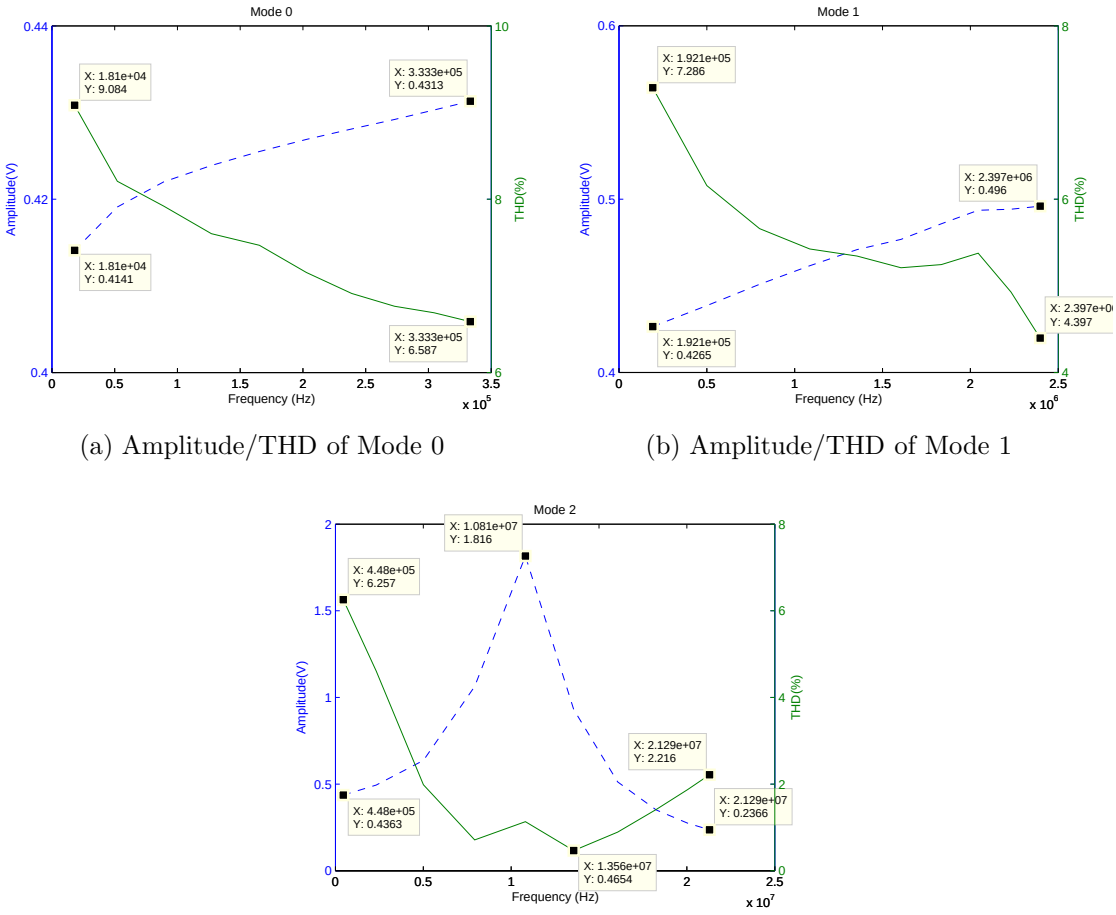


(c) Frequency Range of Mode 2

Figure 5.36: **Frequency ranges for the three operation modes of TSC-WI**

Note that Figure 5.36 and Figure 5.31 are essentially identical, this because in both systems the relaxation oscillator was the same. The bias current defines the operation mode (strong or weak inversion), it is possible to pass from one mode to another increasing or decreasing the amount of polarization current.

Figure 5.37 shows he output characteristics of amplitude and THD for each operation mode. In Mode 0 and Mode 1 a continuous increase in the output amplitude is observed. In Mode 2 an upsurge in the amplitude is observed when the frequency is near of 11MHz as a result of the static and dynamic characteristics of the differential pair when operating at high frequencies.



(a) Amplitude/THD of Mode 0

(b) Amplitude/THD of Mode 1

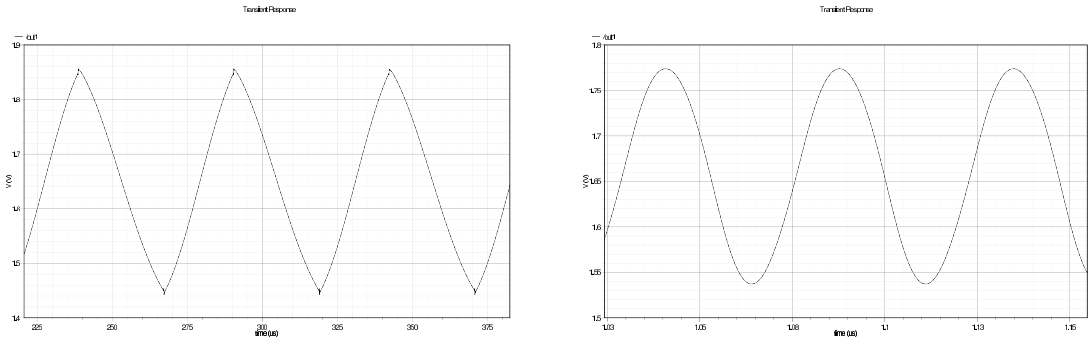
(c) Amplitude/THD of Mode 2

Figure 5.37: **Output characteristics for each operation mode of TSC-WI**

(Amplitude plotted with dotted line with scale axis at left)

5.3.4.6 Results

Needless to say that the voltage vs. current characteristics of current sources is reflected in the voltage vs. frequency characteristic of each mode; in this particular point we may found short traces covering the frequency range 18.1 kHz to 21.29MHz (see Figure 5.38).



(a) Output waveform at 20kHz (b) Output waveform at 20MHz

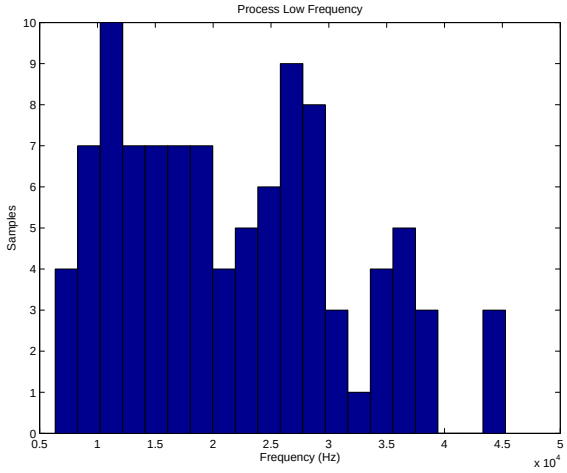
Figure 5.38: **Output waveforms of VCO TSC-WI**

Monte Carlo Analysis

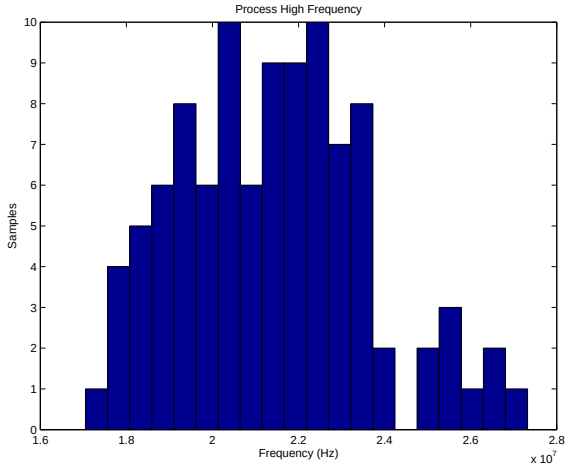
Table 5.13: **Monte Carlo Results for Low and High Frequencies of TSC-WI**

	Low Frequency (kHz)				High Frequency (MHz)		
Measurement	P&M	Mismatch	Process		P&M	Mismatch	Process
Media	21.96	19.37	21.65		21.46	21.24	21.39
SD	11.94	7.09	9.68		2.01	0.362	2.18
Range	3 - 60	8 - 42	6 - 44		16.3 - 25.9	20.44 - 22.02	17 - 27.2
Mode	9(17)	20(14)	10(11)		21.7(11)	21.61(9)	20(7)

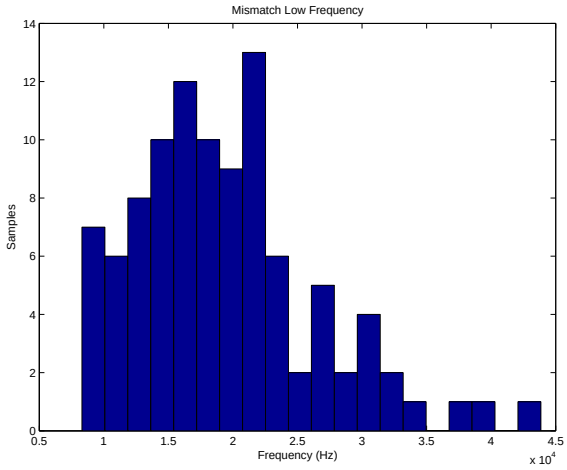
The Monte Carlo test was run at nominal values of 19.37kHz and 21.29MHz, the results are summarized in Table 5.13, the obtained histograms reflect high consistent medias with low standard deviations, no DC conditions were present at the tests.



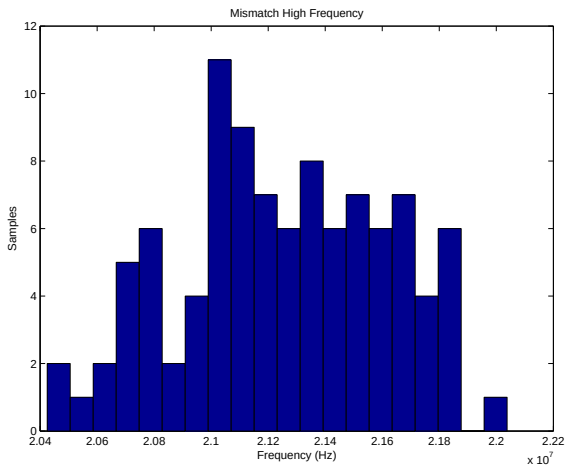
(a) Process L.F.



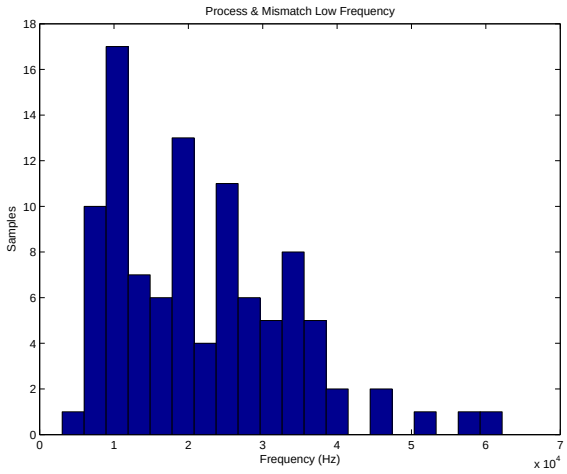
(b) Process H.F.



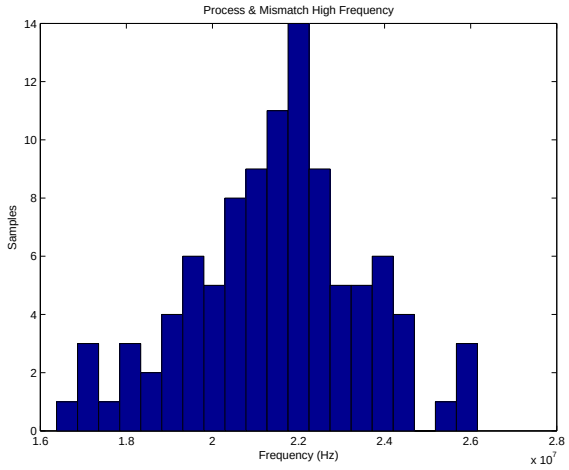
(c) Mismatch L.F.



(d) Mismatch H.F.



(e) Process & Mismatch L.F.

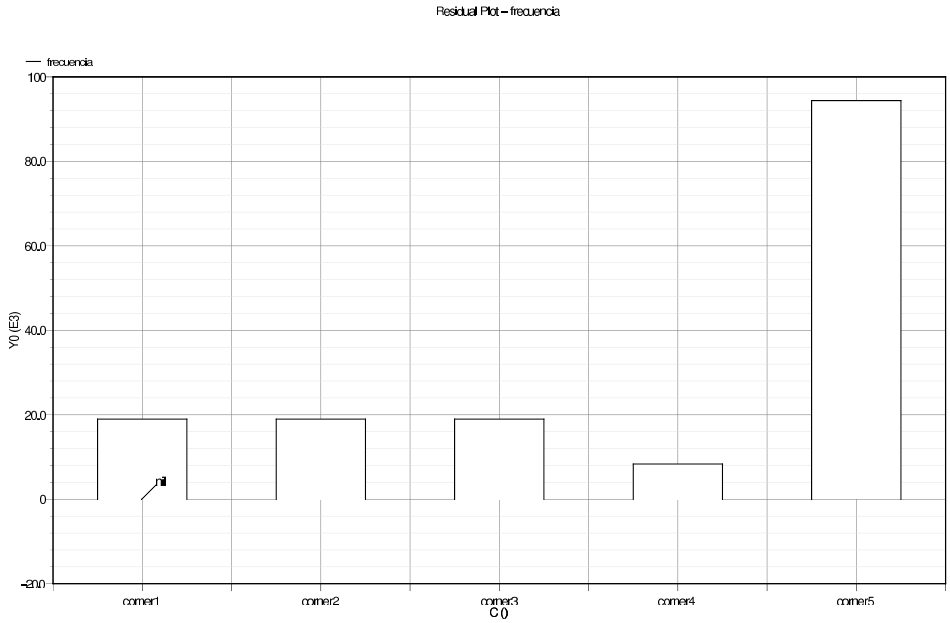


(f) Process & Mismatch H.F.

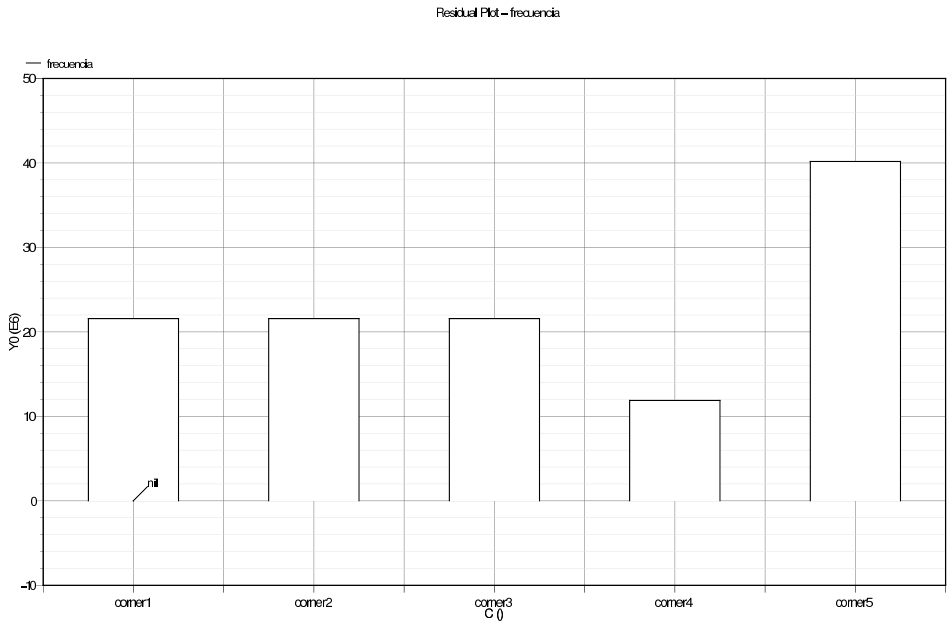
Figure 5.39: **Monte Carlo Results in Low and High Frequency for TSC-WI**

Corner Analysis

The results of the corner analysis are shown in Figure 5.40. The prototype behaves well when submitted to changes in supply sources, again some problems may arise when submitted to worst power condition (corner4). In high frequency the dispersion reduces but the worst speed condition (corner5) may represent a drawback.



(a) Corner analysis at low frequency (20kHz)



(b) Corner analysis at high frequency (20MHz)

Figure 5.40: **Corner Analysis results**

5.3.5 Final results of the analog models

Table 5.14 presents a complete comparison of the results obtained for the four prototypes.

Table 5.14: **Summary of reports for the analog oscillators**

	VCO-OTA alpha		VCO-OTA beta		TS Strong		TS Weak	
Measurement	Low	High	Low	High	Low	High	Low	High
Frequency	19.3KHz	20.86MHz	13.71kHz	21.36MHz	18.1kHz	22.29MHz	18.1kHz	21.29MHz
Power	61μW	5.85mW	66μW	10.62mW	8.02mW	10.42mW	7.34mW	9.75mW
THD	7.346%	6.921%	11.2%	9.82%	3.961%	5.111%	9%	2.215%
Corner ws	9.13kHz	12.34MHz	10.68kHz	11.19MHz	8.56kHz	12.63MHz	8.348kHz	11.89MHz
Corner wp	57kHz	34.2MHz	42.57kHz	33.14MHz	82.59kHz	38.6MHz	94.37kHz	40.18MHz
Amplitude	0.424	2.515	1.0480	0.5046	0.1382	0.331	0.414	0.236
Area	302μm×302μm		434μm×434μm		255μm × 255μm		341μm ×341μm	

- The VCO-OTA alpha can be implemented in a small area, it shows low THD waveforms and the lower power consumption of all analog models, but its operation cannot be guaranteed in the whole input range as seen in Figure 5.21, this condition may worsen if both capacitor are under mismatch effect voiding the oscillation capacity in some ranges.
- The VCO-OTA beta presented high THD measurements and long area, the final design would require the inclusion of a THD control increasing the size of the VCO. Some interesting approaches as those of [71] and [72] include the design of VCO's using the OTA-C models with long sweep ranges; the cost of those implementations is reflected in the OTA size making very difficult the integration of several VCO's.
- The TSC-SI is the smallest design, presents a high linearity response in frequency and amplitude and a very clean sine wave, this is the ideal oscillator of this study.
- The TSC-WI presented some linearity problems reflected in the Amplitude/THD characteristics plots, another drawback is the occupied area and high dispersion shown in its corner analysis.

5.4 Conclusion

The digital oscillator based in the DDS algorithm represent good alternatives for the implementation of the oscillator, the used area can rival with their analog counterparts, also the resolution and easy frequency change control constitute important aspects to be considered. As mentioned before the main reason to disqualify the digital oscillators is the need of a DAC at the output. The size of the DAC may increment dramatically the size of one signal generator, also the speed of the converter and its power may become a major drawback (as an example in a 14bit DAC @ 5MHz a size of 1.4mm^2 is needed consuming a power of 7mW [73], even when the power specification is acceptable, the space requirement may represent a problem).

In the analog side, the reviewed oscillators presented good performances. Even though the schemes based in OTA-C presented good results as in the works of ([41], [71], [72]) problems related to capacitor's mismatch may appear when implementing the VCO (notice that the operation of Mode 1 in the VCO-OTA-alpha analysis is not guaranteed above 2.3V, refer to Figure 5.19b). Linearity and THD at the output are affected making more complex the additional circuitry to deal with those problems. The figure of merit (FOM) for a sinusoidal oscillator is precisely the THD, in our case this FOM would be integrated by THD, linearity and power consumption.

The TSC-SI offers oscillators that can be implemented with just one capacitor presenting good linearity and low THD percentages. Their power consumption remain almost constant in the whole operation range (as seen in Table 5.14), and their amplitudes were located in a narrow span favoring the integration of simple amplitude controls. The TSC-SI is the selected option to become the sine source of the multi-channel oscillator. In the next chapter, the CMOS implementation of the TSC-SI architecture is detailed using a standard 0.35µm analog process.

Table 5.15 serves as a tool in the selection of the best prototype for the VCO. The table help in getting a clearer view of the capabilities of all proposed alternatives. The TSC-SI is evaluated with the best performances among the other analog options.

Table 5.15: **Comparison table of analog prototypes**

Oscillator Scheme	CHARACTERISTIC									
					Corner ws		**Corner wp**			
	Freq. Low	Freq. High	Power Dissipation	THD	Low Freq.	High Freq.	Low Freq.	High Freq.	Amplitude	Area
VCO-OTA- α	4[a]	4	1[b]	3	3	2	2	3	3	2
VCO-OTA- β	1	2	2	4	4	4	1	4	4	3
TSC-SI	2	1	4	1	2	1	3	2	1	1
TSC-WI	3	3	3	2	1	3	4	1	2	4

[a] Worst performance

[b] Best performance

Chapter 6

Implementation of the Multiple-channel Stimulator on a 0.35µm CMOS Technology

This chapter describes in detail the design, implementation and functioning of the modules that conform the multi-channel sinewave generator system. The oscillator is based upon the TSC operating in strong inversion.

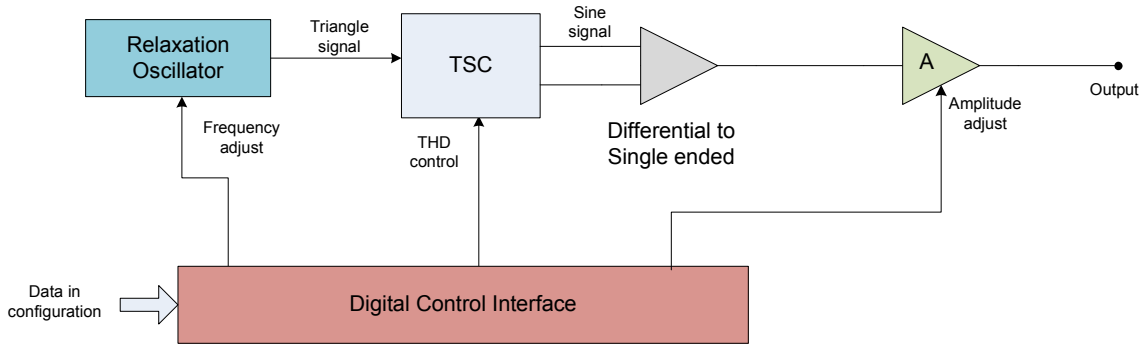


Figure 6.1: **Block diagram of the VCO**

The Figure 6.1 illustrates a block diagram of the complete VCO where the TSC constitutes the central core of the system. The relaxation oscillator allows a capacitor charge through an injected current. Once the capacitor reaches a certain amount of voltage level, a comparator switches the signal down to initiate a discharging transient. A directional module drives the current towards the capacitor or from it. Then, the triangular wave generated in the capacitor is converted to a sinewave with certain amount of distortion. This distortion can be kept at low levels (5%) with a dedicated digital current source (THD control). The multi-channel sine generator system, called SU5[1] includes a digital control over the THD, over the frequency and over the amplitude of the output signal.

[1]Acronym for Signal Unit 5.

Also, the layout process for each building block is revised in detail to provide the necessary fabrication details. The layout of the multi-channel generator was drawn according to the rules for the AMS0.35µ C35B3C4 process from Austriamicrosystems[68]. The rules to avoid mismatch, parasitics and noise, size reduction were applied in the creation of the floorplan according to reference [74].

6.1 Digital Current Source

The variation of frequency in the relaxation oscillator operates by varying the value of the capacitor or by changing the value of the injected current. The first option is not viable due to the lack of on-chip space, therefore the change in frequency must rely on a special designed current source.

The current source must be controlled digitally and also have a sufficient range to cover a broad frequency spectrum. We require to design for currents from 2.5nA to 30µA, with just one DAC. A total of 10,000 steps are needed to increase the quantization levels of the system. The total frequency range is divided in four parts. The digital current source consists of two blocks: a set of four current references, and a 7-bit current DAC.

The four current references permit four frequency modes, described in Table 6.1. Three current sources work in strong inversion and one having the smallest current values works in weak inversion[2]. A Two-bit decoder implemented using standard cells of the CMOS process, activates one of four current references according to the operation mode.

Table 6.1: **Characteristics of the digital current source.**

Mode	Range	Step size	Freq. Range
M0	293pA[3] - 321nA	2.54nA	7.7kHz - 715kHz
M1	286nA - 4μA	30nA	704kHz - 6.3MHz
M2	3.9μA - 7.7μA	30nA	6.2MHz - 10.2MHz
M3	7.4μA - 29.9μA	176nA	10.2MHz - 22.5MHz

Table 6.2: **Characteristics of the digital current source (cont)**

Parameter	Value
Max. Dissipated power	513μW
On-chip size	62μm $\times$ 200μm

[2]Current sources M1 and M2 are similar, the difference between them is the offset displacement, necessary to have the next frequency level.

Figure 6.2 shows the digital current source structure. The current source provides the current level via 127 transistors switched according to the digital code. In this figure only individual transistors can be seen but its important to remark that there is a group of transistors that activate according to the frequency range giving different amounts of current to guarantee a smooth transition between current/frequency ranges. For instance, when Mode 0 is set to its maximum value of current (320nA), the minimum value of current at Mode 1 is 280nA, the maximum current value of mode M1 is 4µA while the minimum current of source M2 is 3.9µA. In this figure only individual transistors can be seen but its important to remark that there is a group of transistors that activate according to the frequency range giving different amounts of current to guarantee a smooth transition between current/frequency ranges.

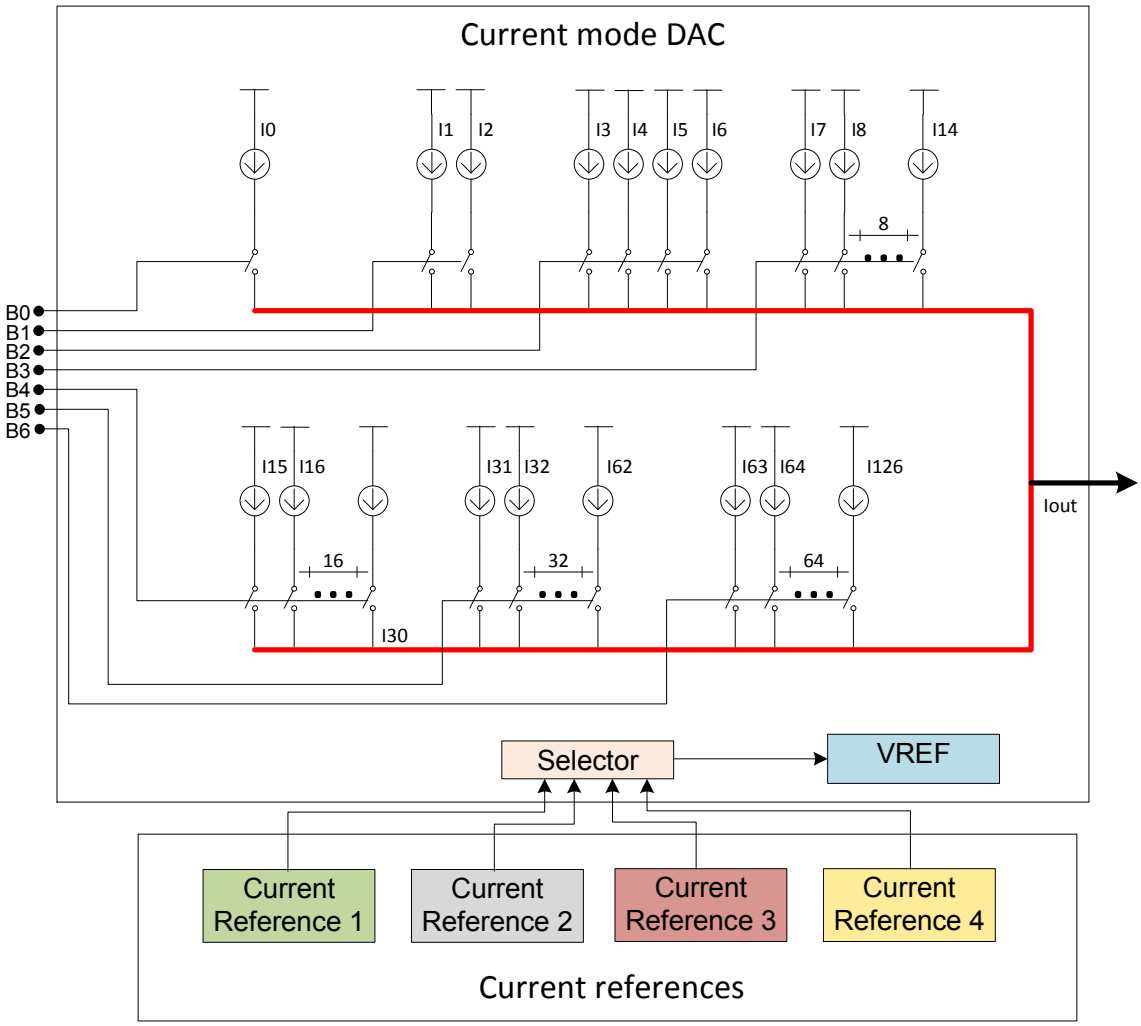


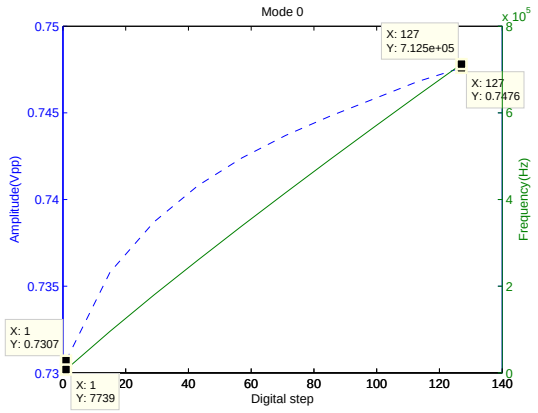
Figure 6.2: **Digital current source**

The overall response of the output signal in amplitude and frequency for every mode is shown in 6.3. Note that the frequency behavior remains relatively linear (except in M3 where higher currents are handled) but with changes in the output amplitude for each operation mode. Also, observe that amplitudes are not constant as a result of the complex contributions of the static (non-linearities of MOS transistors) and dynamic (Slew-Rate) characteristics of the differential pair (refer to subsection 5.3.4.2 and Figure 3.8a).

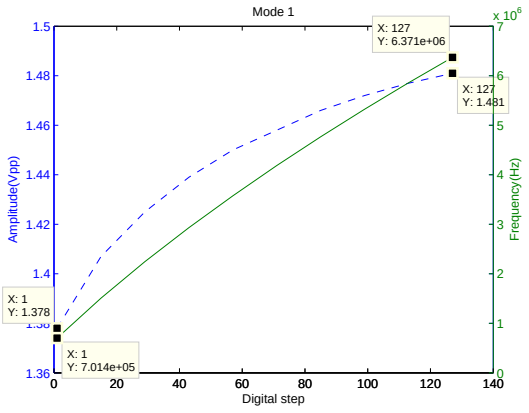
Figure 6.3: **Frequency ranges and amplitude variations for each operation mode**

(Amplitude plotted with dotted line with scale axis at left)

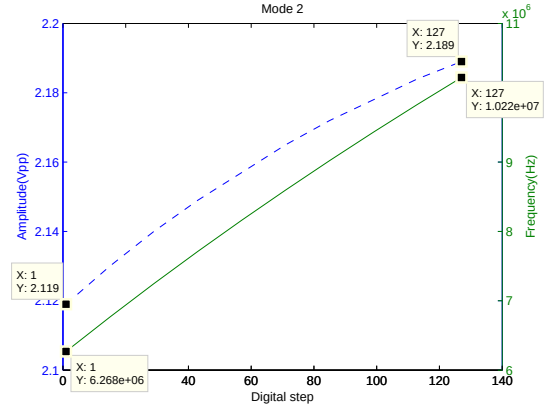
(a) Mode 0



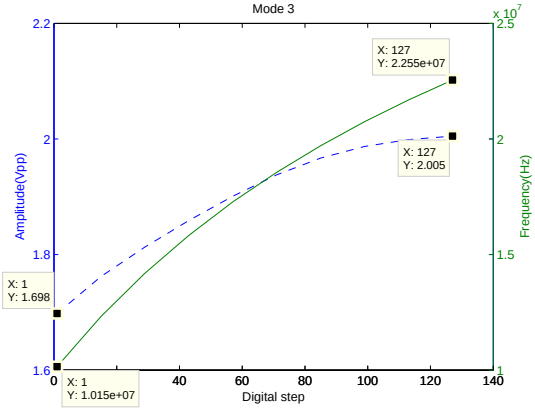
(b) Mode 1



(c) Mode 2



(d) Mode 3



The output of the digital current source is delivered to a *cpoly* capacitor of 548fF with a size of 36µm×17µm. A directional module directs the current charging or discharging the capacitor to allow the signal oscillation. A dual switch was included to decide between charging the capacitor to an initial voltage or performing normal operation. This decision signal, called RESTART, is one of the five control inputs of the integrated circuit.

The digital current source is the biggest module of the VCO having an area of 61µm×198µm. The transistor bank is composed of individual, identical PMOS transistors to minimize possible mismatch effects at the fabrication phase. The digital switch for current references commutes between an input reference and V_{DD} to assure that unused transistors remain shut-down.

The figure Figure 6.4 illustrates the physical layout of the digitally controlled current source developed using cadence. The figure shows the basic building blocks that includes from bottom up: decoder, offset transistors, fixed current sources (references), current output pin, transistor bank, digital switches and digital input pins.

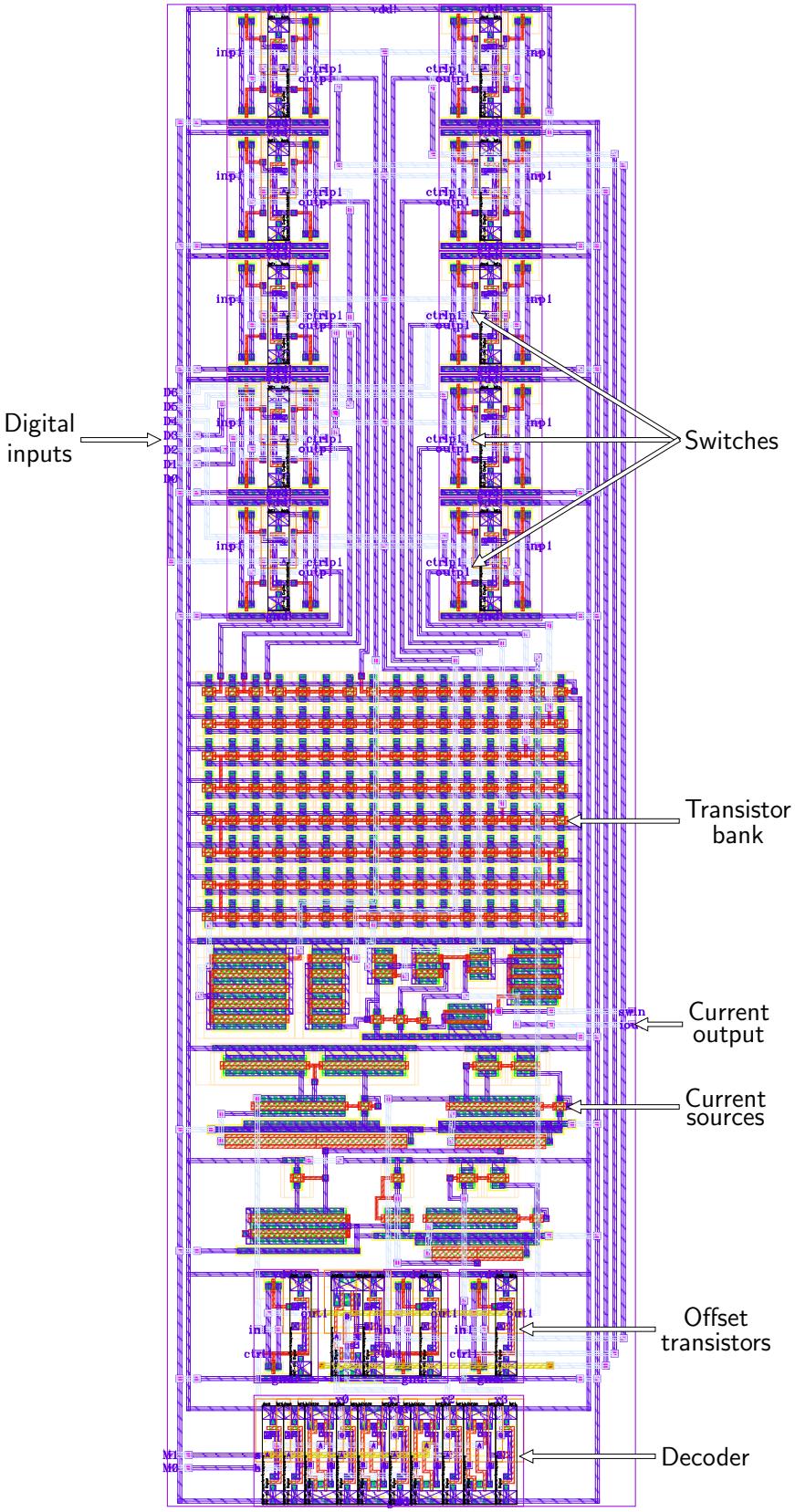


Figure 6.4: **Layout of the digitally controlled current source**

6.2 Digital Dual Switch

Two kinds of switches were implemented for the commutation in the blocks of the multi-channel sine generator. One type switches between two different inputs, the other commutes between one value and V_{DD} used to turn-off PMOS transistors. Both digital switches consist of two CMOS switches connected in parallel but with their terminals reversed. Figure 6.5 shows their electric diagram.

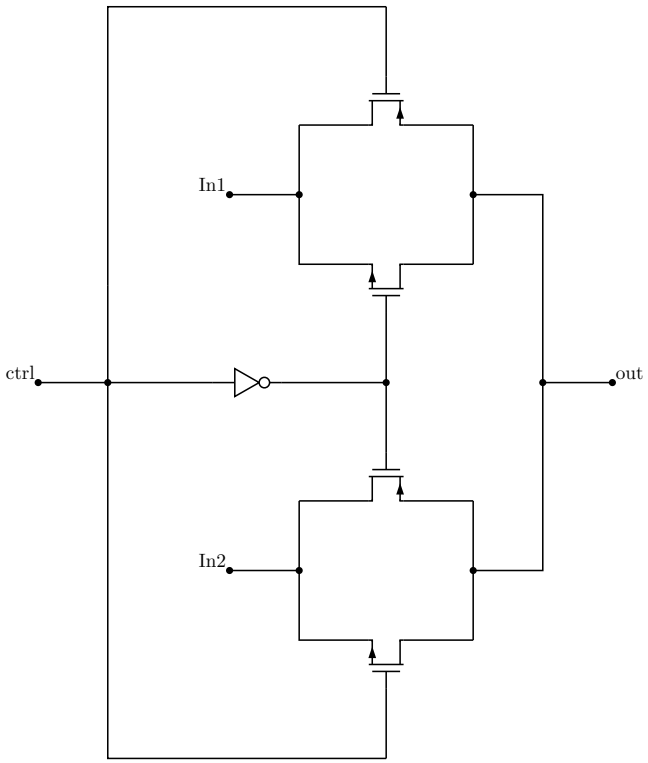


Figure 6.5: **Dual switch**

The switch uses an area of 14µm×16µm and presents an equivalent resistance between 2k to 8k as shown in Figure 6.7. The inverter gate included the INV0 switch selected from the standard CMOS digital library CORELIB due to its small area and because the required fanout in this case is only two transistors. The switches are used to perform configuration tasks so, no special frequency requirements are required. Since the current levels needed by components connected by the switches are very low, no special drivers are needed to turn on modules. The layout of the switch is given in Figure 6.6.

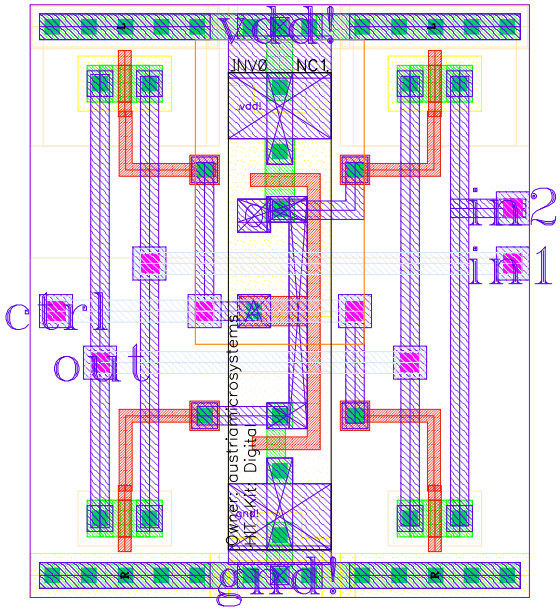


Figure 6.6: **Layout of the digital switch**

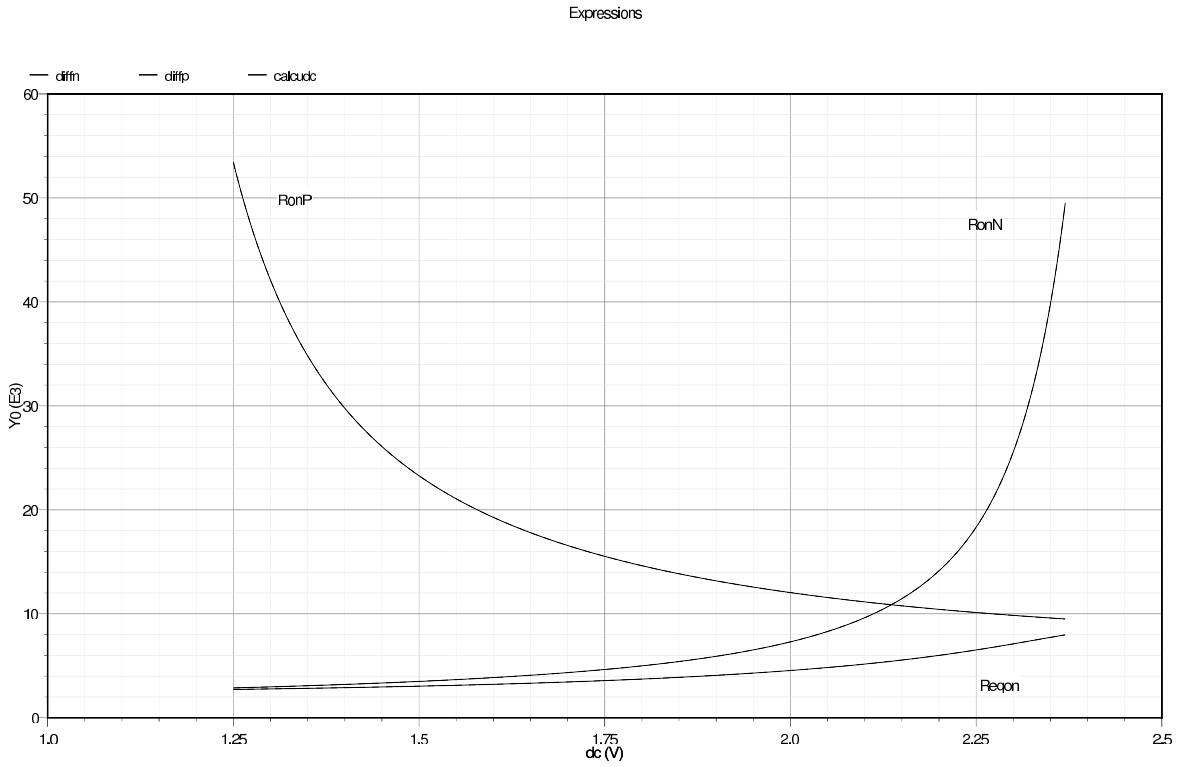


Figure 6.7: **On-resistance of one CMOS switch**

6.3 Comparator

The current from the digital current source charges and discharges the capacitor sequentially. This alternation is done comparing the level of charge in the capacitor against two limits (v_{TH} =1.8V and v_{TL} =1.4V) set by a voltage divider implemented with individual *rpolyh* resistors for matching considerations.

Figure 6.8 shows the comparator designed which follows the topology and design considerations suggested by Allen [75] for open loop architectures. The specifications of maximum operating frequency and minimum chip space were used to synthesize the device.

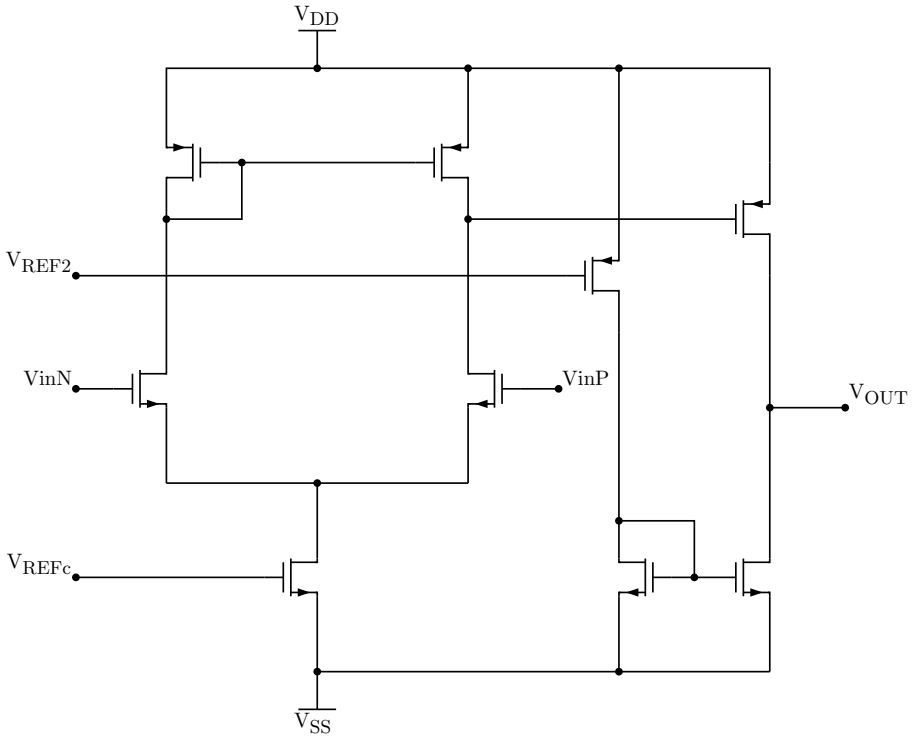


Figure 6.8: **Electric circuit of comparator**

The Figure 6.9 shows the comparator connected as a Schmitt-Trigger device (closed loop hysteresis circuit) to provide the required threshold levels at the capacitor charge and discharge cycles. Table 6.3 summarizes the electrical characteristics of this implementation.

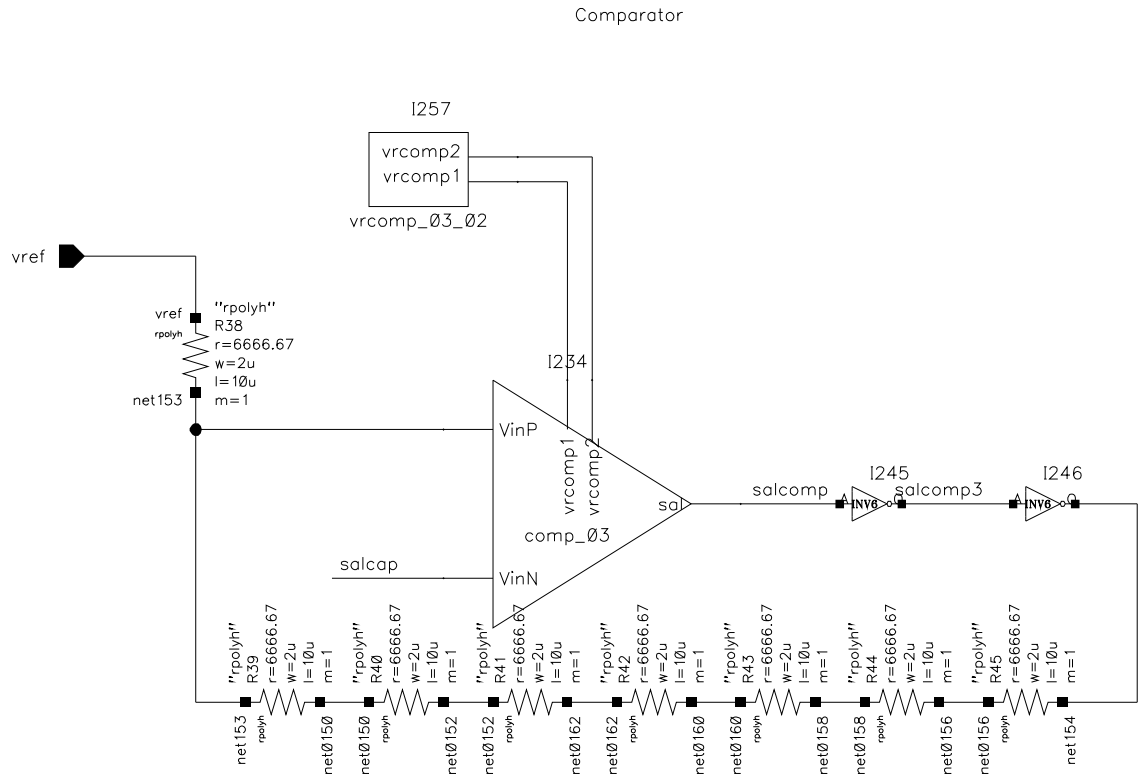


Figure 6.9: **Comparison module**

Table 6.3: **Electrical characteristics of comparator**

Parameter	Value
Offset voltage at input	1.098mV
Rise time	6.44ns
Fall time	4.13ns
Output range	1.97nV - 3.14V [a]
Max. Dissipated power	5.5mW
On-chip size	50.5μm × 27.2μm[b]
	28.4μm × 17.1μm [c]

[a] from a pulse from 0 to 3.3V at the input
[b] Size of comparator
[c] Size of voltage references

A fast transition time must be assured to accomplish with the higher frequency specification, the comparator must switch in less than 40ns (achieving a switching speed of 25MHz), in Figure 6.10 and Table 6.4 we can see that this specification is fulfilled without a problem.

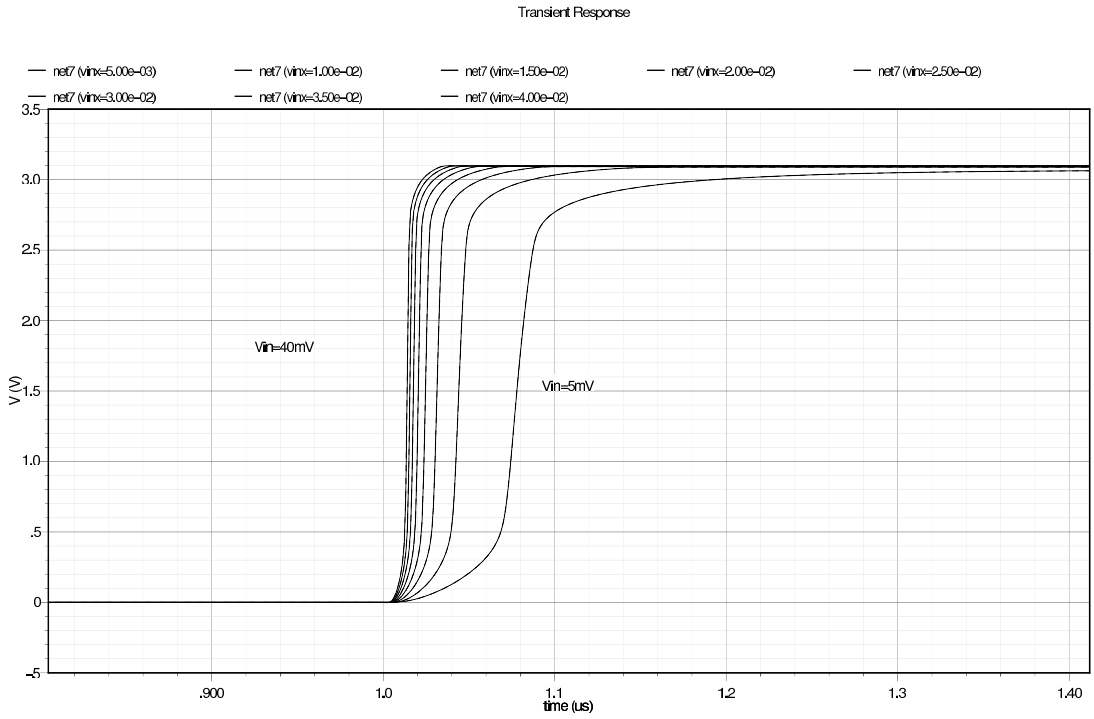


Figure 6.10: **Delay time in comparator for different input voltages**

Table 6.4: **Delay time of comparator**

Input voltage (mV)	Delay time (ns)
5	79
10	45
15	30
20	25
25	20
30	17
35	16.5
40	15.5

Note that in the comparison circuit (shown in Figure Figure 6.9) the voltage references are placed outside the comparator. This measure allows to fit them into empty spaces in the whole layout. Figure 6.11 shows the Schmitt-Trigger layout. The hole comparator includes a voltage divider implemented using individual *rpolyh* resistors (not shown in the figure). The resistors provide good matching and set the comparison level voltages v_{TH} and v_{TL}.

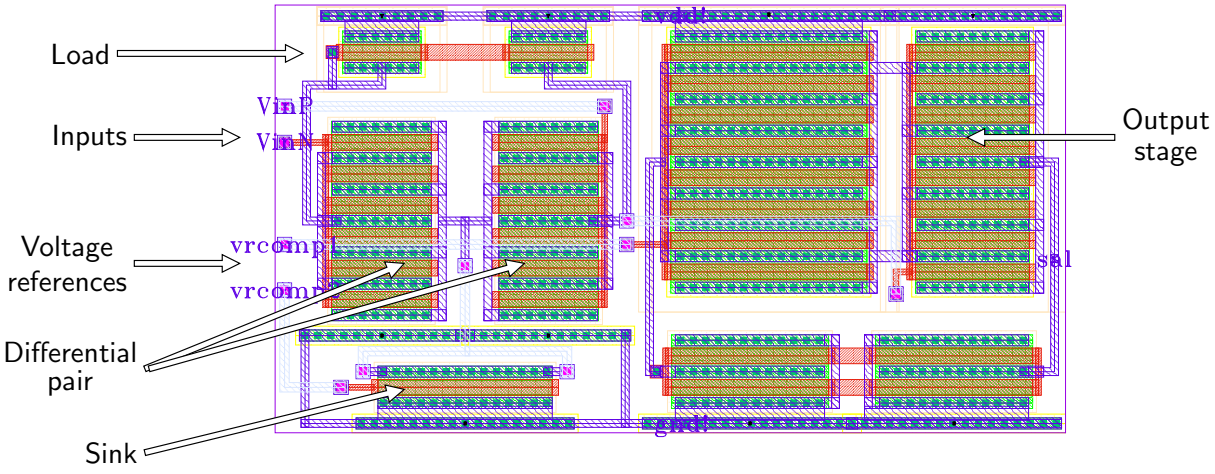


Figure 6.11: **Layout of the comparator**

6.4 THD Control

The differential pair presents inherent static and dynamic non-linearities that lead to complex phenomena. The amount of distortion is a function of frequency. In order to minimize the distortion produced by these side effects, the TSC block was optimized with another current DAC of 32 levels keeping the THD below of 5.11%. The THS control is shown in Figure 6.12. The THD is controlled by a variation in the level of the biasing current of the differential pair.

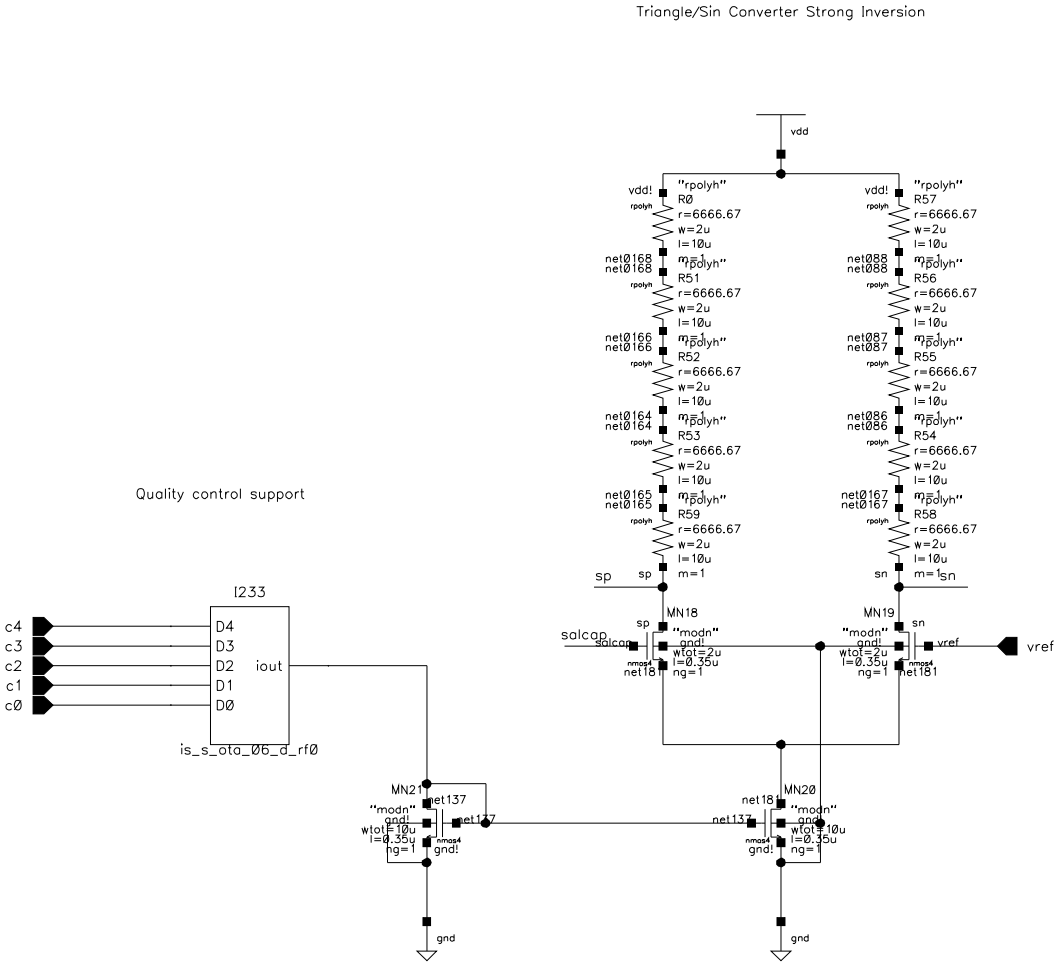


Figure 6.12: **Differential pair and and THD control current source**

Observe that the variation of the quality current certainly diminishes the amount of THD but also alters the amplitude and at lesser degree the frequency of the output signal. Refer to Figure 3.8c to observe the effect of changing the bias current of the differential pair over the output waveform. As an example of THD control, we can see in Figure 6.13 the variations of amplitude, frequency and THD presented by a sine wave of 20kHz when the digital THD control is applied.

The quality control source presents a very good linearity in the whole range of

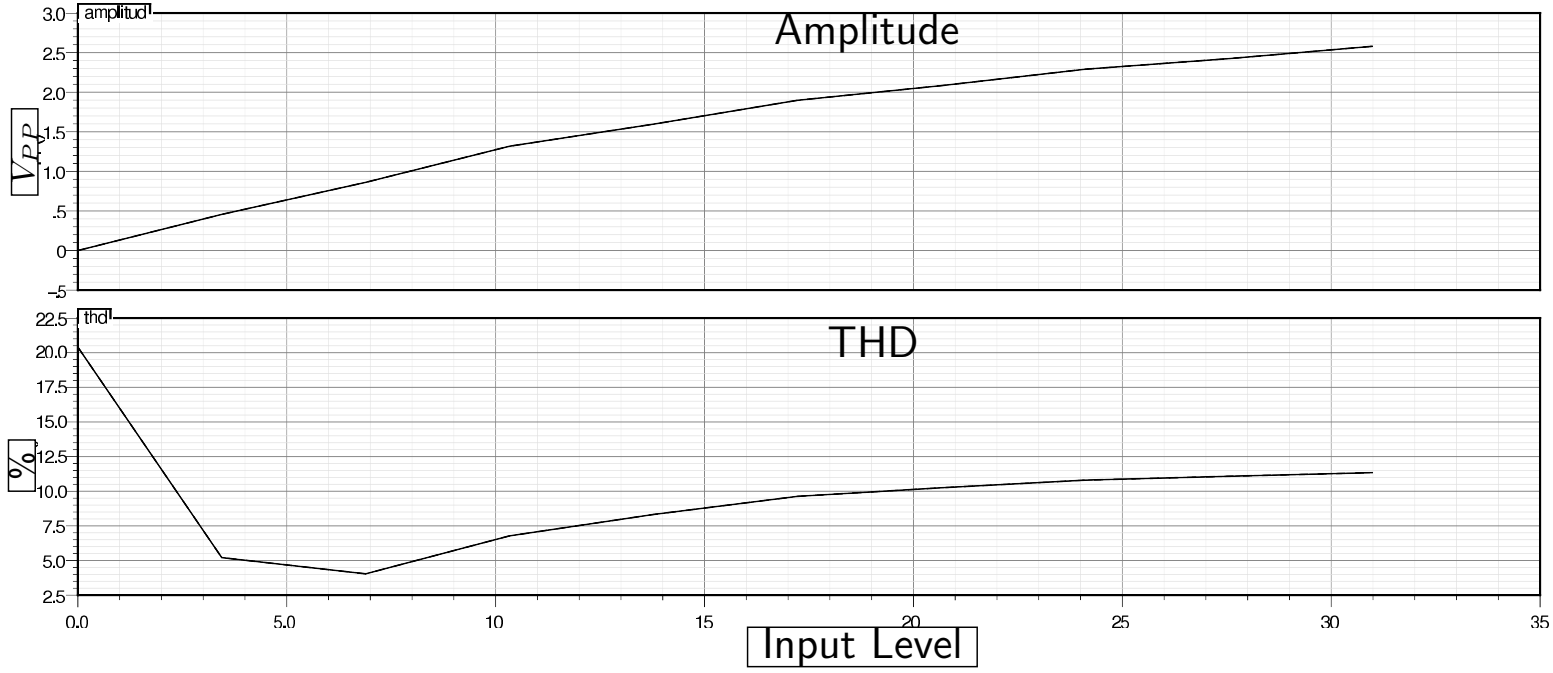


Figure 6.13: **Function of the THD control**

current (from 0 to 6µA). The THD control block that uses a single current source, implemented in a similar way that the digitally controlled current source. The current source of the THD control requires 46µm×70µm of IC space. The layout of the THD control is shown in Figure 6.14.

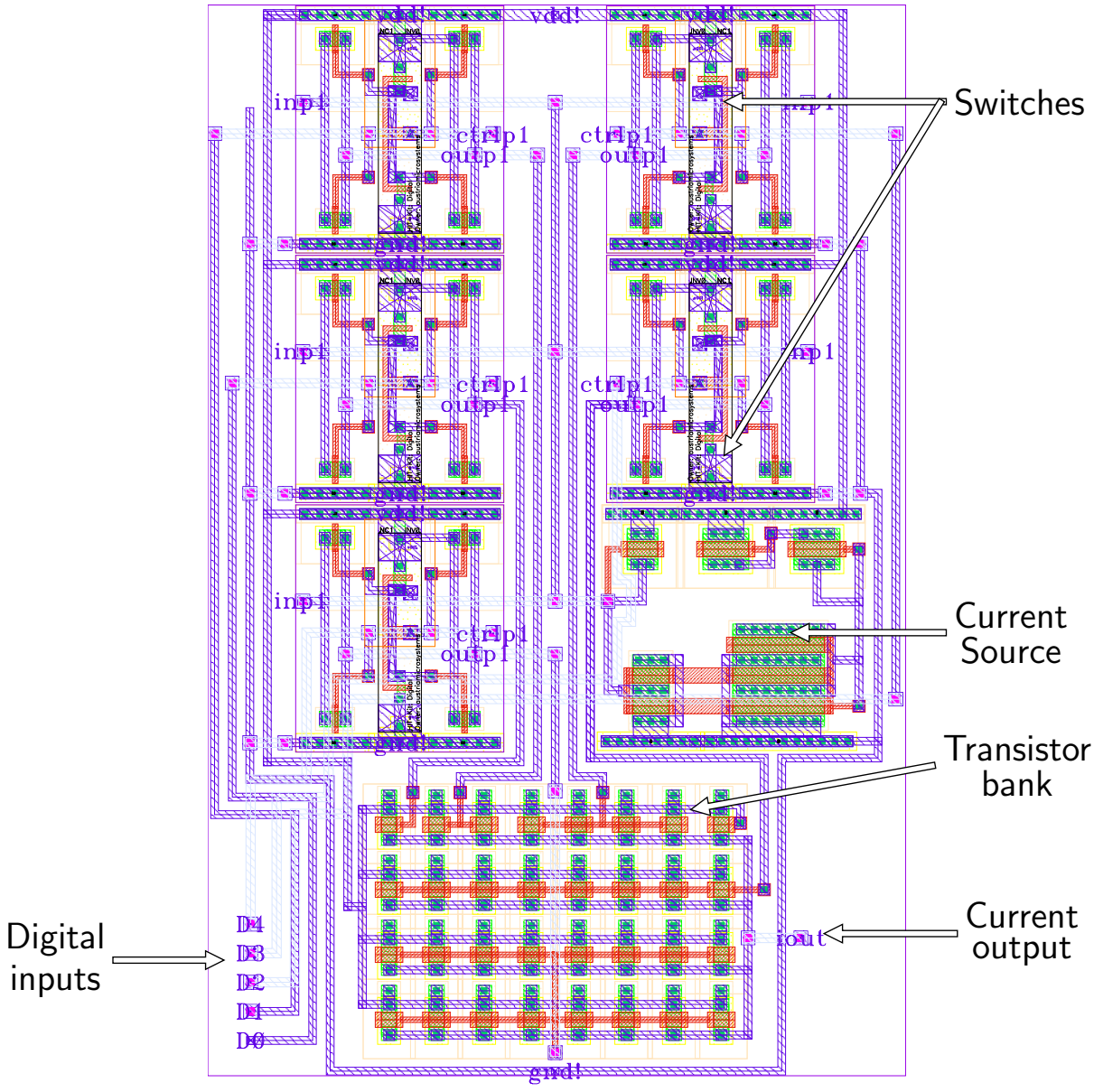


Figure 6.14: **Layout of the THD control**

6.5 Operational Amplifier

The differential voltage is now converted to a single mode signal by means of a subtraction stage implemented by an OpAmp. This component is designed according to Allen/Holberg method for the classical two-stage operational amplifier [75], its electric diagram is depicted in Figure 6.15 and its electric characteristics are summarized in Table 6.5. This operational amplifier is used in two blocks of the final system: in the differential to single ended circuit and the amplitude control system.

In the process to design the operational amplifier there were three important aspects to consider:

Size. Since each oscillator will have two OpAmps (differential to single ended and amplitude control system) the occupied space is a major concern. Therefore, the output transistors and the compensation capacitor must have a "moderate" magnitude (capacitor size: 17µm×22µm, output transistors 40µm×8µm).

Power. The highest current is found at the output transistors(1.1mA). Therefore, its magnitude must be under surveillance to avoid an excessive power dissipation.

Gain Bandwidth and High Slew Rate. These two parameters are the most important specifications and the most difficult to achieve due to the compromise with space, power and functionality; initially, the Gain Bandwidth product must be above 80MHz and the slew rate must be faster than 100V/µs[4]. The speed of response of the opamp must meet the transient characteristics of the waveform generator system in terms of frequency response and unit step response capabilities.

Table 6.5: **Electrical characteristics of OpAmp**

Parameter	Value
GBW	162.8MHz
Phase Margin	58.96°
Gain	51.44dB
Slew Rate	163V/μs
Open loop output resistance	68.55kΩ
CMRR	49.59 dB
PSRR (0Hz)	76.82dB
ICMR	-0.5V $\sim$ +1.3V
Max. Output Swing	49.24mV $\sim$ 3.1686V
Max. Dissipated power	3.354mW
On-chip size	45.7μm × 45.9μm[a]
	23.4μm × 15.2μm [b]

[a]Size of OpAmp
[b]Size of voltage reference

[4]Values needed to accomplish with the required frequency range.

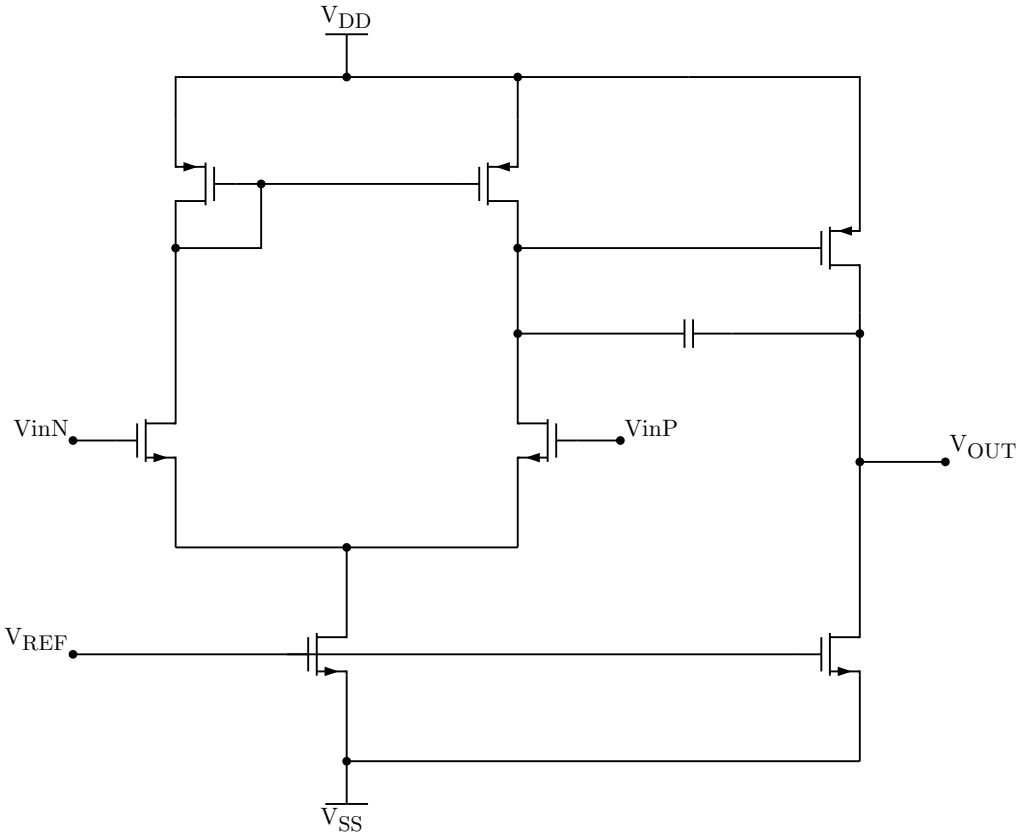


Figure 6.15: **Circuit of implemented OpAmp**

The next figures illustrate the electrical characteristics of the designed opamp. The step response (Figure 6.16) provides a slew-rate of 163V/μs, The PSRR (Figure Figure 6.17) shows a 76.82dB at low frequencies, the obtained gain (Figure 6.18) is 51.4dB and the phase margin (Figure Figure 6.18) surpasses 58°. All those specifications are extremely good and go beyond the minimum requirements for the application. Still it is possible to gain some space and reduce the overall consumed power if some parameter meet the original parameters strictly.

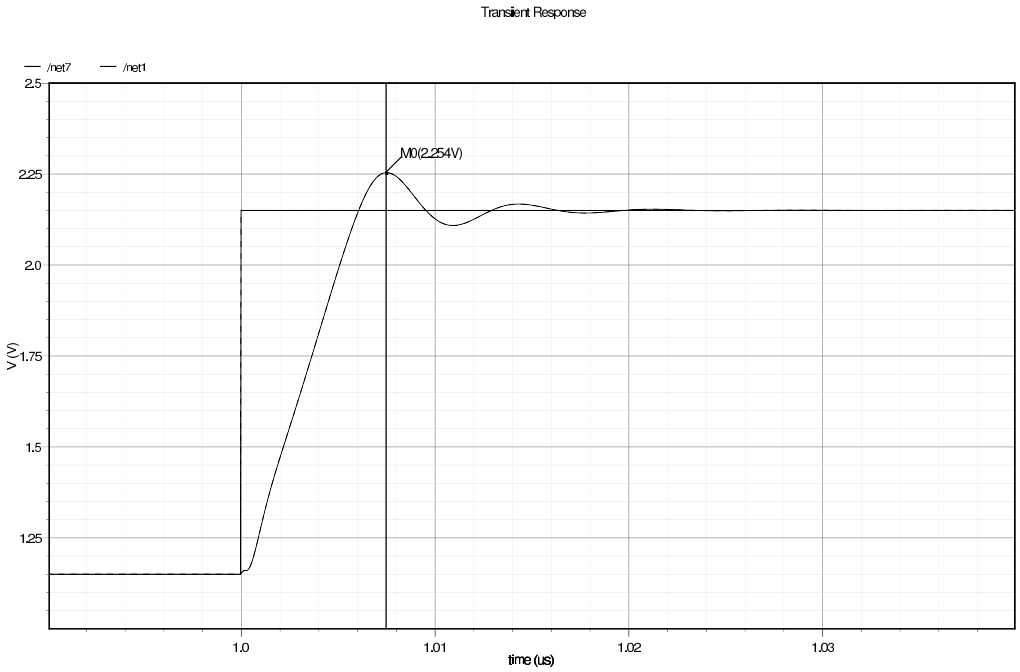


Figure 6.16: **Step response**

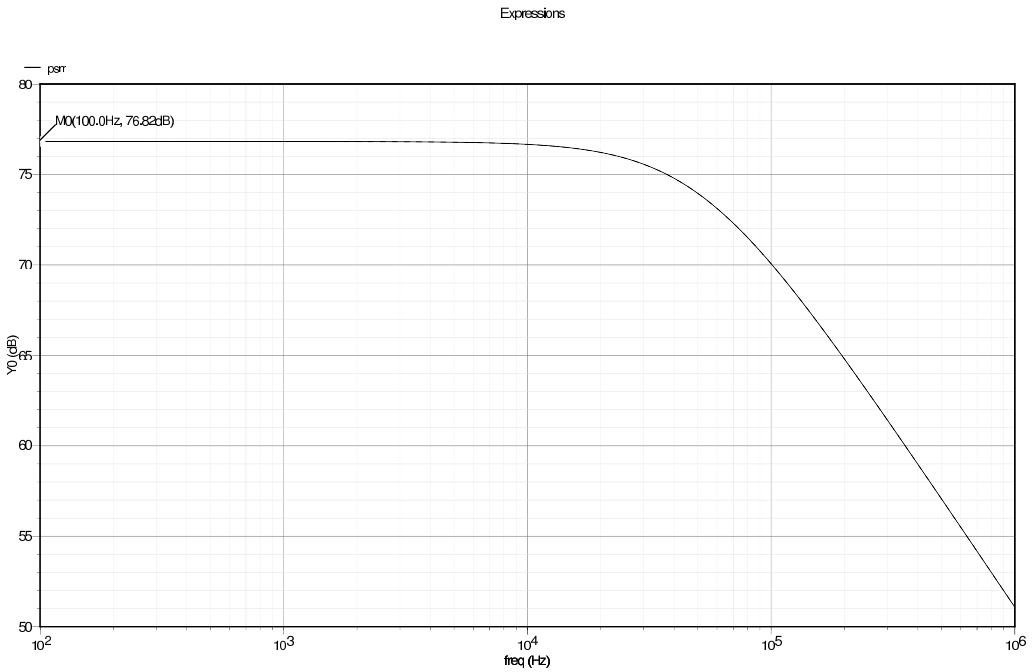


Figure 6.17: **Power Source Rejection Ratio (PSRR)**

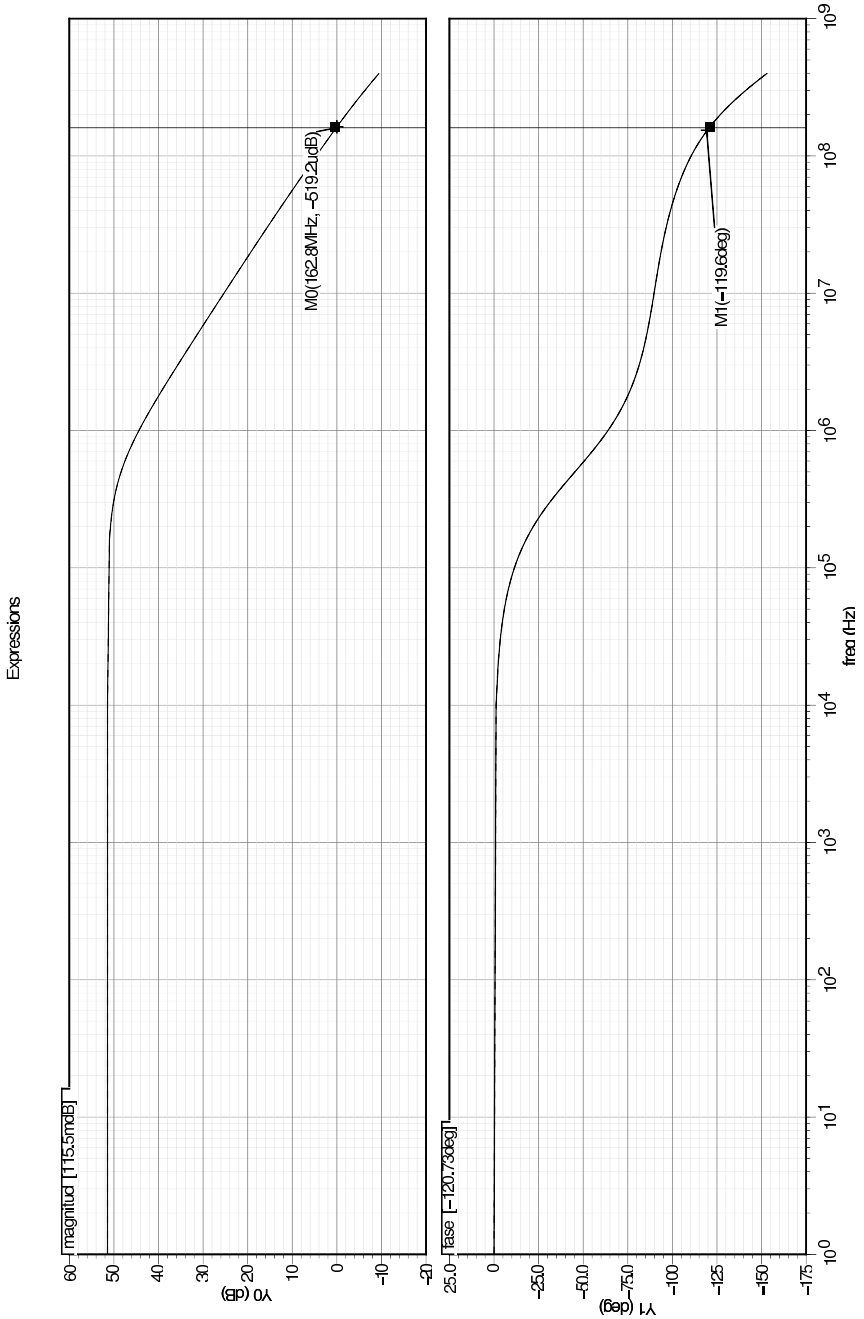


Figure 6.18: **Bandwidth and Phase**

Figure 6.19 shows the opamp's layout developed using the same modular fashion methodology as the comparator device. All voltage references are external to the device. The connection width of the output stage was increased due to the high current requirement for the device. Without including the voltage reference, the opamp size is 45.7µm×45.9µm.

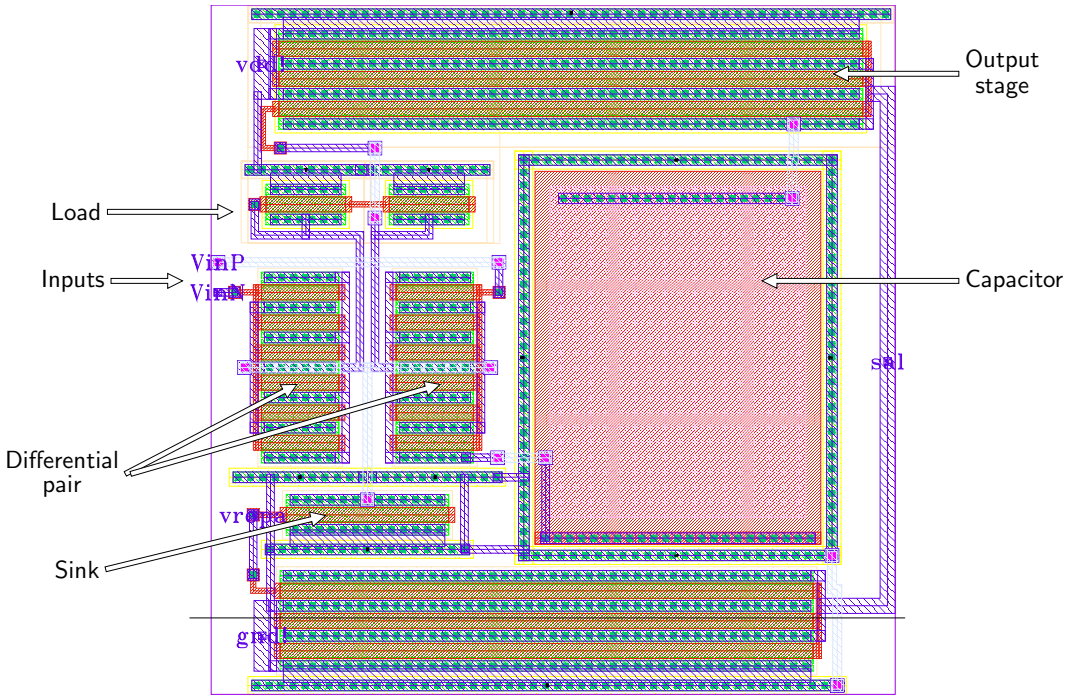


Figure 6.19: **Layout of the opamp**

6.6 Digital Gain Control.

The THD control produces changes in the signal's amplitude and two characteristics are needed in this module: digital control capability and programmable gain to provide good resolution at the entire frequency range.

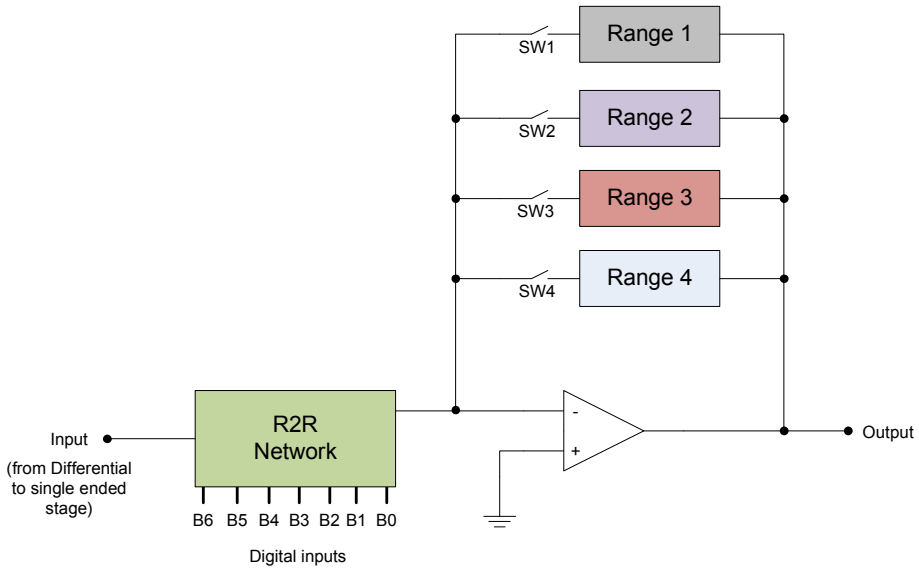


Figure 6.20: **Block diagram of the digital Gain Control module**

Figure 6.20 shows a block diagram of the digital gain control module which has 4 different ranges selected by a decoder using digital switches. For a given range, a R-2R network permits a fine selection of the output amplitude using the control inputs B6 to B0. Table 6.6 illustrates corresponding gain factors, power dissipation and device size.

Table 6.6: **Electrical characteristics of the Digital Gain Control.**

Mode	Gain
M0	2
M1	5
M2	8
M3	11

Max. Dissipated power	3.457mW
On-chip size	75.1μm × 152.45μm

Figure 6.20 illustrates a detailed layout picture of the digital gain control. The figure shows following a bottom-up description the opamp, decoder, gain resistors, gain switches, level switches and digital inputs respectively. The layout uses *rpolyh* with $W/L = 2\mu m/23\mu m$ which produce values of 15.33kΩ and it represents the second largest module having an area of 75.1µm×152.45µm.

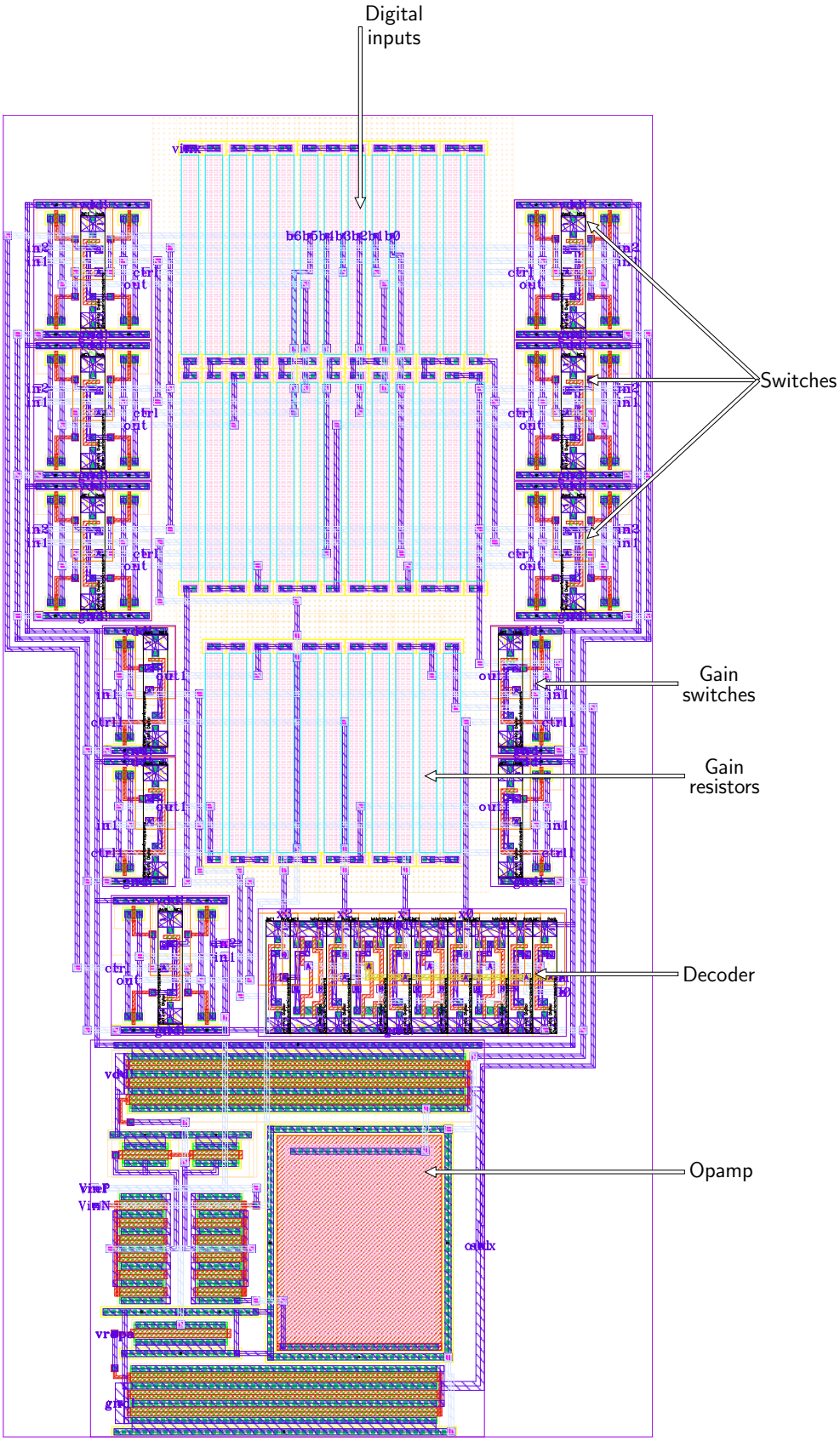


Figure 6.21: **Layout of the Digital gain control**

6.7 Simulation results

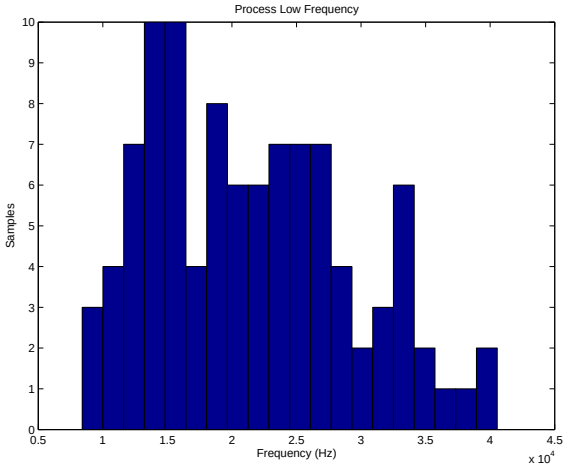
The final prototype was submitted to the same set of tests as described early for the VCO devices. Table 6.7 and 6.22 illustrate the results of the Monte Carlo simulation for the final prototype. Those results show no failure in 100 tests and the mismatch model at low frequency fits the results obtained by the IC implementation. At high frequency the operating range provides an excellent operation of the prototype considering both the process and mismatch models. Moreover, the Figure 6.23 shows the corner analysis whose the first three corners are illustrated. This analysis gets 8-75kHz for the lower frequency limit, and 14-37MHz (corner4 and corner5, respectively) for the upper frequency limits. With these results we can see that the proposed VCO performs according to initial requirements and its implementation on IC is viable.

Table 6.7: **Monte Carlo Results for the final implementation**

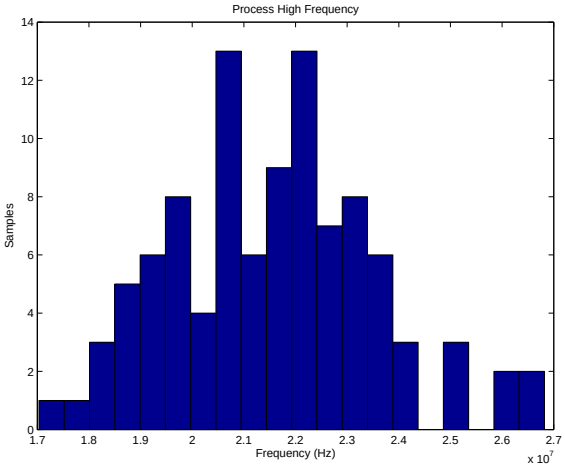
	Low Frequency (kHz)				High Frequency (MHz)		
Measurement	P&M	Mismatch	Process		P&M	Mismatch	Process
Media	21.7	20.9	21.4		21.4	21.4	21.5
Range	4 - 75	8 - 51	9 - 40		18 - 26	20.6 - 22	17 - 27
Mode	15(10)	18(20)	16(10)		19.5(11)	21(13)	20(13)

Figure 6.22: **Monte Carlo Results in Low and High Frequency for the final design**

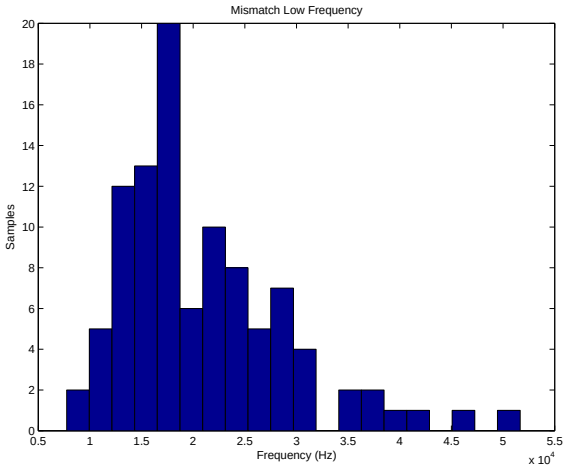
(a) Process L.F.



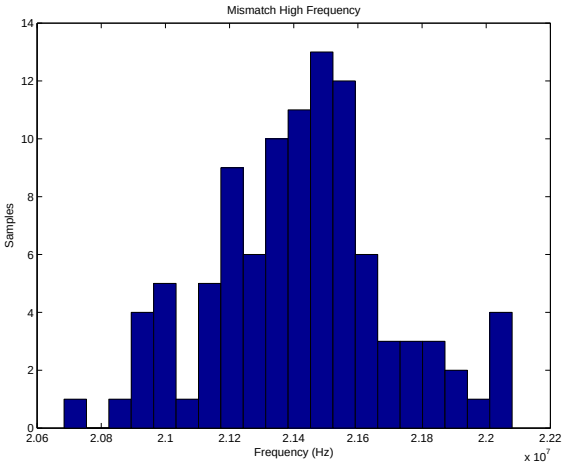
(b) Process H.F.



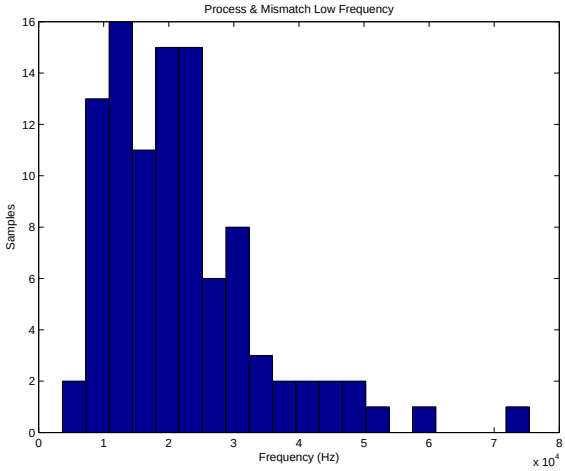
(c) Mismatch L.F.



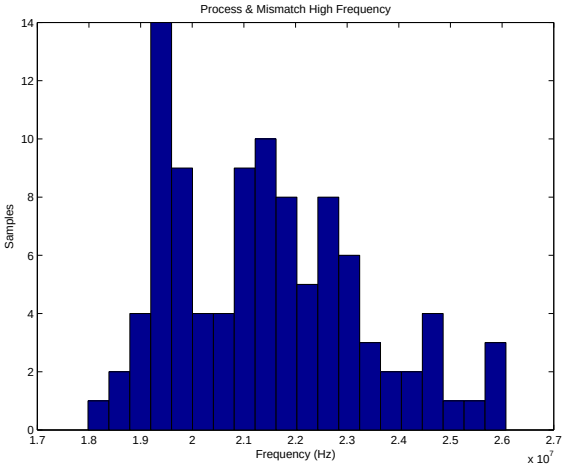
(d) Mismatch H.F.

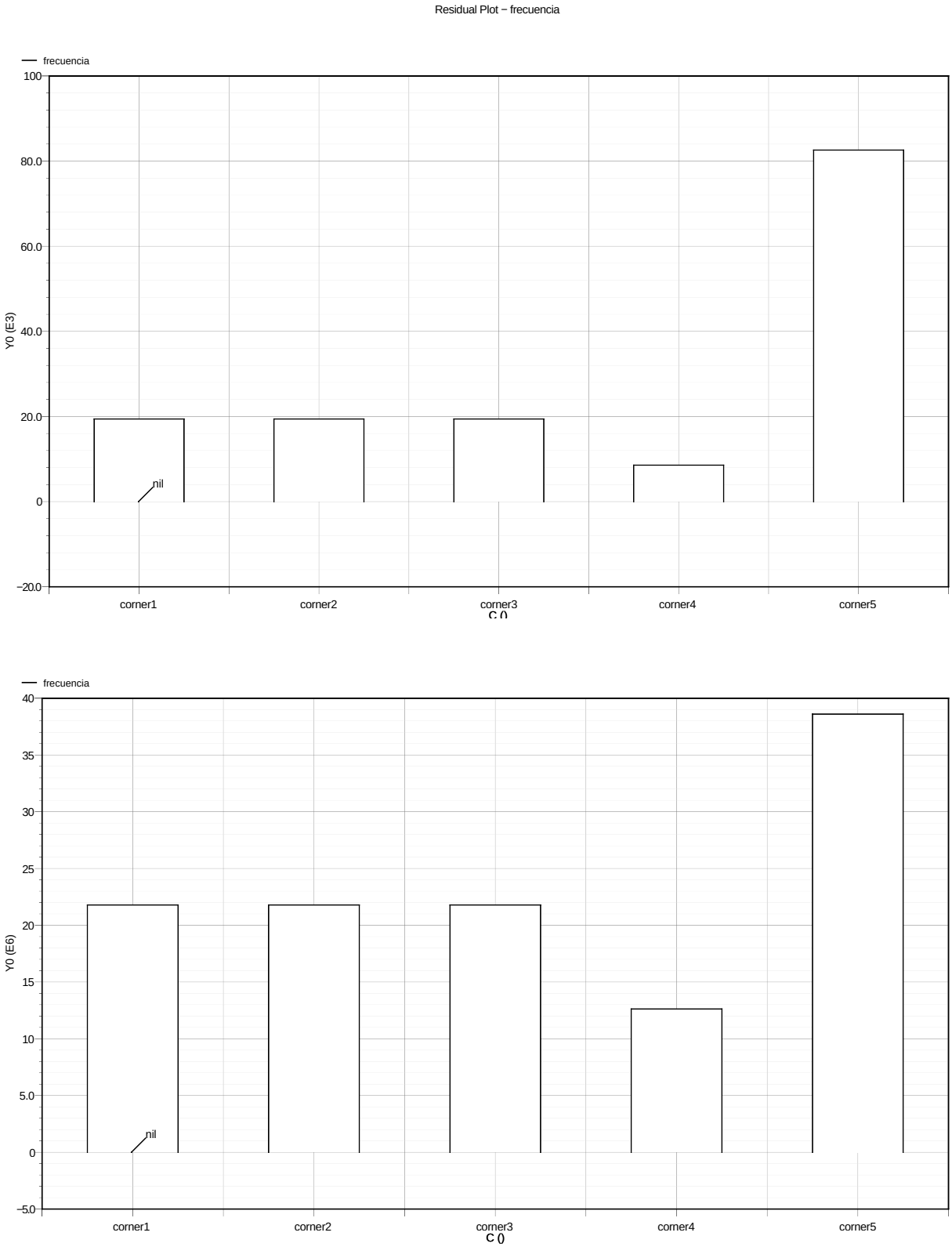


(e) Process & Mismatch L.F.



(f) Process & Mismatch H.F.





(b) Corner analysis in high frequency (20MHz)

Figure 6.23: **Corner Analysis results, final design**

6.8 Digital Control Interface

The digital control interface manages and distributes the incoming data for the VCO system. This interface programs the desired frequency, amplitude and distortion level of the output signal of each VCO. A 23-bit word is required to program one oscillator.

Using serial programming it is possible to cascade a number of oscillators in the same integrated circuit without the need of modifying the interface. Moreover it is possible to chain other IC's containing multichannel generators if necessary. The block diagram of the interface is shown in Figure 6.24.

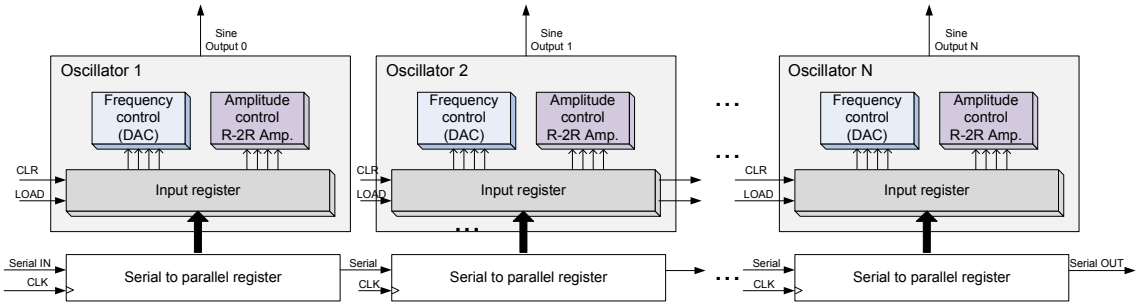


Figure 6.24: **Block diagram of the Digital control interface**

The programming word is organized as depicted in Figure 6.25. The most significant bits configure the change in frequency, then two bits select the frequency range, the following five bits adjust the distortion of the obtained waveform, the next six bits set the amplitude of the sine wave, and finally the last two bits configure the gain mode.

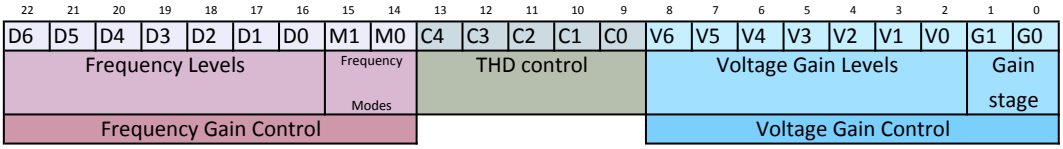


Figure 6.25: **Programming word**

The digital module was synthesized using Encounter(R) RTL, using the library c35CORELIB 2.21 [68]. The design uses 47 gates, requires an area of 186µm×117µm, dissipates 780.4µW, and provides a maximum fanout of 46 clock signals.

The obtained verilog file was processed to get the layout scheme in size and form. Figure 6.26 shows the layout scheme once it was placed on top of the analog layout.

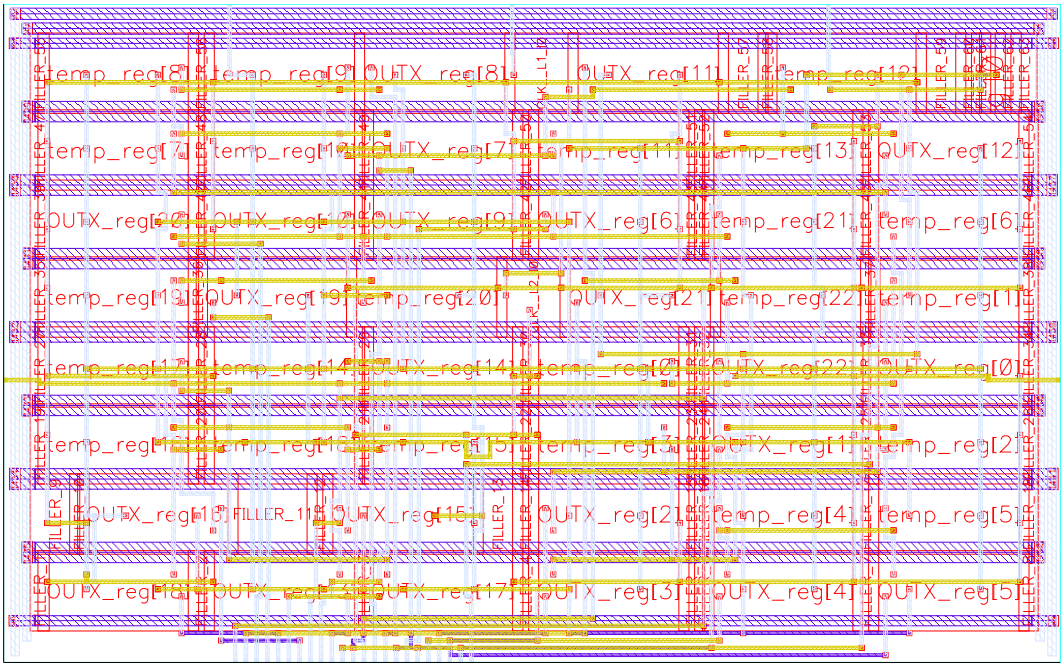


Figure 6.26: **Generated layout for the digital module**

Figure 6.27 shows the complete layout of the VCO system. The figure illustrates from bottom up all subsystems as follows: comparator resistors (voltage divider), voltage references, sine output terminal, triangle to sine converter (TSC), oscillator capacitor, digital gain control, digital current source, THD control circuit, interconnection terminal, serial input (SI), serial output (SO), digital module and input pins. The entire cell area is 186µm×317µm with an estimated power dissipation of 15mW. The layout uses the following metal layers:

1. Metal 1 and Metal 2 (MET1 and MET2) for internal module wiring.
2. Metal 3 (MET3) for communication with other modules.
3. Metal 4 (MET4) for V_{DD} and GND connections.

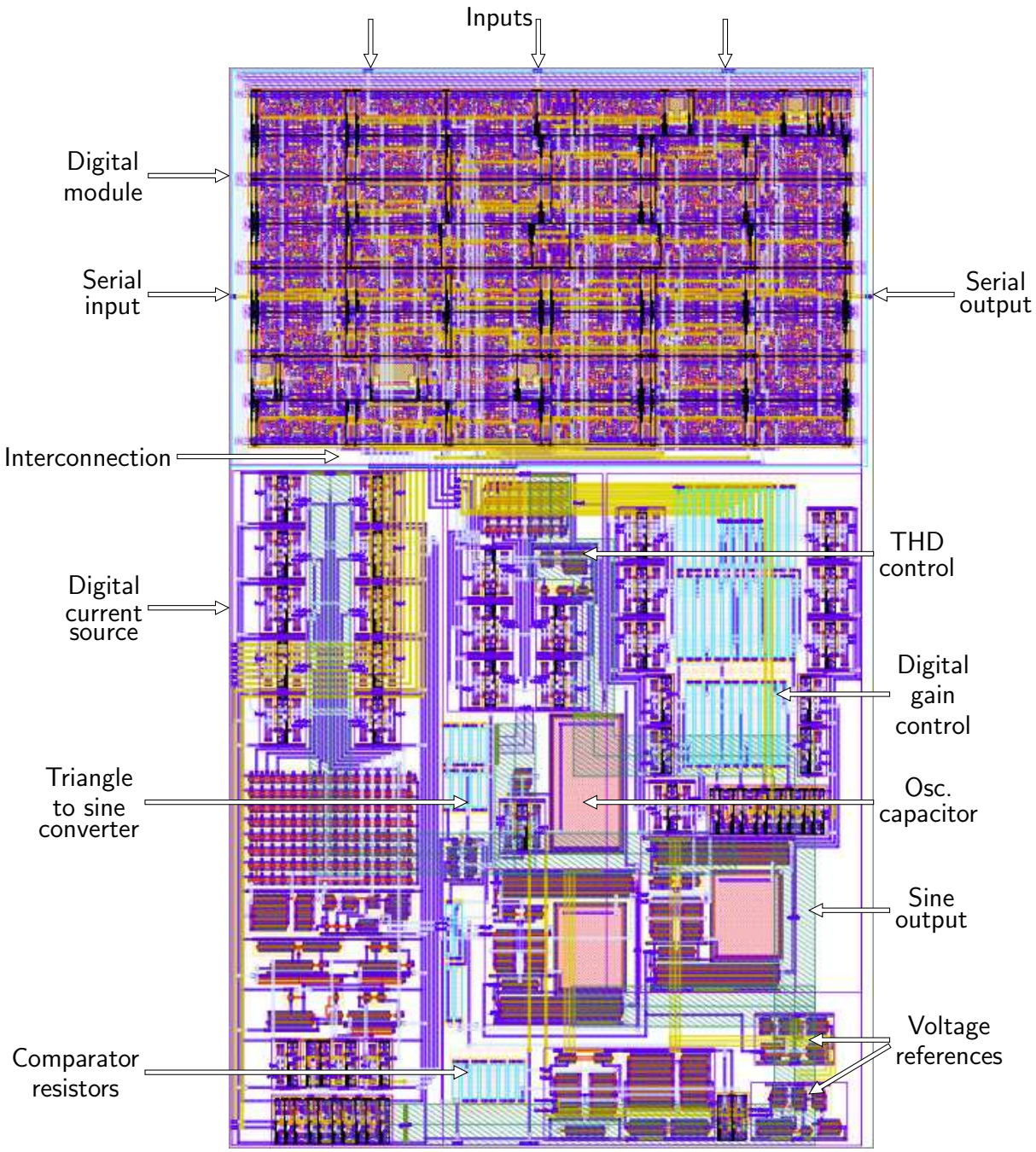


Figure 6.27: **Layout of the complete VCO**

6.9 Integration of the complete system

The final multi-channel sine generator system consists of sixteen identical oscillators, connected in a serial fashion. The 23 bits of the programming word is passed from one VCO to another until the completion of 368 bits needed to program the whole system. The bitstream containing control words is received in the SI input, it is possible to chain another multi-channel generator ASIC using the SO output. The data transmission is synchronized by a clock signal CLK. When the programming word is passed to all the input registers, a LOAD pulse delivers the data to the blocks of each oscillator. A RESET signal erases the input registers while a pulse in RESTART charges the capacitors to an initial state. The signals CLK, LOAD, RESET and RESTART are delivered simultaneously to all oscillators (Figure 6.24).

The Figure 6.28 shows the complete layout of the multi-channel sine generator. The layout consist of: main core formed by 16 VCO's, sine output pins(top, bottom, middle right), digital control signal pins (middle-left) and analog power input pins (middle-right). The layout measures 810µm×1310µm and 1.5cm×2cm, without and with pads respectively. Finally, the following use of special purpose pins were used:

1. Digital signals, control inputs/outputs, ICP
2. Digital power voltage 3.3V, pin VDD3ALLP
3. Digital ground, pin GND3ALLP
4. Analog input/output, pin APRIOP
5. Analog power voltage 3.3V, pin AVDD3ALLP
6. Analog Ground, pin AGND3ALLP

The final layout measures 810µm×1310µm, with the addition of the pads the size increased to 1.5cm×2cm. The digital signals (control inputs/outputs and alimentation) were placed at the left, the used input/output pin was the ICP, the 3.3V source for the digital modules was connected through a VDD3ALLP pin, for the digital ground the used pin was GND3ALLP. For the analog inputs/outputs the used pin was APRIOP, the used pin for the 3.3V source was AVDD3ALLP and for the analog ground AGND3ALLP. The layout of the complete system is shown in Figure 6.28.

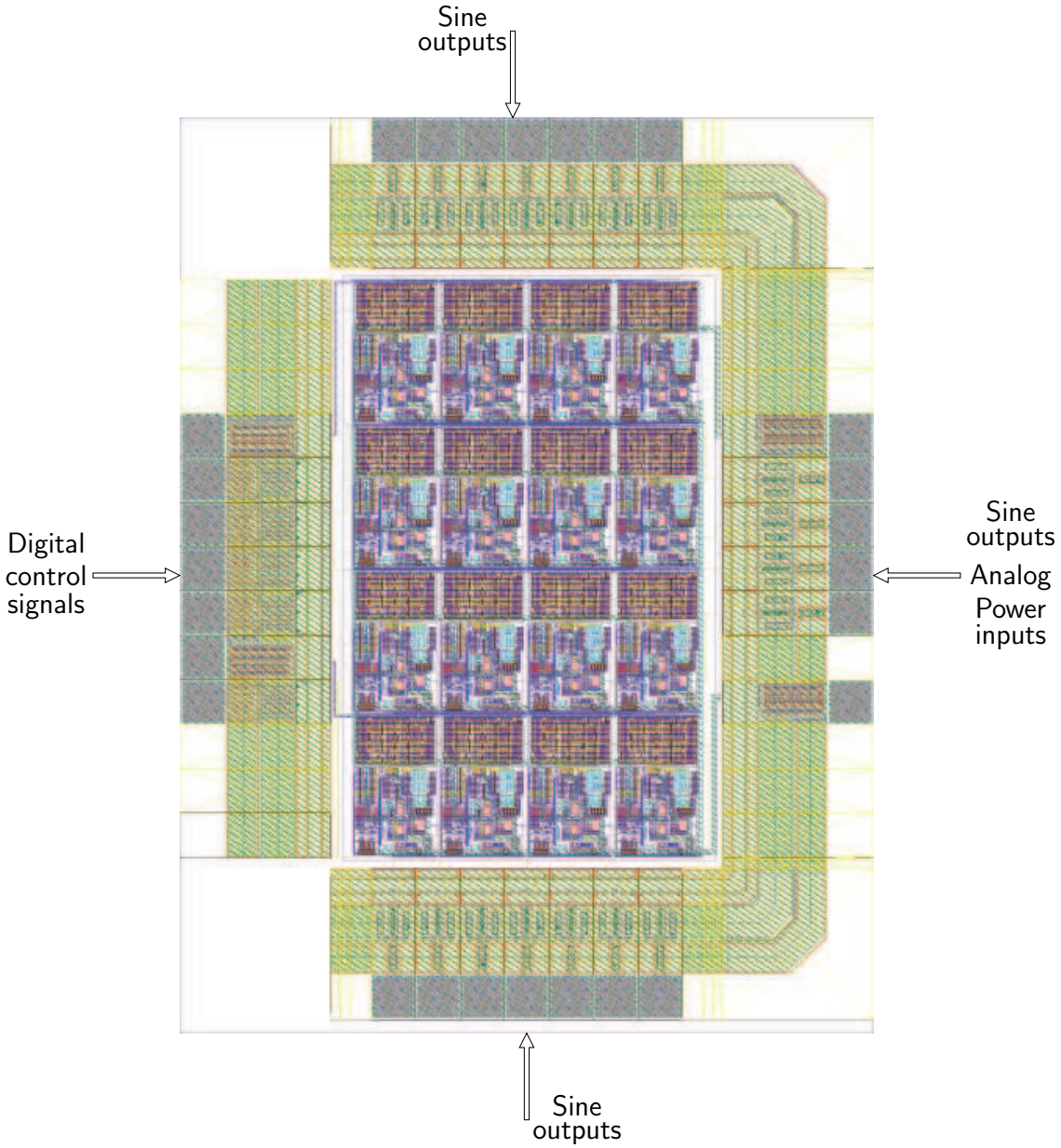


Figure 6.28: **Complete layout of the multi-channel sine generator**

6.10 Interface Card

The connection between the integrated circuit and the microfluidic platform is made through an interface card. The PCB (shown in Figure 6.30) is used to test the multi-channel generator, the protocol programming and the extension of voltage ranges.

6.10.1 Power supply

The board is fed with an input voltage of ±15V, the positive voltage feeds four voltage sources, 3.3V for analog devices, 3.3V for digital devices, 1.2V needed by an FPGA, and 1.65V needed by the multi-channel generator IC.

6.10.2 Digital stage

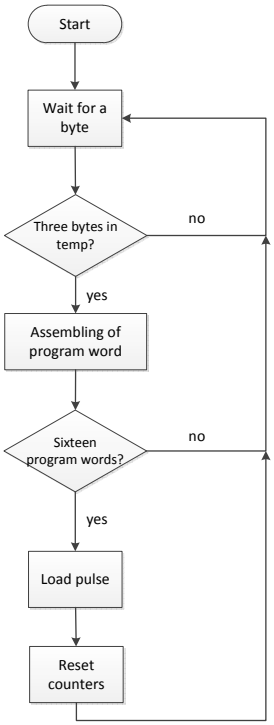


Figure 6.29: **Flow diagram for the actions performed by the FPGA**

The XC3S50AN Spartan FPGA (Xilinx) running at 50MHz performs the digital tasks. The card has a JTAG connector to program the FPGA. Once programmed, the FPGA can work independently without the need of a computer thanks to its 1Mbit nonvolatile flash. The FPGA performs the actions depicted in the flow diagram of Figure 6.29.
The system rests in stand-by until a byte arrives in the RS-232 port and get back to the wait stage until another two bytes have arrived. Three bytes are assembled to conform the programming word for one oscillation unit. When the programming word is complete it is placed in a shift register until the 16 programming words have been arrived and placed in the shift register. Then the transfer to the ASIC begins at 9600 bps and a pulse of LOAD is sent at the end of the transmission to deliver the data at the multi-channel sine generator.
A general purpose 12-bit port was left to provide flexibility in the connection of peripheral devices. Four leds are available for signaling. The card has a serial port to provide communication with a computer performing the programming of stimulation protocols. A supplementary port to configure an external generator mounted in a LOC was also included. The interface card include test points to help in the electric testing of the prototype IC.

6.10.3 Analog output stage

Several electrokinetic tasks make use of voltages above 3.3V, for such reason, the sixteen outputs of the system are amplified with LM6172 low-power, low-distortion opamps connected as non-inverter configurations. It is planned that subsequent versions of the multi-channel sine generator have internal amplifiers in order to reach to higher output voltages. This improvement would require the use of a dedicated high voltage technology supporting at least 20V.

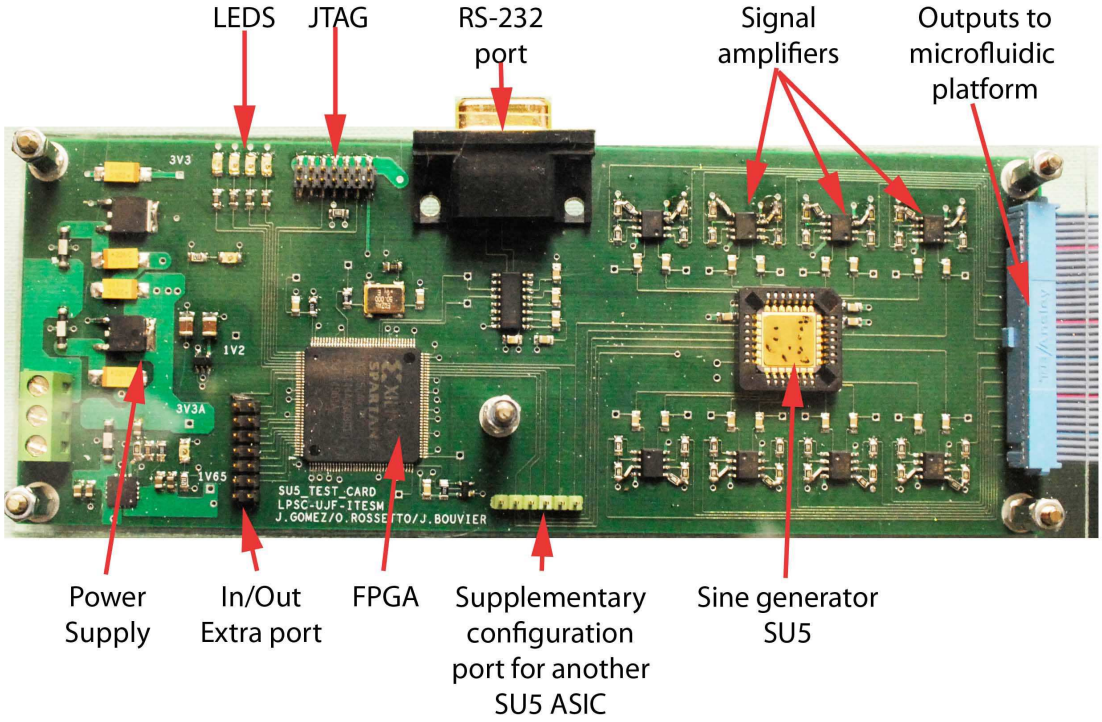


Figure 6.30: **Blocks of the interface board**

6.11 Graphic Interface

The graphic advantages of LabView offer an easy way to configure each oscillator unit. The program collects the setup information for each generator and sends 96 bytes via RS-232 port at 9600 bps. The user may choose the amplitude, frequency, amplitude/frequency ranges and the THD correction for each signal generator.

The Figure 6.31 shows a capture of the oscilloscope screen displaying the output waveforms of four channels. The frequencies of signals were configured between 500kHz and 1.8 MHz, with different values of THD correction. The amplitude was set in 8.8 V_{PP}. The frequency and amplitude of the observed waveforms were consistent to the programming word sent to the IC.

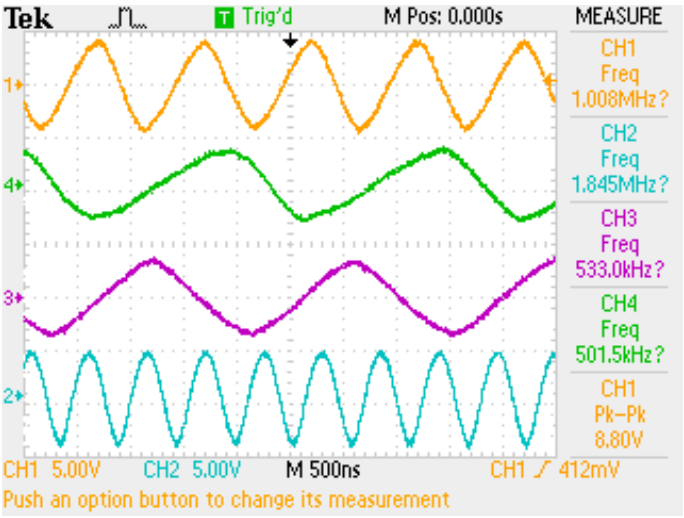


Figure 6.31: **Obtained waveforms as seen in the oscilloscope**

The screen of one configuration screen is depicted in Figure 6.32, in this figure we can see the dedicated controls for each variable (frequency and amplitude levels, ranges for frequency and amplitude and THD control). The interface allows for the manual input of level to make quick changes. The complete interface is shown in Figure 6.33 including the sixteen interfaces to make changes in all the generators.

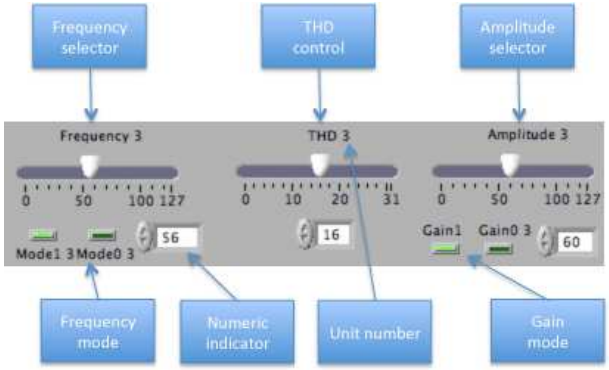


Figure 6.32: **Configuration module for one oscillator unit**

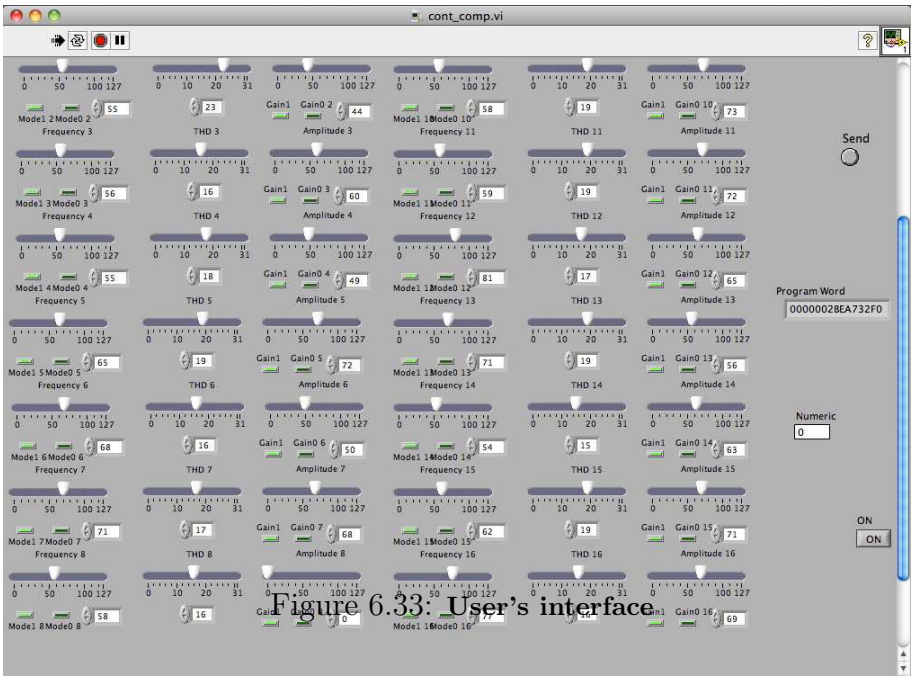


Figure 6.33: **User's interface**

6.12 Conclusion on the implementation

The Multi-channel generator integrated with the interface card programmed with the aforementioned interface, performed as expected. The frequency ranges of the generated waveforms were inside the expected bounds, in fact, the lower and upper limits extend a little bit further, to 7kHz and 22.5 MHz respectively. The system allow the individual programming and deactivation of each generator individually. With this capability, it is possibly to implement stimulation protocols. In a microfluidic application, this feature can be used to perform displacements, filtering, trapping or characterizations of a group of cells or particles simultaneously.

Chapter 7

Electrical Testing of the Stimulator and its Evaluation in Particle Separation

This chapter describes the operation of the multi-channel sine generator in dedicated experiments over microfluidic devices. The operation includes the validation of ranges and electric characteristics relevant to the specific application experiments. The measurements were performed using a Tektronix TDS2004B Digital Storage oscilloscope and the post-processing analysis was performed with MATLAB.

The multi-generator system integrates part of the microfluidic particle separation platform. Experiments were carried out to demonstrate the functionality of the multi-channel generator in its real scenario. The materials, methods and test results are reviewed and analyzed in this chapter.

7.1 Electric characterization

7.1.1 Frequency range

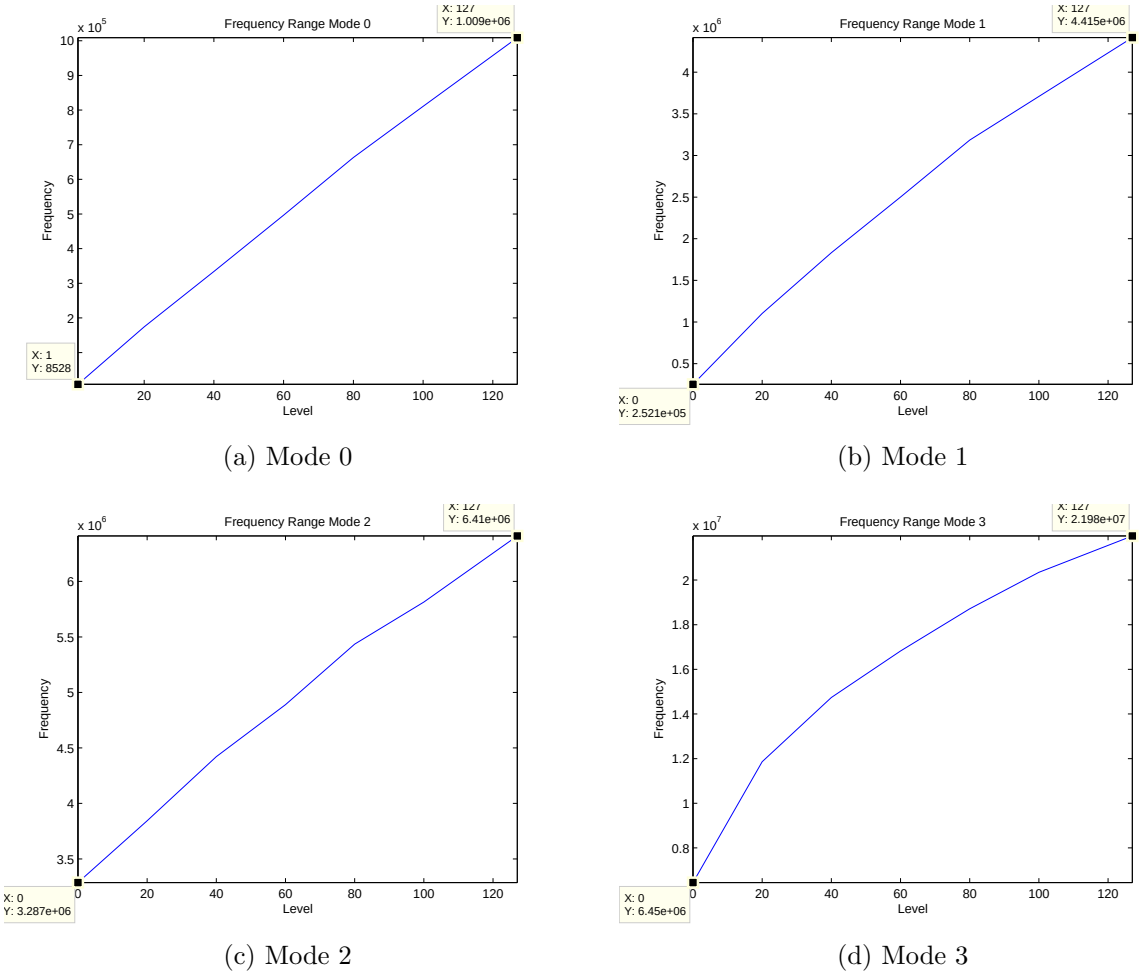
One of the most important characteristics of the multi-channel sine generator is the range of the generated frequency. The lower and upper limits of the sine waveform will define a wide variety of possible experiments of particular interest in electrokinetic microfluidic research. The range for the four frequency modes was obtained setting one oscillator to work with an amplitude of $1V_{PP}$, then a sweep of frequency levels was performed recording their values.

Table 7.1 illustrates the frequency sweep where theoretical and measured range values are recorder. The frequency sweep is also included to provide the minimum frequency resolution that the stimulation system could withstand.

Table 7.1: **Theoretical and measured frequency ranges of the multi-channel oscillator**

Mode	Theoretical	Measured	Freq. Step
M0	7.7kHz - 715kHz	8.4kHz - 1MHz	8kHz
M1	704kHz - 6.3MHz	250kHz - 4.4MHz	130kHz
M2	6.2MHz - 10.2MHz	3.2MHz - 6.4MHz	25kHz
M3	10.2MHz - 22.5MHz	6.4MHz - 22MHz	185kHz

Table 7.1 shows consistent results between simulated and measured results. Since the simulation was made using the typical model we may note shiftings between frequency ranges. Remember that the results of the MonteCarlo analysis predicted a curve of possible relocations for frequency ranges hence the shift of frequency limits in the middle stages. Even though the overall response and functioning of the oscillator was preserved and the frequency requirement was accomplished. Lower and upper frequency limits verify well the corner analysis and entire operation range. The overlapping frequencies can be used to reach frequencies not present in a specific range due to the step size. The plotted frequency range for the four frequency modes is shown in Figure 7.1. Note the exhibited linearity except in the last range where larger currents are present.



(a) Mode 0

(b) Mode 1

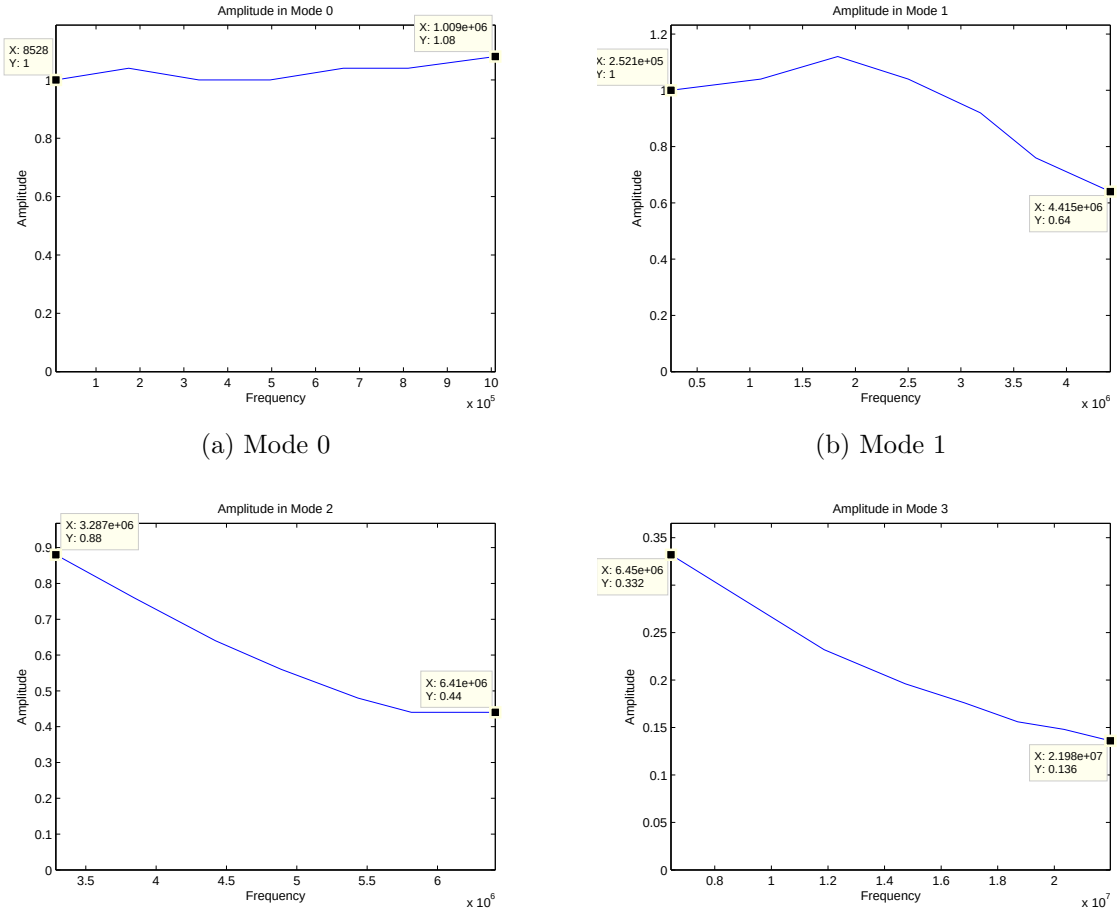
(c) Mode 2

(d) Mode 3

Figure 7.1: **Measured frequency ranges**

7.1.1.1 Bandwidth

Figure 7.2 shows the amplitude of the waveform in terms of frequency for the four operating modes of the system. In this case the oscillator was set to provide $1V_{PP}$ waveform at each operation mode.



(a) Mode 0

(b) Mode 1

(c) Mode 2

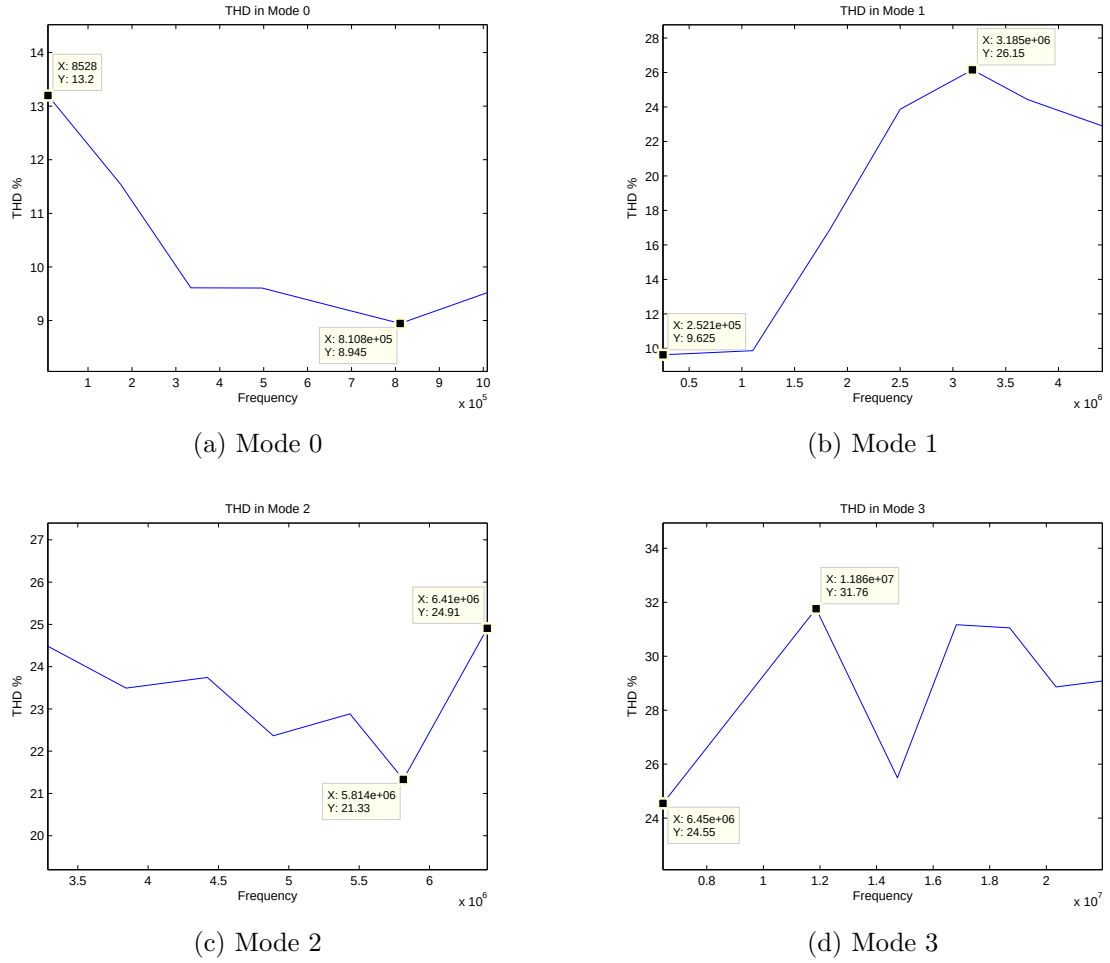
(d) Mode 3

Figure 7.2: **Measured amplitude for each frequency range**

In Mode 0 the amplitude stays constant for all frequency range. Mode 1 shows a drop in amplitude of 36%. Modes 2 and 3, the amplitude drops to 44% and 13.6% respectively, mainly due to the gain-bandwidth limitation of the oscillator. This measurements where performed without compensation from the amplitude control.

7.1.2 THD measurement

Even if the triangle to sine wave converter stage could have been designed to have a perfect sinusoidal transfer function, the resulting output signal have had harmonic distortion if the triangle wave amplitude was not controlled efficiently [42]. This fact led to the inclusion of an open loop control (the control current source) to deal with the variations in the quality of the generated sine wave. From the measures performed at each frequency range we can extract the THD information. Figure 7.3 shows the THD results for the four operating modes.



(a) Mode 0

(b) Mode 1

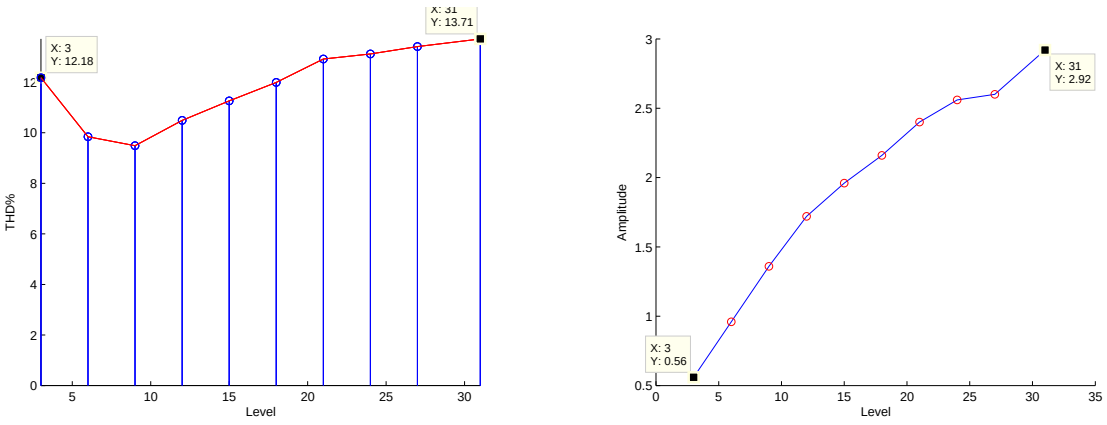
(c) Mode 2

(d) Mode 3

Figure 7.3: **Measured THD for each frequency range**

The measurements of Figure 7.3 were acquired without applying any change to THD control of the multi-channel generator, and they reflect the natural response of the oscillator to changes in the frequency level. However, if the THD control compensate to generate a sine wave of 1MHz, the observed behavior is illustrated by Figure 7.4. Those graphs were generated applying a sweep from 1 to 31 in the THD level.

The THD variations find a minimum around the 9th level of the control current



(a) THD variation

(b) Amplitude Variation

Figure 7.4: **Variations of TDH and signal's amplitude applying the THD control**

source ($\sim$ 1µA). The lowest point changes if another frequency is chosen and the 31 selection levels allow for the finding of the lowest THD. The changes in the bias level of the differential pair bring a variation in the output's amplitude. A good balance of the three variables (frequency, THD and amplitude) must be found when configuring an output signal, when this balance is found it is possible to achieve a THD correction of less than 6%.

7.1.3 Noise

The generated sine waveform includes a certain amount of noise. In order to measure the amount of noise in the output waveform. The system was configured to have an output of 1.15MHz, then, the amplitude range and amplitude level were swept to see the variation in the noise level. The results were collected by means of a digital oscilloscope in form of text files. Then, the files were processed and analyzed using MATLAB. The obtained SNR for all modes ranged from -71dB (worst case presented in Mode 2) to -46dB (Mode 3)[1]. The power consumption during the measurement was 1.1W.

The measured characteristics of the multi-channel generator ensure the proper operation of the device in the delivering of sinusoidal signals in the range of 8.5kHz to 22MHz. The amplitude range offers a suitable span for a variety of experiments in the microfluidics area using electrokinetic forces. The THD control allows an improvement in the quality of the obtained sine signal.

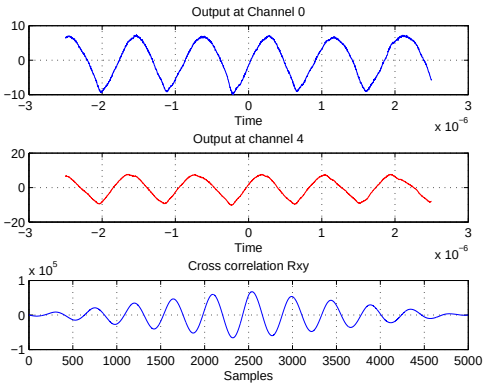
A crosstalk analysis was performed setting the channel 0 to $10V_{PP}$ at 1.1MHz. A measurement of cross-correlation was made against the waveform of an adjacent channel (4)[2] set at the same amplitude and frequency. The next analysis was the cross-correlation

[1]For a commercial signal generator a noise <-55dB is considered as a desirable measure, refer to Agilent 33120 data sheet for further information.

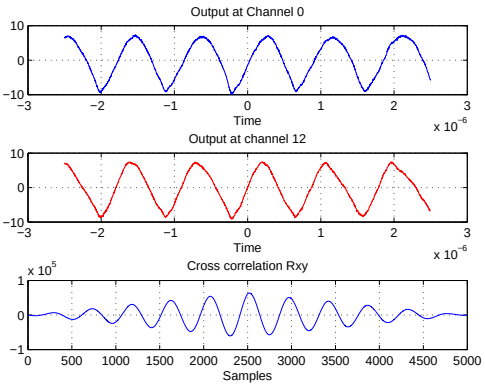
[2]Remember that the output of channel 0 is adjacent to the output of channel 4, because of the

between channel 0 and a non-adjacent channel (in this case channel 12).

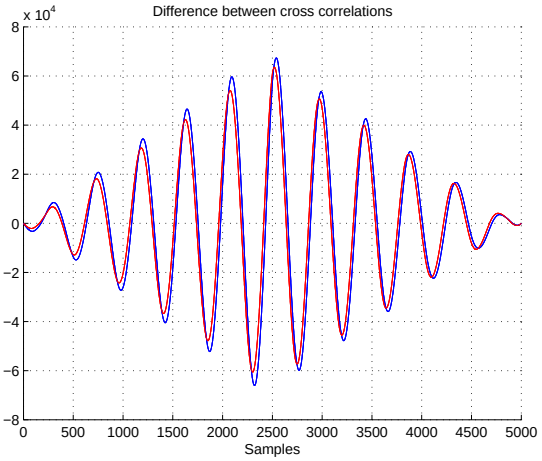
The results of Figure 7.5 show that the effect of adjacent channels as well as far channels is practically negligible. No electric perturbation was noticed nor important noise contribution due to the action of another channel.



(a) Cross correlation between adjacent channels (0 and 4)



(b) Cross correlation between far channels (0 and 12)



(c) Comparison of Cross correlation)

Figure 7.5: **Cross-correlation between channels**

organization of pins in the IC.

7.2 Microfluidic Experiments

Besides of the electric tests conducted on our multi-channel sine generator, a couple of microfluidic experiments were also conducted. In this chapter we are going to review the used microfluidic device, the materials and methods and the obtained results of such experiments.

The experiments performed were carried out in the field of particle separation. In the last years we have witnessed significant advances boosted by the wide use of techniques such as Fluorescence-Activated Cell Sorting (FACS) and Magnetically-Activated Cell Sorting (MACS).

Fluorescence-activated cell sorting (FACS) is a method for isolation of cell subsets in parallel, when a high purity and recovery of a specific subpopulation of cells is required. In this method, the cells to be examined are pressurized into a directed fluid stream, passed through a beam of light and the light scattered by them provides the information about the cell size and structure. The beams illuminate only one cell at a given time. There are cell components that produce fluorescence emissions using fluorescent probes to determine more specific cell characteristics. The most used probes are antibodies labeled fluorochrome[76]. However, it is not widely used in laboratories because of its high cost, limited throughput (between 10^3-10^4 cells/sec), long sorting times, decrement of cell viability and complicated design and operation[77].

Magnetic-Activated cell sorting (MACS) is an excellent tool for separating cells of interest out of mixed cell populations. MACS utilizes magnetic micro/nano particles with antibody proteins that are specific to the cell membrane protein of interest, where magnetic particle-bound cells lie in a magnetic energy gradient[78]. However, the purity and recovery typically may have large variances[77], besides, if the desired cells are present in low concentration, the selection could result in low yield and low purity due to loss of desired cells and insufficient removal of unwanted cells[76].

The 3D Carbon Dielectrophoresis offer an alternative to those techniques eliminating the need of tags while maintaining a high throughput separation process. One of the most important advantages of DEP is the selection of the targeted particle using only its intrinsic dielectric properties, determined only by the particle's individual phenotype.

7.2.1 Microfluidic device

The sine generator was tested using a microfluidic DEP platform, the novelty of this device resides in the use of volumetric (3D) Carbon Dielectrophoresis (CarbonDEP). CarbonDEP refers to the use of carbon surfaces to induce DEP. The carbon surfaces offer important properties such as [79]:

- Very wide electrochemical stability window.
- Excellent biocompatibility.

- Low cost.
- Easy to functionalize.

The microfluidic device consists on a microchannel with four embedded carbon electrodes [80] that are located along the microchannel arranged as two different ports, see Figure 7.7. The connecting leads were fabricated by pyrolysis of two-step photolithography defined SU-8 structures (MicroCHem Corp.) according to C-MEMS standards. The SU-8 is a high contrast, epoxy based photoresist designed for micromachining and microelectronic applications. SU-8 features a thick thermally and chemically stable image. The exposed and cross-linked portions of the film are rendered insoluble to liquid developers. The SU-8 has a very high optical transparency ideal for imaging near vertical sidewalls and for permanent applications where it is imaged, cured and left in place. Briefly the SU-8 is processed as follows [79, 81]:

1. The first step is the spinning at approximately 500rpm for 12s, then at 1400rpm for 30s (Figure 7.6) a).
2. Then, a 10 min soft bake is carried out at 65° and finally a soft bake for 80 min at 95° as depicted in Figure 7.6 b).
3. To define the shape and size of the structures, the substrate is put under UV light passing through a fabricated mask, to print the structures c).
4. The substrate remains under UV radiation during approximately 100s as seen in Figure 7.6 d).
5. A post bake is carried out for 2 min at 65° and for 30 min at 95° (illustrated in Figure 7.6) e).
6. Development is carried out using a SU-8 developer. (Figure 7.6) f).
7. The C-MEMS architectures are obtained in a two-step pyrolisis process in an open ended quartz-tube furnace:
   (a) Samples are post-baked in a N_2 atmosphere at 300°C for about 40 min up to 900 C°C as shown in Figure 7.6 g).
   (b) The N_2 is shut-off and forming gas [H_2/N_2] is introduces during 1 h, then, the heater is turned off and samples are cooled down in a N_2 atmosphere to room temperature (Figure 7.6) h).

The microfluidic platform consists of posts of 70µm high with a diameter of 25µm; the separation between posts is 45µm in the x axis and 100µm in the y axis. The microchannel measures 600µm wide and 100µm high, and was cut on double-sided pressure sensitive adhesive and aligned to a previously drilled polymer cover. The device supports flow rates of 8000µl/min with no leakage. Electrical connections are made with silver conductive paint and common solder resulting in an average contact resistance of

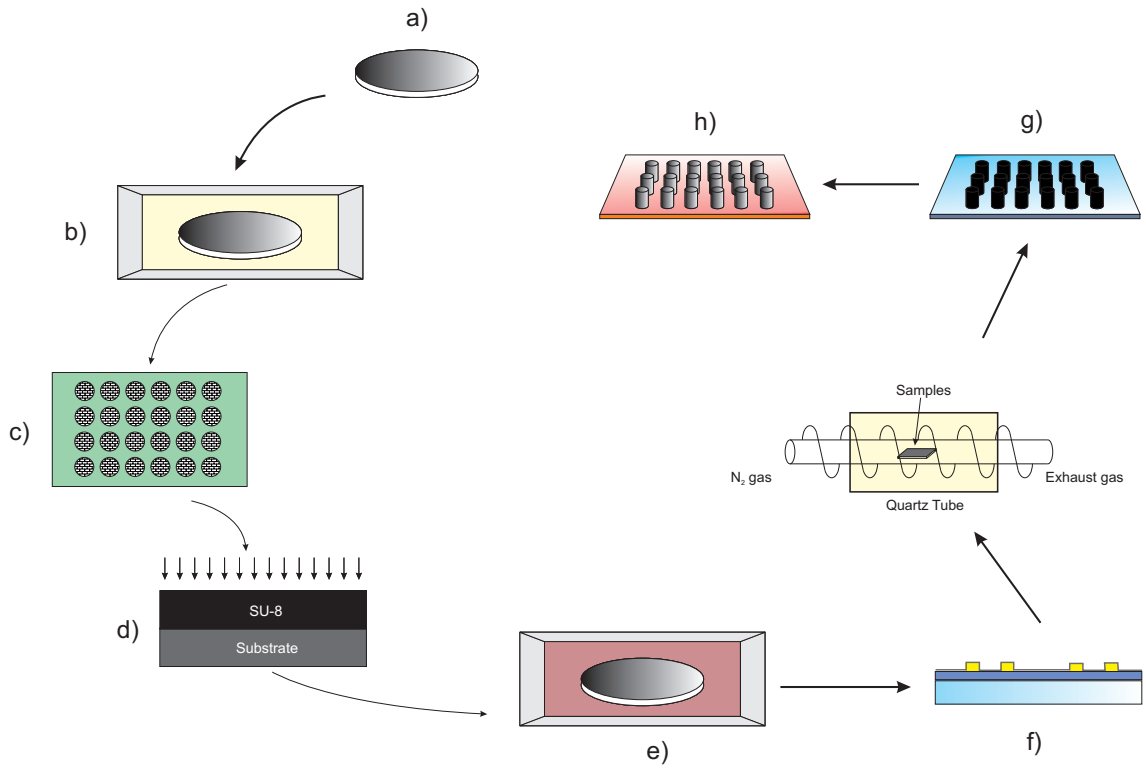
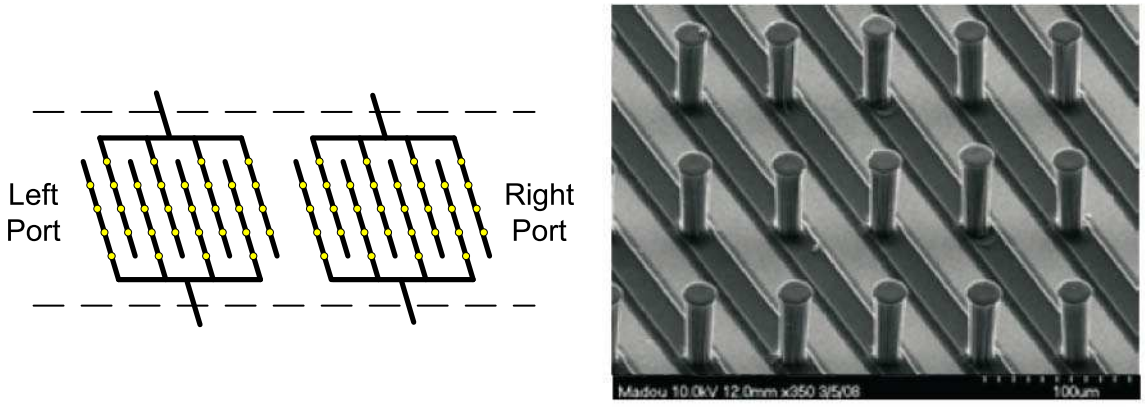


Figure 7.6: **SU-8 for C-MEMS**

120 Ω. A thin layer of SU-8 was coated and patterned around the electrodes to protect the connecting leads from being peeling off while immersed in an aqueous media. The connection between the microfluidic device and the multi-channel sine generator was made by means of platinum wires.

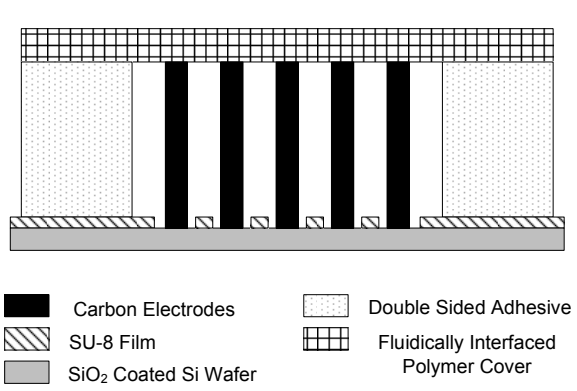


(a) Schematic diagram

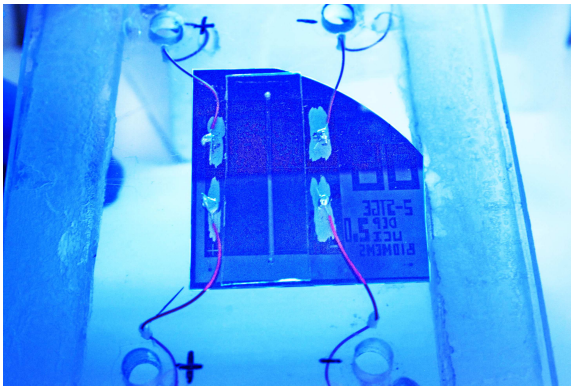
(b) Carbon electrodes (Picture taken by Dr. Madou's group at UCI [80])

Figure 7.7: **Electrodes inside the microchannel**

A cross section of the microfluidic platform is shown in Figure 7.8a and a photography of the microfluidic platform in Figure 7.8b.



(a) Cross section of the microfluidic device as sketched in [80]



(b) Microfluidic platform

Figure 7.8: **Microfluidic device**

7.2.2 Experiment I

7.2.2.1 Materials and methods

Saccharomyces cerevisiae is a versatile organism that is used for production of a whole range of different products. Characteristics of *S. cerevisiae* strains are selected for commercial production of bakers yeast. It has the ability to ferment sugar in the dough vigorously and rapidly [82]. The physiology and the cell function strongly depend on the environment of the cells and on the genetic characteristics of the strains. An important part of research on *S. cerevisiae* physiology has been focused on its aerobic growth whereas anaerobic metabolism is generally considered to be simpler, leading to an equimolar production of carbon dioxide and ethanol [83].

In this experiment *Saccharomyces cerevisiae* (ATCC 24858), with an approximate diameter of 3-5 µm, was cultured in YM (Yeast Malt) broth at 30°C for 18 hours to late log phase (cell concentration of 6×10^6 cells/mL) verified by OD (optical density) measurements at 600 nm. Cells were washed by centrifugation and re-suspension in DI (De-ionized) water to remove the culture media. Finally cells were centrifuged and re-suspended in the buffer media (2% BSA solution) to a concentration of 6×10^6 cell/mL. Carbolxylated polystyrene beads with a diameter of 10.14 µm (Bang Laboratories), where re-suspended in the buffer media to a concentration of 3×10^6 particles/mL. A mixture of *S. cerevisiae* cells and polystyrene beads was developed in order to evaluate a mixed sample. The mixed sample had a final concentration of 3×10^6 cells/mL and 1.5×10^6 particles/mL.

The sample was introduced into the microdevice with a micropipette creating a differential pressure from the inlet reservoir to the outlet which drives the flow as illustrated

in Figure 7.9. Then the different signals are applied in order to simultaneously trap cells and particles in different sections of the microdevice. The microdevice is mounted under an inverted epifluorescent video microscope for microfluidics (LabSmith, Livermore, CA, USA) in order to record the experiment. The elaborated test-bench is a simulated experiment very close to a real biomedical application set-up for a lab-on-a-chip. The experimental set-up is shown in Figure 7.10.

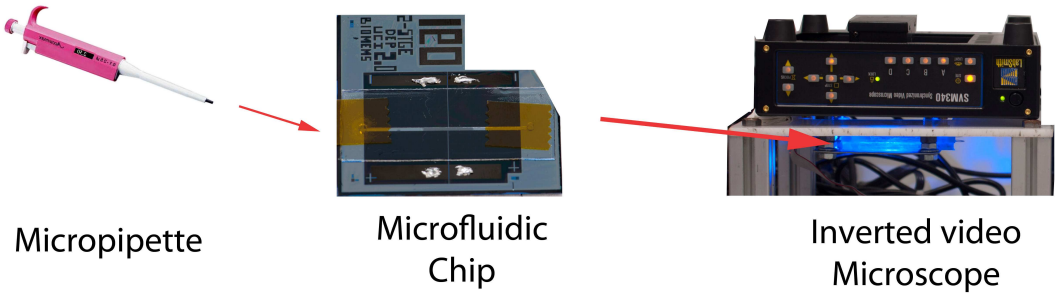


Figure 7.9: **Preliminary steps**

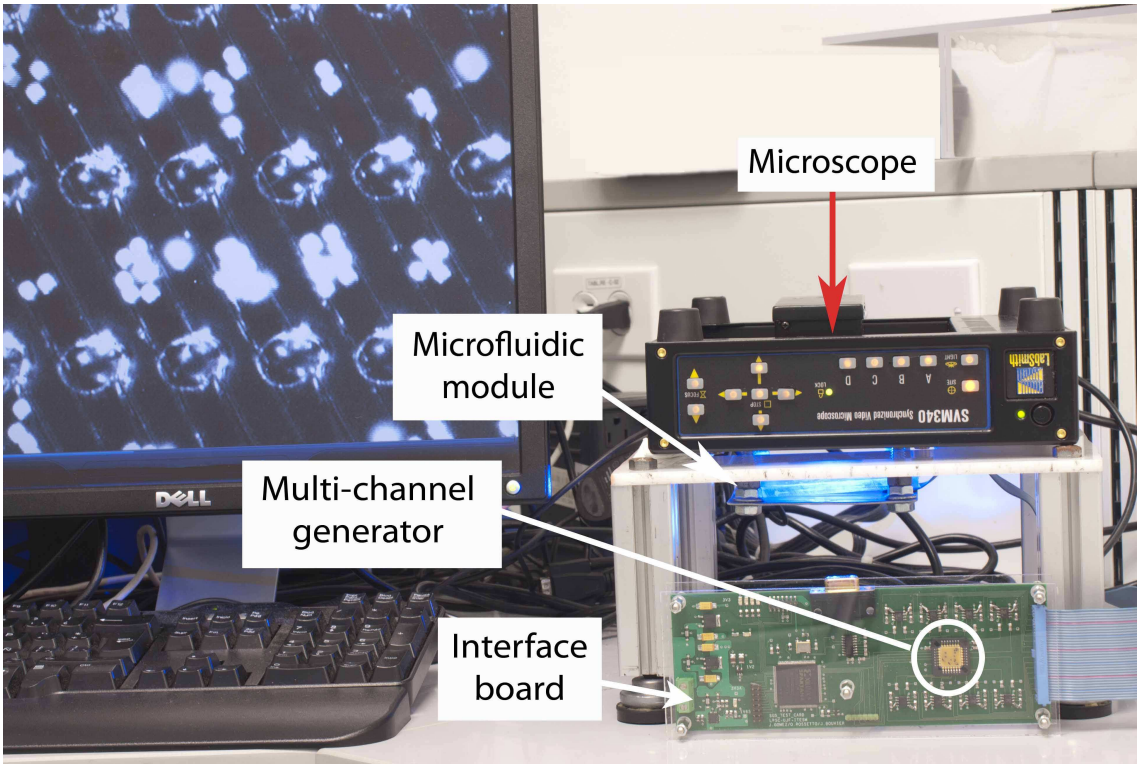


Figure 7.10: **Experimental set-up**

A simulation was performed in order to predict the effects of the DEP over live yeasts and polystyrene beads. The results are shown in Figure 7.11. Note that live

yeasts experiment positive DEP for the entire sweep from 1kHz to 10MHz. The live yeasts properties were simulated according to [84] while properties of polystyrene beads were taken from [85]

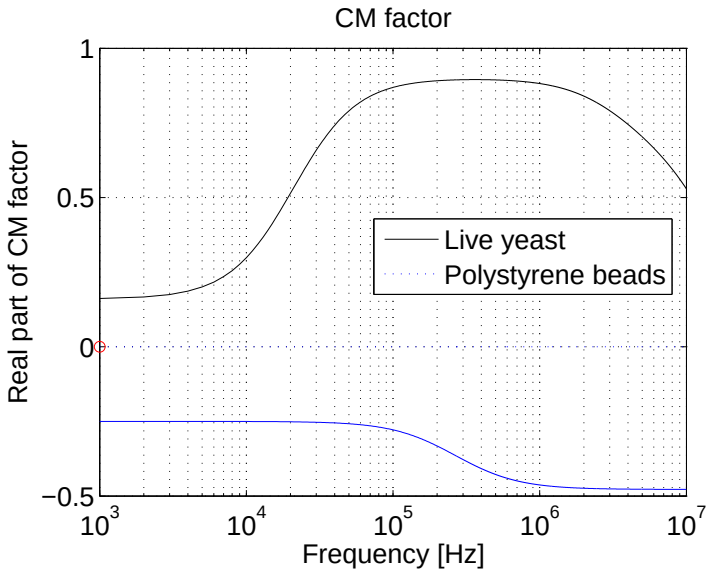


Figure 7.11: **Real part of CM factor for both Live yeasts and Polystyrene beads**

7.2.2.2 Experimental results

After the sample is injected into the microdevice, cells and particles flow freely across the channel over the array of carbon electrodes as the stimulation voltages are off. Then a voltage of 1MHz and $10V_{PP}$ is applied in the left side of the array and a voltage of 50Hz and $10V_{PP}$ is applied in the right side as shown in Figure 7.12. In Figure 7.13a we can observe a high concentration of cells that are immobilized in the left side of the channel (greater in the first rows of electrodes) while polystyrene beads (enclosed in white circles) are repelled from the electrodes since they experience negative DEP. In the right side of the microchannel, where the frequency is 50Hz, cells experience negative DEP and are repelled from the carbon electrodes while polystyrene beads experience positive DEP and are immobilized in the electrodes as shown in Figure 7.13b.

7.2.2.3 Conclusions on the experiment I

We have seen the application of the multi-channel sinusoidal generator in a DEP separation experiment; the generator eliminates the need for bulky and/or discrete signal generators that are commonly used in biotechnology research. The generator was connected to a microfluidic platform where cells and polystyrene beads were simultaneously trapped at different positions along a microchannel. The performed experiment resulted in an accepted paper for the 9th IEEE International NEWCAS Conference [86].

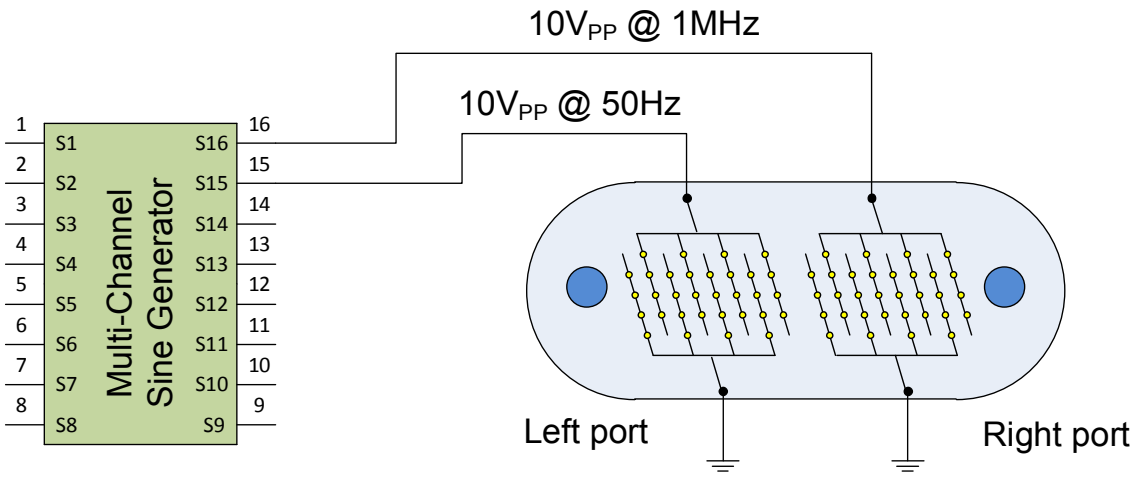
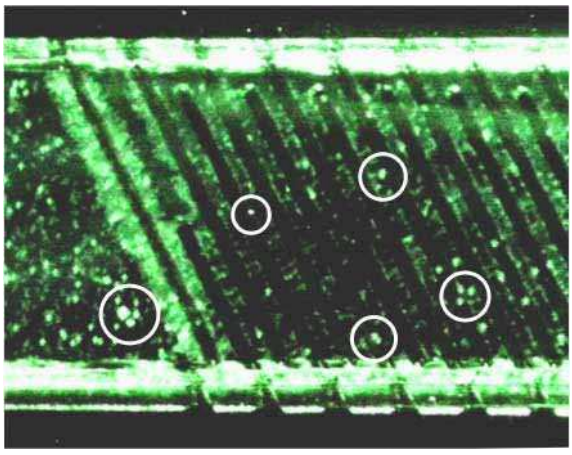
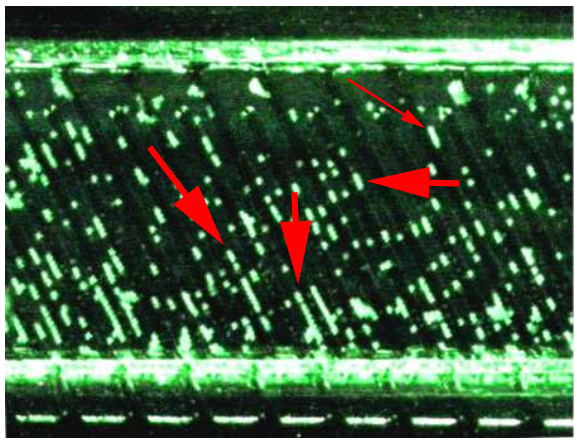


Figure 7.12: **Connections between Stimulator and microfluidic chip.**



(a) Cells being trapped with positive DEP, polystyrene beads experimenting negative DEP (white circles)



(b) Immobilized polystyrene beads due to the effect of positive DEP (pointed by arrows)

Figure 7.13: **Evoked DEP effects in microchannel**

7.2.3 Experiment II

The multichannel sinusoidal generator was connected to the aforementioned CarbonDEP device. Electric potential was applied to the carbon electrodes in the microchannel in order to produce a non-uniform electric field distribution between the carbon structures.

7.2.3.1 Computational Modeling

Simulation of crossover frequency spectra [85] for different experimental settings was performed using MATLAB (The Mathworks Inc., Natick, MA). This allowed for the selection of the best suspending medium conductivity, as well as for the selection of

the most adequate AC electric potential frequencies to be used on the experiments. Dielectric properties for yeast cells were extracted from [84]. To compute the equivalent complex permittivity of yeast, the multishell model presented in [87] was used.

Finite element method based simulations were carried out using COMSOL Multiphysics (COMSOL Inc., Burlington, MA) in order to obtain predictions of the experimental results. The electric field, the Claussius-Mossotti factor and crossover frequency were estimated with these results. The system was set-up to those values making minor fine adjustments in preparation for the experiment.

An array of 5×5 electrode posts was considered on a plane located at 30µm above the channel floor. At this height the effect of the planar electrodes located at the bottom of the channel are negligible. The channel geometry is shown in Figure 7.14 and is based on the microfluidic chip dimensions mentioned later in subsection 7.2.3.2. Boundary conditions were set to electric insulation at the channel walls, and uniform AC electric potential at the electrodes. The mesh for this geometry consisted of 124,698 elements. The rectangle in Figure 7.14b) shows the section from which data for Figure 7.15 and Figure 7.16 was obtained.

Two different experiments were planned: separation of live and dead yeast cells using an AC signal of $7V_{PP}$ with a frequency of 8kHz, and trapping of live and dead yeast cells using an AC signal of $7V_{PP}$ with a frequency of 50kHz. Estimations of the experimental results for the first experiment are shown in Figure 7.15 and those for the second in Figure 7.16.

From Figure 7.15 it can be observed that for the first experimental setup dead cells will experience a positive DEP force, causing the dead cell population to be attracted to the electrode posts. On the other side, live cells will experience a negative repulsive force. For the second experimental setup, shown in Figure 7.16, both live and dead cells will experience positive DEP. The power consumption of the system during the experiment was as expected 1.1W.

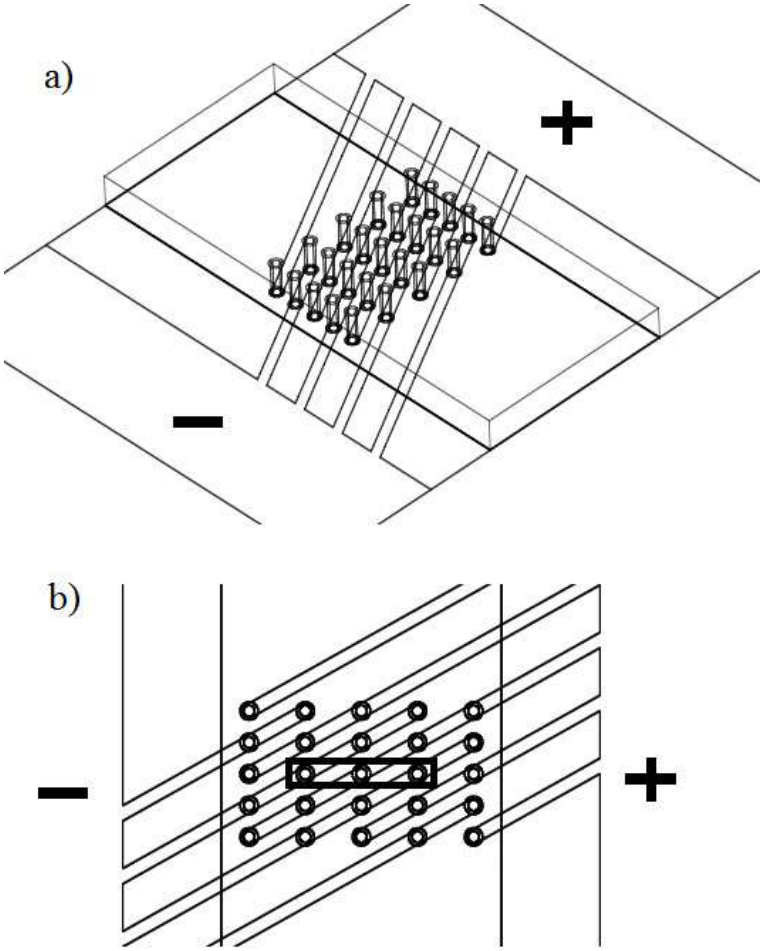


Figure 7.14: **Representation of embedded carbon electrodes.**

a) 3D view, b) top view.

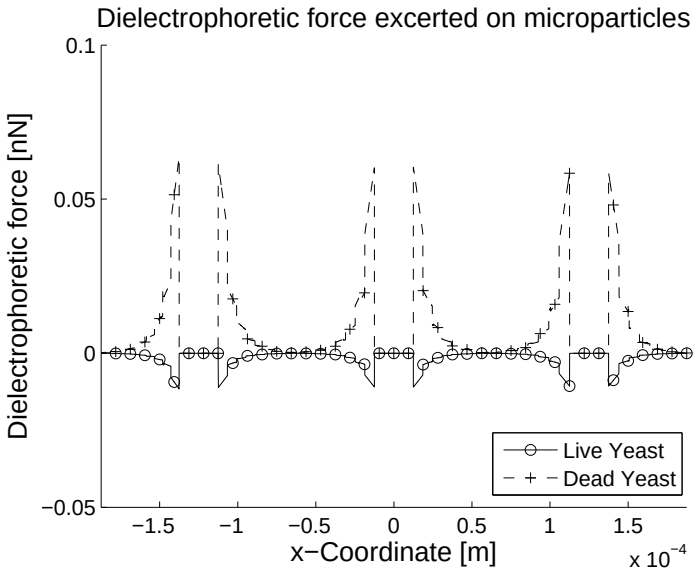


Figure 7.15: **Behavior of cells under DEP.**

Dead cells are being attracted to electrode posts, while live cells are repelled from electrode posts.

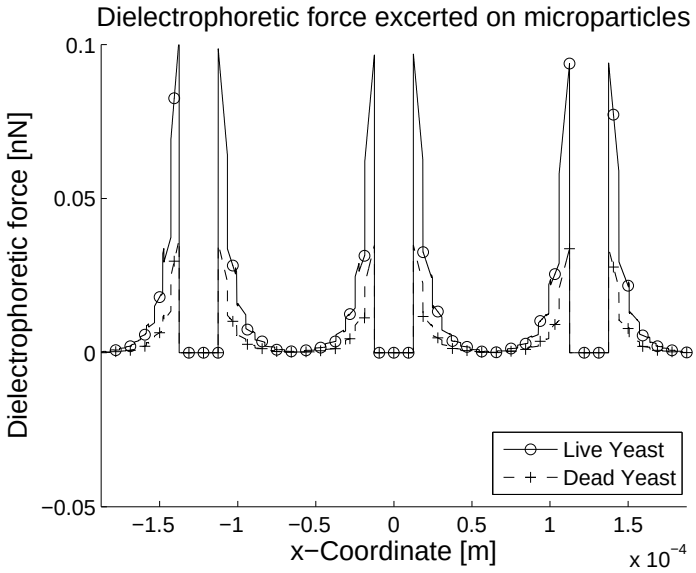


Figure 7.16: **Second experimental set.**

Live and dead cells experimenting positive DEP

7.2.3.2 Materials and methods

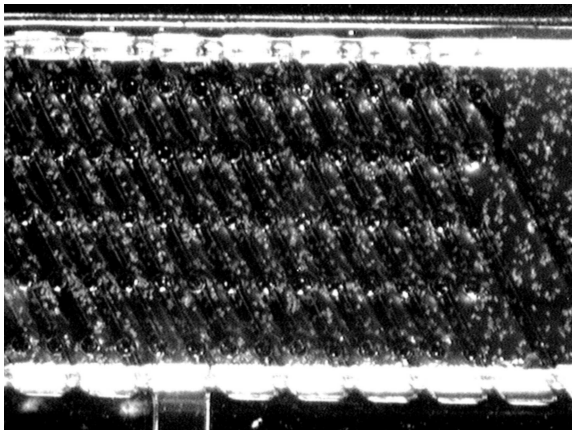
In this experiment, electric potential from two of the outputs of the multi-channel generator was applied to the carbon electrodes in the microchannel in order to produce a non-uniform electric field distribution between the carbon structures. The 3-Dimensional carbon structures are 40µm high with a 12.5µm radius and a center to center separation of 45µm and 100µm in the X and Y axis, respectively. As suspending medium, deionized water with KH_2PO_4 to a final conductivity of 21µS/cm was employed. Conductivity was measured with a multi-parameter bench meter (Model HI 255, Hanna Instruments, Woonsocket, RI, USA). *Saccharomyces cerevisiae* ATCC 24858 cells were growth in YM Broth at 30°C and 175rpm for 18h until late log phase. Cells were then centrifuged and re-suspended with DI water to remove the excess of culture media within the cells to a final concentration of 6×10^7cells/mL in the suspending medium. Cells were labeled with Syto®9 fluorescent (490/520) green stain.

To obtain non-viable yeast cells, a sample of cells from the culture media is centrifuged and washed with DI water to be further heated to 80°C for 20 minutes. Non-viable cells are then labeled with propidium iodide fluorescent (490/635) color red and re-suspended in the suspending medium to a final concentration of 6×10^7cells/mL. The sample mixture was introduced into the microdevice employing a micropipette. The microdevice was mounted under an inverted epifluorescence video microscope for microfluidics SVM340 (LabSmith, Livermore, CA, USA) turned upside down as shown before in Figure 7.10. A personal computer was employed to manipulate the communication and operation of the microscope.

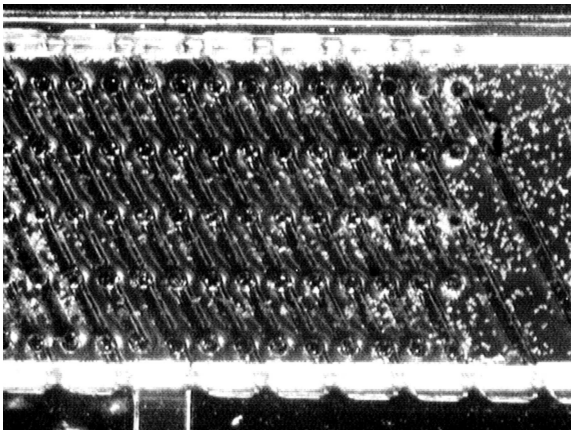
7.2.3.3 Results

In Figure 7.17, a mixture of viable and non-viable yeast cells within the arrange of carbon structures is shown. Figure 7.17a shows the steady flow (right to left) of cells when no signal is applied into the system. Live and dead cells are mixed along the microchannel. Live cells are shown brighter in contrast with the darker dead cells. When a sinusoidal signal of 8kHz with a potential of $7V_{PP}$ is applied in the carbon electrode arrange in the right side of the channel and a 50kHz signal with a potential of $7V_{PP}$ is applied in the left side arrange, cells became rearranged according to the dielectrophoretic force acting on them.

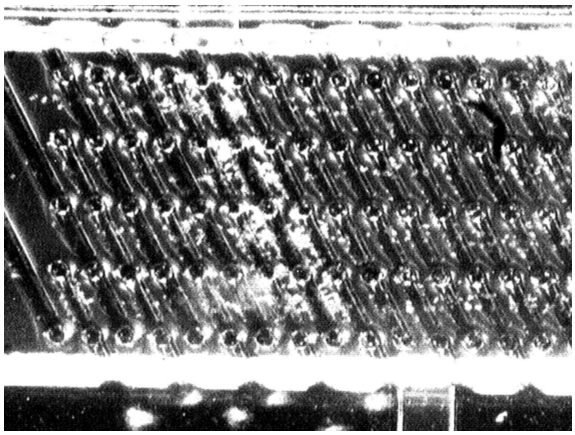
According to the simulation results, in the right side arrange of electrodes, live cells are repelled from the carbon structures since they exhibit a negative DEP force. In the other hand, dead cells will be attracted to the carbon structures experiencing positive DEP force. In Figure 7.18b , dead cells were attracted to the carbon structures and the planar electrodes thus concentrating while live cells were repelled from this regions where the electric field gradient is greater, away from the carbon structures in agreement with the simulation results in Figure 7.15. In the left side arrange of electrodes, according to the simulation results shown in Figure 7.16, cells were attracted to the regions of greater gradient, being trapped in the carbon structures (Figure 7.17c).



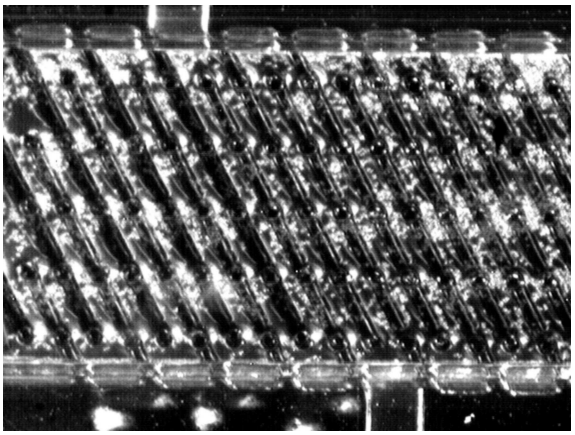
(a) Steady flow, no signal applied



(b) Dead cells attracted to carbon structures



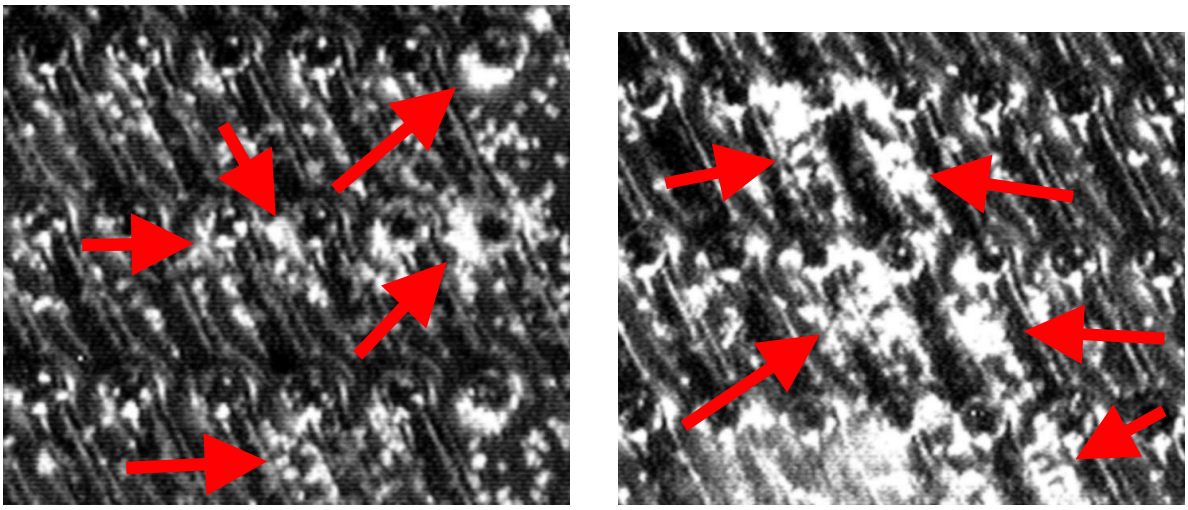
(c) Left side of the array with cells being trapped in the carbon structures



(d) Signal turn-off in both sides of the electrodes

Figure 7.17: **Dielectrophoretic effects observed in the microfluidic device**

In Figure 7.17d, when the signal in both arranges of electrodes is turn off, cells detached from the carbon electrodes and flow along the channel as concentrated plugs of cells, thus showing that DEP force is reversible. Figure 7.18 shows a zoomed view of trapping.



(a) Zoomed view of dead cells attracted to carbon structures

(b) Zoomed view of cells trapped in the carbon structures

Figure 7.18: **Zoomed view of positive DEP behavior.**

Dead cells at left, live cells at right

7.2.3.4 Conclusions on the experiment II

In this second experiment, we could make a successful separation of viable and non-viable cells according to simulations and observed physical results. The used cells worked in the frequency range of the multichannel sinusoidal generator then it was not necessary to add external circuitry to get a lower frequency, the functionality of the generator was again demonstrated. The results of this experiment, are included in [88].

Chapter 8

Conclusions

The process of design and implementation of an integrated circuit capable to offer sixteen independent sine signals has been developed and tested. It is intended to be used in electrokinetic experiments. We have analyzed several analog and digital models to implement the oscillator and the performance of the chosen option. Also, details in the implementation of the several modules that conform the VCO and the complete multi-channel generator have been provided. After the prototype development, we arrived to the following conclusions:

The implementation of the digital algorithms based in the DDFS for the generation of sine signals offer good performance, low power consumption and good resolution. On the other hand they are limited by supplementary circuitry such as DAC's, filters and amplifiers. The use of sine generators based upon the delta dirac unstable oscillator is advisable in the generation of fixed frequencies due to its dependance of clock speed.

Even though the use of OTA-C in the design of VCO's with wide frequency ranges has been well documented and used ([39], [40], [41], [71], [72], [89],), still the implementation relies on a specially designed OTA (extending the occupied area for each VCO) and the use of two capacitors that could lead to important mismatch errors causing operating problems.

The TSC demonstrated to be an excellent option for the integration of multiple VCO's using just one capacitor and offering wide frequency ranges; its major drawback lies in the THD control that brings important amplitude changes in the correction of the distortion. It is possible to implement automatic THD controls sacrificing occupation area.

To our knowledge no other device with multiple sine outputs with the discussed amplitudes and frequency ranges exist. Biotechnology research groups have placed our system as an option in the electrokinetic domain where multiple stimulation signals are required simultaneously.

The multi-channel generator presented in this work can be applied in a variety of experiments were electrokinetic forces are used for particle trapping, separation and characterization. The availability of sixteen independent channels allows stimulation of

different ports located along one or several microfluidic channels.

The use of the multi-channel generator in the separation of two different particles was demonstrated with a 2-stage microfluidic platform stimulating the ports with sine signals at different frequencies without degrading the sample in the process. Preliminary results over a complete experimental set-up for dedicated LOC allow us to recommend the full capabilities of the designed ASIC in the separation, filtering and characterization tasks.

8.1 Future work

The work in the integration of intelligent stimulation systems along with electrokinetic platform continues. In the case of the multi-channel sine generator, the next natural step will be the integration of high voltage amplifiers in the same integrated chip, eliminating the need of using an interface card. The integration of the power stage will reduce dramatically the size of the stimulator platform.

Another pending task is the interconnection of the stimulation system with the electrokinetic platform. The deposition of metal on materials for microfluidic devices is a complex process, which greatly limits the potential that can be applied. The most used technique to communicate the microfluidic systems with microelectronic devices is the modular interconnection. The main three interconnection technologies are Wirebond (WB), Tape automated bond (TAP) and Flip chip (FC) [4]. Another interconnection option, the chip-on board is used in [14]. The next assignment is study better options to integrate both stimulation system and microfluidics stage. The next prototype should be integrated to form a complete LOC system.

The use of a smaller standard CMOS process will reduce the size of the ASIC, allowing the incorporation of more oscillators, amplifiers, sensing systems, and data acquisition modules.

In the experimental sessions we have seen operations in frequencies ranging from 8 kHz to 50kHz, a decrease in the digital step size for the selection of frequency will provide of a better resolution in sensitive frequency ranges. The next prototype must count on a larger frequency resolution.

Certainly, one of the most ambitious plans of the Biointeractive Systems and BioMEMS Research Chair is the implementation of the separation/characterization platform described early in exploiting the capabilities of the multi-channel sinusoidal system. This will be possible in the near future with the arrive of the newer microfluidic platforms.

Bibliography

[1] J. Vankka, "Direct digital synthesizers: Theory, design and applications," Dissertation for the degree of Doctor of Science in Technology, Helsinki University of Technology, Espoo, Finland, Nov. 2000.

[2] R. Martinez-Duarte, J. Andrade-Roman, S. O. Martinez, and M. Madou, "A high throughput multi-stage, multi-frequency filter and separation device based on carbon dielectrophoresis," *NSTI-Nanotech 2008*, vol. 3, pp. 316–319, 2008. [Online]. Available: http://www.nsti.org

[3] D. L. Polla, "Biomems applications in medicine," in *Proc. International Symposium on Micromechatronics and Human Science*, Nagoya, Japan, Sep. 2001, pp. 13–15.

[4] H. K. Oliver Geschke and P. Telleman, Eds., *Microsystem Engineering of Lab-on-a-chip Devices*. Denmark: wiley-VCH, 2008.

[5] "Biosite triage system," Biosite Inc. [Online]. Available: http://www.biosite.com/products/triageOverview.aspx

[6] "Agilent 2100 bioanalyzer," Agilent. [Online]. Available: http://www.genomics.agilent.com

[7] S. K. Sia and L. J. Kricka, "Microfluidics and point of care testing," *Lab chip*, vol. 8, pp. 1982–1983, 2008.

[8] P. Tabeling, *Introduction to Microfluidics*. Oxford UK: Oxford, 2006.

[9] A. T. Woolley, G. F. Sensabaugh, and R. A. Mathies, "High-speed DNA genotyping using microfabricated capillary array electrophoresis chips," *Analytical Chemistry*, vol. 69, pp. 2181–2186, Jun. 1997.

[10] A. T. Woolley and R. A. Mathies, "Ultra-high-speed DNA fragment separations using microfabricated capillary array electrophoresis chips," in *Proc. National Academy of Sciences*, vol. 91, USA, Nov. 1994, pp. 11 348–11 352.

[11] X.-B. Wang, Y. Huang, P. R. C. Gascoyne, and F. F. Becker, "Dielectrophoretic manipulation of particles," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 660–669, May 1997.

[12] Y. Li and K. Kaler, "Dep based cell separation utilizing planar microelectrode array," *Electrical Insulation and Dielectric Phenomena, 2002 Annual Report Conference on*, pp. 680–684, Oct. 2002.

[13] E. G. Cen, L. Qian, and K. V. Kaler, "An integrated microchip for dielectrophoresis based characterization and manipulation of cells," in *Proceedings of the 25th Annual International Conference of the IEEE EMBS*, Cancun, Mexico, Sep. 2003, pp. 17–21.

[14] N. Manaresi, A. Romani, G. Medoro, L. Altomare, A. Leonardi, M. Tartagni, and R. Guerrieri, "A CMOS chip for individual cell manipulation and detection," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 12, pp. 2297–2305, Dec. 2003.

[15] I. Doh, K.-S. Seo, and Y.-H. Cho, "A continuous cell separation chip using hydrodynamic dielectrophoresis process," in *Micro Electro Mechanical Systems, 2004. 17th IEEE International Conference on. (MEMS)*, Maastricht, The Netherlands, Jan. 2004, pp. 29–32.

[16] A. Enteshari, G. Jullien, O. Yadid-Pecht, and K. Kaler, "All CMOS low power platform for dielectrophoresis bio-analysis," in *Proceedings of ESSCIRC*, Grenoble, France, Sep. 2005, pp. 339–342.

[17] B.-G. Kim, K.-S. Yun, and E. Yoon, "Active positioning control of single cell/microbead in a micro-well array chip by dielectrophoresis," *Micro Electro Mechanical Systems, 2005. MEMS 2005. 18th IEEE International Conference on*, pp. 702–705, Jan. 2005.

[18] K. W. Current, K. Yuka, C. McConaghy, P. R. C. Gascoyne, J. A. Schwartz, J. V. Vykoukal, and C. Andrews, "A high-voltage integrated circuit engine for a dielectrophoresis-based programmable micro-fluidic processor," *MEMS, NANO and Smart Systems, 2005. Proceedings. 2005 International Conference on*, pp. 153–158, Jul. 2005.

[19] B.-C. Liu, T.-I. Chen, and C.-H. Liu, "A cell separation chip using micro-structures filter and multi-frequencies dielectrophoresis," *Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS '05. The 13th International Conference on*, vol. 2, pp. 1733–1736, Jun. 2005.

[20] J. T. Y. Lin, W. Wan, and J. T. W. Yeow, "Working towards a sample preparation device with carbon nanotubes," *Nanotechnology, 2007. IEEE-NANO 2007. 7th IEEE Conference on*, pp. 116–121, Aug. 2007.

[21] T.-C. Shih, K.-H. Chu, and C.-H. Liu, "A programmable biochip for the applications of trapping and adaptive multisorting using dielectrophoresis array," *Journal of Microelectromechanical Systems*, vol. 16, no. 4, pp. 816–825, Aug. 2007.

[22] J. Andrade, "Design of an electronic circuit driver for a multiple stages dielectrophoretic filter," M. of Sc. thesis, Instituto Tecnológico y de Estudios Superiores de Monterrey, Monterrey, Mexico, 2008, to be published.

[23] H. Liao, J. Yu, J. Wang, J. Chen, Y. Liao, and J. Yi, "A system platform design of travelling wave dielectrophoresis microchip based on sopc," in *Computer Science and Software Engineering, 2008 International Conference on*, vol. 4, Dec. 2008, pp. 66 –69.

[24] M. Khorasani, M. Behnam, L. van den Berg, C. Backhouse, and D. Elliott, "High-voltage CMOS controller for microfluidics," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 3, no. 2, pp. 89 –96, Apr. 2009.

[25] H. Wake and M. Brooke, "Low voltage electrophoresis on a CMOS chip," in *Circuits and Systems, 2007. MWSCAS 2007. 50th Midwest Symposium on*, Aug. 2007, pp. 1042 –1045.

[26] T.-Y. Chao and C.-H. Liu, "Microfluidic-driving multi-function manipulation array of micro-scale biological sample via ac electroosmosis," in *Solid-State Sensors, Actuators and Microsystems Conference, 2009. TRANSDUCERS 2009. International*, Jun. 2009, pp. 624 –627.

[27] M. Miled and M. Sawan, "A new CMOS/microfluidic interface for cells manipulation and separation in LoC devices," in *Quality Electronic Design (ASQED), 2010 2nd Asia Symposium on*, Aug. 2010, pp. 194 –197.

[28] L. Zheng, S. Li, P. Burke, and J. Brody, "Towards single molecule manipulation with dielectrophoresis using nanoelectrodes," *Nanotechnology, 2003. IEEE-NANO 2003. 2003 Third IEEE Conference on*, vol. 2, pp. 437–440, Aug. 2003.

[29] M. Al-Ibrahim and A. Al-Khateeb, "Digital sinusoidal oscillator with low and uniform frequency spacing," *Circuits, Devices and Systems, IEE Proceedings* -, vol. 144, no. 3, pp. 185–189, Jun 1997.

[30] M. Al-Ibrahim, "A simple recursive digital sinusoidal oscillator with uniform frequency spacing," in *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*, vol. 2, may 2001, pp. 689 –692 vol. 2.

[31] A. Bellaouar, M. O'brecht, A. Fahim, and M. Elmasry, "Low-power direct digital frequency synthesis for wireless communications," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 3, pp. 385 –390, mar 2000.

[32] E. Murphy and C. Slattery. (2004, Aug.) All about direct digital synthesis. Ask The Application Engineer - 33. [Online]. Available: http://www.analog.com/analogdialogue

[33] G. Chang, A. Rofougaran, M.-K. Ku, A. A. Abidi, and H. Samueli, "A low-power CMOS digitally synthesized 0-13Mhz agile sinewave generator," in *International Solid-State Circuits Conference, Digest*, Presidio, US, Feb. 1994, pp. 32–33.

[34] A. Yamagishi, M. Ishikawa, T. Tsukahara, and S. Date, "A 2-v,2-Ghz low-power direct digital frequency synthesizer chip set for wireless communication," in *Custom Integrated Circuits Conference*, Kanagawa, Japan, May 1995, pp. 319–322.

[35] J. Tierney, C. M. Rader, and B. Gold, "A digital frequency synthesizer," *IEEE Trans. Audio Electroacoust.*, vol. 19, no. 1, pp. 48–57, Mar. 1971.

[36] L. Chunming, "Doctoral dissertation," Ph.D. dissertation, Harbin Institute of Technology, Harbin, China, 1995.

[37] L. Min and L. Yalu, "A method for calculating total harmonic distortion of digital sinusoidal waveform," in *Electronic Measurement and Instruments, 2007. ICEMI '07. 8th International Conference on*, 16 2007-July 18 2007, pp. 3–947–3–951.

[38] M. Schanerberger and S. Awad, "The implementation of a digital sine wave oscillator using the TMS320C25: distortion reduction and applications," *Instrumentation and Measurement, IEEE Transactions on*, vol. 39, no. 6, pp. 870–873, Dec 1990.

[39] B. Linares-Barranco, A. Rodriguez-Vazquez, E. Sanchez-Sinencio, and J. Huertas, "Generation, design and tuning of OTA-C high frequency sinusoidal oscillators," *Circuits, Devices and Systems, IEE Proceedings G*, vol. 139, no. 5, pp. 557–568, Oct. 1992.

[40] B. Linares-Barranco, "Design of high frequency transconductance mode CMOS voltage controlled oscillators," Ph.D. dissertation, University of Seville, Seville, Spain, May 1990.

[41] B. Linares-Barranco, A. Rodriguez-Vazquez, E. Sanchez-Sinencio, and J. Huertas, "A 10 Mhz voltage-controlled OTA quadrature oscillator," *Electronics Letters*, vol. 25, no. 12, pp. 765–767, Jun. 1989.

[42] R. M. J.W. Fattaruso, "Triangle-to-sine wave conversion with MOS technology," *Solid-State Circuits, IEEE Journal of*, vol. 20, no. 2, pp. 623 – 631, Apr 1985.

[43] S. Franco, *Design with operational amplifiers and analog integrated circuits*, 3rd ed. Boston, MA: McGraw Hill, 2003.

[44] Z. Tang, O. Ishizuka, and H. Matsumoto, "MOS triangle-to-sine wave convertor based on subthreshold operation," *Electronics Letters*, vol. 26, no. 23, pp. 1983 –1985, nov. 1990.

[45] R. Meyer, W. Sansen, and S. Peeters, "The differential pair as a triangle-sine wave converter," *Solid-State Circuits, IEEE Journal of*, vol. 11, no. 3, pp. 418 – 420, jun 1976.

[46] R. Gregorian and G. C.Temes, *MOS operational amplifiers, Analog MOS integrated circuits for signal processing.* New York, United states of America: A Wiley - Interscience publication, 1986.

[47] M. Tavakoli and R. Sarpeshkar, "A sinh resistor and its application to tanh linearization," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 2, pp. 536 – 543, feb. 2005.

[48] P. Furth and H. Ommani, "Low-voltage highly-linear transconductor design in subthreshold CMOS," in *Circuits and Systems, 1997. Proceedings of the 40th Midwest Symposium on*, vol. 1, aug 1997, pp. 156 –159 vol.1.

[49] V. Ugaz, R. Elms, R. Lo, F. Shaikh, and M. Burns, "Microfabricated electrophoresis systems for dna sequencing and genotyping applications: current technology and future directions." *PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A-MATHEMATICAL PHYSICAL AND ENGINEERING SCIENCES*, vol. 362, no. 1818, pp. 1105 – 1129.

[50] H. A. Pohl, *Dielectrophoresis*. Cambridge, U.K.: Cambridge University Press, 1978.

[51] P. Gascoyne and J. Vykoukal, "Dielectrophoresis-based sample handling in general-purpose programmable diagnostic instruments," *Proceedings of the IEEE*, vol. 92, no. 1, pp. 22 – 42, Jan. 2004.

[52] P. Gascoyne, W.-B. Wang, Y. Huang, and F. Becker, "Dielectrophoretic separation of cancer cells from blood," in *Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE*, vol. 2, Oct. 1995, pp. 1366 –1373 vol.2.

[53] G. H. Markx, Y. Huang, X.-F. Zhou, and R. Pethig, "Dielectrophoretic characterization and separation of micro-organisms," *Microbiology*, vol. 140, no. 3, pp. 585–591, 1994. [Online]. Available: http://mic.sgmjournals.org/cgi/content/abstract/140/3/585

[54] M. P. Hughes, "Nanoparticle manipulation by electrostatic forces," in *Handbook of Nanoscience, Engineering, and Technology*, W. A. G. III, D. W. Brenner, S. E. Lyshevski, and G. J. Iafrate, Eds. Boca Raton, Fl.: CRC Press, 2003, ch. 16, pp. 1–32.

[55] B. J. Parc and M. J. Madou, "3-D electrode designs for flow-through dielectrophoretic systems," in *Microfluidic applications in biology : from technologies to systems biology*, N. Lion, J. S. Rossier, and H. H. Girault, Eds. Germany: Wiley-VCH, 2002, ch. 17, pp. 253–273.

[56] C.-H. Chuang, C.-H. Wei, Y.-M. Hsu, and J.-T. Lu, "Multilayer electrodes DEP chip for single-cell level impedance measurement," *NEMS '07. 2nd IEEE International Conference on Nano/Micro Engineered and Molecular Systems, 2007.*, pp. 821–825, Jan. 2007.

[57] *Insulator-based dielectrophoretic particle separator and concentrator - iDEP*, Fact Sheet, Sandia National Laboratories, Livermore, CA, 2005. [Online]. Available: www.sandia.gov/news/publications/fact/idep2005-5329p.pdf

[58] (2005) Novel dielectrophoresis device may revolutionize sample preparation. [Online]. Available: http://medgadget.com/archives/2005/08/novel_dielectro.html

[59] B. H. Lapizco-Encinas, B. A. Simmons, and E. B. C. Y. Fintschenko, "Insulator-based dielectrophoresis for the selective concentration and separation of live bacteria in water," *Electrophoresis*, vol. 25, pp. 1695 – 1704, Jun. 2004.

[60] E. B. Cummings and A. K. Singh, "Dielectrophoresis in microchips containing arrays of insulating posts: Theoretical and experimental results," *Analytical Chemistry*, vol. 75, pp. 4724–4731, Sep. 2003.

[61] G. J. McGraw, R. V. Davalos, J. D. Brazzle, J. Hachman, M. Hunter, J. Chames, G. J. Fiechtner, E. B. Cummings, Y. Fintschenko, and B. A. Simmons, "Polymeric insulator-based dielectrophoresis (iDEP) for the monitoring of water-borne pathogens," in *Micromachining and Microfabication Process Technology X*, M. A. Maher and H. D. Stewart, Eds. Bellingham: pie-Int Society Optical Engineering, 2005, pp. 59–68.

[62] H. Shafiee, M. B. Sano, E. A. Henslee, J. L. Caldwell, and R. V. Davalos, "Selective isolation of live/dead cells using contactless dielectrophoresis (cdep)." *Lab On A Chip*, vol. 10, no. 4, pp. 438 – 445, 2010.

[63] D. E. Chang, S. Lorie, and I. Mezie., "Separation of bioparticles using the travelling wave dielectrophoresis with multiple frequencies," *Decision and Control, 2003. Proceedings. 42nd IEEE Conference on*, vol. 6, pp. 6448–6453, Dec. 2003.

[64] *LeonardoSpectrum User's Manual*, Mentor Graphics, Dec. 2008.

[65] *ICStation Reference Manual*, Mentor Graphics, 2009.

[66] "DAC902 data sheet," Texas Instruments. [Online]. Available: http://www.ti.com

[67] "AD811 data sheet," Analog Devices. [Online]. Available: http://www.analog.com

[68] (2010) austriamicrosystems ag. [Online]. Available: http://www.austriamicosystems.com/

[69] D. O'Riordan, *Recommended Spectre Monte Carlo Modeling Methodology*, downloaded from www.designers-guide.org, Cadence Designed Systems, 2003.

[70] A. Nedungadi and T. Viswanathan, "Design of linear CMOS transconductance elements," *Circuits and Systems, IEEE Transactions on*, vol. 31, no. 10, pp. 891–894, Oct 1984.

[71] Y. Huang, E. Drakakis, and C. Toumazou, "A wide tuning range CMOS oscillator for an optoelectronic retinal prosthesis system," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, may 2007, pp. 2359 –2362.

[72] T. Serrano-Gotarredona and B. Linares-Barranco, "7-decade tuning range CMOS OTA-C sinusoidal VCO," *Electronics Letters*, vol. 34, no. 17, pp. 1621 –1622, aug 1998.

[73] L. Gallin-Martel, D. Dzahini, F. Rarbi, and O. Rossetto, "A low power 5 ms/s 14 bit switched capacitors digital to analog converter," in *IC Design and Technology (ICICDT), 2010 IEEE International Conference on*, june 2010, pp. 240 –243.

[74] C. Saint and J. Saint, *IC Mask Design, Essential Layout Techniques*. New York: McGraw HIll, 2002.

[75] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd ed. New York, Oxford: Oxford University Press, 2002.

[76] A. Kumar and A. Bhardwaj, "Methods in cell separation for biomedical application: cryogels as a new tool," *IOP Biomedical Materials, electronic journals*, no. 3, pp. 1–11, Aug. 2008.

[77] H. T. Soh, J. Y. J. Wang, U. Kim, X. S. Hu, and J. Q. andCarl Meinhart, "Dielectrophoretic particle sorter," U.S. Patent WO/2006/058 245, Jan. 06, 2006.

[78] J. H. Kang and J.-K. Park, "Technical paper on microfluidic devices - cell separation technology," *Asia Pacific Biotech News*, vol. 9, no. 21, pp. 1135–1146, 2005.

[79] C. Wang, G. Jia, L. Taherabadi, and M. Madou, "A novel method for the fabrication of high-aspect ratio C-MEMS structures," *Microelectromechanical Systems, Journal of*, vol. 14, no. 2, pp. 348 – 358, april 2005.

[80] R. Martinez-Duarte, R. A. Gorkin, K. Abi-Samra, and M. J. Madou, "The integration of 3D carbon-electrode dielectrophoresis on a CD-like centrifugal microfluidic platform." *Lab Chip*, vol. 10, no. 8, pp. 1030–43, 2010. [Online]. Available: http://www.biomedsearch.com/nih/integration-3D-carbon-electrode-dielectrophoresis/

[81] H. Sato, H. Matsumura, S. Keino, and S. Shoji, "An all SU-8 microfluidic chip with built-in 3D fine microstructures," *Journal of Micromechanics and Microengineering*, vol. 16, no. 11, p. 2318, 2006.

[82] G. Najafpour, *Biochemical Engineering and Biotechnology*. Amsterdam, The Netherlands: Elsevier, 2007.

[83] J. Urrieta-Saltijeral, C. Dussap, A. Pons, C. Creuly, and J. Gros, "Metabolic flux modelling as a tool to analyse the behavior of a genetically modified strain of *Sacchaaccharomyces Cerevisiae*," in *Engineering and Manufacturing for Biotechnology*, ser. Focus on Biotechnology, M. Hofman, J. Anné, M. Cuyper, J. W. M. Bulte, M. Hofman, and P. Thonart, Eds. Springer Netherlands, 2002, vol. 4, pp. 143–156.

[84] M. Urdaneta and E. Smela, "Multiple frequency dielectrophoresis," *Electrophoresis*, vol. 28, no. 18, pp. 3145–3155, 2007.

[85] I. Ermolina and H. Morgan, "The electrokinetic properties of latex particles: comparison of electrophoresis and dielectrophoresis," *Journal of Colloid and Interface Science*, vol. 285, no. 1, pp. 419–428, MAY 1 2005.

[86] J. Gomez-Quinones, H. Moncada-Hernandez, R. M.-D. Olivier Rossetto, B. H. Lapizco-Encinas, M. Madou, and S. O. Martinez-Chapa, "An application specific multi-channel stimulator for electrokinetically-driven microfluidic devices," in *The 9th IEEE International NEWCAS Conference*, Bordeaux, France, Jun. 2011.

[87] T. B. Jones, *Electromechanics of particles*. New York: Cambridge University Press, 1995.

[88] J. Gomez-Quinones, V. H. Perez-Gonzalez, H. Moncada-Hernandez, O. Rossetto, G. Dieck-Assad, and S. O. Martinez-Chapa., "A multi-channel sinusoidal generator for electrokinetic stimulation of microfluidic platforms," in *The Electronics Robotics and Automotive Mechanics Conference CERMA*, Cuernavaca, Mexico, Nov. 2011.

[89] B. Linares-Barranco, A. Rodriguez-Vazquez, E. Sanchez-Sinencio, and J. Huertas, "CMOS OTA-C high-frequency sinusoidal oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 26, no. 2, pp. 160–165, Feb 1991.