The 90 nm Double-DICE Storage Element To Reduce Single-Event Upsets

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Abstract — **In this paper, we introduce the Double-DICE storage element, which reduces charge sharing and collecting between the sensitive nodes of sensitive pairs in a Dual Interlocked Cell (DICE) storage cell in 90 nm technology. Interleaving two DICE storage cells in layout separates sensitive nodes by 8.5 μm, which is well beyond the minimum required of 5 μm shown in an earlier work. This reduces the probability of charge collecting in a sensitive pair in one DICE caused by a Single-Event strike. An area savings of 33.3 % results as compared to the case where no interleaving is used with the same nodal separation.**

I. INTRODUCTION

Ionizing radiation can cause unwanted effects in semiconductor devices, such as flipping the state of memory cells if sensitive nodes are stricken or cumulative effects such as trapped charges induced by radiation accumulate. Accordingly, the effect of radiation falls into one of two major categories: Total Ionizing Dose (TID) and Single-Event Upset (SEU). TID refers to the cumulative effect described above. As technology has scaled and gate oxides have become very thin, TID hardness has improved since the small feature sizes make it difficult for trapped charges to accumulate. On the other hand, SEU has become more problematic since small feature sizes translate to smaller capacitances and held charges, meaning radiation events of smaller energies can upset vulnerable nodes. Over the past two decades, different Radiation-Hardened-by-Design (RHBD) approaches, such as Triple Modular Redundancy (TMR) [1], Temporal Latch [2], or Dual Interlocked Cell (DICE) [3], shown in Fig. 1, have been proposed. The latter one is a well-known storage cell design that uses redundancy to overcome susceptibility to upset. If a radiation particle strikes a sensitive node (drain of a NMOS or a PMOS in off mode), and it loses its charge, the redundant nodes restore the state of this affected node and prevent an upset in the storage cell logic. The DICE design provides excellent protection against SEU for sub-micron technologies, where a single radiation strike results in charge collection at only one node.
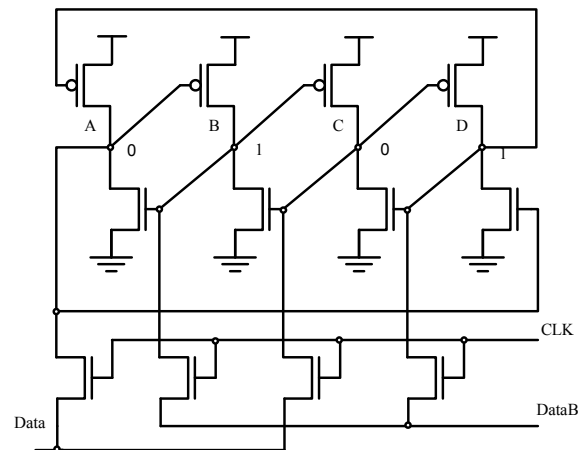

Fig. 1. The DICE Storage Cell [3]

As technologies scale down to the deep sub-micron regime, nodal charge and device spacing are reduced as a consequence of feature size reduction. These characteristics can result in charge collecting and charge sharing in multiple nodes [4]-[6]. Recent studies have shown that bipolar amplification between PMOS devices due to the n-well potential collapse and charge diffusion between NMOS devices in the case of a single strike are the main charge sharing mechanisms [7]. Through 3-D Technology Computer-Aided Design (TCAD) simulations, Amusan et al., showed that the n-well potential collapse from an angular strike with a Linear Energy Transfer (LET) of 21 MeV.cm^2/mg can extend as far as 5 μm from the strike location for a 90 nm technology [8]. Therefore, any hardened design with sensitive PMOS pairs located within this distance are susceptible to parasitic bipolar effects. Even a heavily contacted N-well can not effectively keep the well potential sufficiently high at all points and prevent collapse. As intuition would also support, it has been shown experimentally by the same group that nodal separation between sensitive pairs in a DICE element improves the tolerance to single-event soft errors [9]. Thus, if the sensitive nodes are known in a circuit, one effective SEU

mitigation technique is proper separation of these nodes above a given threshold [10]-[11].

In this paper we use a layout technique to reduce susceptibility to upsets for DICE elements in 90 nm technology. The technique involves the interleaving of two DICE cells at a layout level to meet the required spacing between sensitive nodes in an area-efficient manner. By interleaving two cells, the separation of sensitive nodes can be accomplished without the arbitrary wasting of area to space the nodes sufficiently apart. We call the new cell the "Double-DICE" storage element. We have designed the Double-DICE layout in a manner that is consistent with standard cell library practices. Therefore, this cell can be easily integrated into a 90 nm standard cell library and used in a regular ASIC design flow using synthesis and place&route tools.

The remainder of the paper is organized as follows: Section II reviews the structure of the DICE storage element; Section III presents the design of the Double-DICE storage element; Section IV presents and discusses the results; Section V talks about future work and technology scaling issues; and Section VI concludes the paper.

II. THE DICE STORAGE ELEMENT

The DICE design has been widely used due to its excellent SEU hardness and not being dependent on optimal transistor sizing. Two fundamental concepts are used in this design. First, redundancy provides a source of uncorrupted data after a single-event strike. Second, data in the uncorrupted section provides state restoring feedback to recover the corrupted data. The DICE design has four nodes (A, B, C and D in Fig. 1) that store the data as two pairs of complementary values, effectively comprising a pair of bi-stable latches, which is the essential element to all storage elements. In write and read operations, these complementary pairs are accessed simultaneously through four NMOS pass gates. We call the complementary pairs (e.g. A and C, B and D) sensitive pairs in this paper, since simultaneous changes in both of the nodes in one of these pairs will upset the state of the cell. Therefore, these nodes should be placed far enough from one another to prevent the value changing in both of them due to one single-event strike.

III. THE DOUBLE-DICE STORAGE ELEMENT

The central idea of this paper is to make the DICE design more resistant to SEU by exploiting the interleaving of the sensitive nodes of one DICE with sensitive nodes of another DICE to separate the nodes of a sensitive pair in an area-efficient manner. In this way charge sharing between adjacent devices is not the problem anymore, since each cell is immune to charge collection in more than one node. This method saves area, because the otherwise empty spaces between the separated devices are filled with circuitry from another DICE. The main disadvantage to this approach is that more complicated wiring, including higher-level metals usually reserved for top-level routing, may be needed to complete all necessary connections within the Double-DICE cell. With limited cell height restrictions, higher-level metal layers may be needed since all the connections between nodes must traverse distances over other nodes. However, as will be shown below for our target library, we were able to avoid using higher-level metals for the 90 nm technology.

IV. IMPLEMENTATION AND RESULTS

We used the NAND-based DICE design, shown in Fig. 2 [8], [12], since it is a robust design even with minimum sizing. This design uses two inverters instead of the four NMOS pass gates shown in Fig. 1 and thus needs only single-ended inputs instead of differential inputs. In order to separate sensitive nodes in a sensitive pair, each DICE cell was broken into two identical blocks (or tiles), as shown in the dotted box of Fig. 2. Each tile contains two sensitive nodes from two different sensitive pairs (e.g. A and B or C and D nodes in Fig. 1).

We have implemented a Double-DICE latch and a Double-DICE flip-flop by interleaving the tiles from two different DICE cells. The cells were laid out using the Cadence layout editor in IBM 90 nm technology. Each tile is 4.26 µm wide. Interleaving these tiles from two different DICE elements separates sensitive nodes by 8.5 µm. Only metal 1 and metal 2 were used in this design, reserving the higher level metal layers for top level routings.

The layout of one tile (half of a DICE cell) and the Double-DICE latch are shown in parts a and b of Fig. 3, respectively.

The total area of one Double-DICE latch is compared to the area of two DICE latches with the sensitive node separations of 8.5 µm and 5µm (minimum suggested distance between sensitive nodes [8]) in Table 1.

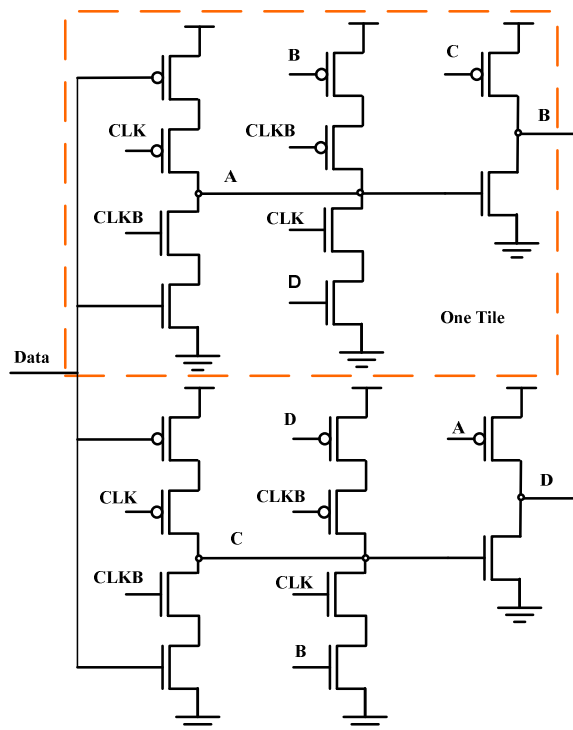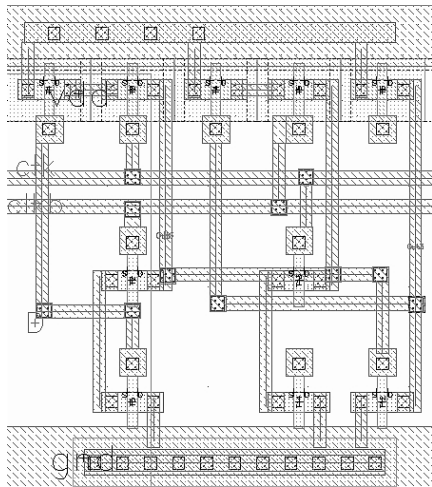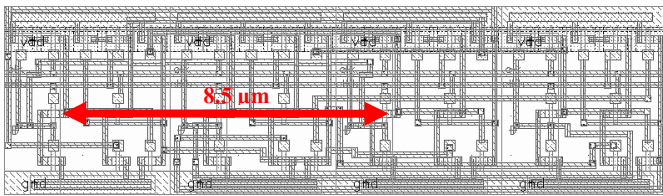Fig.2. One DICE latch is composed of two identical tiles

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(a)

8.5 μm

(b)

Fig.3. a) Tile Layout b) Double-DICE latch layout with 8.5 μm separation between two sensitive nodes

Table 1 shows that the Double-DICE latch has 33.33 % less area compared to a pair of DICE latches with a sensitive nodal distance of 8.5 μm; the area saving drops to 8 % when a sensitive nodal separation of 5 μm is used. This means that we could make DICE latches more tolerant to SEU without compromising area. Indeed, a significant area savings results. The total area of one Double-DICE flip-flop is 167.66 μm². Although intuitively we would not expect much impact on performance with the slightly longer wires connecting nodes in the Double-DICE design, we conducted simulations to confirm that assumption. The Double-DICE and DICE flip-flop performances are shown in Table 2. From SPICE simulations, Clock to Q delays are measured for a DICE and a Double-DICE flip-flop at a clock rate of 500 MHz and data rate of 250 MHz.

It can be seen from Table 2 that interleaving and adding additional routing has some non-negligible impact on the Clock to Q delay. To see this impact we conducted post layout simulations. The increases in Clock to Q delay for rise and fall edges are only 23 and 28 percent, respectively. The extra immunity offered by the nodal separation distance far outweighs this minor speed penalty, though. Moreover, this result implies that the Double-DICE flip-flop is still fast enough to operate in the GHz range.

In this work we implemented the Double DICE Latch and flip-flop, but the same method can be easily applied to other storage cell elements based on the redundant bi-stable latch concept. For instance if one were using redundant bi-stable latches as the basis of radiation-tolerant SRAM cells, by interleaving every two bits of memory in the SRAM, the whole SRAM could be made more immune to SEU without compromising space or memory capacitance.

TABLE 1. Area Comparison

Structure	Double-DICE latch	2 DICE latches nodal distance 8.5 μm	2 DICE latches nodal distance 5 μm
Total area μm²	81.79	122.688	88.9

TABLE 2. Performance Comparison from post layout simulations

Structure	DICE Flip-Flop	Double-DICE Flip-Flop	Change
Clock to Q Delay (rise) ps	86	113	23%
Clock to Q Delay (fall) ps	118	165	28%

V. TECHNOLOGY SCALING

In this layout configuration we have shown that the sensitive nodal separation is close to double that of the suggested distance for 90 nm technology. This result provides a very good immunity margin.

As we move to smaller technologies, the distance required for mitigating SEUs in sensitive nodes increases while the nodes actually become closer together in layout, assuming proportional scaling based on feature size. Consequently the immunity margin shrinks to a smaller value. As long as the sensitive nodal separation falls in the immunity margin, the same Double-DICE storage element can be used for such smaller feature sizes. For example if 65 nm technology is used, the width of a tile is around 2.84 μm. Accordingly, the distance between the sensitive nodes becomes approximately 5.7 μm in the Double DICE design. Assuming the same 5 μm sensitive nodal separation distance is still effective for this technology, the resulting nodal separation is sufficient, albeit with little margin. However, if the required sensitive nodal separation exceeds the resulting layout distance then interleaving of more than two storage elements is needed to meet the required distance. For example, for 45 nm, interleaving of four DICE cells may be required. This will change the Double DICE storage element to a Quadrature-DICE storage element, shown in Fig. 4.

Therefore, as technology scales down, the number of interleaved elements, as well as the amount of wiring, must increase to maintain an adequate separation of sensitive nodes. Thus, the use of higher metal levels may be needed. This effect may cause a problem for standard cell routing tools which will now be restricted from using those higher-level metals, at least when routing signals over such Quadrature-DICE cells. However, once again the benefit of increased

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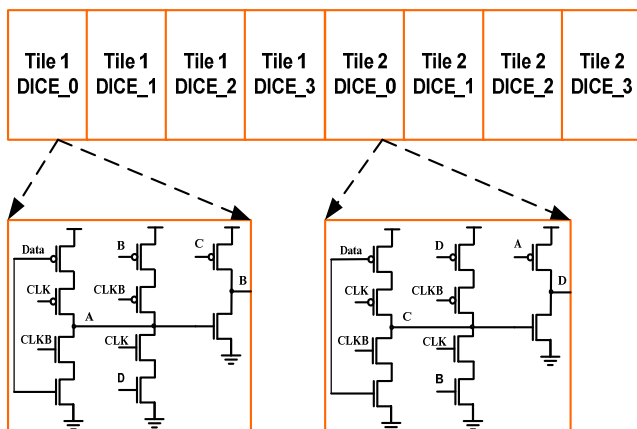immunity to SEU will probably far outweigh this disadvantage.

Fig 4. Quadrature-DICE Latch. Interleaving four different DICE latches.

VI. CONCLUSION

We proposed a Dual-DICE design, which interleaves two DICE storage cells to make them more resistant to upsets caused by charge sharing and creation of lateral parasitic bipolar transistors in multiple PMOS devices in deep sub-micron technologies. The fact that the sensitive nodes and pairs are known in the DICE design and its symmetric structure make the interdigitation easy and feasible. In this design we attained a nodal separation distance of 8.5 µm, which is 70% greater than the distance separation required for precluding SEU in 90 nm technology. The design provides an area savings as compared to the alternative approach and results in a very small Clock to Q delay overhead. The area savings of the Dual-DICE as compared to an alternative approach of using two separate DICE elements that are not interleaved is 33.3 % with a sensitive nodal separation of 8.5 µm and 8 % for the minimum nodal separation (5 µm).

As technology scales, the required nodal separation increases while nodal distances in layout decreases. With the margin we have in the presented Double-DICE design, it is possible to use the same design for smaller technologies when the required nodal separation is within the immune margin. Otherwise, more than two storage elements should be interleaved, which may require more complicated wiring and use of higher metal layers for routing.

REFERENCES

[1] W. Peterson,"Error-Correcting Code', 2nd edittion. Cambridge, MA: MIT Press, 1980, p.560

[2] D.G. Mavis, P.H. Eaton, "Soft error rate mitigation techniques for modern microcircuits", Reliability Physics Symposium Proceedings, 40th Annual, 7-11 April 2002, pp. 216-225

[3] T.Calin, M. Nicolaidis, and R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology", IEEE Transactions on Nuclear Science, Vol 43, No. 6, December 1996, pp. 2874-2878

[4] R. Valazco, T. Calin, M. Nicolaidis, S.C. Moss, S.D. LaLumondiere, V. T. Tran, and R. Koga, "SEU-hardened storage cell validation using a pulsed laser", IEEE Trans. Nucl. Sci., Vol. 43, No. 6, pp. 2843-2848, Dec 1996.

[5] J. Benedetto, C. Salomonson-Begay, and P. McGuirk, "Single event upset hardening limitations in deep sub-micron digital designs due to critical node crowding", presented at the Hardened Electronics Radiation Technology (HEART), Tampa, FL, Mar. 2005.

[6] B.D. Olson, D. R. Ball, K. M. Warren, L. W. Massengill, N. F. Haddad, S. E. Doyle, and D. McMorrow, "Simultaneous single event charge sharing and parasitic bipolar conduction in a highly-scaled SRAM design", IEEE Trans. Nucl. Sci., Vol. 52, No. 6, pp. 2132-2136, Dec. 2005

[7] O. A. Amusan, A.F. Witulski, L.W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, "Charge collection and charge sharing in a 130 nm CMOS technology", IEEE Trans. Nucl. Sci., Vol. 53, No. 6 , pp. 3253-3258, Dec. 2006.

[8] O. A. Amusan, L. W. Massengill, M. P. Baze, B. L. Bhuva, A. F. Witulski, S. DasGupta, et all. " Directional sensitivity of single event upset in a 90 nm CMOS due to charge sharing", IEEE Trans. Nucl. Sci., Vol. 54, No. 6, pp. 2584-2589, Dec. 2007.

[9] O. A. Amusan, L. W. Massengill, M. P. Baze, B. L. Bhuva, A. F. Witulski, J. D. Black, et all. "Mitigation techniques for single event induced charge sharing in a 90 nm bulk CMOS process", IEEE Physics Symposuim, Phoenix, 2008.

[10] J. E. Knudsen, L. T. Clark, "An Area and Power Efficient Radiation Hardened by Design Flip-Flop", IEEE Trans. Nucl Sci., Vol.53, No.6, pp.3392-3399, Dec. 2006

[11] T. Chen, J. Chen, L. T. Clark,J. E. K.,G.Samson, "Ultra-Low Power Radiation Hardened by Design Memory Circuits", IEEE Trans. Nucl Sci., Vol.54, No.6, pp.2004-2011, Dec.2007

[12] R. Naseer, J. Draper, "The DF-DICE storage element for immunity to soft errors", Midwest Symposium on Circuit and Systems, Vol. 1, pp. 303-306, Aug. 2005.