Diffusion Barrier Cladding in Si/SiGe Resonant Interband Tunneling Diodes and Their Patterned Growth on PMOS Source/Drain Regions

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***Abstract*—Si/SiGe resonant interband tunnel diodes (RITDs) employing δ-doping spikes that demonstrate negative differential resistance (NDR) at room temperature are presented. Efforts have focused on improving the tunnel diode peak-to-valley current ratio (PVCR) figure-of-merit, as well as addressing issues of manufacturability and CMOS integration. Thin SiGe layers sandwiching the B δ-doping spike used to suppress B out-diffusion are discussed. A room-temperature PVCR of 3.6 was measured with a peak current density of 0.3 kA/cm^2. Results clearly show that by introducing SiGe layers to clad the B δ-doping layer, B diffusion is suppressed during post-growth annealing, which raises the thermal budget. A higher RTA temperature appears to be more effective in reducing defects and results in a lower valley current and higher PVCR. RITDs grown by selective area molecular beam epitaxy (MBE) have been realized inside of low-temperature oxide openings, with performance comparable with RITDs grown on bulk substrates.**

***Index Terms*—CMOS compatibilty, dopant diffusion, Ge-Si alloys, low-temperature oxide, molecular beam epitaxy, negative differential resistance, patterned growth, rapid thermal annealing, resonant interband tunneling diodes, silicon.**

I. Introduction

SINCE the development of the Esaki diode in 1958 based on interband tunneling [1], the tunnel diode has been an additional option for the circuit designer, with its unusual negative differential resistance (NDR) property. Its folded current–voltage (I–V) characteristic facilitates such circuit elements as simple latches by the serial connection of two tunnel diodes [2]. Furthermore, the tunneling phenomenon is a majority carrier effect and is not governed by conventional transit time effects, but due to a lack of robust manufacturing techniques and compatibility with Si CMOS processing, the discrete Esaki tunnel diode has become relegated to niche applications, such as local oscillators and frequency locking circuits.

The development of the resonant tunneling diode (RTD) in 1974 based upon intraband tunneling using double barriers [3] provided an alternative pathway, using electron confinement within the conduction band through bandgap engineering, by harnessing advancements in epitaxial growth techniques in the late 1960s and early 1970s. This approach works well for the III–V compound semiconductor material systems, where significant conduction band offsets are possible.

The union of tunnel diodes and transistors into monolithic circuits has demonstrated new circuit architectures that i) reduce component count, ii) speed circuit switching, and iii) reduce power consumption. The end result is more computational power per unit area than a transistor-only circuit topology. Some circuit examples that have been demonstrated using III–V RTDs are ultra-low power refresh-free tunnel diode SRAM circuits [4] and compact A/D converters [5]. This approach will become increasingly attractive to the CMOS community if a viable Si-based tunnel diode can be added in a simple manner after the high-temperature CMOS steps were concluded [6]. Adding an Si-based tunnel diode is viewed as one potential avenue by the CMOS community to extend the technology roadmap [7], [8].

Until recently, a viable Si-based tunnel diode for integration with CMOS has eluded investigation. Some of the first attempts explored Si-based RTDs. For intraband tunneling, the natural heterojunction system is Si/SiGe, but due to a small conduction band offset between Si and Ge, the achievable electron confinement reported is below 150 meV with the use of thick relaxed SiGe buffer layers to engineer the strain energy to place the Si wells and Si barriers under compressive strain. Initial reports on Si-based RTD's demonstrated a peak-to-valley current ratio (PVCR) of 1.2 at room temperature [9]. Nevertheless, some recent progress is advancing the state-of-the art in Si/SiGe RTDs with PVCRs reported up to 2.9 [10].

Research on alternative Si-based RTDs is seeking a suitable wide bandgap barrier that is also compatible with crystalline

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Si wells, but this presents a daunting epitaxial growth problem. Some Si-based RTD structures used SiO_2 [11], [12] or Al_2O_3 [13] barriers, but severe constraints on epitaxial overgrowth of a thin (<5 nm) crystalline Si quantum well atop the amorphous oxide barrier as well as the Si/oxide interface roughness have hampered progress [14]. A more promising avenue amongst recent Si-based RTD investigations is exploring alternative barriers such as CaF_2 that do permit epitaxial overgrowth of crystalline Si, but epitaxial growth of the CaF_2 is on $\langle 111 \rangle$ Si substrates, which are not CMOS compatible [15], [16].

An interesting approach that is gaining attention is a paradigm shift back to an Esaki-like interband tunnel diode. This effectively replaces the challenging epitaxy found in the Si-based RTDs with a new challenge of achieving degenerate doping during a near-equilibrium epitaxial growth technique. The discrete Esaki tunnel diodes of the 1960s using alloying techniques have set benchmarks for Si Esaki diodes with room-temperature PVCR as high as 4.0 [17] and Ge Esaki diodes with PVCR of 8.3 [18]. A modern version of the Esaki diode using spin-on glass dopant diffusion has reported PVCRs up to 2.2 that could be more promising for monolithic integration [19]. It should be noted that a PVCR beyond 3 does not increase the speed index significantly [20]. In addition, a significant advantage for interband tunnel diodes is that both elastic and inelastic scattering can contribute to valley current in an intraband tunnel diode, but only inelastic scattering can contribute to the valley current of an interband tunnel diode [20].

The first successful epitaxially grown Si-based interband tunnel diode was shown by Jorke *et al.* with a PVCR of 2 at room temperature by inserting a thin i-layer between the p^+-n^+ emitter-base junction [21], but this fine work was largely overlooked by the scientific community, as the context of the overall paper was upon bipolar junction transistors (BJTs).

Another interband tunnel diode structure was proposed by Sweeny and Xu [22] using δ-doping to create confined states in the valence and conduction bands on the p-side and n-side of a p-n junction, respectively. This creates an interband resonance tunneling condition between the states. This class of tunnel diodes was aptly named the resonant interband tunnel diode (RITD) class. An initial attempt at creating an epitaxially grown Si-based RITD using δ-doping injectors showed some bistability but no room-temperature NDR [23].

More fundamental to the success of a Si-based interband tunnel diode are the processing steps that are used that anticipate dopant segregation and diffusion during epitaxial growth and processing and minimize their detrimental effects. Eventually, dopant segregation effects [24] were overcome by the far-from-equilibrium technique of low-temperature molecular beam epitaxy (LT-MBE) [25], [26] to effectively create the first Si-based RITD [27]. This Si/SiGe RITD combined several key points: i) δ-doping injectors, ii) a composite i-layer inserted as a spacer layer between the δ-doped injectors to minimize interdiffusion, iii) LT-MBE to suppress segregation and diffusion, and iv) a short post-growth rapid thermal anneal (RTA) heat treatment to reduce point defects created during the LT-MBE process that elevate the excess current. Using this modified approach resulted in initial reports of room-temperature PVCR in Si-based RITDs using δ-doping at 1.54 with a peak current density of 3.2 kA/cm^2 [26] but quickly leaped to over 2 at a peak current density of 22 kA/cm^2 when the substrate temperature during MBE growth was further reduced [28]. A variety of alternative Si/SiGe RITDs have been demonstrated as well as some that are Si-only [28]–[30] and both polarity "n-on-p" [27]–[31] and "p-on-n" RITDs [32] as well as vertically-stacked p-n-p RITDs that exhibit symmetrical NDR about the origin for simple latches [33]. Measured peak current densities have been engineered between 0.2 A/cm^2 and 32 kA/cm^2 using Sb as the n-type dopant [27]–[33]. Antimony is greatly affected by segregation [24] during growth and a switch to P as the n-type dopant has been shown to elevate PVCR [34], [35].

These four basic points have now led other research groups to reproduce these results using other MBE growth reactors [34]–[36] and have even lead to PVCRs up to 6 at room temperature in an Si-based interband tunnel diode [35].

Further refinements to the basic RITD structure continue to maximize PVCR and integrate these structures with Si CMOS processing. To maximize the PVCR, a higher peak current density and a lower valley current density are desired. For a Si-based RITD, the peak current density is determined by the electron tunneling probability through the tunneling barrier, which depends on the dopant profile of both sides of the p-n junction. Sharper dopant profiles will lead to higher tunneling current and, thus, higher peak current density. Valley current density becomes elevated by the defects within the tunneling barrier created during the LT-MBE growth process. LT-MBE is needed to minimize dopant diffusion and segregation during epitaxy. Post-growth annealing can reduce the point defect density, thus lowering the valley current density. However, this also unfavorably broadens the dopant profiles, especially B, which is a fast interstitial diffuser, and thus, the peak current density can also be reduced if overannealed. Given that SiGe can act as an effective diffusion barrier for B in a Si matrix [37], structures with SiGe layers cladding the B δ-doping layer were grown in order to preserve the sharp B profile during high temperature post-growth annealing to reduce the point defect density. Table I summarizes the results of prior Si-based tunnel diodes in chronological order.

Preliminary attempts at integration of tunnel diodes with Si CMOS began with a hybrid approach using epitaxial lift-off and a pick-and-place technique of selectively pasting III–V RTDs onto large bond pads connected to a CMOS circuit [38]. This was effective in demonstrating the proof of principle, but due to large parasitics capacitances amounting to an aggregate capacitance of 1740 fF, which was 1681 fF higher than desired, the circuit performance gains over all-CMOS circuits were not realized. A true monolithic integration of Si-based Si/CaF_2 RTDs with Si CMOS is just beginning [39].

In this manner, the aim of this work is to raise the thermal budget of the RITDs in order to maximize the PVCR and relax monolithic integration constraints. In addition, preliminary results for selectively grown tunnel diodes onto CMOS wafers are reported.

II. Experimental

Epitaxial growth was achieved in an MBE growth system using elemental Si and Ge sources heated by electron-beams. The structures were grown on 76 mm B-doped ($\rho = 0.015$

TABLE I
COMPARISON OF PERFORMANCE, PEAK-TO-VALLEY CURRENT RATIO (PVCR) AND PEAK CURRENT DENSITY (Jp), OF Si-BASED TUNNEL DIODES REALIZED BY EPITAXIAL GROWTH TECHNIQUES IN CHRONOLOGICAL ORDER

Device Configuration	PVCR	Jp (A/cm2)	References
Si Esaki	3.80	1,000	Franks *et al.* (1965) [17]
Ge Esaki	8.30	-	Germanium Power Devices [18]
Si/SiGe RTD	1.20	400	Ismail *et al.* (1991) [9]
Si Esaki	2.00	900	Jorke *et al.* (1993) [21]
Si/SiGe RITD	1.54	3,200	Rommel *et al.* (1998) [28]
Si/SiGe RITD	2.05	22,000	Rommel *et al.* (1999) [29]
Si-only RITD	1.41	10,800	Thompson *et al.* (1999) [30]
Si-only RITD	2.05	2,300	Thompson *et al.* (1999) [31]
Si/SiGe RITD	4.20	3,000	Duschl *et al.* (1999) [34]
Si/SiGe RITD	6.00	1,500	Duschl *et al.* (2000) [35]
CaF2/CdF2 RTD	7.6×10^5	63	Watanabe *et al.* (2000) [15]
CaF2/Si/CaF2 RTD	6.30	N/A	Watanabe *et al.* (2000) [16]
Si/SiGe RTD	2.90	4,300	See *et al.* (2001) [10]
Si/SiO2 RTD	1.80	0.002	Ishikawa *et al.* (2001) [11]
Si/Al2O4 RTD	3.0-4.5	N/A	Shahjahan *et al.* (2002) [13]
Si Esaki	2.00	100	Wang *et al.* (2002) [19]
Si/SiGe RITD	3.60	300	This Work

Ω·cm–0.04 Ω·cm) Si (100) wafers. Prior to device fabrication, portions of the wafers were heat treated using a forming gas ambient (H_2/N_2) in an RTA at various temperatures for 1 min. A Ti/Au backside contact was thermally evaporated on all of the samples. Then, Ti/Au dots with a range of diameters were patterned on the surface of the wafers via standard contact lithography. A buffered oxide etch was used prior to metallization to remove the native oxide. Using the Ti/Au dots as a self-aligned mask, HF/HNO_3 wet etching was performed to define the diode mesa.

The I–V characteristics were measured using a probe station with a needle probe to make contact to the top of the mesa and the chuck to make contact to the backside contact. A semiconductor parameter analyzer was used to sweep the voltage and measure the resulting device currents.

III. RESULTS AND DISCUSSIONS

A. SiGe Diffusion Barriers Cladding the B δ-Doping Injector

Three structures were designed to study the effect of the SiGe cladding layer. All structures maintained the fundamental tunnel barrier thickness of 6 nm, as measured between the two δ-doping layers, which to first order determines the tunneling distance. RITD141, which is the control device, employed a symmetrical 1 nm Si/4 nm $Si_{0.6}Ge_{0.4}$/1 nm Si (1/4/1) spacer, as shown in Fig. 1, which is similar to many past structures studied by the authors. Fig. 2 shows RITD042 with an asymmetrical 0 nm Si/4 nm $Si_{0.6}Ge_{0.4}$/2 nm Si (0/4/2) spacer, resembling the modification provided by Duschl *et al.* [34], [35]. Note that the SiGe layer was directly grown atop the B δ-layer without the thin Si offset layer. Fig. 3 shows RITD042clad, which is the same as RITD042, except that a 1-nm $Si_{0.6}Ge_{0.4}$ cladding layer was also grown below the B δ-layer and outside the tunneling spacer. In this structure, the B δ-layer was essentially clad by thin SiGe on both sides. It should be stressed that all structures maintained the same fundamental tunnel barrier thickness of 6 nm, as measured between the two δ-doping layers, to facilitate easy comparison of the results. For all these three structures, the nominal n-type and p-type bulk doping levels in the injectors are 5×10^{19} cm^{-3}, whereas the nominal n-type and p-type δ-doping levels are 1×10^{14} cm^{-2}.

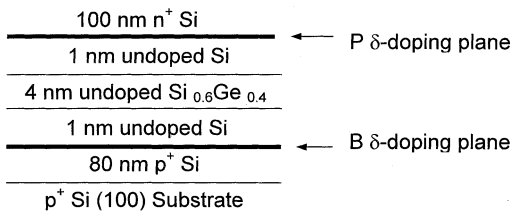

Fig. 1. Schematic diagram of RITD141, which is a (1/4/1) RITD that uses a 1-nm Si/4 nm $Si_{0.6}Ge_{0.4}$/1 nm Si undoped spacer configuration.

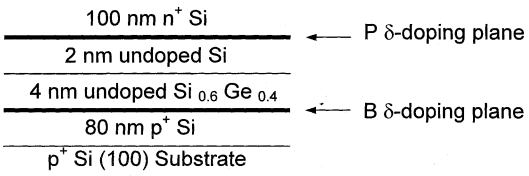

Fig. 2. Schematic diagram of RITD042, which is a (0/4/2) RITD that uses a 4–nm $Si_{0.6}Ge_{0.4}$/2 nm Si undoped spacer configuration. Note that the SiGe layer was directly grown atop the B δ-layer without the thin 1–nm Si offset layer.

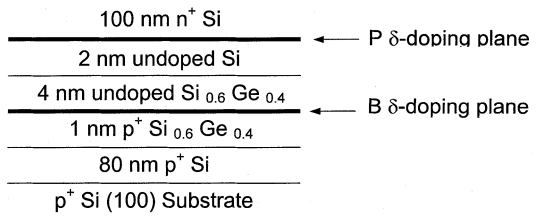

Fig. 3. Schematic diagram of RITD042clad, which is a RITD (0/4/2) with cladding layer that uses a 4–nm $Si_{0.6}Ge_{0.4}$/2 nm Si undoped spacer configuration like RITD042 but with an additional SiGe cladding layer outside the active δ-to-δ spacing. As a result, the B δ-layer was essentially clad by thin SiGe on both sides.

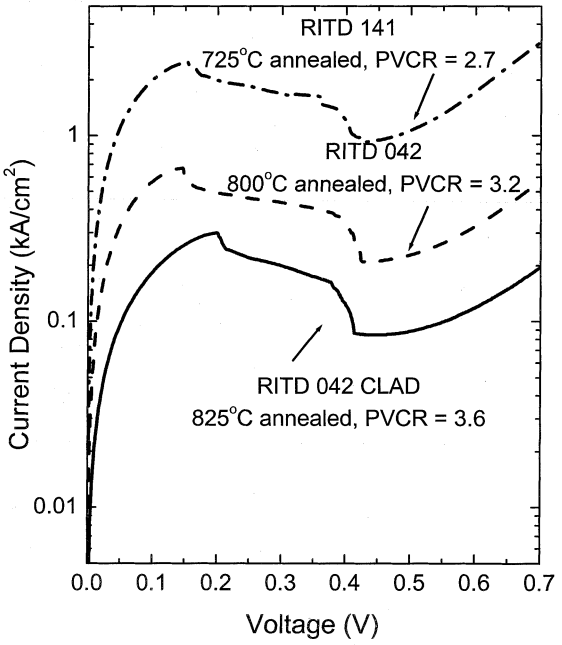

Fig. 4. Measured room-temperature I–V characteristics of the three RITD structures showing the highest PVCR for each structure. RITD141 showed a PVCR of 2.7 with a peak current density of 2.5 kA/cm^2. RITD042 showed a PVCR of 3.2 with a peak current density of 0.7 kA/cm^2. RITD042clad showed a PVCR of 3.6 with a peak current density of 0.3 kA/cm^2. Note that the optimized annealing temperatures are different for each structure, but the duration was held at 1 min each. Estimated relative uncertainties are $\pm 2\%$ in current density and $\pm 1\%$ in voltage.

Fig. 4 shows the I–V characteristics of these three structures with the highest PVCR. RITD141 demonstrates a PVCR of 2.7 with 1–min annealing at 725 °C. RITD042 obtained a PVCR of 3.2 using 1-min annealing at 800 °C, whereas RITD042clad further improved its PVCR to 3.6 with 1-min annealing at 825 °C. The peak current density was reduced with the higher anneal temperatures. It is evident that RITD042clad exhibited superior PCVR performance over structures RITD141 and RITD042 and also withstood a much higher annealing temperature. To gain insight to why the I–V characteristics of the three structures are so different, further investigation of the dopant interdiffusion was performed, both experimentally and through theoretical calculations.

Atomic concentration profiles were obtained from RITD042, which was annealed at 800 °C for 1 min, by secondary ion mass spectrometry (SIMS) using a high-performance magnetic sector secondary ion mass spectrometer. The net impact energy of the primary beam—3 keV O_2^+—was selected in order to minimize profile broadening by ion beam mixing. Depth scales were obtained from stylus profilometry ($\pm 3\%$ uncertainty). The atomic carrier concentrations of B and Sb were calibrated with implant standards ($\pm 10\%$ uncertainty).

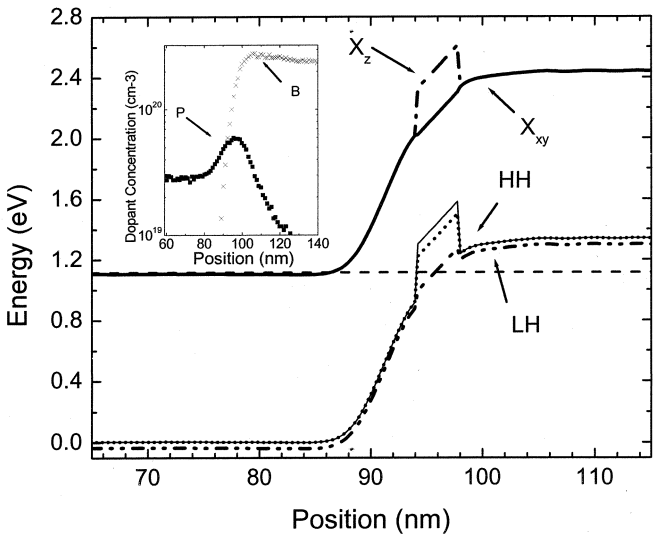

Fig. 5. Calculated band diagram using self-consistent Thomas-Fermi calculations of the electrostatic potential using a semiclasssical density-of-states and measured SIMS data of RITD042 annealed at 800 °C for 1 min. Illustrated in the band diagram are the heavy hole (HH), and light hole (LH) bands in the valence band and the X_z and X_{xy} valleys of the conduction band.

The band diagram, which is shown in Fig. 5, was calculated based on the SIMS data. These are self-consistent Thomas–Fermi calculations of the electrostatic potential using a semiclassical density of states. Due to limitations in SIMS depth resolution at the nanometer dimension, this presents a worst-case scenario for the band diagram. The resulting band diagram suggests RITD042 should work quite well. There exists significant overlap of the bands; see Fig. 5. Modeling of Structures RITD141 and RITD042clad, which are not shown, revealed band diagrams with no serious difference to RITD042. Therefore, the differences amongst the three structures should be reflected more due to changes in the out-diffusion of dopants that arise during the annealing steps as a result of their structural differences than the intrinsic structural differences.

To approach the interdiffusion from a different angle, a commercial software package [40] was employed to predict the dopant displacement during the post-growth RTA anneal. Fig. 6 illustrates the effect of adding the SiGe cladding layer adjacent to the B δ-doping layer on the B out-diffusion. An assumption was made that the diffusion starts with the as-grown B δ-doping layer having a rectangular shape with a lateral 0.2–nm waist. Cases such as no SiGe cladding layer, SiGe cladding layer on the right side of the δ-doping layer, and SiGe cladding layers on both sides are simulated. Note that not all of the curves in Fig. 6 correspond to the three structures studied here. However, the results in Fig. 6 clearly show that B out-diffusion is suppressed by SiGe cladding layers on both sides.

Fig. 7 shows the simulated Boron profile of RITD141, RITD042, and RITD042clad when subjected to a 1–min anneal at 800 °C. RITD042clad, which has SiGe cladding layers on both sides of the B δ-layer, shows the sharpest B peak as

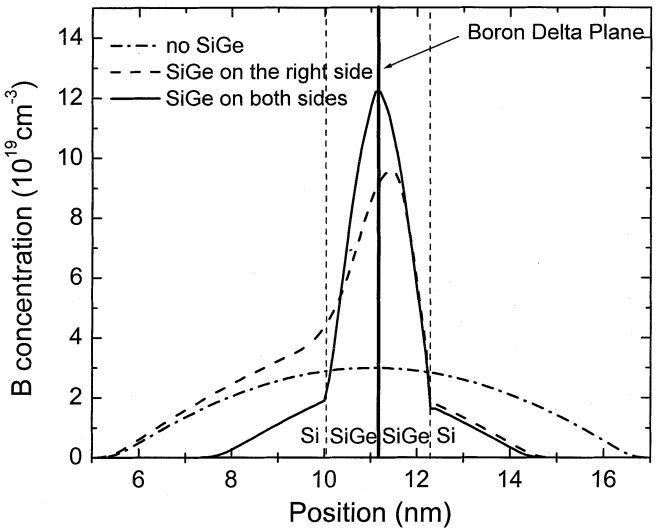

Fig. 6. Simulated B δ-doping layer diffusion i) with no SiGe cladding layer, ii) SiGe cladding layer on the right side of the δ-doping layer, and iii) SiGe cladding layers on both sides of the B profile, respectively. The as-grown δ-doping spike is assumed to be 10^{21} cm^{-3} spread over a 1-nm lateral width.

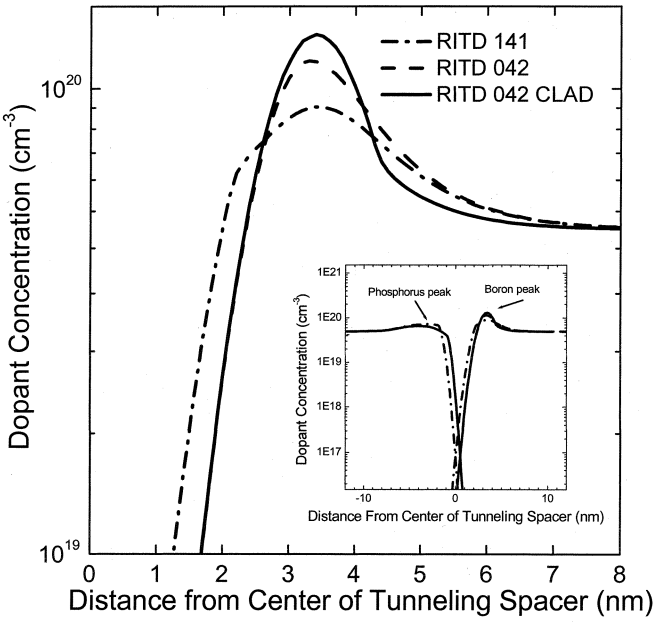

Fig. 7. Modeled B-dopant profile of structures RITD141, RITD042, and RITD042clad by simulating a 1-min RTA anneal at 800 °C. Note that RITD042clad with SiGe cladding layers on both sides maintains the sharpest B peak.

expected. The Boron profiles with Phosphorus profiles of these three structures are shown in the inset of Fig. 7.

Fig. 8 shows the band diagram calculated using the modeled interdiffusion profiles shown in Fig. 7. Here, a strong shift in the band diagrams is visible for the three structures modeled. This is consistent with the large changes in tunnel diode PVCR for the three different structures. The authors believe the true doping profile and corresponding RITD band diagram lies between the result shown in Fig. 5, based on direct SIMS measurements, and the modeled doping profile in Fig. 7 and its associated band diagram shown in Fig. 8.

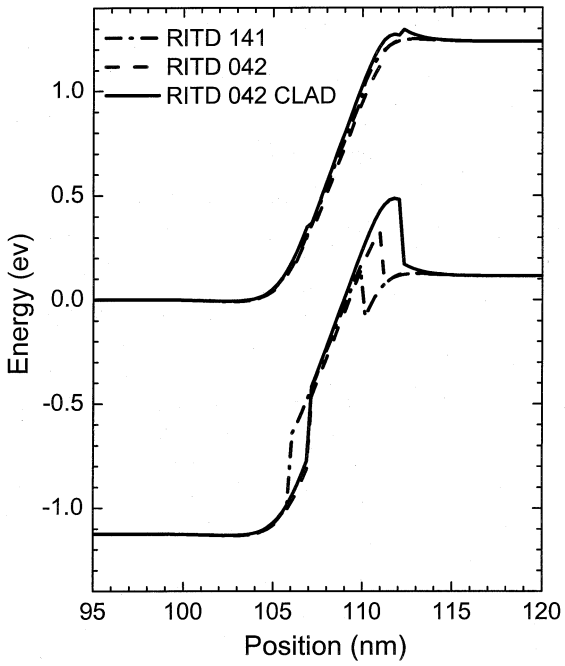

Fig. 8. Calculated band diagram using self-consistent Thomas-Fermi calculations of the electrostatic potential using a semi-classsical density-of-states of the three RITD structures shown in Fig. 7. For clarity, not all band valleys are presented.

To fully understand the influence that B out-diffusion has on tunnel diode performance, the diodes were subjected to a range of anneal temperatures; see Fig. 9. Post-growth RTA processing has been shown to reduce point defects that contribute to elevated valley current but deleteriously broaden the B δ-doping [27]. Consequently, an optimal RTA temperature exists that maximizes PVCR, which is clearly shown in Fig. 9. Note that the optimal annealing temperatures for these three structures are different, and RITD042CLAD shows the highest optimal annealing temperature, while RITD141 shows the lowest optimal annealing temperature. These results illustrate that insertion of the SiGe cladding layers suppresses B out-diffusion so that higher RTA temperatures can be employed to more effectively reduce point defects while minimizing the B diffusion to ensure a high peak current density. There is a 100 °C difference between the best PVCR from RITD141 and the best PVCR from RITD042clad, indicating that RITD042clad can withstand a higher thermal budget. Consequently, RITD042clad demonstrates the highest PVCR among these three structures.

The effect of the SiGe cladding layer can also be demonstrated by Fig. 10, which shows a comparison of the isothermal I–V characteristics of these three structures all annealed at 825 °C for 1 min. All three of these structures show similar valley current density indicating equivalent point defect removal, whereas RITD042clad shows the highest peak current density, due to the least amount of B out-diffusion.

B. Patterned Growth Atop PMOS Source/Drain Implants for Monolithic Integration With CMOS

Integration of Si-based tunnel diodes with CMOS will require some modifications to the existing CMOS fabrication steps. To minimize the impact and limit the number of steps

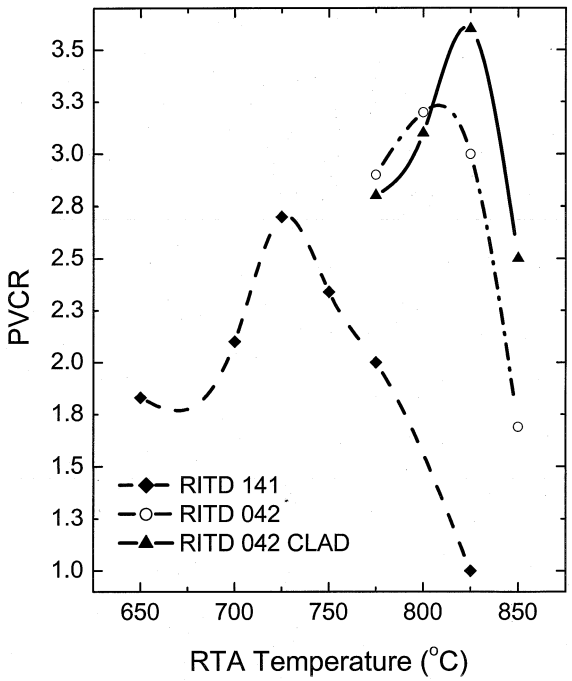

Fig. 9. Comparison of the PVCR versus annealing temperature is shown for the three different structures studied. Note that RITD042clad shows both the highest optimal annealing temperature and the highest PVCR, which is consistent with the diffusion modeling. The lines are joins of the data points to assist the reader. Estimated relative uncertainties are ±2% in current density and ±1% in voltage.

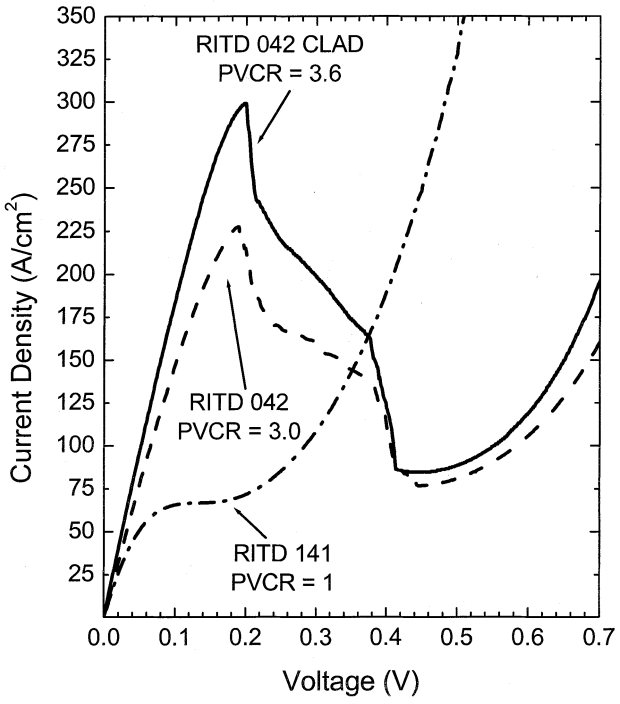

Fig. 10. I–V characteristics of structures RITD141, RITD042, and RITD042clad are compared with all having undergone the same RTA heat treatment at 825 °C for 1 min. Note that the valley currents are nearly coincident, indicating each has an equivalent removal of point defects, but room-temperature PVCR is different in the three different structures. Estimated uncertainties are ±3% in PVCR and ±5 °C in RTA temperature.

in the process, integration will most likely occur by growing the Si-based tunnel diode onto pre-existing CMOS circuitry

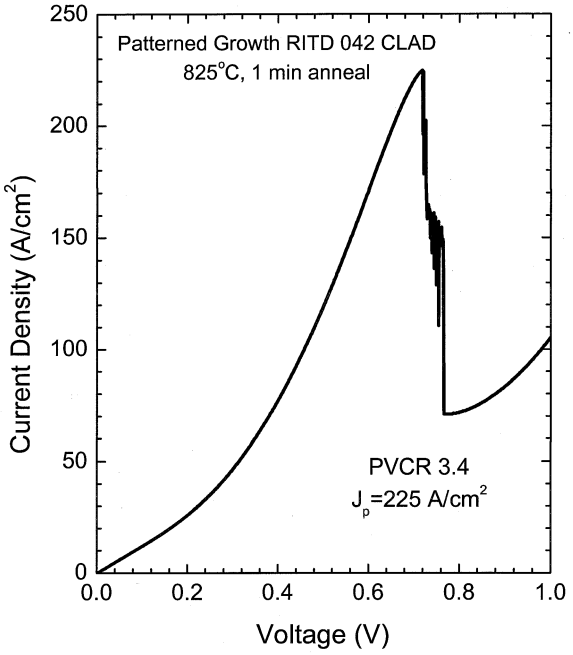

Fig. 11. Measured I–V characteristics of a patterned grown RITD042clad structure through an oxide opening of a fully processed CMOS wafer. Estimated relative uncertainties are ±2% in current density and ±1% in voltage.

following all high-temperature CMOS processing but prior to CMOS metallization and interconnect metallizations. We have used patterned growth through oxide openings and onto implanted regions to validate the ability to place RITDs atop PMOS source and drain implant regions. The effect of residual implant damage on the RITD characteristic is being investigated in a separate study.

The influence of patterned growth was investigated by growing tunnel diodes through openings in a low-temperature oxide (LTO) deposited by chemical vapor deposition (CVD) at 425 °C. Windows of varying size were patterned in 300 nm of LTO grown on a p^+ Si substrate. RITD042CLAD was then replicated on this sample, using identical growth conditions. The epitaxial layer covered the entire wafer and was crystalline in the openings and amorphous atop the SiO_2. The wafers then underwent RTA heat treatments similar to those performed on the discrete RITDs discussed earlier. The RITD mesa in the LTO opening was then patterned and etched with an SF_6 reactive ion etching plasma. The MBE layer grown atop the oxide was removed at this point; consequently, approximately 50 nm of the original LTO was unintentionally removed. A second LTO layer of 300 nm was then deposited and patterned for contact cuts to the devices. Al/Si was sputter deposited over the sample with a thickness of 600 nm, patterned, and wet etched to form contacts. The metal was sintered in a tube furnace under N_2/H_2 ambient at 420 °C for 20 min.

The resulting device I–V characteristics are shown in Fig. 11. Patterned growth devices fabricated on a bulk p+ substrate exhibited a PVCR of 3.4 and a peak current density of 225 A/cm^2. This is virtually identical to the PVCR of RITDs fabricated on a bulk sample. However, the observed peak voltage is shifted higher due to an increased series resistance observed in these devices either due to elevated ohmic contact resistance or due

to a depletion/accumulation layer at the regrown interface [41], [42]. This will be studied further.

IV. Conclusions

By introducing thin SiGe layers cladding the B δ-doping layer, B out-diffusion is likely suppressed during post-growth annealing, which raises the thermal budget. A room-temperature PVCR of 3.6 was measured with a peak current density of 0.3 kA/cm^2. A higher RTA temperature appears to be more effective in reducing defects and results in a lower valley current and higher PVCR. Patterned growth of RITDs inside LTO openings also exhibited PVCR as high as 3.4 and showed little performance degradation compared with bulk-grown RITDs.

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