High Performance Resonant Tunneling Electronic Circuit with Suitable Resistance Parameters

Chih Chin Yang*, Yen Chun Lin, Hsiao Hsuan Cheng

Department of Microelectronics Engineering, National Kaohsiung Marine University No.142, Haijhuan Rd., Nanzih Dist., Kaohsiung City 81157, Taiwan *corresponding author, e-mail: chchyang@mail.nkmu.edu.tw

Abstract

Well-defined experimental and simulating single peak to valley current density ratio (PVCDR) resonant tunneling electronic circuit (RTEC) element is proposed in this research. The variation of passive element value in RTEC structure is explored using simulation method, which obtains the optimum PVCDR values about 66. The simulating peak current density (PCD) value is such high as 38 mA. Even though the experimental PCD value is less, but the PVCDR value is as high as 22.5, which value is favorably compared with semiconductor resonant tunneling devices (RTDs) in single PVCDR RTEC element. The obvious triple negative differential resistance (NDR) is also completed using composition of three suitable single RTEC elements. Also, experimental triple PVCDR RTEC element significantly exhibits three NDR curves with obvious three PVCDR values about 3.4, 3.8, and 6.0, respectively. Both peak voltage (PV) value and valley voltage (VV) values of experimental triple PVCDR RTEC element is less than 2.8 V, which value is profitable in development of commercial product. Power consumption of triple PVCDR RTEC element is as low as 75.5 μ W, which low power consumption will shrink the difficulty of element packaging in heat dissipation.

Keywords: resonant tunneling, electronic circuit, resistance, current density.

Copyright © 2012 Universitas Ahmad Dahlan. All rights reserved.

1. Introduction

Negative differential resistance (NDR) device has been vigorously developed recently with respect to enhancement of high peak current density (PCD) value and high peak to valley current density ratio (PVCDR) values [1-4]. The application of high performance NDR device is a key factor for fabrication of well-defined information facility and communication elements. Advanced NDR device substitutes the traditional electronic elements, which is to improve the functions of communication and information technologies. The utilizations of inspected novel and nonlinear resistance characteristic are better than the traditional electronic element in dimension, switching time, and element functions. The negative resistance effect is not emerged by general traditional electronic circuit. Although the NDR characteristic has been proposed by using passive elements recently, the negative resistance element of well property is not yet completed [5]. The key cause is that the selection of passive element is not achieved. Optimum NDR device manufactured using passive elements by the regulation of every passive element value is to obtain highest PVCDR and PCD values in NDR curve which is explored in detail in this paper. NDR devices are still with potential developments and appliances in future as NDR device is fabricated by the combination and design of general and traditional electronic elements using integrated circuit fabrication technology.

The electronic device, fabricated by utilizing NDR characteristic, are called resonant tunneling device (RTD). The traditional RTDs with quantum well, quantum wire, and quantum dot structures are generally manufactured by using precise semiconductor fabrication techniques such as molecular beam epitaxy (MBE), metal organic chemical vapor deposition (MOCVD), vapor phase epitaxy (VPE) etc. The performance of semiconductor RTD is remarkable in PVCDR and PCD values [1][3], but the high manufacture cost, poison and explosion, and pollutant in fabrication of semiconductor RTD can not be averted. The manufacture of semiconductor RTD frequently uses toxic chemical elements and compound at high temperature. The considerations of global warming and environment pollution on the earth are obligation in future for development of integrated circuit technology. To ameliorate the

phenomena as above, the new issue for the fabrication of RTD element is proposed in recent [5]. The suggested RTD element using passive elements is not maturity. The passive electronic circuit with resonant tunneling characteristic so called resonant tunneling electronic circuit (RTEC) element in this paper is proposed to elevate the functions of RTD element. The RTEC element, although, is assembled by utilizing passive elements with a great quantity of volume in dimension, the RTEC element can be manufactured on a chip by foundry.

The values of RTEC element are the controllable high PCD value and high PVCDR value. The NDR curve with high PVCDR value cross the load line, which results in wider operation region, can be applied in digital circuit of high noise margin and switching circuit of high speed. PVCDR value is enumerated by PCD value over valley current density (VCD) value. High PVCDR is because of high PCD value or low VCD value. High PCD value is accomplished in necessitarianism via special design and construction of RTEC element. Limitation of parasitic effect in electronic circuit is obstacle to improve the PVCDR value by raising PCD value. In view of the difficulty of raising PCD value, the PVCDR should be amplified by decay of VCD value. Low VCD value is determined by transient instant of between "on" state and "off" state of transistor in RTEC element. Resistance values in RTEC element play an important role in VCD value. In this paper, the VCD value is deeply pondered, because of its significance for PVCDR value. The PCD value is the hinge for output power of RTEC element, because the calculation of output power is defined PCD value by average of peak voltage (PV) and valley voltage (VV). The more PCD value is, the more output power is. PCD value is not relationship with VV value and PV value. However, PCD value is decided in which kinds of active element and passive element in RTEC element. The NDR curve is single alone in I-V characteristic of general RTD. While the RTEC element is constructed by way of suitable design, the novel multiple NDR characteristic is inevitably appeared. The multiple NDR curves of RTEC element possess useful and potential applications in digital circuit, high frequency circuit, switching circuit, and memory device.

RTEC element with multiple NDR curve is extensively useful in digital circuits and analog circuits including multiple value memory [6-7], flash memory [8-9], RAM and ROM [10-11], high speed and high frequency MOS [12-14], logical element and system [15-17], multiplexer [18-19], adder [20-21], encoder and decode [22-23], flip flop [24], sequence generator [25], algorithm circuit [26-27], threshold circuit [28-29], and latch circuit [30]. Owing to multiple NDR characteristic of RTEC element, the RTEC element with multiple value logical level can construct the memory of large volume and high speed. After the RTEC element is optimized, the cut off frequency will be also ascended in radio frequency.

2. Research Theory and Method

The fundamental of semiconductor RTD is stated by quantum physics theory which as quantum carriers tunnel from the quantum well of emitter punch through the potential barrier to the quantum well of collector, the resonant tunneling phenomenon occurs. Due to the design of barrier potential and quantum well mechanisms, the current-voltage characteristic of semiconductor RTD engenders both positive differential resistance (PDR) and negative differential resistance (NDR) values. The phenomenon of PDR value and characteristic of ordinary passive element is similarity, although the RTD is in particular design of quantum mechanism. The phenomenon of NDR values in RTD is formed due to the tunneling mechanism as above statement. The alternation of NDR characteristic is in accord with quantum structure including thicknesses and properties of materials in both potential barriers and quantum wells. The NDR characteristic of semiconductor RTD is with the limitation of output power because of its device limitation in dimension, and limitation of fabrication and utilization of rare substance. The RTEC element is the optimum substitution of the semiconductor RTD to solve the difficulties of semiconductor RTD.

The basic RTEC element is consist of pre-stage transistor Q_1 with current gain β_1 , two bias resistors R_1 and R_2 , pre-stage load resistors R_3 , feedback resistor R_4 between two transistors, and output stage transistor Q_2 with current gain β_2 [5]. The resistances in basic RTEC element resolve switching state of two transistors whether "on" state or not. Operation points of transistors decide the PCD value and PVCDR value of RTEC element. The key factor of well-defined NDR characteristic is VCD value but not PCD value. VCD value of RTEC element is also determined by the regulation of all resistances in element. In this section, the NDR curve is divided four piecewise regions including two high resistance regions, one positive difference resistance region, and one negative differential resistance region. At low applied bias voltage, two transistors are all at "off" state which is the first high resistance region of NDR curve and no application function for RTEC element. In this situation, the RTEC element is corresponded to two bias resistors in series with each other and pre-stage load resistors in series with feedback resistor. Then, the two groups are paralleled each other, which the high equivalent resistances R₁ is produced in RTEC element. The high resistance region is like the diode current region of semiconductor RTD, as expressed in equation (1). In the second region, the applied bias voltage is gradually raised up, which the pre-stage transistor is still at "off" state but the output stage transistor is turn "on". In this region, two bias resistors are still in series with each other, and the pre-stage load resistors is reduced by dividing transistor gain, which equivalent resistance R_{\parallel} is as expressed in equation (2). The third I-V region is the negative differential region with negative differential slop characteristic. In this region, all transistors are at "on' state, in which situation the equivalent resistance R_{III} of RTEC element is a small negative value, as expressed in equation (3). As the applied bias voltage becomes higher value, the prestage transistor is still at "on" state but the output stage transistor turns "off", which the equivalent resistance R_{IV} of RTEC element becomes high positive value, as expressed in equation (4).

$$R_{\rm I} = \frac{(R_1 + R_2)(R_3 + R_4)}{(R_1 + R_2) + (R_3 + R_4)} \tag{1}$$

$$R_{\rm II} = \frac{R_3(R_1 + R_2)}{R_3 + (1 + \beta_2)(R_1 + R_2)}$$
(2)

$$R_{\rm III} = \frac{R_3 R_1}{(1 - \beta_1 \beta_2) R_3 + (1 + \beta_2) R_1}$$
(3)

$$R_{\rm IV} = \frac{R_1 R_3}{(R_1 + R_3)} \tag{4}$$

The derivation of equivalent resistance values as above in NDR curve makes an inference about increase of the PVCDR value by decreasing bias resistance R_1 , and increasing feedback resistance R_4 and transistor gain β_2 in suitable R_2 and R_3 values. PVCDR value can be improved by using above methods, but when the number of RTEC element stage is increased, the PVCDR value is still influenced, because of loading effect in RTEC element. In this paper, the simulating and experimental researches in regulation of the feedback and bias resistances in RTEC element are respectively completed. The simulation process is arranged by progress altering the resistances in RTEC element to obtain the optimum PVCDR value. The optimum resistances are applied in experimental research to obtain the multiple NDR curve.

3. Simulation Results and Discussion

Variance of I-V characteristics with variable R₁ value in fixed value of R₂=3 K Ω , R₃=1 K Ω , and R₄=5 K Ω is simulated. As Figure 1 shows, varied R₁ value from 2.5 K Ω to 3.5 K Ω , the PCD value shoots up 17.1 mA from 5.8 mA and the PVCDR value rises to 15.5 from 5.3. CVD value remains steady even out at around 1.1 mA. Because of stabilization of VCD value at about 1.1 mA, the increase of PVCDR value can be attributed to increase of PCD value, which is believed that this is related to the continued increase of bias resistance R₁ value. Therefore, the PVCDR value can be regulated by altering bias resistance R₁ value. The PV and VV values are risen from 0.85 V to 1.0 V and 0.9 V to 1.1 V, respectively, which break point of PV and VV values are caused by R₁ value. The V_T value remains constant at different R₁ values. The power consumption of RTEC element in Fig.1 is 3.2 mW, 5.7 mW, and 9.6 mW, respectively, as the R₁ value is arranged in 2.5 K Ω , 3.0 K Ω , and 3.5 K Ω . The R₁ value absolutely influences the power consumption of RTEC element.

In Figure 2, the diagram shows the relationship between I-V characteristic and bias resistor R_2 value. In this situation, both PVCDR value and PCD value are also proportional to R_2

value. The role of bias resistor R₂ value is almost likely with R₁ in RTEC element, but it is a inverse outcomes in both PCD and PVCDR values, because partial voltage is different in Q₁ by R₁ value or R₂ value. Variance of I-V characteristics with R₂ value in R₁=3 K Ω , R₃=1 K Ω , and R₄=5 K Ω is simulated respectively.

After the R₂ is graduate decreased, the PCD value is enormous risen and the VCD value slightly gets higher. The PV and VV values are inversely R₂ value, also. V_T values remain steady in 0.7 V, which is not influenced by R₂ value. The PVCDR value is plunged from 32.5 to 14 by arranging R₂ value from 2 K Ω to 4 K Ω . The variety of PVCDR value is influenced by both PCD value and VCD value in this situation. The power consumption value is also declined from 14.1 mW to 3.4 mW by arranging R₂ value from 2 K Ω to 4 K Ω . As the R₂ value is reached twice, the power consumption is almost shrunk three-quarters.



Figure 1. Variance of I-V characteristics with R₁ variable value and fixed value of R₂=3 K Ω , R₃=1 K Ω , and R₄=5 K Ω .



Figure 2. Variance of I-V characteristics with R_2 variable value and fixed value of R_1 =3 K Ω , R_3 =1 K Ω , and R_4 =5 K Ω .







Figure 4. Variance of I-V characteristics with R_4 variable value and fixed value of $R_1=3$ K Ω , $R_2=3$ K Ω , and $R_3=1$ K Ω .

Variation of R₃ value for I-V characteristic in single PVCDR RTEC element simulation is exhibited in Figure 3, where R₁, R₂, and R₄ are fixed at 3 K Ω , 3 K Ω , and 5 K Ω , respectively. In this diagram, the PCD and VCD values drop 87 and 80 percent with increase of the R₃ value,

respectively, because R_3 is load resistance of the pre-stage transistor Q_1 . The different result in region II of NDR curve is because the R_3 is not a bias resistance in pre-stage, which results in the without relation between PV value and R_3 value. The VV value is absolutely influenced by R_3 value because second stage of RTEC element is worked at the same time, shown in the negative resistance region of NDR curve. The V_T is also changed with R_3 value, because R_3 is not a bias resistor for Q_2 transistor of the second stage. As R_3 value is changed, the PVCDR value is not significantly altered, which PVCDR values is only changed between 48 and 65. Although the R_3 value is not a main factor for PVCDR value, the R_3 absolute value can result in large enough PVCDR value, as reached to 65. The more R_3 value is, the more output power is, because the power consumption becomes less.

The function of feedback resistor R_4 is to settle the VCD value and then results in high PVCDR value more than 40, as represented in Figure 4. Although the PCD value is expanded, as the feedback resistor R_4 is went up, the lower and stable VCD value is just the key point for high PVCR value. All of V_T , VV, and PV values remain steady in 0.7 V, 1.0 V, and 0.9 V respectively, which is not influenced by R_4 value. R_4 value is extremely significant in PVCDR value. Therefore, the research result of R4 value would be used to construct the well-defined NDR characteristic. Variation of R_4 value for I-V characteristic in single PVCDR RTEC element simulation is exhibited in Figure 4, where R_1 , R_2 , and R_3 are fixed at 3 K Ω , 3 K Ω , and 1 K Ω , respectively.

4. Experimental Results and Discussions

After the simulating research is completed, the experimental research is progressed to verify the calculated result as above. Figure 5 shows the experimental results which contains single, double, and triple PVCDR characteristics. Figure 5 (a) is the experimental I-V characteristics of single PVCDR RTEC element with R_1 =3 K Ω , R_2 =3 K Ω , R_3 =1 K Ω and R_4 =5 K Ω . The PCD value and VCD value are 45 μ A and 2 μ A, respectively. The current density values of experimental result are less than those of simulating result, because of the leading effect and parasitic effect. The PVCDR value of experimental result about 22.5 is more than that of the simulation result about 15.5 at optimum R_1 value. The PV value and VV value in the experimental result of single RTEC are about 1.3 V and 1.4 V, respectively, more than those of simulating results about 0.3 V. The cause is that the physical consumption of experimental RTEC structure. The more PV value and VV value in the experimental result of single RTEC is reasonable in compare with simulating result, which can be eliminated by the improvement of RTEC element fabrication.

In this paper, the experimental RTEC element with double NDR curve is proposed. Experimental I-V characteristics of double PVCDR RTEC element with $R_1=3 \text{ K}\Omega$, $R_2=3 \text{ K}\Omega$, R₃=0.82 K Ω , R₄ =5.6 K Ω in first stage, and with R₁=6 K Ω , R₂=3 K Ω , R₃=0.5 K Ω , R₄ =0.5 K Ω in second stage is exhibited in Figure 5 (b). In this double PVCDR RTEC experimental structure, both PCD value and PVCDR value are less than those of single PVCDR RTEC element of either experimental result or simulating result. The double PVCCDR RTEC element is constructed by cascade of two single RTEC elements. The cascaded both single PVCDR RTEC elements will consumptive the operation current from the first RTEC element to the second RTEC element. This cause results in the higher PV and VV values, and declines the PCD value and PVCDR value even though the VCD value is also lessened down obviously. This phenomenon is normally like the results of semiconductor RTD. The more number of RTEC stage is, the more influence of multiple stages each other in PVCDR value is. The important issue in double PVCDR RTEC element is the similitude between the two NDR curves, but not PVCDR value. The triple PVCDR RTEC element is also similar with the phenomenon of double PVCDR RTEC element as above, as shown in Figure 5(c). Figure 5 (c) significantly exhibits three NDR curves with obvious three PVCDR values about 3.4, 3.8, and 6.0, respectively. The PVCDR values are reasonable values for the triple PVCDR RTEC element, because of cascading effect of multiple RTEC elements.

Experimental I-V characteristics of triple PVCDR RTEC element with R₁=3 K Ω , R₂=3 K Ω , R₃=0.82 K Ω , R₄ =5.6 K Ω in the first stage, with R₁=6 K Ω , R₂=3 K Ω , R₃=0.5 K Ω , R₄ =0.5 K Ω in the second stage, and with R₁=13 K Ω , R₂=4 K Ω , R₃=1 K Ω , R₄ =0.5 K Ω in the third stage is designed at optimum NDR characteristic after the passive element values in triple PVCDR RTEC is adjusted suitability.



Figure 5 (a) Experimental I-V characteristics of single PVCDR RTEC element with R₁=3 KΩ, R₂=3 KΩ, R₃=1 KΩ and R₄ =5 KΩ. (b) Experimental I-V characteristics of double PVCDR RTEC element with R₁=3 KΩ, R₂=3 KΩ, R₃=0.82 KΩ, R₄ =5.6 KΩ in first stage, and with R₁=6 KΩ, R₂=3 KΩ, R₃=0.5 KΩ, R₄ =0.5 KΩ in second stage. (c) Experimental I-V characteristics of triple PVCDR RTEC element with R₁=3 KΩ, R₂=3 KΩ, R₃=0.82 KΩ, R₄ =5.6 KΩ in the first stage, with R₁=6 KΩ, R₂=3 KΩ, R₃=0.5 KΩ, R₄ =0.5 KΩ in the second stage, and with R₁=13 KΩ, R₂=4 KΩ, R₃=1 KΩ, R₄ =0.5 KΩ in the third stage.



Figure 6. Physical diagram of experimental I-V characteristics in triple PVCDR RTEC element.

and experiment in single FVODICICIE elements.					
I-V	Simulation (at optimum resistance values)				Experiment
characteristic					
of 1 st NDR	R ₁	R ₂	R₃	R_4	
PCD (mA)	17	25	38	33	0.045
VCD (mA)	1.1	0.9	0.8	0.5	0.002
PV (V)	1.0	1.0	1.0	0.9	1.3
VV (V)	1.1	1.1	1.1	1.0	1.4
V _T (V)	0.6	0.7	0.7	0.6	0.6
PVCDR	16	28	48	66	22.5
Power(mW)	10	14	20	16	0.034

Table 1. Comparison of I-V characteristic with simulation and experiment in single PVCDR RTEC elements.

The PV and VV values in third stage of RTEC element are respectively about 2.5 V and 2.8 V. Higher PV and VV values are acceptable in industry application. The consumption power is as high as about 37.1 μ W, 52.0 μ W, and 75.5 μ W in every RTEC stage, that heat dissipation of RTEC device on chip must be considered. In short, the well-defined characteristics of experimental triple PVCDR RTEC element in this paper are proposed with well I-V characteristic, multiple NDR values, high PVCDR value, and high PCD value. The physical diagram of experimental I-V characteristics in triple PVCDR RTEC element is exhibited in

1339

Figure 6. I-V measurement of experimental PVCDR RTEC element is by utilizing Kitheley 2400 current-voltage instrument to obtain the NDR characteristic in low current measurement about μ A in unit. The high resolution measurement in current and voltage is to precisely calculate PVCDR values in every stage of triple PVCDR RTEC element.

4. Conclusions

In this paper, the well-defined single PVCDR RTEC element by alter of passive element value in RTEC structure is achieved using simulating and experimental methods, as expressed in Table 1. The simulated PVCDR value reaches 66 and the experimental PVCDR value attains 22.5. Experimental applied bias voltage both PV value and VV value are not more than 1.4 V, even though the values are more than those of simulating results. Lower V_T about 0.6 V in single PVCDR RTEC element both simulating result and experimental result is beneficial in communization to fall down the consumption power. Low enough VV values of both simulating research and experimental research are the successful key factor for high performance RTEC element with regulated suitable resistors is composed to triple PVCDR RTEC element which the remarkable triple NDR curves is exhibited.

References

- [1]. Yang CC. High Performance Multiple stepped quantum well resonant microwave devices. *Electronics Letters*. 2006; 42(25): 1485-1487.
- [2]. Yang CC, Su YK. Well-defined electrical properties high-strain resonant interband tunneling structure. *Microelectronics Journal*. 2008; 39(1): 67-69.
- [3]. Yang CC, Su YK. High performance aluminum arsenic intraband resonant microwave devices. *Microelectronics Journal*. 2008; 39(1): 90-93.
- [4]. Yang CC. Frequency Computation of Resonant Signal in Resonant Tunneling Circuit for Communication. 2010 Second International Joint Journal Conference on Computer and Communication Technology (IJJCCT 2010). Jeju Island, Korea. 27-28 December 2010.
- [5]. Gan KJ, Su YK. Novel multipeak current-voltage characteristics of series-connected negative differential resistance devices. *IEEE Electron Dev. Lett.* 1998; 19(4): 109-111.
- [6]. Yan ZX, Deen MJ. A new resonant-tunnel diode-based multivalued memory circuit using a MESFET depletion load. *IEEE Journal of Solid-State Circuit*. 1992; 27(8): 1198-1202.
- [7]. Inokawa H, Fujiwara A, Takahashi Y. A multiple-valued logic and memory with combined singleelectron and metal-oxide-semiconductor transistors. *IEEE Transactions on Electron Devices*. 2003; 50(2): 462-470.
- [8]. Lee JD, Hur SH, Choi JD. Effects of floating-gate interference on NAND flash memory cell operation. *IEEE Electron Device Letters*. 2002; 23(5), 264-266.
- [9]. Grossi M, Lanzoni M, Ricco R. A novel algorithm for high-throughput programming of multilevel flash memories. *IEEE Transactions on Electron Devices*. 2003 ;50(5): 1290-1296.
- [10]. Lin FRL, Lin SY, Lee ML, Boe CH, Yeh CP, Wu PH, Ni J, King YC, Hsu CCN. Novel sourcecontrolled self-verified programming for multilevel EEPROMs. *IEEE Transactions on Electron Devices*. 2000; 47(6): 1166-1174.
- [11]. Versari R, Esseni D, Falavigna G, Lanzoni M, Ricco B. Optimized programming of multilevel flash EEPROMs. *IEEE Transactions on Electron Devices*. 2001; 48(8): 1641-1646.
- [12]. Noor AF, Iskandar F, Abdullah M, khairurrijal K. Numerical simulation of tunneling current in an anisotropic metal-oxide-semiconductor capacitor. *TELKOMNIKA Indonesian Journal of Electrical Engineering*. 2012; 10(3): 477-485.
- [13]. Liu WC, Laih LW, Cheng SY, Chang WL, Wang WC, Chen JY, Lin PH. Multiple negative-differentialresistance (MNDR) phenomena of a metal-insulator-semiconductor-insulator -metal (MISIM)-like structure with step-compositioned In_xGa_{1-x}As quantum wells. *IEEE Transactions on Electron Devices*. 1998; 45(2): 373-379.
- [14]. Jun S, Ki DM. MOSFET stair-shaped I-V circuit and applications. *Electronics Letters*. 1997; 33(24): 2077-2078.

- 1340 🔳
- [15]. Jin N, Chung SY, Heyns RM, Berger PR, Ronghua Y, Thompson PE, Rommel SL. Tri-state logic using vertically integrated Si-SiGe resonant interband tunneling diodes with double NDR. *IEEE Electron Device Letters*. 2004; 25(9): 646-648.
- [16]. Liu WC, Wang WC, Pan HJ, Chen JY, Cheng SY, Lin KW, Yu KH, Thei KB, Cheng CC. Multipleroute and multiple-state current-voltage characteristics of an InP/AllnGaAs switch for multiple-valued logic applications. *IEEE Transactions on Electron Devices*. 2000; 47(8): 1553-1559.
- [17]. Hoof CV, Genoe J, Hove MV, Rossum MV, Mertens R, Borghs G. Four logic states using two resonant tunneling diodes. *Electronics Letters*. 1989; 25(4): 259-260.
- [18]. Tanabe A, Nakahara Y, Furukawa A, Mogami T. A redundant multivalued logic for a 10-Gb/s CMOS demultiplexer IC, *IEEE Journal Solid-State Circuits*. 2003; 38(1): 107-113.
- [19]. Chan HL, Mohan S, Mazumder P, Haddad GI. Compact multiple-valued multiplexers using negative differential resistance devices. *IEEE Journal of Solid-State Circuits*. 1996; 31(8): 1151-1156.
- [20]. Gonzalez AF, Bhattacharya M, Kulkarni S, Mazumder P. CMOS implementation of a multiple-valued logic signed-digit full adder based on negative-differential-resistance devices. *IEEE Journal of Solid-State Circuits*. 2001; 36(6): 924-932.
- [21]. Huber JL, Chen J, McCormack JA, Zhou CW, Reed MA. An RTD/transistor switching block and its possible application in binary and ternary adders. *IEEE Transactions on Electron Devices*. 1997; 44(12): 2149-2153.
- [22]. Huang CH, Wang JS, Huang YC. Design of high-performance CMOS priority encoders and incrementer/decrementers using multilevel look ahead and multilevel folding techniques. *IEEE Journal Solid-State Circuits*. 2002; 37(1): 63-76.
- [23]. Wang JS, Huang CH. High-speed and low-power CMOS priority encoders. IEEE Journal Solid-State Circuits. 2000; 35(10): 1511-1514.
- [24]. Uemura T, Baba T. A three-valued D-flip-flop and shift register using multiple-junction surface tunnel transistors. *IEEE Transactions on Electron Devices*. 2002; 49(8):1336-1340.
- [25]. Blakley JJ. Architecture for hardware implementation of programmable ternary de Bruijn sequence generators. *Electronics Letters*. 1998; 34(25):2389-2390.
- [26]. Wahyuningrum RT, Damayanti F. Efficient Kernel-based two-dimensional principal component analysis for smile stages recognition. *TELKOMNIKA Indonesian Journal of Electrical Engineering*. 2012; 10(1): 113-118.
- [27]. Wang L, Almani AEA. Fast conversion algorithm for very large Boolean functions. *Electronics Letters*. 2000; 36(16): 1370-1371.
- [28]. Temel T, Morgul A. Implementation of multi-valued logic, simultaneous literal operations with full CMOS current-mode threshold circuits. *Electronics Letters*. 2002; 38(4): 160-161.
- [29]. Piestrak SJ, Dandache A. Minimal test set for multi-output threshold circuits implemented as bubble sorting networks. *Electronics Letters*. 2000; 36(3): 202-204.
- [30]. Current KW. Voltage-mode CMOS quaternary latch circuit. *Electronics Letters*. 1994; 30(23): 1928-1929.