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Fuzzy based controller for dynamic Unified Power Flow Controller to enhance power transfer capability

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ABSTRACT

In this paper, a dynamic model of Unified Power Flow Controller (UPFC) is developed to improve the power transfer capability (PTC) through the transmission line. Improvement of the bus voltages profiles along with the reduction of total power losses is also intended with UPFC's presence. The UPFC shunt and series controllers are developed based on Fuzzy Logic (FL) which has been designed as a stand-alone module in PSCAD environment. Sinusoidal pulse width modulation (SPWM) technique is applied as a modulation technique to generate switching signals for the converter switches. The proposed UPFC controller is tested by using IEEE-5 and 14 bus systems with various case studies. The performance of the proposed controllers is also compared with different control methods. From the test results, significant improvement of PTC has been achieved with the minimization of total power losses.

1. Introduction

The continuous expansion and up-gradation of power system have become essential to satisfy the ever growing power demand due to limited energy resources, and deregulated electricity market. In addition, building new transmission lines to meet the increasing electricity demand has also been restricted by economic and environmental constraints [1]. As a result, utilities are compelled to optimally utilize the existing resources which made the transmission lines overloaded followed by reduced stability, voltage variation increment and looped power flow [2]. These issues have led the system planners to look for the new strategies to improve the power system performance with economic means to transfer bulk power.

As a solution to the mentioned issues, keen attention has been paid to Flexible Alternating Current Transmission System (FACTS) devices which are driven from modern power electronics components. Over last decade FACTS devices have been extensively used to improve PTC through the transmission lines and enhance system controllability resulting in minimizing power losses in transmission network [3]. Among different types of FACTS devices UPFC has got the epic popularity. Since, it comprises with the actions of two FACTS devices which made it capable of voltage regulation, series compensation, and phase angle regulation simultaneously, lead to the discrete control of active and reactive power transmitted together through the line [4,5].

In the past, several steady state model of FACTS devices such as for SVC [6,7], STATCOM [8], TCSC [9–11] and UPFC [12–14] have been proposed. These models were used in power system planning to enhance power transfer capability (PTC), reduce power losses and minimize voltage deviation. The models cannot be used to study real time operation of power system network. Therefore, it is essential to develop dynamic model of FACTS devices so that the real time analysis of power system network can be conducted. However, the biggest challenge of the real time applications of FACTS devices is the design of their internal controllers. Especially control system of UPFC because it is a multi-variable controller. If the control system of the shunt and the series converters of UPFC is such that the shunt converter is not able to meet the real power demand of the series converter, then the DC capacitor voltage might collapse resulting in the removal of the UPFC from the power system [15]. Different control strategies for UPFC have been designed in the literatures. In [16–18], decoupled control method has applied to UPFC to control the active/reactive powers flow. Here, the transmission line current has divided into D-axis and Q-axis currents which control individually the real power and reactive power of the transmission line. However, because of the variation of the power system operating points the transmission parameters change continuously. Therefore, the performance of a decoupling control system may vary significantly depending on the operating

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Nomenclature

K_p	proportional gain of PI controller
K_i	integrator gain of PI controller
Vmag_sh	magnitude of injected shunt voltage
angle_sh	angle of injected shunt voltage
Vs_measured	measured value of sending – end voltage
Vs_reference	reference value of sending – end voltage
Vdc_measured	measured value of DC link capacitor voltage
Vdc_reference	reference value of DC link capacitor voltage
Vs_a, *Vs_b*, *Vs_c*	phase voltages of sending – end
Vr_a, *Vr_b*, *Vr_c*	phase voltages of receiving – end
a_s	phase angle of sending-end voltage
$P_{measured}$	measured real power
$Q_{measured}$	measured reactive power
$P_{reference}$	reference real power
$Q_{reference}$	reference reactive power
V_d	direct components of the series injected voltage
V_q	quadrature components of the series injected voltage
Vmag_se	magnitude of injected series voltage
a_r	phase angle of receiving – end voltage
sin ()	trigonometric function
FACTS	flexible AC transmission systems
FL	fuzzy logic
PTC	power transfer capability
PI	proportional-integral
PLL	Phase Locked Loop
SPWM	sinusoidal pulse width modulation
VSC	voltage source converter
STATCOM	static synchronous compensator
SVC	static var compensator
TCSC	thyristor controlled series capacitor
SSSC	static synchronous series compensator
EP	evolutionary programming
UPFC	Unified Power Flow Controller
PSO	particle swarm optimization
GA	genetic algorithm
HS	harmony search
ANN	artificial neural network
OPF	optimal power flow

point of power system network. By considering the variation of the power system parameters in [19–21] another control algorithm for UPFC has been proposed based on cross-coupled method. The drawbacks of both decoupled and cross-coupled based UPFC controller is the ignorance of the dynamics of the DC link capacitor while designing the control system. Also the interaction between the two converters has not eliminated completely. To eliminate this interaction in [22] another controller for UPFC based on coordination control of real and reactive powers has proposed. Though the problem of interaction has overcome but the shortcoming of this strategy is the complexity of the control system has increased. Two control loops (inner and outer) are required to regulate the real and reactive power flow. Afterwards simplified controllers for UPFC have been developed in [23–25] where only a single loop has used to regulate each power system parameters. There is a common requirement of all the controllers discussed above is the need of output feedback control system for regulating the power system parameters. The problem in the design of an output feedback proportional-integral (PI) control system for UPFC is the presence of low margin of stability associated with the series inductance of the transmission line. Later on intelligent controllers with specific reference to fuzzy logic controllers or artificial neural network have been proposed to overcome the problem. UPFC has employed in [26,27] to damp oscillation and improve transient stability where the controllers of both converters have been designed using ANN. But the difficulty of ANN based controller is to generate the training patterns of the controller for complex power system network.

In contrast, FL controller is capable of solving complex problems whose system behavior is not well understood. Another advantage of FL controller is its robustness to system parameters and operating conditions changes [28]. Different controllers for UPFC have been presented in [29–31], based on FL. However, all the UPFC's control methods are developed for the application of oscillation damping of power system network. Very few literatures are reported on FL based UPFC's application to enhance the power flow and maintain voltage profile of the system dynamically. In [32], dynamic flow of power is analyzed using FL based UPFC where only shunt converter has designed with FL. For series converter rotating orthogonal-coordinate method has used. However, during the shunt converter design, instead of taking sending end voltage as feedback signal it considered receiving end voltage as feedback. Another study [33] proposed controller of UPFC using FL to improve voltage profile.

Different from previous works, in this study a new control system for dynamic UPFC is proposed to enhance PTC and bus voltage profile, as well as to reduce power capacity loss. Both controllers of series and shunt converters of UPFC are developed using FL controller. By using FL controller, the problem of stability that usually occurs with PI controller based feedback control can be overcome. Furthermore, the application of FL controller reduced the complexity of UPFC's internal control system, which commonly occurs in conventional controllers such as decoupled and cross coupled controllers. In this study, PSCAD software is used to model and test the proposed UPFC controller. Since PSCAD doesn't provide FL toolbox, a new module for the FL is developed in C language. By using C, the simulation can be done within the PSCAD environment. The proposed UPFC controller is tested by using IEEE-5 and 14 bus systems. In addition, comparative studies also have been conducted to prove the advantage of the proposed controller over different control methods of UPFC.

The rest of the paper is organized as follows: Section 2 focuses on UPFC model. Section 3discusses about the newly developed shunt and series control systems of UPFC along with the FL tool box design in PSCAD. Section 4presents the simulation results after connecting UPFC in two IEEE case studies including two comparative studies to prove the effectiveness of the proposed controller. The significant points of this paper are summarized in the conclusion.

2. UPFC model

The dynamic model of the UPFC is shown in Fig. 1. UPFC connects to the transmission line with shunt and series voltage source converters (VSC) which are coupled via a common DC link. Normally, the shunt VSC is considered as STATCOM and series one as a static synchronous series compensator (SSSC). Low pass AC filters are connected in each phase to prevent the flow of harmonic currents generated due to switching. The transformers connected at the output of converters to provide the isolation, modify voltage/current levels and also to prevent DC capacitor being shorted due to the operation of various switches. Insulated gate bipolar transis-

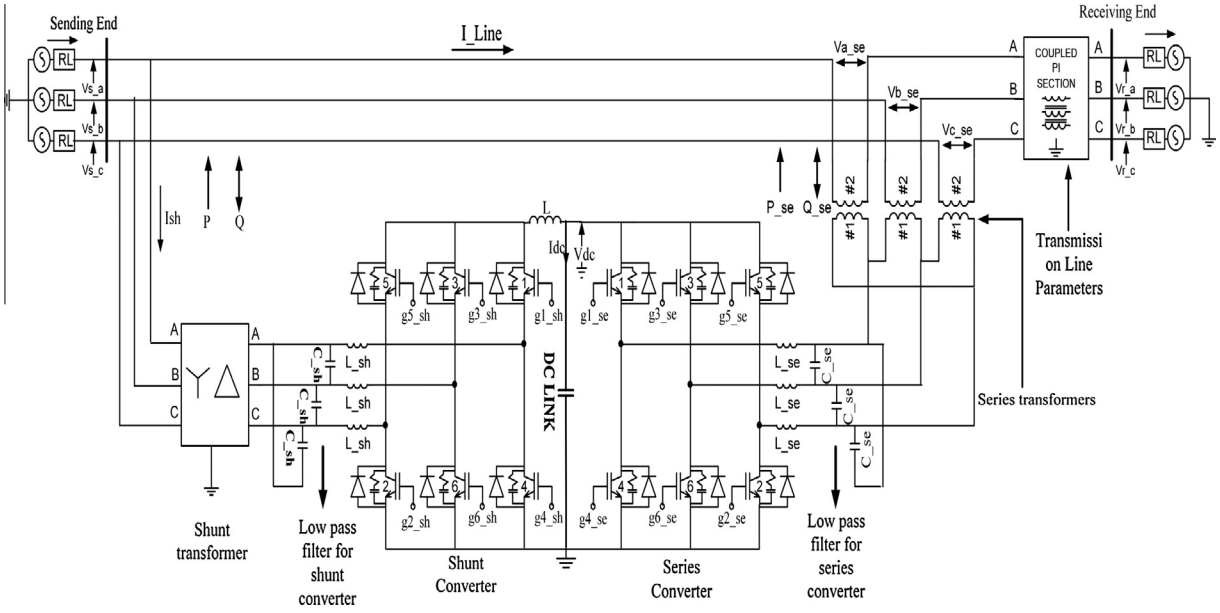


Fig. 1. Dynamic model of UPFC.

tors (IGBTs) with anti-parallel diodes are used as switching devices for both converters [34].

3. UPFC Controller

UPFC controller consists of two controllers namely series and shunt controller. The block diagrams of proposed shunt and series controllers are presented in Fig. 2(a) and (b) respectively.

3.1. Shunt controller

A controlled current has been drawn by the shunt converter from the transmission line with the motives:

- To maintain the transmission line voltage at its reference value by absorbing or providing reactive power from the transmission line.
- To retain the voltage level of the DC link capacitor at its reference value by drawing real power from the line.

The control algorithm of shunt converter build inside PSCAD/EMTDC software is given in Fig. 3(a) and (b). Fig. 3(a) represents the FL controllers of bus voltage and DC voltage to generate (*Vmag_sh*) and (*angle_sh*) and Fig. 3(b) illustrates PWM method to generate firing signals for the UPFC shunt converter switches.

In order to control the bus voltage, sending-end voltage (*Vs_measured*) is measured instantly and subtracted from its reference value (*Vs_reference*) as per unit (*pu*) which reveals V_s*_error*. This error signal and the rate of change of error (V_s*_error_rate*) have been given as inputs to a FL block.

The FL block is built in PSCAD software by writing C-programming which is discussed at the later part of this section. The output of FL gives the magnitude of injected shunt voltage (*Vmag_sh*) in pu. Similarly, DC link capacitor voltage (*Vdc_measured*) is also measured and subtracted from its reference value (*Vdc_reference*) to get V_{dc}*_error*. Another FL with inputs error signal and the rate of change of error (V_{dc}*_error_rate*) are employed to obtain angle (*angle_sh*) in degree by multiplying it to $180/\pi$. Phase Locked Loop (PLL) extracts the phase angle of sending-end voltage (*a_s*).The difference of these angles (*a_s – angle_sh*) and the magnitude (*Vmag_sh*) have used in 'sin ()' function to obtain the reference signals for pulse width modulation (PWM). In PWM block, the reference signals are compared with carrier (triangle) signal which has a switching frequency of 4.5 KHz. The outputs of the comparators are given as firing signals for the converter switches.

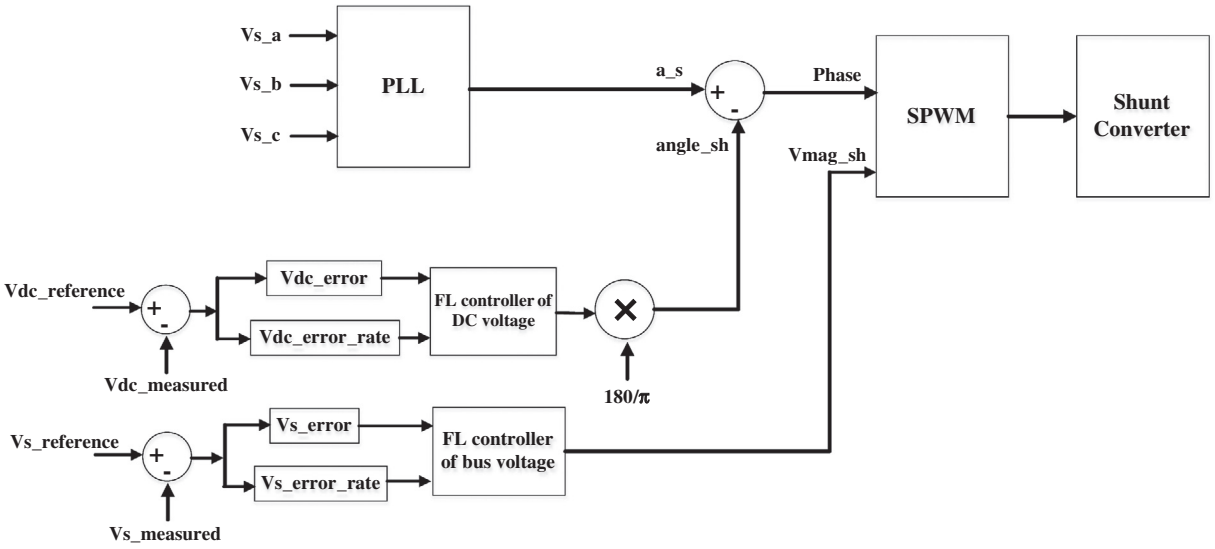
Here, the FL blocks are used in the shunt converter control algorithm have developed in an innovative way by writing C-program in PSCAD software itself. From the controller stated in Fig. 3(a), it can be seen that 2 FL blocks have been used. Each FL block consists of two inputs and one output. For explanation convenience all the input and output parameters of the FL controllers are named identically. The first input is the error obtained from the difference between reference value and the measure values of the parameters like line AC voltage, DC voltage. The other input is error-rate which is one-sampling before error values. The linguistic variables of error are LN (large negative), MN (medium negative), SN (small negative), Z (zero), SP (small positive), MP (medium positive), and LP (large positive). Similarly error rates are LN1 (large negative1), MN1 (medium negative1), SN1 (small negative1), Z1 (zero1), SP1 (small positive1), MP1 (medium positive1), and LP1 (large positive1). The linguistic variables of output are NB (negative big), NM (negative medium), NS (negative small), ZO (zero output), PS (positive small), PM (positive medium), and PB (positive big). The FL controllers are constituted of the following steps as shown in Fig. 4.

In fuzzification, the real input values are converted into fuzzy set values which assign the degree to which these inputs belong to each of the appropriate fuzzy sets. Fuzzification is carried out through equation of slope. In Fig. 5, for determining membership degree of LN membership function of error input is shown and explained by Eqs. (1)–(4).

Equation of slope,

$$\frac{y_2 - y_1}{x_2 - x_1} = \frac{y - y_1}{x - x_1} \tag{1}$$

where y_1 is the minimum value of membership degree, y_2 is maximum value of membership degree, x_1 is minimum value of



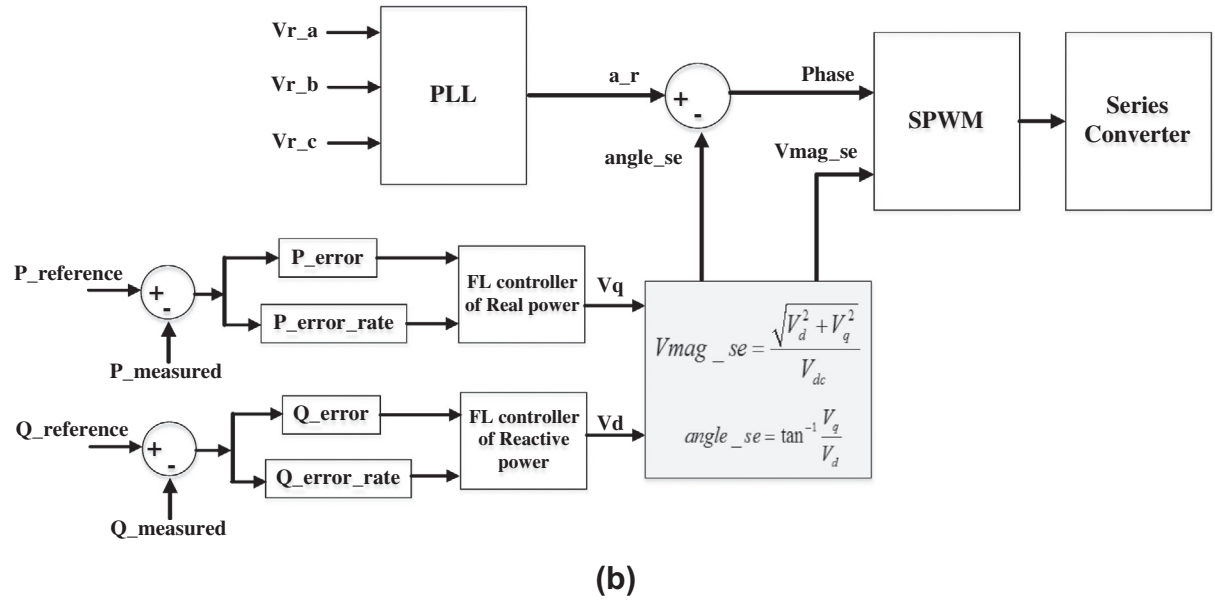


Fig. 2. Block diagram of proposed (a) shunt controller and (b) series controller of UPFC.

membership function, x_2 is maximum value of membership function, y is membership degree, x is the input variable.

It can be noticed that first part of equation 1 represents the slope formula:

$$m = \frac{y_2 - y_1}{x_2 - x_1} \tag{2}$$

By putting the parameters names from Fig. 5 Eq. (1)becomes,

$$\frac{y_2 - y_1}{u.limit - l.limit} = \frac{y - y_1}{error - l.limit} \tag{3}$$

To calculate the membership degree for the membership function, Eq. (3)becomes:

$$m.\text{degree} = slope \times (error - l.limit) + y_1 \tag{4}$$

Eq. (4) gives the fuzzified values of the real input value. All the membership functions of the FL controllers consist of triangular based membership functions as they provide smooth control and are shown in Fig. 6(a)–(c).

The fuzzy based input and output membership functions are formed in C-program by using one dimensional array concept. The triangular membership functions are divided into two slope equations for fuzzifications. The one dimensional array in C-program for Fig. 5 is given as:

$$float\ LN[3] = \{-0.9, -0.675, -0.45\}$$

For vertical axis another one dimensional array is employed representing the corresponding values of membership function along vertical axis:

$$float\, vert[3] = \{0, 1, 0\}$$

where vert represents the vertical axis and values 0, 1 and 0 are corresponding values of −0.9, −0.675 and −0.45 along vertical axis as shown in Fig. 5. A sample program for fuzzification of one part of membership function from −0.9 to −0.675 as shown in Fig. 5 is given as:

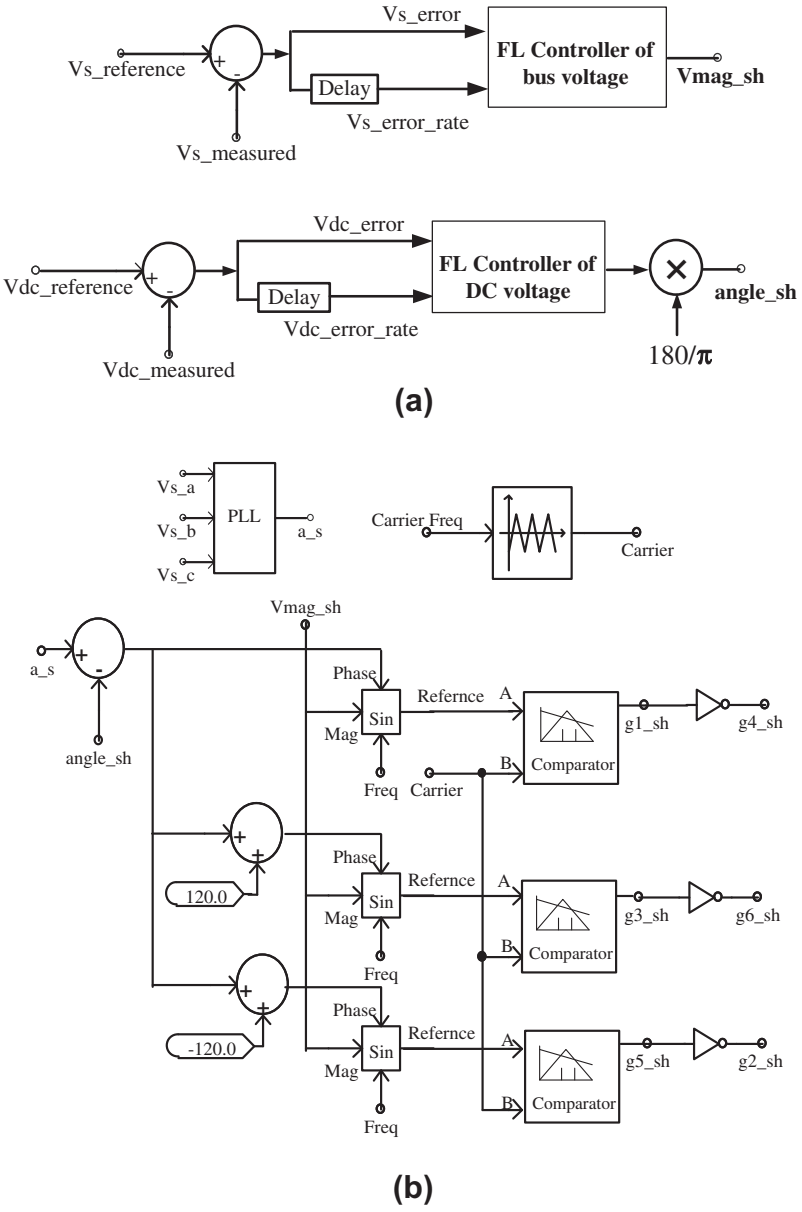


Fig. 3. (a) FL controllers of bus voltage and DC voltage to generate Vmag_sh and angle_sh and (b) SPWM technique to generate signals for shunt converter switches of UPFC.

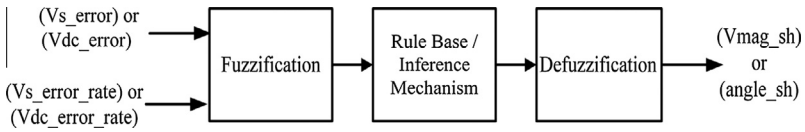


Fig. 4. Internal architecture of FL controller.

$if(error \geqslant LN[0]\ \&\&\ error \leqslant LN[1])$
{
$x_1 = LN[0];$
$y_1 = vert[0];$
$x_2 = LN[1];$
$y_2 = vert[1];$
$slope = \frac{(y_2 - y_1)}{(x_2 - x_1)};$
$m.\text{degree} = slope \times (error - l.limit) + y_1;$
}

Similarly all other input and output membership functions of fuzzy based controllers are fuzzified by using one dimensional array concept. The fuzzy rule base is used in IF-THEN rule form to assign the input and output control such as:

IF error is LN and error-rate is LN1
THEN output NB
IF error is LN and error-rate is LP1
THEN output ZO

The other rules of FLs are summarized in Table 1.

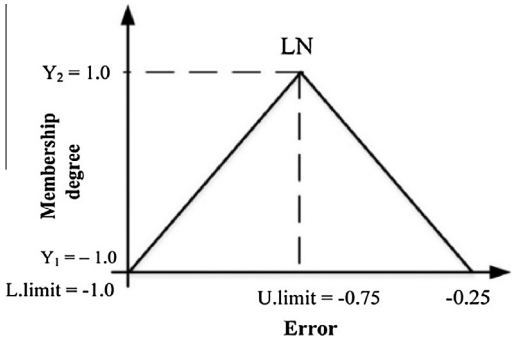


Fig. 5. Fuzzification of error at certain time constant.

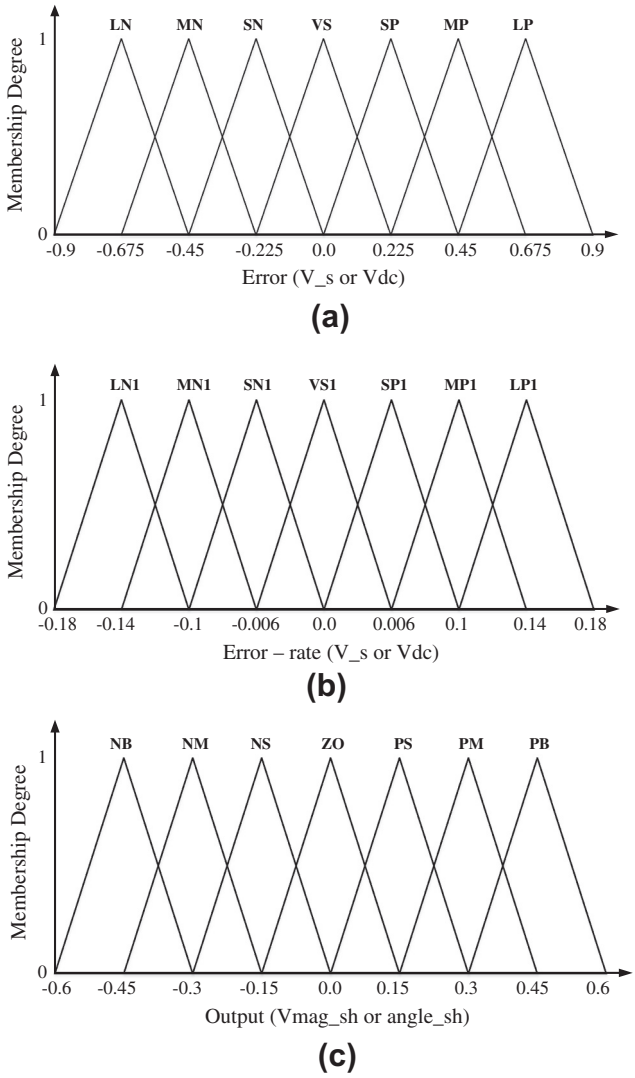


Fig. 6. Membership functions of (a) error, (b) error-rate and (c) output for V_s and Vdc.

The inference mechanism evaluates the active signals for taking control actions from the fuzzy rules. Finally, defuzzification is carried out through weighted average to convert the fuzzy linguistic variable into real crisp values. Defuzzification through weighted average is determined as:

Table 1
Rule table for FL controllers of AC or DC voltages.

Error	Error-rate						
	LP1	MP1	SP1	VS1	SN1	MN1	LN1
LP	PB	PB	PB	PM	PM	PS	ZO
MP	PB	PB	PM	PM	PS	ZO	NS
SP	PB	PM	PM	PS	ZO	NS	NM
VS	PM	PM	PS	ZO	NS	NM	NM
SN	PM	PS	ZO	NS	NM	NM	NB
MN	PS	ZO	NS	NM	NM	NB	NB
LN	ZO	NS	NM	NM	NB	NB	NB

$$\text{Weighted Average} = \frac{\sum_{i=1}^{n} m_i \times w_i}{\sum_{i=1}^{n} m_i} \tag{5}$$

where m_i is membership degree of each output rule, w_i is weight associated with each rule, n is the number of active rules.

3.2. Series controller

The series converter controls the power flow across the line by injecting a voltage in series with the line current having controllable magnitude and angle.

The control system of series converter developed in PSCAD environment is illustrated in Fig. 7(a) and (b). Fig. 7(a) represents the FL controllers of real and reactive powers to obtain the magnitude and phase angle of the series injected voltage. And Fig. 7(b) illustrates PWM signals block to generate switching signals for series converter switches of UPFC.

The real and reactive power ($P_{measured}$ and $Q_{measured}$) flow through the line are measured and subtracted from their reference value ($P_{reference}$ and $Q_{reference}$). These revealed the error signals *P_error* and *Q_error*. These two error signals and their rate of change (*P_error_rate* and *Q_error_rate*) are given as inputs to two FL controllers as shown in Fig. 7(a). The outputs of the two fuzzy logic controllers provide the orthogonal components of the series injected voltage (V_q and V_d). Using these values the magnitude and phase angle of series injected voltage has been calculated by using the following equations:

$$Vmag\_se = \frac{\sqrt{V_d^2 + V_q^2}}{V_{dc}} \tag{6}$$

$$angle\_se = \tan^{-1}\frac{V_q}{V_d} \tag{7}$$

The phase angle of receiving-end voltage (*a_r*) is obtained through *PLL*. The angle (*angle_se*) obtained from Eq. (7) is subtracted from angle (*a_r*) of receiving-end voltage. The resultant angle and the magnitude of the voltage calculated from Eq. (6) are used in 'sin ()' function block to obtain reference signals for PWM. Then these reference signals are compared with carrier (triangle) signals as shown in Fig. 7(b). The switching frequency of the carrier has kept same like shunt controller i.e. 4.5 kHz. The firing signals of IGBTs are generated by comparing reference with carrier signals.

For series controller the FL controllers are designed in the same way like shunt controller. The differences have been observed only in specifying the inputs and outputs of the FL controllers and linguistic variables of the outputs. The inputs of the real power FL controller are (*P_error* & *P_error_rate*) and for reactive power FL controller these are (*Q_error* & *Q_error_rate*). The outputs of both real and reactive power FL controllers are named as V_q and V_d respectively. For real power FL controller output variables are VSP (very small positive), SP (small positive), MPS (medium positive small), MP (medium positive), MPB (medium positive

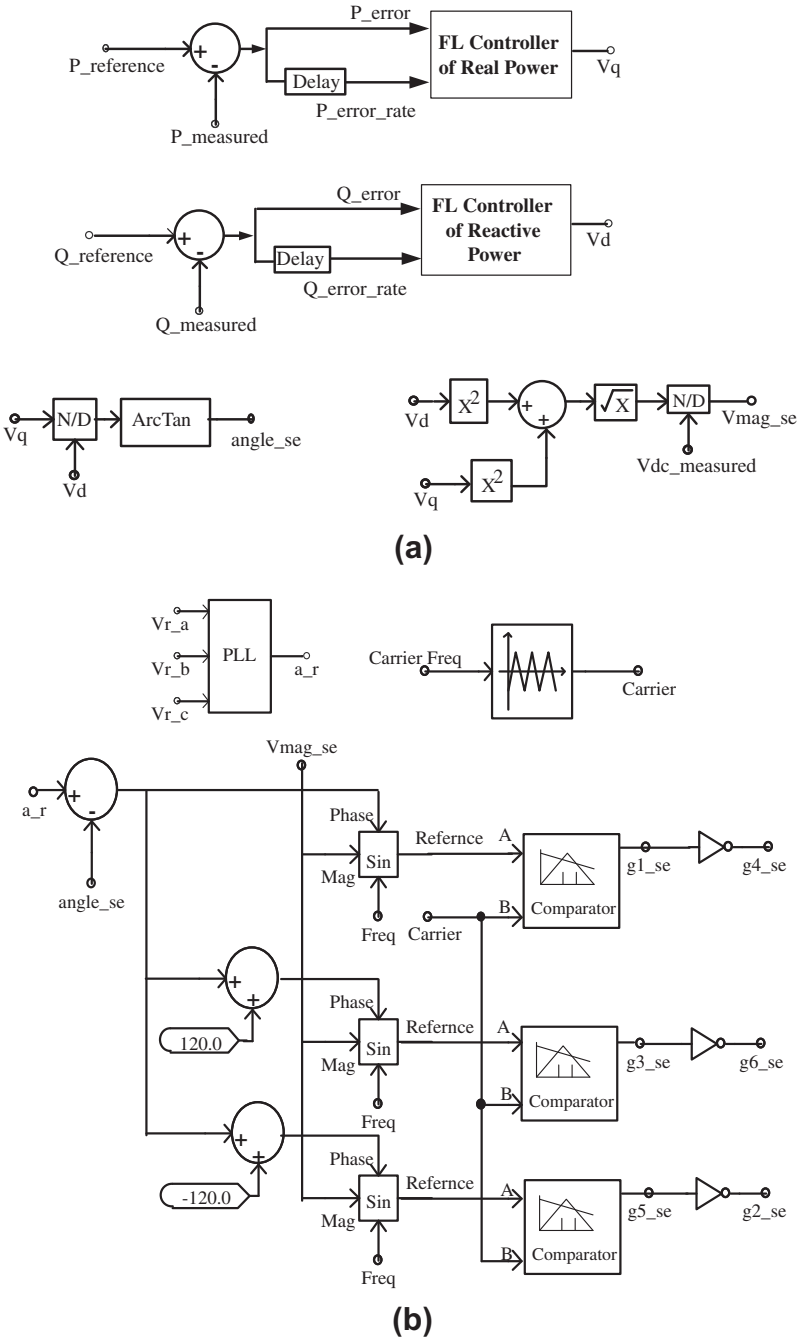


Fig. 7. (a) FL controllers of real and reactive powers to generate *Vmag_se* and *angle_se*, and (b) SPWM technique to generate signals for series converter switches of UPFC.

big), BP (big positive), and VBP (very big positive). For reactive power FL the output linguistic variables are VBN (very big negative), BN (big negative), MNB (medium negative big), MN (medium negative), MNS (medium negative small), SN (small negative) and VSN (very small negative). Also, the universe of discourse is different for inputs and outputs in fuzzification process of both the FL controllers shown in Fig. 7(a). The membership functions for error, error-rate and outputs of both real and reactive powers are illustrated in Figs. 8 and 9 respectively.

Tables 2 and 3 represented the IF-THEN rules used in the two FLs for active and reactive powers.

Basically, the UPFC controller will depend on the loading of the power system network. Whenever, there are changes in the loading, some adjustment of the membership of fuzzy logic controller are required.

4. Results and discussions

In this section, IEEE-5 bus and IEEE-14 bus test systems are selected as case studies to evaluate the performance of the proposed controller based UPFC. The bus systems have built inside PSCAD software using the dynamic components available inside PSCAD library.

4.1. Case study: IEEE 5 bus system

At first, the performance of UPFC has been tested in IEEE 5 bus system for PTC enhancement. In this test system, buses 1 and 2 are generator buses (PV buses) and buses 3, 4, 5 are load buses (PQ buses). The base case has been taken as 175 kV and 100 MVA. A single line diagram of the network is presented in Fig. 10 along with the location of UPFC.

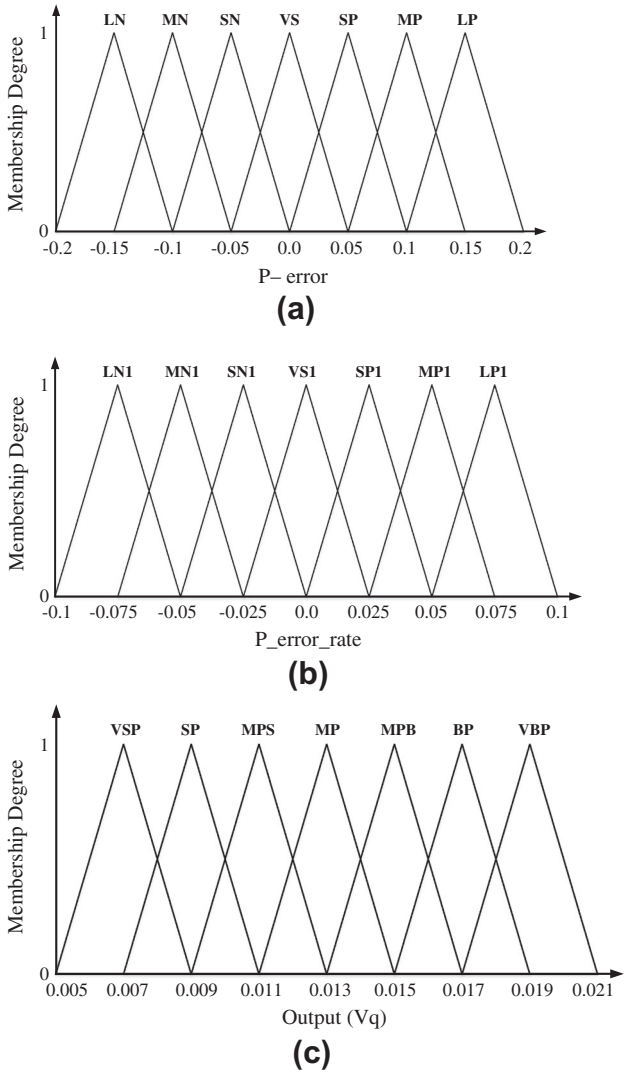


Fig. 8. Membership functions of (a) P_error, (b) P_error_rate and (c) quadrature component of injected voltage (V_q).

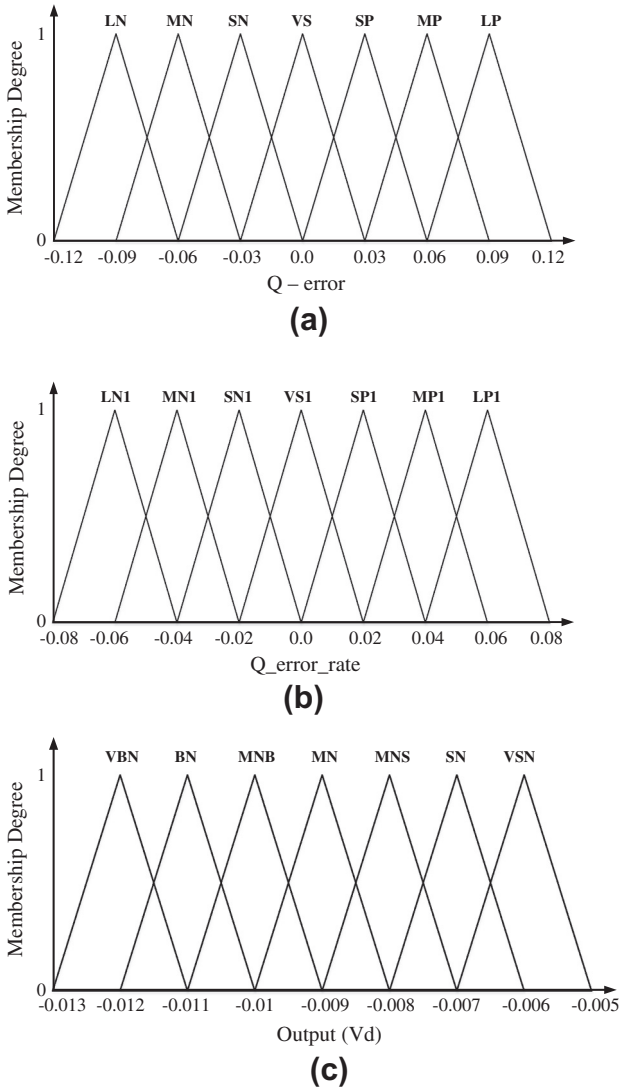


Fig. 9. Membership functions of (a) Q_error, (b) Q_error_rate and (c) direct component of injected voltage (V_d).

After connecting UPFC across line 2–3, improvement has been observed in the power flow through the line. The simulation results of real and reactive powers with and without UPFC are shown in Figs. 11 and 12 respectively. It is found that without UPFC the flow of real and reactive power were 0.76 p.u (76 MW) and 0.0732 p.u (7.32 MVAR) respectively. As soon as UPFC has been connected to the line 2–3 the real and reactive power flow have become 0.797 p.u (79.7 MW) and 0.0657 p.u (6.57 MVAR) respectively. Moreover, UPFC's presence not only increased the real power flow but also helped to reduce the power capacity losses in the network. Before connecting UPFC the real and reactive power capacity losses were 6.2 MW and 4.502 MVAR respectively. While the real and reactive power capacity losses have reduced to 5.492 MW and 3.905 MVAR respectively when UPFC placed in the network.

As the aim of UPFC is to maintain the AC bus voltage profile, hence with UPFC's connection the voltage profiles across both ends of the line have enhanced too. Figs. 13 and 14 illustrated that before connecting UPFC the magnitudes of the voltages were 0.9846 p.u and 0.935 p.u across sending and receiving ends respectively. While voltages have enhanced to 1.002 p.u and 0.961 p.u after UPFC has connected to the line. Furthermore, with UPFC the difference of phase angles ($\theta_{se} - \theta_{rec}$) between sending and receiving ends also reduced from 7.143° to 5.05° which is shown in Fig. 15.

Table 2
Rule table for real power FL controller.

Error	Error-rate						
	LP1	MP1	SP1	VS1	SN1	MN1	LN1
LP	VBP	VBP	VBP	BP	BP	MPB	MP
MP	VBP	VBP	BP	BP	MPB	MP	MPS
SP	VBP	BP	BP	MPB	MP	MPS	SP
VS	BP	BP	MPB	MP	MPS	SP	SP
SN	BP	MPB	MP	MPS	SP	SP	VSP
MN	MPB	MP	MPS	SP	SP	VSP	VSP
LN	ZO	NS	NM	NM	NB	NB	NB

Another important factor associated with UPFC is the proper charging of the DC link capacitor. Since, it controls the real power flow between the two converters. From Fig. 16 it is viewed that the DC link capacitor has charged to 21.08 kV with UPFC which is 1.414 times of the secondary terminal voltage of the shunt transformer. According to Fig. 17, a voltage of approximately 10.35 kV has

Table 3
Rule table for reactive power FL controller.

Error	Error-rate						
	LP1	MP1	SP1	VS1	SN1	MN1	LN1
LP	VSN	VSN	VSN	SN	SN	MNS	MN
MP	VSN	VSN	SN	SN	MNS	MN	MNB
SP	VSN	SN	SN	MNS	MN	MNB	BN
VS	SN	SN	MNS	MN	MNB	BN	BN
SN	SN	MNS	MN	MNB	BN	BN	VBN
MN	MNS	MN	MNB	BN	BN	VBN	VBN
LN	MN	MNB	BN	BN	VBN	VBN	VBN

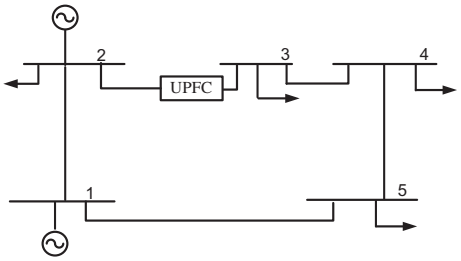


Fig. 10. Single line diagram IEEE 5 bus system.

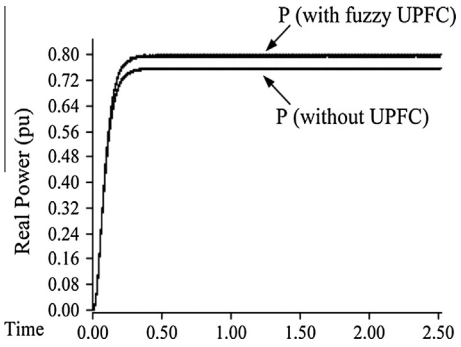


Fig. 11. Real power on line 2–3.

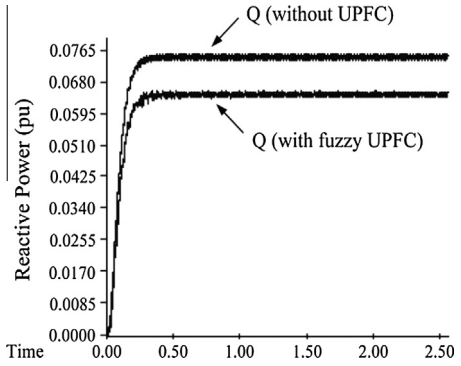


Fig. 12. Reactive power on line 2–3.

injected to the line in series with a line current of 0.7 kA. From the graph a phase difference between the injected voltage and line current has observed which has indicated the flow of both real and reactive power flow through the line.

Finally, all the bus voltages are represented in Fig. 18 for both UPFC and without UPFC cases. Overall it can be seen that UPFC has contributed to maintain nominal voltage profile across all the buses.

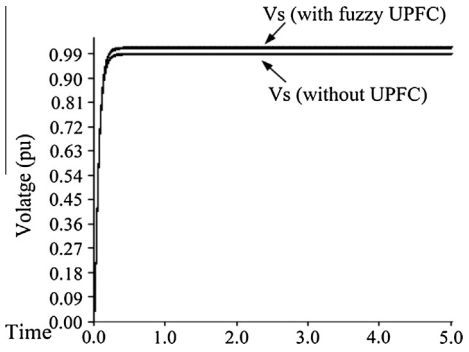


Fig. 13. Sending end voltage across line 2–3.

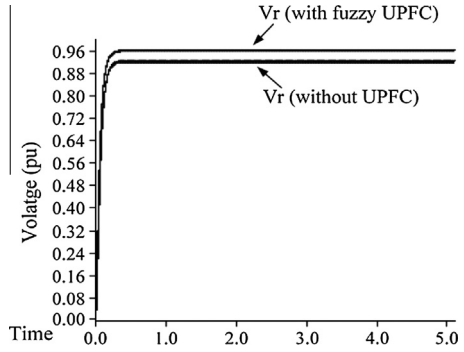


Fig. 14. Receiving end voltage across line 2–3.

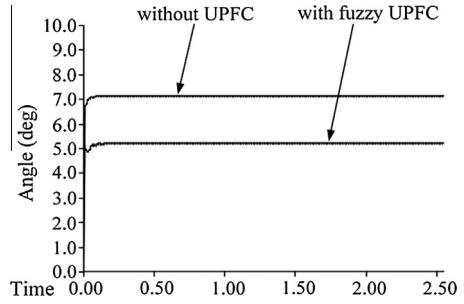


Fig. 15. Angle difference (θ_{se} - θ_{rec}) between two ends of line 2–3.

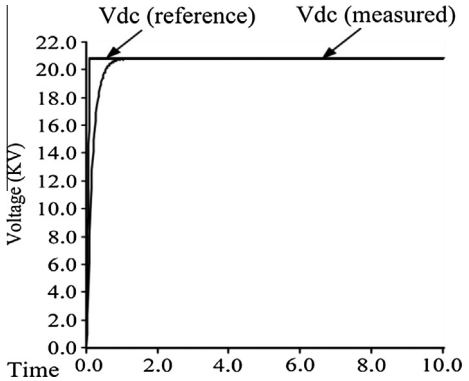


Fig. 16. DC voltage across DC link capacitor in IEEE 5 bus system.

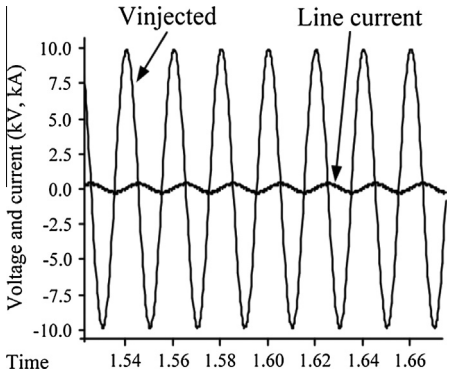


Fig. 17. Series injected voltage and line current for IEEE 5 bus system.

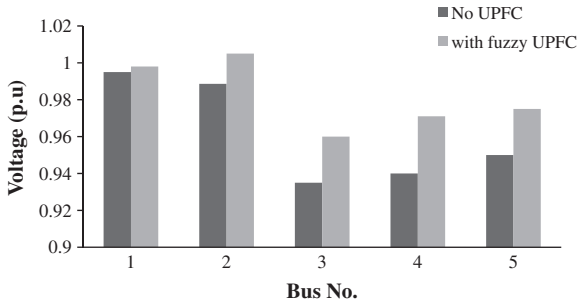


Fig. 18. Voltage profile across all the buses in IEEE-5 bus system.

4.2. Case study: IEEE 14 bus system

A single line diagram of the IEEE-14 bus network is depicted in Fig. 19. It is a classical power system constitutes of 2 generator buses, 11 load buses and 19 lines. To provide reactive power support it got three synchronous condensers at buses 3, 6, 8. The base case has been taken as 138 kV and 100 MVA. In this case study, UPFC has been placed across line 9–14 as shown in Fig. 19.

According to Figs. 20 and 21, the flow of real power and reactive power are 0.06235 p.u (6.235 MW) and 0.1005 p.u (10.05 MVAR) respectively during UPFC is disconnected from line 9–14. When UPFC connected to the line, the real power flow has reached to 0.07284 p.u (7.284 MW), which has found 1.015 MW more than its nominal value. On the other hand, reactive power has reduced by 0.655 MVAR (from 10.05 MVAR to 9.395 MVAR) from its nominal value which is presented in Fig. 21. Similar way the real and reactive power capacity losses have reduced from 13.562 MW to 11.023 MW and 26.6206 MVAR to 22.736 MVAR respectively when UPFC has connected to the network.

In case of bus voltages across line 9–14 both receiving and sending ends voltage magnitudes have increased when UPFC is connected to the line. Referring to Fig. 22, with UPFC the sending end voltage has reached to 1.008 p.u from 0.9886 p.u. Similarly, receiving end voltage becomes 0.973 p.u with UPFC as per Fig. 23 which was 0.944 p.u without UPFC. In addition, the phase angle difference between both the ends decreases too. From Fig. 24, this difference is found 0.23° without UPFC which has become 0.0753° as soon as UPFC started to operate.

As per Fig. 25, the DC link capacitor has charged up-to its nominal value which was set to 10.421 kV. The graph of series injected voltage and line current with UPFC are presented in Fig. 26 whose values are 5.04 kV and 0.2 kA respectively.

All the bus voltages with respect to their bus numbers are plotted in Fig. 27 for both with and without UPFC. It has been observed that after UPFC has placed to the network all the bus voltages has improved.

4.3. Comparison among the performances of different control methods of UPFC

In this section, to prove the effectiveness of the proposed controller two comparative studies have been presented. In first study, the comparison is conducted between the performances of proposed UPFC controller based on FL and PI controllers. Another study is carried out among the proposed controller and the controllers from previous literatures of UPFC. In addition, since the main functions of UPFC are to control power flow and maintain bus voltage profile. Hence, in the comparative studies the references of powers and AC bus voltages have been chosen different to ensure UPFC's validation in governing the power system parameters.

4.3.1. Comparison between performances of FL and PI based proposed UPFC controller

In Table 4, a comparison is presented between the performances of UPFC with proposed FL controller and UPFC with a controller which has designed just by replacing FL controller with PI controller in the proposed method. Initially, without UPFC the

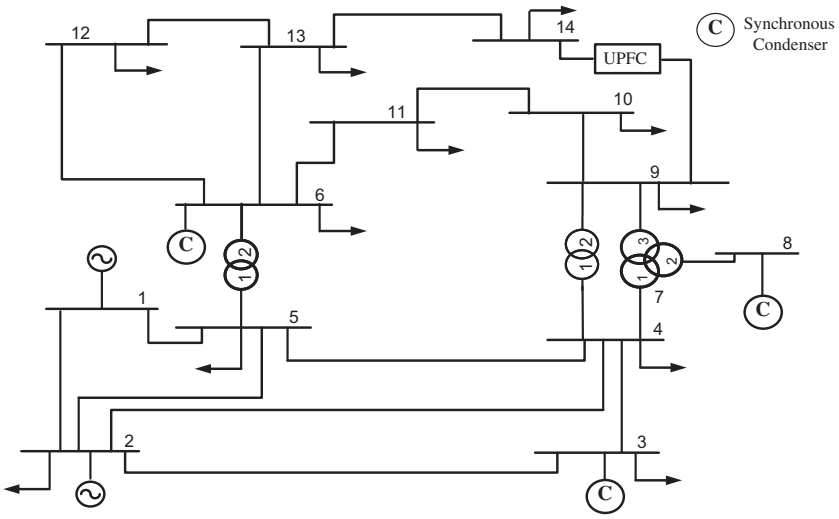


Fig. 19. Single line diagram of IEEE 14 bus system.

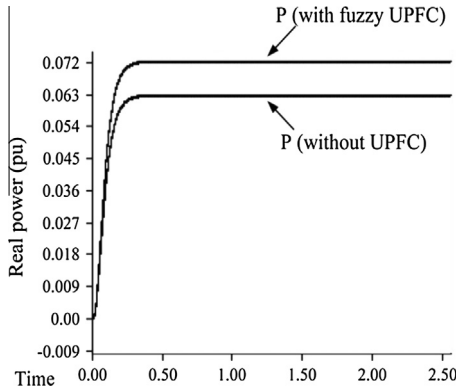


Fig. 20. Real power on line 9–14.

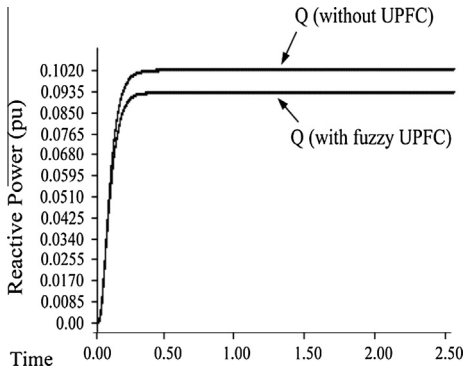


Fig. 21. Reactive power on line 9–14.

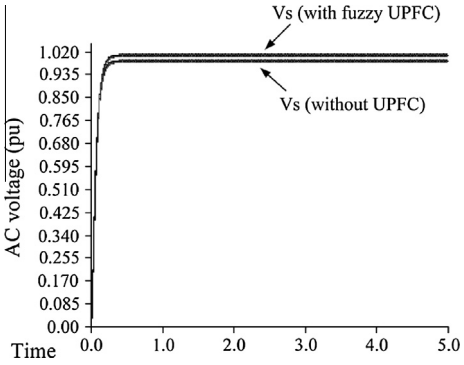


Fig. 22. Sending end voltage across line 9–14.

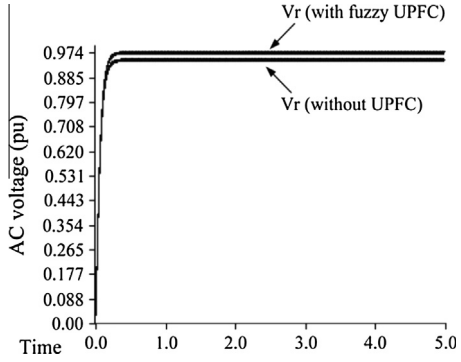


Fig. 23. Receiving end voltage across line 9–14.

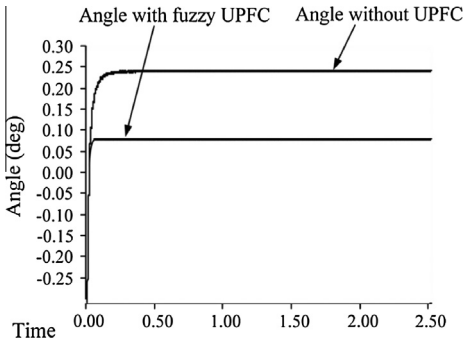


Fig. 24. Angle difference ($\theta_{se} - \theta_{rec}$) between two ends of line 9–14.

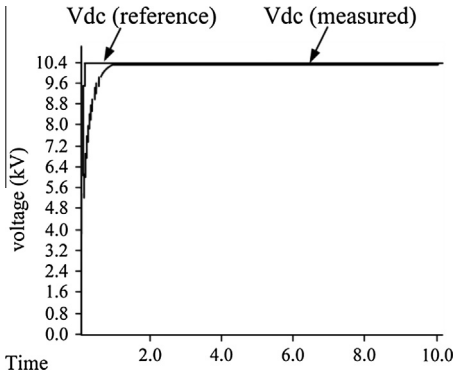


Fig. 25. DC voltage across DC link capacitor in IEEE 14 bus system.

reference values of bus voltage, DC capacitor voltage, real and reactive powers are set for both the case studies. The reference values of real and reactive are set to 80 MW and 6.55 MVAR respectively for IEEE-5 bus system. From the table it has been found that the real power flow with PI control based UPFC is 77.6 MW while with FL based UPFC it has become 79.7 MW. The flow of reactive power with PI and FL controlled UPFC is 6.7 MVAR and 6.57 respectively. Both real and reactive power flow with FL based UPFC have reached closed to the reference values. In contrary, with PI based UPFC the power flow on the line always fall short from the reference values. The reasons for PI based UPFC's lacked performance is in PI based UPFC 4 PI controllers have been used. And it is very difficult to tune the exact gains (K_p and K_i) values of these controllers. For IEEE-14 bus system, the reference values of real and reactive power flow have fixed to 7.3 MW and 9.375 MVAR respectively. The real power flow has found 6.9 MW and 7.284 MW with PI and FL based UPFC respectively where the flow of reactive power observed are 9.758 MVAR and 9.395 MVAR.

In case of bus voltage profile enhancement FL based UPFC has exhibited better performance than PI based UPFC. For IEEE-5 bus system, based on the sending end voltage of 0.9846 p.u without UPFC case the reference for sending end voltage has set to 1.005 p.u. With FL based UPFC this voltage has reached to 1.003 p.u, while PI based UPFC has only abled to enhance this voltage up to 0.9974 p.u. In case of IEEE-14 bus network, for reference value of 1.01 p.u, PI based UPFC has improved the sending end voltage only 0.755% i.e. 0.9981 p.u from its nominal value. On the other hand, this voltage enhancement percentage has found 1.99% with FL based UPFC. For receiving end voltage of the line also FL based UPFC has outperformed the PI based UPFC in both the case studies. The reduction in the angle differences ($\theta_{se} - \theta_{rec}$) between two ends of the line also found better with FL based UPFC than PI based UPFC in both case studies.

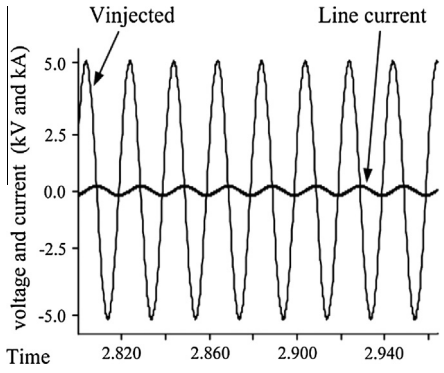


Fig. 26. Series injected voltage and line current for IEEE 14 bus system.

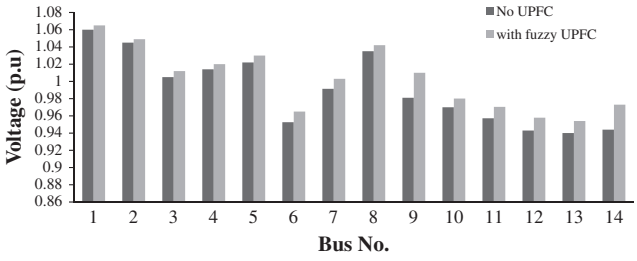


Fig. 27. Voltage profile across all the buses in IEEE-14 bus system.

According to Table 4, without UPFC the real and reactive power capacity losses in IEEE-5 bus system were 6.2 MW and 4.502 MVAR respectively. After PI based UPFC has placed in the line these losses are reduced to 5.756 MW and 4.254 MVAR compared to their nominal values. However, the reduction in real and reactive power capacity losses with FL based UPFC is observed much better i.e. real and reactive power capacity losses have reduced 0.264 MW and 0.35 MVAR respectively more compared to PI based UPFC. For IEEE-14 bus system also the reduction in power capacity losses with FL based UPFC is higher than the PI based UPFC. Without UPFC the real power capacity loss was 13.562 MW which became 12.543 MW and 11.023 MW after PI and FL based UPFC respectively connected to the network. Similarly, reactive power capacity loss also without UPFC (26.6206 MVAR) is found higher than the reactive power capacity losses with PI (24.15 MVAR) and FL (22.7363 MVAR) based UPFC.

The most important parameter for controlling the real power flow in the line is the charging of DC link capacitor. Therefore, it is very essential for the DC link capacitor to charge up to its reference value. For IEEE-5 bus system this value was set to 21.1 kV. When PI based UPFC has started operating the capacitor took 2.35 s to charge up-to19.85 kV where the same capacitor in case of FL based UPFC charged to 21.08 kV within 0.55 s. The capacitor in IEEE-14 bus system charged to 9.45 kV and 10.435 kV for PI and Fuzzy based UPFC respectively with a time period of 2.6 s and 0.75 s. Since the response of UPFC controller is related to the charging of the capacitor. Hence, it can be said that the response time of the FL based UPFC is better than the PI based UPFC.

4.3.2. Comparison among performance of proposed and different control methods of UPFC

In this part, the performance of proposed controller are compared with the performances of different control methods [18,21,22,25] based UPFCs to prove the robustness of the proposed controller. In Tables 5 and 6, the comparisons are presented for both IEEE-5 and IEEE-14 bus systems respectively.

From Table 5, it can be seen that in IEEE-5 bus network, real and reactive power flow with the proposed FL based UPFC almost reached to the reference values which have set to 90 W and 6 MVAR respectively. Whereas the other control methods based UPFC [18,21,22,25] have performed less efficiently than the proposed method. In addition, the proposed FL based UPFC improved the voltage profile of the sending end bus closed to the reference value of 1.01 pu. However, UPFCs with other control methods cannot boost the UPFC bus voltage to the expected level. The percentage of accuracy level of the proposed UPFC control system is found always over 99% for controlling any power system parameters. On the other hand, the percentage of accuracy level for other UPFC control methods is below 97.5%. Moreover, the reduction of real and reactive power capacity losses with FL based UPFC are observed higher than the rest of control systems based UPFCs. It is observed that with proposed FL based UPFC the reduction in real and reactive power capacity losses are 10.64% and 12.5% respectively. However, the real power capacity losses for UPFCs designed with control methods from [18,21,22,25] are 6.2%, 7.01%, 7.8% and 7.75% respectively. In terms of reactive power capacity losses the percentages of reduction are 5.04%, 6.6%, 9.26% and 10.27% respectively.

For IEEE-14 bus system, the proposed FL based UPFC has outperformed the UPFC with other control methods discussed in [18,21,22,25], alike IEEE-5 bus networks. The results are tabulated in Table 6.

Though UPFC based on FL controller has significant advantages, the main limitation is on the selection of membership function when the reference values of the power system parameters change. When the reference values of the parameters change, the error signals also change. To regulate that signal properly membership functions of the FL controller need to be adjusted. This adjustment can be done by changing the IF-THEN rules of the FL controller

Table 4
Comparison between FL and PI based UPFC controller performance for IEEE 5 and 14 bus system.

Transmission network parameters	Case studies					
	IEEE 5 bus system (line 2–3)			IEEE 14 bus system (line 9–14)		
	Without UPFC	With PI UPFC	With fuzzy UPFC	Without UPFC	With PI UPFC	With fuzzy UPFC
Real power (MW)	76	77.6	79.7	6.45	6.9	7.284
Reactive power (MVAR)	7.32	6.7	6.57	10.05	9.758	9.395
Sending end voltage (p.u.)	0.9846	0.9974	1.004	0.9886	0.9981	1.008
Receiving end voltage (p.u.)	0.935	0.9458	0.961	0.9446	0.956	0.973
Angle difference ($\theta_{se} - \theta_{rec}$) (deg)	7.143	5.85	5.05	0.23	0.145	0.0753
Real power capacity losses (MW)	6.2	5.756	5.492	13.562	12.543	11.023
Reactive power capacity losses (MVAR)	4.502	4.254	3.905	26.62	24.15	22.736
DC link capacitor voltage (KV)	–	19.85	21.08	–	9.45	10.435
Capacitor charging time (s)	–	2.15	0.55	–	2.25	0.75

Table 5
Comparison among the performances of different control methods of UPFC controller for IEEE-5 bus system.

Parameter	Real power (MW)		Reactive power (MVAR)		Sending end voltage (pu)		Average % of accuracy (%)	Real power loss (MW)	Reactive power loss (MVAR)
Control methods	Reference	Measured	Reference	Measured	Reference	Measured			
Proposed	90	89.34	6.0	6.025	1.01	1.009	99.45	5.492	3.905
Ref. [18]	90	87.23	6.0	6.273	1.01	0.9945	97.01	5.865	4.32
Ref. [21]	90	87.9	6.0	6.215	1.01	0.9971	97.64	5.832	4.25
Ref. [22]	90	88.15	6.0	6.151	1.01	1.001	98.1	5.78	4.05
Ref. [25]	90	88.21	6.0	6.145	1.01	1.003	98.15	5.75	4.035

Table 6
Comparison among the performances of different control methods of UPFC controller for IEEE-14 bus system.

Parameter	Real power (MW)		Reactive power (MVAR)		Sending end voltage (pu)		Average % of accuracy (%)	Real power loss (MW)	Reactive power loss (MVAR)
Control methods	Reference	Measured	Reference	Measured	Reference	Measured			
Proposed	8.0	7.945	9.0	9.023	1.015	1.0147	99.55	11.02	22.736
Ref. [18]	8.0	7.763	9.0	9.431	1.015	0.9975	96.69	12.95	24.95
Ref. [21]	8.0	7.805	9.0	9.325	1.015	1.0032	97.62	12.56	24.46
Ref. [22]	8.0	7.829	9.0	9.3	1.015	1.0045	97.92	12.3	23.92
Ref. [25]	8.0	7.865	9.0	9.275	1.015	1.0051	98.23	12.16	23.55

which could be time consuming. However, this limitation is not going to affect the performance of the UPFC.

5. Conclusion

This paper has presented a new control system for dynamic UPFC to improve the power transfer capability through power transmission lines. The new controller of UPFC has been developed based on FL controller. The new controller based UPFC has proved its robustness not only by enhancing the power flow ability of the network but also reducing the power losses and improving bus voltages of the networks. The active power flow with proposed controller based UPFC has improved 4.86% and 14.26% compared to its nominal value in IEEE-5 and IEEE-14 bus networks respectively. In the same networks real power capacity losses also reduced by 10.56% and 15.23% more with UPFC connected to the transmission line. Meanwhile, with UPFC the bus voltages across the networks are also improved to their respective nominal values.

For verification, the performances of FL based UPFC controller has been compared with PI based UPFC controller where FL based controller has outperformed PI based controller. The simulation results show that FL based UPFC improves real power flow capability 2.577% more than PI based UPFC in IEEE-5 bus system. For IEEE-14 bus system, the real power flow with FL based UPFC has increased 4.62% more compared to that of PI based UPFC. In addition, the reduction in real power capacity losses with FL based UPFC has found 4.238% and 6.95% compared with PI based UPFC for both IEEE-5 and 14 bus systems respectively. After placing FL based UPFC substantial improvement in networks bus voltages has also observed which is observed better than that of PI based UPFC.

The robustness of the proposed control method for UPFC has also proved better compared to other control methods of UPFC.

Acknowledgments

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