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Bioinspired neuromorphic module based on carbon nanotube/C60/polymer composite

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Abstract

It is extremely challenging to imitate neural networks with their high-speed parallel signal processing, low power consumption, and intelligent learning capability. In this work, we report a spike neuromorphic module composed of "synapstors" made from carbon nanotube/C60/polyimide composite and "CMOS Somas" made from complementary metal-oxide semiconductor electronic circuits. The "synapstor" emulates a biological synapse with spike signal processing, plasticity, and memory; the "CMOS Soma" emulates a Soma in a biological neuron with analog parallel signal processing and spike generation. Spikes, short potential pulses, and input to the synapstors trigger postsynaptic currents and generate output spikes from the CMOS Somas in a parallel manner with low power consumption. The module can be modified dynamically on the basis of the synapstor plasticity. Spike neuromorphic modules could potentially be scaled up to emulate biologic neural networks and their functions.

Keywords

Carbon nanotube polymer composite, neuromorphic module, C60, CMOS Soma

Introduction

Neural networks in the brain can process tremendous amounts of signals with low power consumption (<100 W) and modify themselves for learning.[1,2] The neural networks have been imitated by computers and electronic circuits.[3,4] For example, IBM researchers used Blue Gene supercomputer to perform a simulation of a cortical neural network on the scale of a cat brain.[5] The signal processing speed of the Blue Gene was ~600 times slower than the real cortical neural network, while the power consumption of the former was ~14,000 times higher than the latter. The disadvantages of the computer are primarily caused by (1) the nature of the serial signal processing architecture of the computer preventing it from processing efficiently the massive amount of signals in a parallel fashion similar to the neural network[6]; (2) the power consumption of complementary metal-oxide semiconductor (CMOS) transistors (the basic element of the computer) which is approximately six orders higher than that of a synapse, the junction between two neurons, and the basic element of the neural network.[3,7] Various electronic devices, such as memristors,[8–15] floating-gate silicon transistors,[16,17] nanoparticle organic transistors,[18,19] phase change memory,[20,21] carbon nanotube (CNT) transistors,[22] and CMOS electronic circuits[23–25] have been used to emulate the functions of the synapses and neurons. Although CMOS circuits could successfully imitate the functions of synapses, they had a power consumption that was approximately three to six orders higher than the synapses.[22,23,26] Conversely, the various electronic devices had lower power consumption and smaller sizes than the CMOS circuits, but they still had much higher power consumption than biological synapses and neurons,[11,17] were difficult for parallel signal processing,[8,18] or deficient in the synaptic plasticity for the modification and learning of

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neural networks.[22] In the present work, we describe a spike neuromorphic module composed of CNT/C60 transistors and CMOS Somas. The CNT/C60 transistor, called a "synapstor," emulates a biological synapse with spike (a short potential pulse) signal processing, plasticity, and memory, and operates at low power consumption (2.6 nW/synapstor). A CMOS electronic circuit, called a "CMOS Soma," emulates the functions of a Soma in a biological neuron with analog parallel signal processing and spike generation. The spike neuromorphic module can potentially be utilized as a basic unit of a large-scale neuromorphic circuit with high-speed parallel signal processing, low power consumption, and learning capabilities for adaptive motor control, pattern recognition, perception, and artificial intelligence.

Experimental

CNT/C60 synapstors

The CNT/C60 synapstors are the key elements in the spike neuromorphic module enabling learning functions and low power consumption to the module (Figure 1(a)). The CNT/C60 synapstor has a transistor structure (inset in Figure 1(a)) with nonvolatile analog memory function.[27] The CNT network was fabricated by spin coating 98% semiconducting single-walled CNT solution (IsoNanotubes-S) onto a SiO_2 surface on a Si substrate. The CNT channel, of 10 μm in length and 8 μm in width, was defined by photolithography and connected by a Ti/Au (5 nm/100 nm) source and drain electrodes. A 30 nm thick polyimide (PI) layer was spin coated onto the top of the CNT channel. C60 molecules were dispersed in the PI layer by dissolving a C60 derivative, 6,6-phenyl-C61 butyric acid methyl ester (PCBM), in a 1-vinyl-2-pyrrolidinone solvent with a PCBM:PI weight ratio of 1:22, and a 30 nm thick C60/PI layer was deposited onto the CNT channel by spin coating the C60/PI solution. The C60 molecules, which function as electron acceptors, are dispersed in the PI layer to modify the source–drain current through the CNTs, and the CNTs are used in the channel due to its sensitive response to the charge in the C60 molecules. A 30 nm thick Al_2O_3 layer was deposited onto the PI layer. Finally, a Ti/Al (15 nm/100 nm) top gate electrode was deposited by e-beam evaporation and patterned by photolithography.

Spike neuromorphic module

The structure of the spike neuromorphic module including two complementary CMOS Soma circuits is shown schematically in Figure 1(b). A set of input spikes (X+) applied on excitatory synapstors triggers excitatory postsynaptic currents (EPSC) with positive polarity, while a set of input spikes (X−) applied on inhibitory synapstors similarly triggers inhibitory postsynaptic currents (IPSC) with negative polarity. Both EPSC and IPSC form the total postsynaptic current (PSC = EPSC − IPSC) and then jointly flow into the interface circuit (Buf in Figure 1(b)). Since the voltage at the shared drain of synapstors was forced to be 0 V by an operational amplifier in the interface circuit, all EPSCs and IPSCs from the synapstors were accumulated without any interference or coupling between them. The interface circuit then directs the positive portion of PSC (|PSC|) toward a positive CMOS Soma (Soma+) and the negative portion of PSC (|−PSC|) toward a negative CMOS Soma (Soma−), respectively. The positive or negative portions of PSC serve as an input current to Somas to trigger output spikes by emulating the integrate-and-fire mechanism of biological Somas.[28] Although a biological neuron does not have the negative Soma, it is added to incorporate negative inputs and outputs in the spike neuromorphic module for engineering applications in the future.

A leaky transistor (M1) in Soma+ or Soma− sets a threshold current by a potential bias, V_{TH}, applied on its gate. The positive or negative portions of PSC subtracted from the threshold current are integrated with respect to time by a capacitor ($C_{I\&F+}$ and $C_{I\&F-}$) to build up a potential ($V_{I\&F+}$ and $V_{I\&F-}$) on the capacitor at Soma+ or Soma−, respectively. When the $V_{I\&F}$ was above a logical threshold of the first stage amplifier (A1), then the output from the A1 was set to a logic high (5 V) and propagated through the following amplifiers to the output node. Before the output node was set to high, a feedback transistor (M3) was turned on to fully charge the capacitor. After the output node was set to high, the discharge transistor (M2) was turned on to release the stored charges on the $C_{I\&F}$ and restart the integration of the PSC. The current levels of the M2 and M3 determined the output spike duration, which was set to 1 ms. The rate of output spikes from Soma+ and Soma− is shown as a function of PSC in Figure 1(c). When the PSC was below a threshold current (~5 nA), which was set by the leaky current through transistor M1, there was no spike output from the Soma. When the absolute value of the I_{PSC} increased from 5 to 40 nA, the output spike rate increased monotonically with the increasing |PSC|. When |PSC| was above 40 nA, the output spike rate was saturated gradually. The saturated output spike frequency was approximately 70 Hz when |PSC| approached ~100 nA.

The illustrative operation of the spike neuromorphic module is shown in Figure 2 with a single input spike with a 1 ms duration and a 5 V amplitude. When an input spike is applied at the gate of a synapstor (Figure 2(a)), electrons are attracted to and trapped

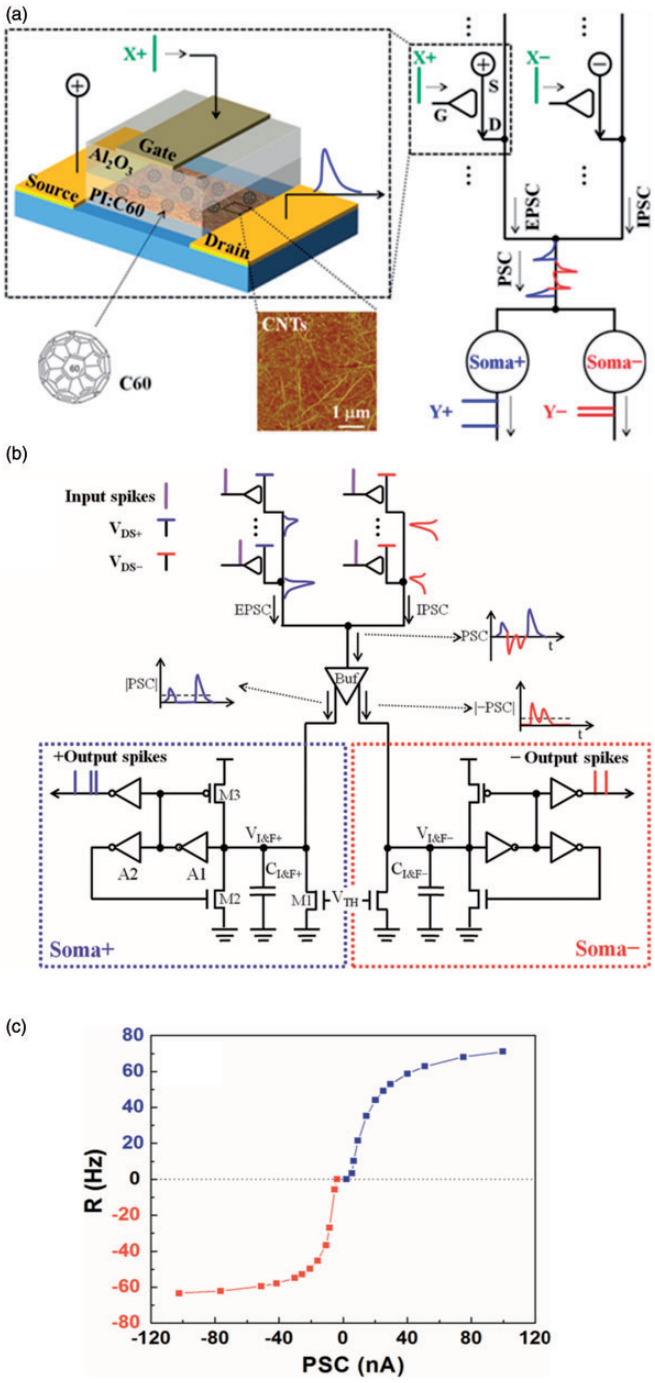

Figure 1. (a) A scheme showing the structure of a spike neuromorphic module with multiple CNT/C60 synapstors and two complementary positive/negative CMOS Somas (marked as "Soma+" and "Soma−"). An inserted schematic diagram shows the structure of a CNT/C60 synapstor with a carbon nanotube (CNT) channel connected by Ti/Au source and drain electrodes. The synapstor gate is composed of a PI layer with C60 molecules, and an Al_2O_3 insulation layer, and a Ti/Al top electrode. An inserted atomic force microscope (AFM) image shows a network of randomly distributed CNTs in the synapstor channel. A 0.5 V potential (denoted as "+") is applied on the sources (denoted as "S") of the excitatory synapstors, and a −0.5 V potential (denoted as "−") is applied on the sources of the inhibitory synapstors. Spikes applied on the gate (denoted as "G") of the excitatory synapstors (X+) trigger excitatory postsynaptic current (EPSC), and spikes applied on the inhibitory synapstors (X−) trigger inhibitory postsynaptic current (IPSC). The EPSCs and IPSCs jointly flow from the synapstor drains (denoted as "D") into a pair of Somas, triggering positive output spikes (Y+) from Soma+, and negative output spikes (Y−) from Soma−. (b) A schematic shows the structure of a spike neuromorphic module with Soma+ (a blue dotted box) and Soma− (a red dotted box). (c) The rates of output spikes from Soma+ and Soma− are shown as a function of the postsynaptic current (PSC). The blue dots and line represent the output spike rate from Soma+, and the red dots and line represent the output spike rate from Soma−. The negative rate represents the rate of negative output spikes from Soma−.

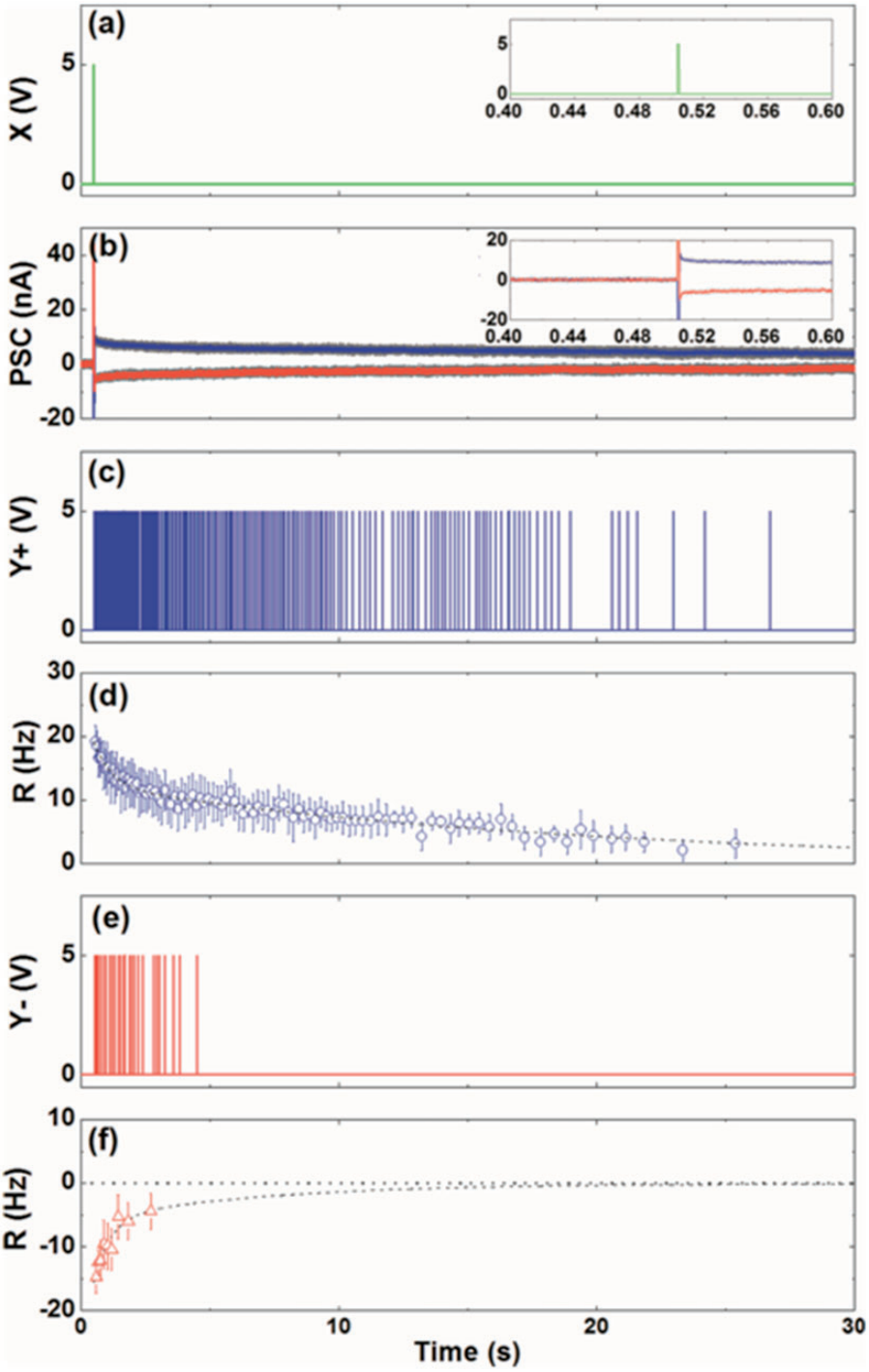

Figure 2. (a) An input spike, X, applied on a synapstor at t = 0.5 s. The inset shows the close-up view of an input spike X from t = 0.4 s to t = 0.6 s. (b) The average postsynaptic current (PSC) triggered by the input spike is plotted versus time with the EPSC shown in blue and the IPSC shown in red. The inset shows the close-up view of EPSC and IPSC from t = 0.4 s to t = 0.6 s. The gray lines represent the standard deviation of 10 independent tests under the same test conditions. (c) Output spikes, Y+, triggered from Soma+ by the EPSC are shown versus time. (d) The average rate, R, of the output spikes Y+ and its best fitting (dashed) line are plotted versus time. The error bars represent the standard deviation of 10 independent tests under the same test conditions. (e) Output spikes, Y−, triggered from Soma− by the IPSC are shown versus time. (f) The average rate, R, of the output spikes Y− and its best-fitting (dashed) line are plotted versus time. The negative rate represents the rate of output spikes from Soma−. The error bars represent the standard deviation of 10 independent tests under the same test conditions.

inside the C60 molecules at the PI layer of the synapstor. After completion of the input spike, the electrons trapped in the C60 molecules attract holes in the p-type CNTs, resulting in an increase of the hole concentration and the source–drain current through the CNT channel. The electrons trapped in the C60 molecules gradually leak out of the C60 molecules via the PI layer, resulting in the gradual decay of the source–drain current against time, which emulates a PSC triggered by a spike in a biological synapse. An input spike can trigger an EPSC when it applies to an excitatory synapstor having a positive source–drain voltage of 0.5 V, whereas it can trigger an IPSC when applying to an inhibitory synapstor having a negative source–drain voltage of −0.5 V. In the spike neuromorphic module, input channels for excitatory and inhibitory synapstors are physically separated. However, any input channels can be shared regardless of synapstors' type or number of synapstors because the format of input spikes is universal to all synapstors. An average EPSC from 10 individual tests on an excitatory synapstor is plotted against time in Figure 2(b). The EPSC reached a peak value (~ 13 nA) at the end of the spike and gradually decayed back to the resting current (~ 0 nA) in approximately 60 s. An average IPSC from 10 individual tests on an inhibitory synapstor is also plotted against time in Figure 2(b). The IPSC reached a peak value (~ −9 nA) at the end of the spike and gradually decayed back to the resting current in approximately 60 s. In the spike neuromorphic module, input spikes can trigger multiple EPSCs and IPSCs via multiple excitatory and inhibitory synapstors. The average amplitude of EPSCs measured from 31 excitatory synapstors in the spike neuromorphic module was 12.7 nA, with a standard deviation of 2.1 nA; the average amplitude of IPSCs measured from 31 inhibitory synapstors in the spike neuromorphic module was −11.1 nA, with a standard deviation of 1.7 nA. The average power consumption of the synapstors in the spike neuromorphic module was estimated to be 2.6 nW/synapstor under an input spike rate of 1 Hz.

A series of positive output spikes (Y+) from Soma+ triggered by a single input spike to an excitatory synapstor are shown in Figure 2(c), and the average output spike rate, R, over 10 individual tests is shown against time in Figure 2(d). Equivalently, a series of negative output spikes (Y−) from Soma− by the single spike were applied on an inhibitory synapstor as shown in Figure 2(e), and the average output spike rate, R, from 10 individual tests is shown against time in Figure 2(f). The R gradually decreased against time when the EPSC and IPSC decayed against time. The R can be described by the linear convolution between the input spike X and a transfer function G, $R(t) = G \otimes X = \left(A\, e^{-(t-t_1)/\tau_A} + Be^{-(t-t_1)/\tau_B}\right) \times u(t-t_1)$, where $X = \delta(t-t_1)$ with $\delta(t)$ denoting a unit impulse function and t_1 representing the moment when the single input spike was applied, and $G = \left(A\, e^{-t/\tau_A} + Be^{-t/\tau_B}\right) \times u(t)$ with u(t) representing a unit step function. From those best fitting to the experimental data (Figure 2(d) and (f)), the fitting parameters in the function were derived as A = 12.2 Hz, B = 6.96 Hz, $\tau_A = 18.8$ s, and $\tau_B = 0.69$ s for the excitatory synapstor, and A = 5.55 Hz, B = 9.95 Hz, $\tau_A = 6.76$ s, and $\tau_B = 0.63$ s for the inhibitory synapstor. The two different exponential decaying constants (τ_A and τ_B) imply that there are two different mechanisms involving in the transient response of synapstors. First one is believed that the electrons trapped at C60 molecules are released to and recombined at semiconductor CNTs, leading to a longer decaying time ($\tau_A > 5$ s for all the synapstors) in the PSC and output spike rates, while the second one is presumed that the electrons trapped at the C60 molecules nearby metallic CNTs are escaped to and annihilated by metallic CNTs which generally a rapid process, leading to a shorter decaying time ($\tau_B < 1$ s for all the synapstors) in the PSC and the output spike rates. The decaying times in synapstors are similar with ones from CNT network transistors with charge injection.[29] The variable decaying time is presumed to be mainly related to the distribution of semiconducting or metallic CNTs around C60 molecules.

Results

Temporal response to a pair of spikes applied on an excitatory synapstor

A series of input spikes with different spatiotemporal distributions can be input into the spike neuromorphic module in parallel and trigger a series of output spikes. In the simplest example, a pair of input spikes with various interspike time intervals, Δt, ranging between 1 and 30 s, was applied on an excitatory synapstor to trigger positive output spikes (Y+) from Soma+. The average rate of positive output spikes triggered by the pair of input spikes on an excitatory synapstor with a fixed time interval (Δt = 1, 5, 10, 20, and 30 s, respectively) was derived from 10 independent tests and plotted versus time in Figure 3(a) to (e). The first input spike triggered an EPSC and a series of positive output spikes; the second input spike triggered another EPSC, and further increased the rate of the positive output spikes. The output spike rate, R, can be described by the function $R(t) = \sum G \otimes X_i + \Delta$, where $X_i(t) = \delta(t - t_i)$ with t_i representing the moment when the *i*th input spike was applied ($i = 1$ or 2), $G = \left(A\, e^{-t/\tau_A} + Be^{-t/\tau_B}\right) \times u(t)$ is the linear transfer function of the synapstor defined previously for the single input spike case, and

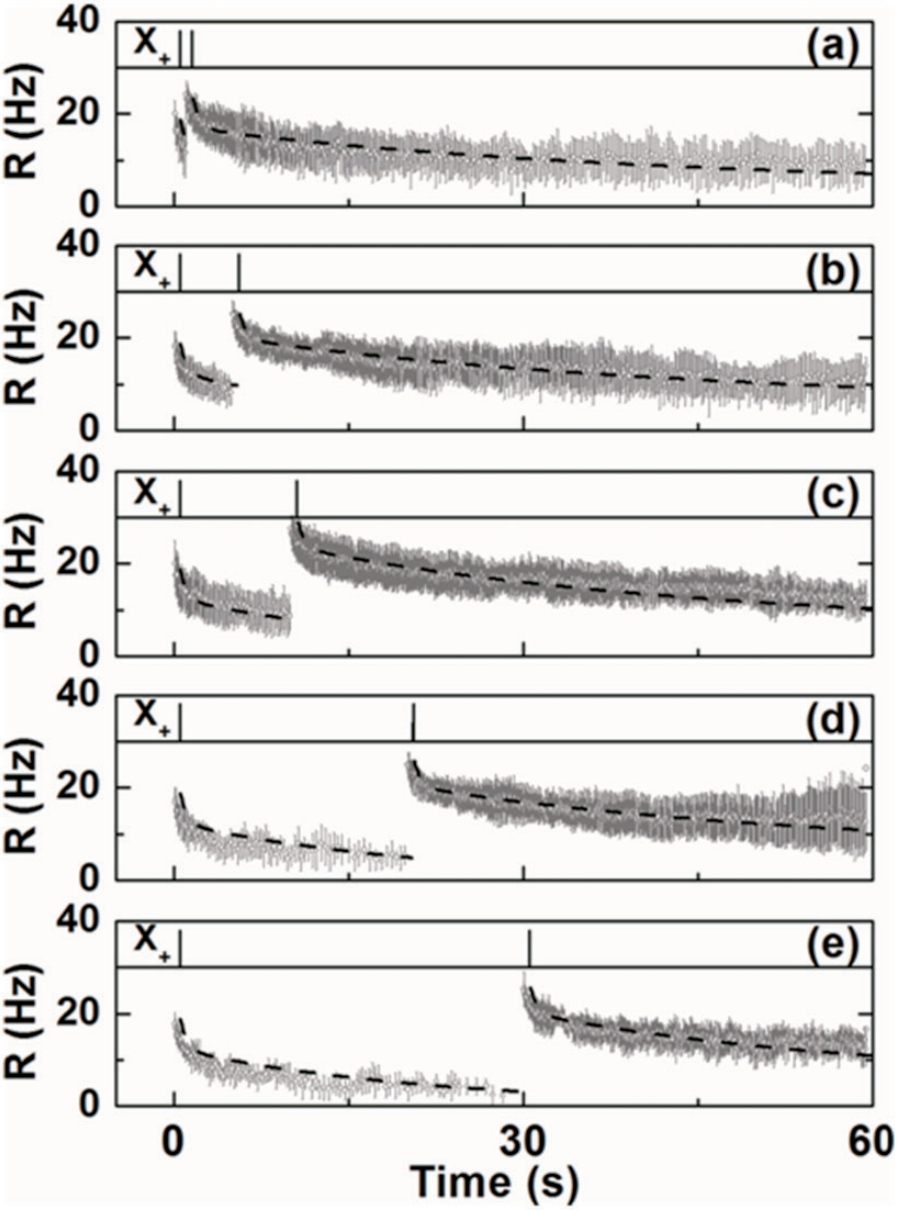

Figure 3. A pair of input spikes, X_+, applied on the excitatory synapstor with the interspike interval of (a) 1 s, (b) 5 s, (c) 10 s, (d) 20 s, and (e) 30 s is shown in the top diagrams. The rate of output spikes, R, triggered by the pair of input spikes is plotted as open circles versus time with their best-fitting functions (dashed lines) in the bottom diagrams. The error bars represent the standard deviation of 10 independent tests under the same test conditions.

$\Delta = \left(Ce^{-(t-t_2)/\tau_C} + De^{-(t-t_2)/\tau_D}\right) \times u(t-t_2)$ denotes a high-order nonlinear term related to the interspike time interval $\Delta t = t_2 - t_1$. From the best fitting to the experimental data, the fitting parameters in the function were derived as $A = 12.1$ Hz, $B = 6.6$ Hz, $\tau_A = 21.7$ s, $\tau_B = 0.60$ s, $\tau_C = 125$ s, and $\tau_D = 20$ s, which do not change versus Δt. The parameters C and D are a function of the Δt: When Δt increased from 1 to 30 s, the C slightly decreased from 11.1 to 10.4, and the D gradually increased from -17 to -5.5, which indicates that the nonlinear correlation between the input and output spikes becomes more significant with the smaller Δt. When the second input spike was applied with a smaller Δt, it can be presumed that fewer electrons injected into the C60 molecules by the first input spike had been released yet. The repulsion forces from the injected electrons allowed the injection of fewer electrons into the C60 molecules by the second input spikes, resulting in the smaller amplitude of EPSC, the less output spikes triggered by the second input spike, and the increase in the magnitude of the negative nonlinear term D. The nonlinear correlation

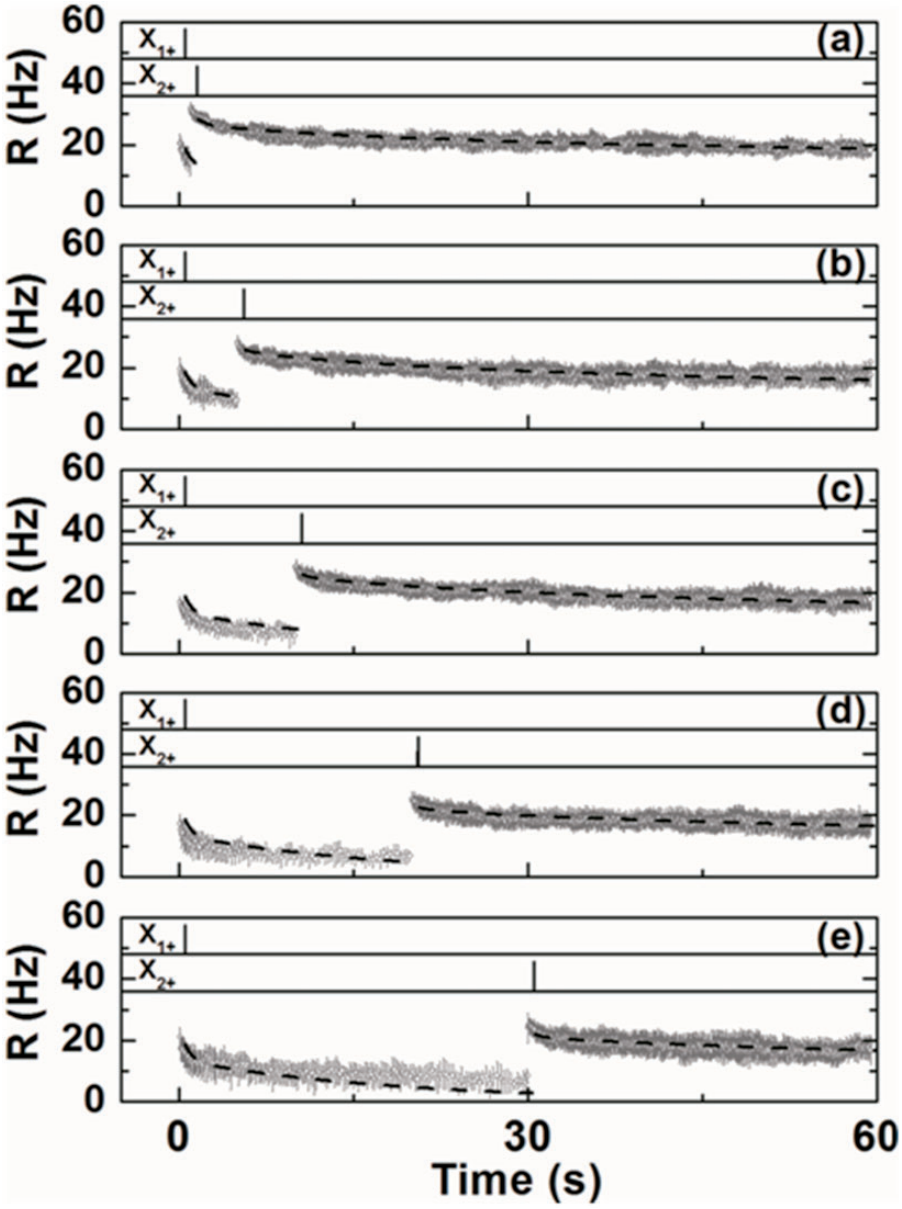

Figure 4. A pair of input spikes, X_{1+} and X_{2+}, applied on two excitatory synapstors with an inter-spike interval of (a) 1 s, (b) 5 s, (c) 10 s, (d) 20 s, and (e) 30 s is shown in the top diagrams. The rate of output spikes, R, triggered by the pair of spikes is plotted as open circles versus time with their best-fitting functions (dashed lines) in the bottom diagrams. The error bars represent the standard deviation of 10 independent tests under the same test conditions.

between the input and output spikes has also been observed in the biological neural network.[30,31]

Spatiotemporal response to a pair of spikes applied on two synapstors

The spike neuromorphic module was also tested by inputting two spikes onto two different synapstors, respectively, with interspike intervals ranging between 1 and 30 s. When the first input spike was applied on the first excitatory synapstor, and the second input spike was applied on the second excitatory synapstor, the average rate of the output spikes, R, triggered by the two input spikes from 10 independent tests was measured and plotted versus time, as shown in Figure 4(a) to (e). The first input spike triggered an EPSC from the first excitatory synapstor and a series of positive output spikes (Y+); the second input spike triggered another EPSC from the second excitatory synapstor, and further increased the rate of the positive output spikes. Oppositely, when the first input spike was applied on an excitatory synapstor, and the

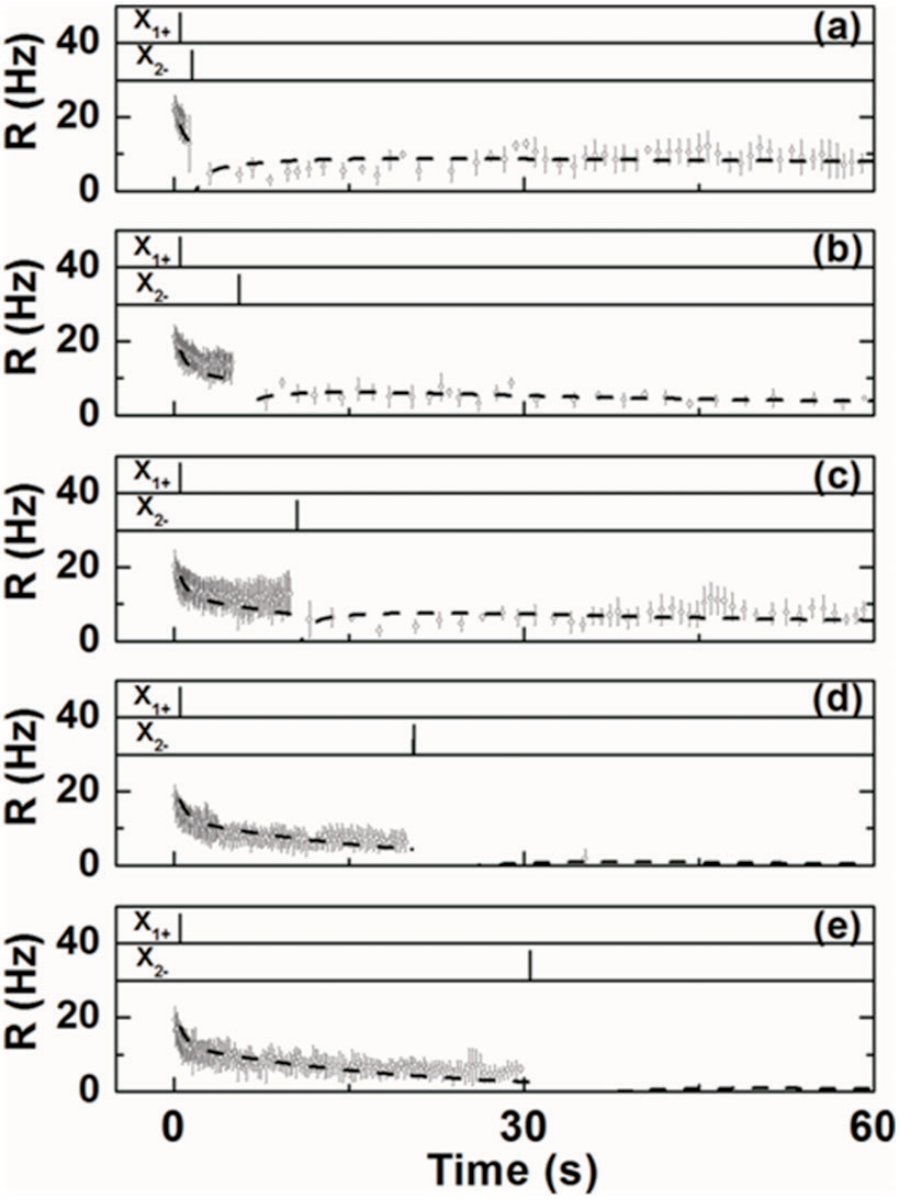

Figure 5. A pair of input spikes, X_{1+} and X_{2-}, applied on an excitatory and an inhibitory synapstors with interspike intervals of (a) 1 s, (b) 5 s, (c) 10 s, (d) 20 s, and (e) 30 s is shown in the top diagrams. The rate of output spikes, R, triggered by the pair of spikes is plotted as open circles versus time with their fitting functions (dashed lines) in the bottom diagrams. The error bars represent the standard deviation of 10 independent tests under the same test conditions.

second input spike was applied on an inhibitory synapstor in the spike neuromorphic module, the average rate of the output spikes, R, triggered by the two input spikes from 10 independent tests was measured and plotted versus time in Figure 5(a) to (e). Since EPSC (PSC with positive polarity) and IPSC (PSC with negative polarity) are merged at the interface circuit on their way to Somas, an IPSC, which was triggered by the following second input spike to an inhibitory synapstor, was able to reduce or even quench the positive output spikes (Y+) triggered by an EPSC from an excitatory synapstor by the first input spike. The output spike rate, R, can be described by the function $R(t) = \sum G_j \otimes X_i + \Delta$, where $X_i(t) = \delta(t - t_i)$ with t_i representing the moment when the *i*th input spike was applied ($i = 1$ or 2), $G_j(t) = \left(A_j e^{-t/\tau_{Aj}} + B_j e^{-t/\tau_{Bj}}\right) \times u(t)$ is the linear transfer function of the *j*th synapstor ($j = 1$ or 2) defined previously for the single input spike, and $\Delta = \left(C_{12} e^{-(t-t_2)/\tau_C} + D_{12} e^{-(t-t_2)/\tau_D}\right) \times u(t - t_2)$ denotes a nonlinear term related to the interspike time interval $\Delta t = t_2 - t_1$. From the best fitting to the experimental data, the parameters in the fitting function for the pair of spikes applied on the two excitatory synapstors were derived as $A_1 = 13.2\,\text{Hz}$, $B_1 = 5.5\,\text{Hz}$, $\tau_{A1} = 18.8\,\text{s}$,

$\tau_{B1} = 0.69\,s$, $A_2 = 18.2\,Hz$, $B_2 = 1.1\,Hz$, $\tau_{A2} = 237.6\,s$, and $\tau_{B2} = 0.94\,s$, which do not change versus Δt. However, when the Δt increased from 1 to 30 s, the C_{12} decreased from 5.68 to 0, and D_{12} increased from -10 to -0.07. The parameters in the fitting function for the pair of spikes applied on the excitatory and the inhibitory synapstors were derived as $A_1 = 12.3\,Hz$, $B_1 = 5.4\,Hz$, $\tau_{A1} = 19\,s$, and $\tau_{B1} = 0.69\,s$ for the excitatory synapstor; $A_2 = -6.26\,Hz$, $B_2 = -10\,Hz$, $\tau_{A2} = 6.69\,s$, and $\tau_{B2} = 0.64\,s$ for the inhibitory synapstor, which do not change versus Δt. However, when the Δt increased from 1 to 30 s, the C_{12} decreased from 11.4 to 0.32, and D_{12} increased from -12 to 0. The change of the parameters C_{12} and D_{12} indicates that the nonlinear correlation between the input and output spikes becomes more significant with the smaller Δt. Since the two input spikes were applied on the two separated synapstors, and triggered EPSC/IPSC that were linearly superimposed in the Somas, the nonlinearity was primarily induced by the Somas. The first spike induced PSC to the linear correlation range between the PSC and output spikes in the Somas, but the second spike triggered the EPSC or IPSC, which increased the PSC to its nonlinear saturation range or decreased the PSC to the nonlinear range close to the PSC threshold, inducing the nonlinear correlation between the input and output spikes. When the second input spike was applied with a smaller Δt, it induces more significant change of the PSC, more substantial nonlinearity and the increase of the magnitude of the C_{12} and D_{12}.

Synaptic plasticity

The change of single PSC amplitudes from an excitatory and an inhibitory synapstors was measured to test the plasticity of the CNT/C60 synapstors in the spike neuromorphic module. The single PSC amplitudes were modified by applying modification spikes with ± 8 V amplitude to increase or decrease the single PSC amplitudes. As shown in Figure 6(a), the single PSC amplitudes of the synapstors were increased with increasing numbers of the -8 V modification spikes applied on the synapstors. The single PSC amplitude of the excitatory synapstors was increased by approximately 400% after application of 10 -8 V spikes, and the change was then saturated. The single PSC amplitude of the inhibitory synapstor was increased by approximately 100% after application of two -8 V spikes, and the change was then saturated. As shown in Figure 6(b), the single PSC amplitudes of the synapstors were decreased with increasing numbers of the 8 V modification spikes applied on the synapstors. The single PSC amplitude of the excitatory synapstors was decreased by approximately -80% after the application of six spikes with a 8 V amplitude, and the change was then saturated. The PSC amplitude of the inhibitory synapstor was decreased by -60% after the application of six 8 V spikes, and the change was then saturated. The difference in the plasticity between the excitatory and inhibitory synapstors might have been induced by the variation of the randomly aligned CNT network in the synapstor channels.

Plasticity of neuromorphic module

The modification of synapses, that is, the synaptic plasticity, is crucial for learning and memory in the spike neuromorphic module. CNT/C60 synapstors can be modified in analog mode by applying spikes on the gate of a CNT/C60 synapstor. To test the synaptic plasticity, a series of spikes were applied on an excitatory and an inhibitory synapstors. After consecutive application of five input spikes on the excitatory synapstor and four input spikes on the inhibitory synapstor at a frequency of 1 Hz (Figure 7(a)), the input spikes on the excitatory synapstor triggered EPSCs and a series of positive output spikes (Y+) from Soma+, while the input spikes on the inhibitory synapstor triggered IPSCs and a series of negative output spikes (Y−) from Soma− (Figure 7(b)). The synapstors were then modified by separately applying two 1 ms 8 V spikes on the excitatory synapstor, and two 1 ms 8 V spikes on the inhibitory synapstor. After the modification, output spikes were again triggered by the five input spikes on the excitatory synapstor and the four input spikes on the inhibitory synapstor (Figure 7(c)). The positive output spike rate (Y+) from Soma+ was decreased to zero, and the negative output spike rate (Y−) from Soma− was slightly increased. The amplitudes of EPSCs and IPSCs from the synapstors were decreased by the modification spikes, resulting in the decrease of the positive output spike rate from Soma+. However, the IPSC amplitudes did not decrease as much as the EPSC amplitudes, resulting in the net increase of the PSC magnitude and negative output spike rate from Soma−. The synapstors were then modified by separately applying two 1 ms -8 V spikes on the excitatory synapstor and two 1 ms -8 V spikes on the inhibitory synapstor. The amplitudes of EPSCs and IPSCs from the synapstors were increased by the modification spikes. After the modification, the rate of the output spikes triggered by the five input spikes on the excitatory synapstor was increased, and the rate of the output spikes triggered by the four input spikes on the inhibitory synapstor was increased further (Figure 7(d)). The rate of the output spikes shown in Figure 7 was fitted by the function $R(t) = \sum G_j \otimes X_i$, where $X_i(t) = \delta(t - t_i)$ with t_i representing the moment when the *i*th input spike was applied,

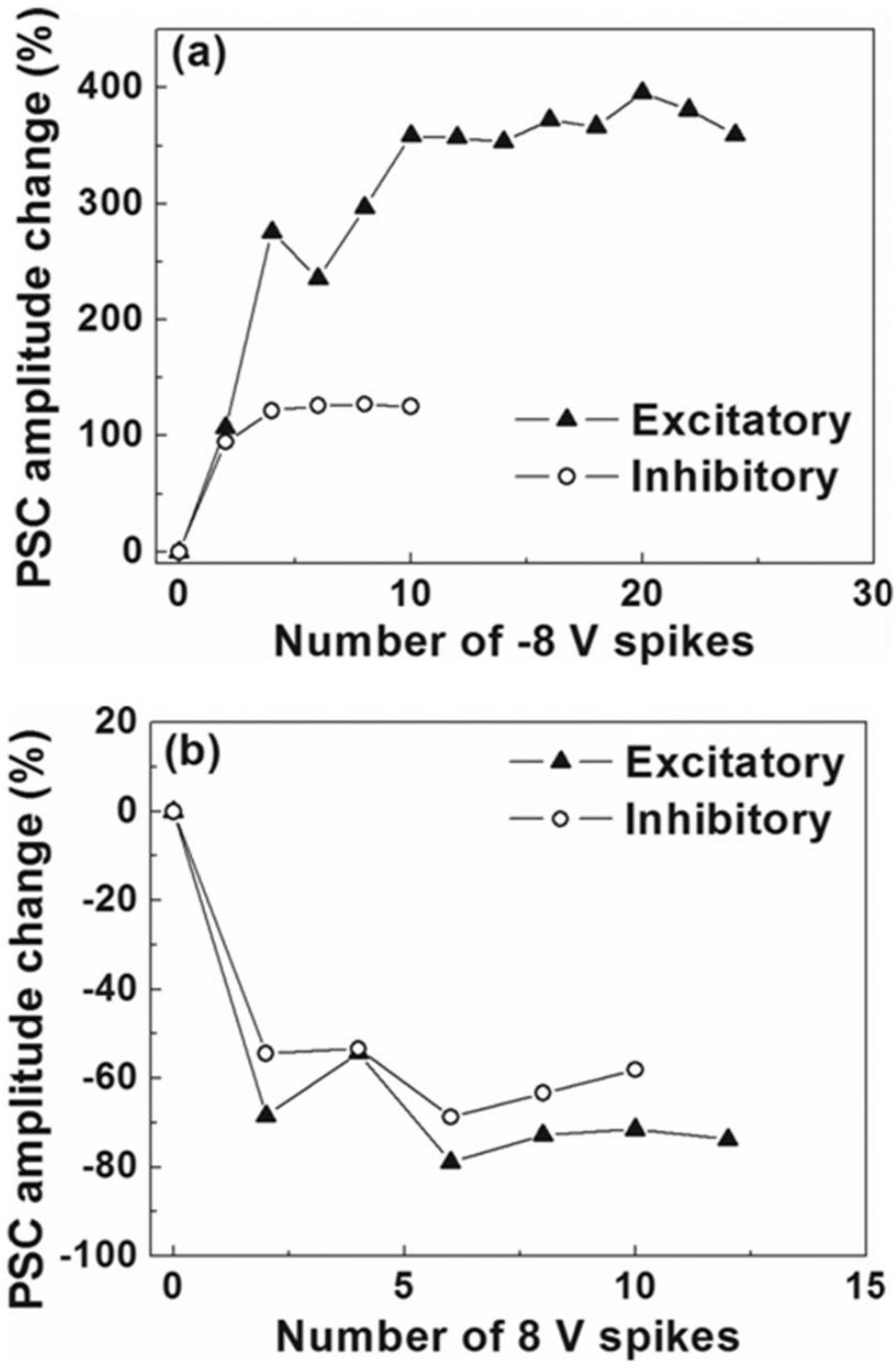

Figure 6. The plasticity of synapstors. (a) The changes of the PSC amplitudes of an excitatory and an inhibitory synapstors are shown as a function of the numbers of the −8 V modification spikes applied on them. (b) The changes of the PSC amplitudes of an excitatory and an inhibitory synapstors are shown as a function of the numbers of the 8 V modification spikes applied on them.

$G_j(t) = \left(A_j e^{-t/\tau_{Aj}} + B_j e^{-t/\tau_{Bj}}\right) \times u(t)$ is the linear transfer function of the *j*th synapstor defined previously for the single input spike. From the best fitting to the experimental data, the fitting parameters in the function were derived. The average values of $A_1 + B_1$ for the excitatory synapstor were decreased from 12.83 to 0, and $A_2 + B_2$ for the inhibitory synapstor were slightly increased from −8.2 to −10.81 by the 8 V modification spikes. The average values of $A_1 + B_1$ for the excitatory synapstor were increased from 0 to 14.62, and $A_2 + B_2$ for the inhibitory synapstor were increased from −10.81 to −16.28 by the −8 V modification spikes.

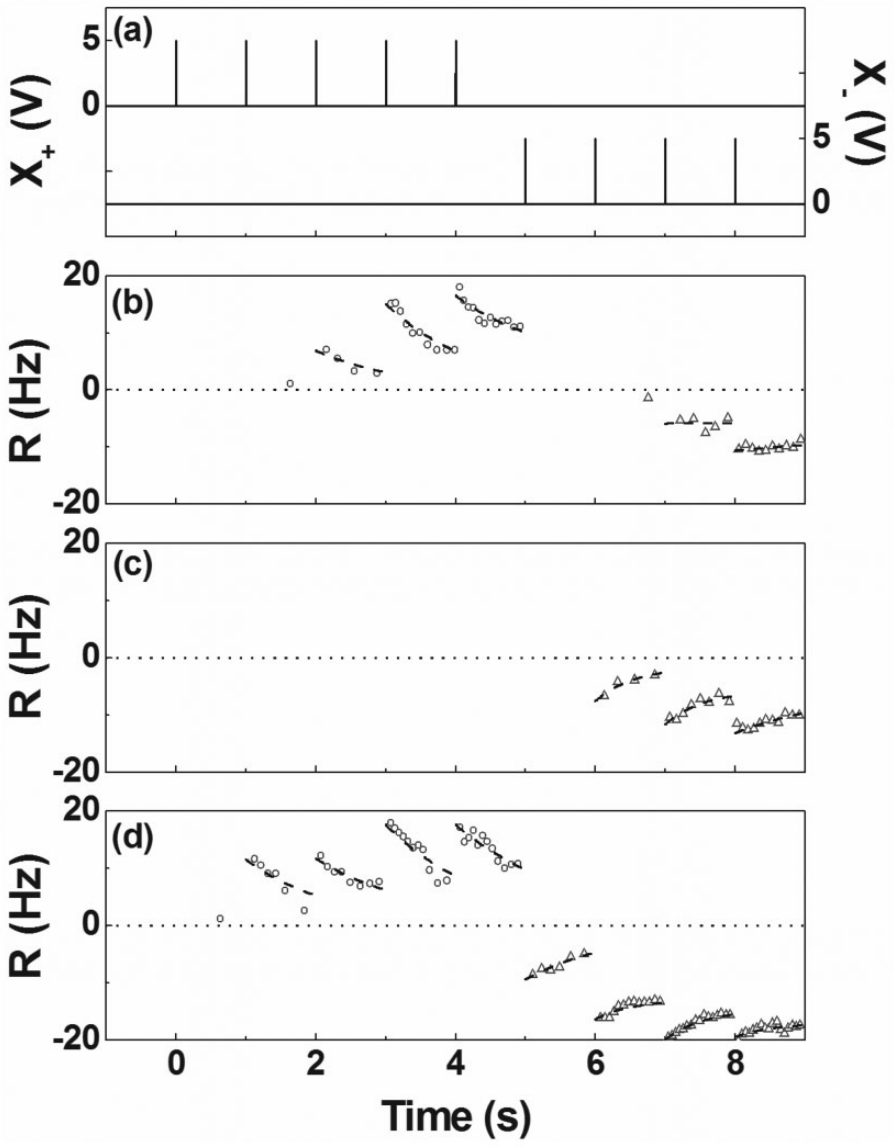

Figure 7. The nonvolatile modification (plasticity) of a spike neuromorphic module. (a) A series of input spikes are applied on an excitatory synapstor (top) and an inhibitory synapstor (bottom). (b) The rates of positive (open circles) and negative (open triangles) output spikes triggered by the input spikes shown in (a) are plotted versus time. (c) After the spike neuromorphic module is modified by applying two 8 V modification spikes on the excitatory and the inhibitory synapstors separately, the rates of positive (open circles) and negative (open triangles) output spikes triggered by the input spikes shown in (a) are plotted versus time. (d) After the neuromorphic module is modified by applying two −8 V modification spikes on the excitatory and the inhibitory synapstors separately, the rates of positive (open circles) and negative (open triangles) output spikes triggered by the input spikes shown in (a) are plotted versus time. The negative rate represents the rate of output spikes from Soma−. The best-fitting function to the output spike rates are plotted as the dashed lines.

The 8 V modification spikes applied on the synapstors inject electrons into the C60 molecules, and the electrons trapped in the C60 molecules increased the electronic energy levels in the C60 molecules, which meant that fewer electrons were injected into the C60 molecules by the following input spikes, and the PSC amplitudes in the synapstors were decreased. Conversely, the −8 V modification spikes on the synapstors expelled electrons from the C60 molecules, and the electronic energy levels in the C60 molecules were reduced, which allowed more electrons to be injected into the C60 molecules by the following input spikes, and increased the PSC amplitudes in the synapstors. The electrons injected/expelled by the +/−8 V modification spikes could not be injected or expelled again by the 5 V input spikes, therefore the nonvolatile changes of the synapstors were only induced by the modification spikes.

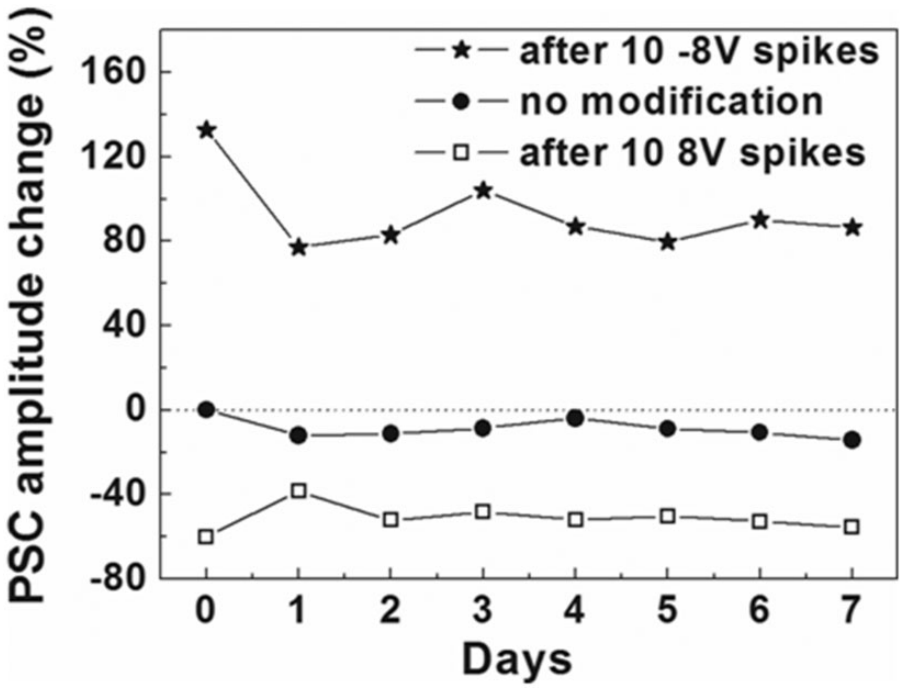

Figure 8. The changes of the PSC amplitudes of three synapstors are shown versus time after application of 10 modification spikes of −8 V on the first synapstor (solid stars), no application of any modification spike on the second synapstor (solid circles), and after application of 10 modification spikes of 8 V on the third synapstor (blank squares).

Volatility of CNT/C60 synaptic plasticity

The volatility of the plasticity of the CNT/C60 synapstors was tested by measuring the PSC amplitudes versus time for a week after the modification of the PSCs (Figure 8). Three synapstors were selected for the nonvolatility experiments: The PSC of the first synapstor was increased by application of 10 modification spikes of −8 V; no modification spike was applied on the second synapstor; the PSC of the third synapstor was decreased by application of 10 modification spikes of 8 V. After application of the modification spikes on each CNT/C60 synapstor, we measured the PSC amplitudes on a daily basis by application of a 5 V input spike on them. After application of 10 modification spikes of −8 V, the PSC amplitude of the first synapstor was increased by 120% and then stabilized at an approximately 80% increase from its original value for a week. With regard to the second synapstor having no modification spike, the PSC amplitude remained at approximately 90% of its original value for a week. After application of 10 modification spikes of 8 V, the synaptic weight of the third synapstor decreased by approximately 60% from its original value and then stabilized at that value for a week. The synaptic weights in the synapstors can be modified by the modification spikes, and the modifications can last for at least one week.

Conclusion

A spike neuromorphic module has been demonstrated by integrating CNT/C60 synapstors and CMOS Soma circuits. A spike input to a synapstor induced the dynamic change of electrons trapped in the C60 molecules in the synapstor gate, resulting in a PSC through the CNT channel in the synapstor. A spike applied on an excitatory synapstor triggered an EPSC, and a spike applied on an inhibitory synapstor triggered an IPSC. Multiple input spikes with various spatiotemporal distributions triggered EPSCs and IPSCs in parallel, which jointly flowed into two complementary CMOS Soma circuits and produced positive output spikes (Y+) from a positive CMOS Soma (Soma+) and negative output spikes (Y−) from a negative CMOS Soma (Soma−). The positive (negative) output spike rate increased with the increasing rate of input spikes applied on the excitatory (inhibitory) synapstors and decreased with the increasing rate of input spikes applied on the inhibitory (excitatory) synapstors. However, the output spike rates were not the linear function of the input spike rates, due to the nonlinear characteristics in the synapstors and Somas. Modification spikes applied on the synapstors changed the densities of the electrons trapped in the C60 molecules in the synapstors, inducing nonvolatile analog changes of the PSCs in the synapstors and the plasticity

of the spike neuromorphic module. Spike neuromorphic modules may potentially be scaled up to emulate biologic neural networks and their functions.

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Conflict of interest

None declared.

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References

1. Versace M and Chandler B. The brain of a new machine. *IEEE Spectrum* 2010; 47: 30–37.
2. Jain AK, Mao JC and Mohiuddin KM. Artificial neural networks: a tutorial. *Computer* 1996; 29: 31–44.
3. Mead C. Neuromorphic electronic systems. *Proc IEEE* 1990; 78: 1629–1636.
4. Brette R, Rudolph M, Carnevale T, et al. Simulation of networks of spiking neurons: a review of tools and strategies. *J Comput Neurosci* 2007; 23: 349–398.
5. Ananthanarayanan R, Esser SK, Simon HD, et al. The cat is out of the bag: cortical simulations with 109 neurons, 1013 synapses. In: *ACM/IEEE conference high performance networking computing, storage and analysis*, Portland, OR, 2009, pp.1–12. IEEE.
6. Backus J. Can programming be liberated from von Neumann style – functional style and its algebra of programs. *Commun ACM* 1978; 21: 613–641.
7. Bohr M. The new era of scaling in an SoC world. In: *Solid-state circuits conference – digest of technical papers, 2009 ISSCC 2009 IEEE International,* San Francisco, CA, 2009, pp.23–28. IEEE.
8. Hasegawa T, Ohno T, Terabe K, et al. Learning abilities achieved by a single solid-state atomic switch. *Adv Mater* 2010; 22: 1831–1834.
9. Seo K, Kim I, Jung S, et al. Analog memory and spike-timing-dependent plasticity characteristics of a nanoscale titanium oxide bilayer resistive switching device. *Nanotechnology* 2011; 22(25).
10. Yu SM, Gao B, Fang Z, et al. A low energy oxide-based electronic synaptic device for neuromorphic visual systems with tolerance to device variation. *Adv Mater* 2013; 25: 1774–1779.
11. Nayak A, Ohno T, Tsuruoka T, et al. Controlling the synaptic plasticity of a Cu2S Gap-type atomic switch. *Adv Funct Mater* 2012; 22: 3606–3613.
12. Snider GS. Spike-timing-dependent learning in memristive nanodevices In: *2008 IEEE international symposium on nanoscale architectures*, Anaheim, CA, 2008, pp.85–92. IEEE.
13. Jo SH, Chang T, Ebong I, et al. Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett* 2010; 10: 1297–1301.
14. Kim KH, Gaba S, Wheeler D, et al. A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications. *Nano Lett* 2012; 12: 389–395.
15. Serrano-Gotarredona T, Masquelier T, Prodromakis T, et al. STDP and STDP variations with memristors for spiking neuromorphic learning systems. *Front Neurosci* 2013; 7(2).
16. Ramakrishnan S, Hasler PE and Gordon C. Floating gate synapses with spike-time-dependent plasticity. *IEEE Trans Biomed Circuits Syst* 2011; 5: 244–252.
17. Chen YJ, McDaid L, Hall S, et al. A programmable facilitating synapse device. In: *IEEE IJCNN,* Hong Kong, 2008, pp.1615–1620. IEEE.
18. Alibart F, Pleutin S, Bichler O, et al. A memristive nanoparticle/organic hybrid synapstor for neuroinspired computing. *Adv Funct Mater* 2012; 22: 609–616.
19. Alibart F, Gao LG, Hoskins BD, et al. High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm. *Nanotechnology* 2012; 23(7).
20. Kuzum D, Jeyasingh RG, Lee B, et al. Nanoelectronic programmable synapses based on phase change materials for brain-inspired computing. *Nano Lett* 2012; 12: 2179–2186.
21. Bichler O, Suri M, Querlioz D, et al. Visual pattern extraction using energy-efficient "2-PCM Synapse" neuromorphic architecture. *IEEE Trans Electron Dev* 2012; 59: 2206–2214.
22. Kim K, Chen CL, Truong Q, et al. A carbon nanotube synapse with dynamic logic and learning. *Adv Mater* 2013; 25: 1693–1698.
23. Indiveri G, Linares-Barranco B, Hamilton TJ, et al. Neuromorphic silicon neuron circuits. *Front Neurosci* 2011; 5: 73.
24. Poon CS and Zhou K. Neuromorphic silicon neurons and large-scale neural networks: challenges and opportunities. *Front Neurosci* 2011; 5: 108.
25. Pickett MD, Medeiros-Ribeiro G and Williams RS. A scalable neuristor built with Mott memristors. *Nat Mater* 2013; 12: 114–117.
26. Laughlin SB, van Steveninck RRD and Anderson JC. The metabolic cost of neural information. *Nat Neurosci* 1998; 1: 36–41.
27. Shen AM, Chen CL, Kim K, et al. Analog neuromorphic module based on carbon nanotube synapses. *ACS Nano* 2013; 7: 6117–6122.
28. Indiveri G. A low-power adaptive integrate-and-fire neuron circuit. In: *Proceedings of the 2003 IEEE international symposium on circuits and systems, Vol 4*, Bangkok, Thailand, 2003, pp.820–823.

29. Minni Q, Zhi-Jun Q, Zhang Z-B, et al. Charge-injection-induced time decay in carbon nanotube network-based FETs. *Electron Dev Lett IEEE* 2010; 31: 1098–1100.
30. Freeman WJ. A pseudo-equilibrium thermodynamic model of information processing in nonlinear brain dynamics. *Neural Networks* 2008; 21: 257–265.
31. Andrzejak RG, Lehnertz K, Mormann F, et al. Indications of nonlinear deterministic and finite-dimensional structures in time series of brain electrical activity: dependence on recording region and brain state. *Phys Rev E* 2001; 64.