

DC-DC Buck Converter with Inrush Current Limiter

Master Thesis Project

by

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by

ELENI MANOUSAKA

Abstract

The Green Village envisions a sustainable, energy autarkic environment realized at the heart of the TU Delft campus. This environment will implement a DC electricity infrastructure with the main voltage level inside the buildings, being 380V. This innovative power system requires the development of new power electronics that can be used to such a grid and contribute to its high performance and reliability. The first test container is meant for testing this electricity system and the relative equipment. This project proposes a buck conversion method with inrush current limiting circuit designed for connecting the test container's energy consumers to the 380V DC main bus, in order to achieve optimum operation, in terms of near peak efficiency and safety. Within the framework of this study, the "Femtogrid" system, which is the electricity system used by the test container, is explained and simulated. Additionally, the operation of the buck (step-down) converter and the boost (step-up) converter, that are the main elements of "Femtogrid" system, are studied and their control methods are analyzed. Moreover, some common electronic devices are tested with DC and AC input voltage, revealing important information regarding their behavior in normal and standby mode. An even better performance of some devices when running on DC is observed. The experiments showed high inrush currents due to the charging of the input capacitors during turn-on. Therefore, an inrush current limiter (ICL) is necessary in order to protect the system components from damage. The buck converter topology proposed in this project is the LLC resonant buck converter topology, which holds features like very high efficiency, isolation and small number of components. The ICL consists of a MOSFET in combination with some passive elements that can drive the MOSFET in such a way that the inrush current of the circuit can be limited by controlling the gate charge characteristic of the MOSFET. A prototype was simulated, built and tested. The simulations showed that the ICL should be able to limit the inrush current at a very low level.

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Chapter 1: Introduction

As years go by, energy demand is growing voraciously, fossil fuel reserves are being depleted and a climate change is being witnessed. These are, today, some of the biggest challenges that the planet faces. In order to secure a good future for the present generation as well as the next ones, the current energy emissions should be reduced and the energy production should be based on renewable energy sources.

Power electronics is an essential part of efficient energy production, transmission and consumption and in recent years they have become vital to the renewable energy sector. Nowadays, 70% of all the electrical energy is processed by power electronics (Aalborg University). Power electronics are found in all the everyday electronic devices and play an important role in ensuring a reliable and efficient energy supply and incorporating the renewable energy sources into the energy system. It is a fact that renewable energy is dominated by power electronics. The main focus within the development of power electronics is high efficiency, minimum losses, size and weight. Moreover, they aim to guarantee the secure operation of the system.

1.1 Green Village

The transition of the today's world towards a more sustainable one, led to the idea of the "Green Village" to be born. The Green Village vision is to "create a sustainable, lively and entrepreneurial environment where we discover, learn and show how to solve society's urgent challenges" (van Wijk, 2013). This will be realized at the TU Delft campus, finally converting it to a "green" and innovative campus, called the "Green Campus".

The Green Village development will be based on the following four missions:

- Clean energy producer
- Waste as resource
- Clean water producer
- Clean air producer

These missions develop in time and require a lot of research and innovation. Likewise, the Green Village is a lively environment which changes over time, ending to a temporary settlement. Its main objective is

to create a place where scientists, students and companies work together, interchange ideas and realize “green” solutions.

The Green Village will be built based on the principles of the circular economy. All the materials and equipment will be owned by a resource company and eventually taken back after use so that they can be reused in other projects or products. The Green Village will consist of a group of temporary structures, built for a period of 5-10 years. Figure 1.1.1 gives an artistic impression of how the Green Village will look like.



Fig. 1.1.1: Artistic impression of Green Village (The Green Village: a living village as a lab and showcase for innovative energy technology, 2012)

The lightning system of the Green Village will be based on the LED technology. LEDs will be also used in applications such as furniture, walls, floors, screens, even in clothes. The electricity grid will be DC, connecting all the power supply units with the power consuming and storage units. Fuel cells will be used for transportation, applied in the fuel cell cars, as well as electricity, water and H_2 production (van Wijk, 2013). These technologies in combination with other innovative ones, will be implemented in the projects of the Green Village. Some projects, landmark for the Green Village, are “the Harp”, “the Energy Wall” and “the Car Park Power Plant” (Figure 1.1.2). More information about the Green Village project can be found on the website: <http://www.thegreenvillage.org/>.



Fig. 1.1.2: Green Village projects (van Wijk, 2013)

1.2 DC VS AC

Traditionally, AC power is the primary mechanism for the majority of transmission and distribution networks. This happens basically due to the fact that it is much easier to convert AC from one voltage level to another by using transformers. Different voltage levels are necessary in the grid in order to secure high efficiency and small power losses. Moreover, AC power is easier to control/interrupt in switching and fault situations, leading to a capital investment far less than DC infrastructure.

However, DC holds a tremendous amount of promise especially in a future based on renewable energy sources. Solar panels, batteries and fuel cells generate or store DC power. Also, most of the electronic devices require DC power for their operation. It is obvious then that a DC power grid would reduce the conversion stages significantly, as it eliminates the DC to AC and back to DC conversions. This leads to a reduced cost and increased efficiency. DC technology is estimated to be 10% to 20% more energy efficient than traditional AC (validusDC, 2012). Fewer conversion points mean fewer hot spots, power losses and system vulnerabilities, resulting in a system with higher reliability, stability and a faster recovery time. At the same time, the integration of the renewable energy sources to the grid as well as the energy storage become easier.

The need for less components decreases equipment, installation and maintenance costs. It is also proved that the DC distribution power grids require less conductor material than the AC grids (Boeke & Wendt). For instance, a 380V DC grid can transfer the same power level and same cable loss with 63% less cable cross section than a 230V AC grid.

The advent and extensive use of power electronics also lead towards the DC direction. In broad terms, the task of power electronics is to process and control the flow of electric energy by providing with

voltages and currents the circuit in a form optimally suited for the user loads. Power electronic manufacturers face the challenge to develop components that comply with the continuously increasing grid requirements and are competitive in the market.

1.3 Green Village Electricity Grid

For the abovementioned reasons, the electricity in the Green Village will be provided by a smart DC grid (van Wijk, 2013). This grid will connect all the power supply units with the power storage facilities and power consuming devices. The main power sources will be solar panels and wind turbines, while the power storage will be done mainly in fuel cells. The power consuming devices that will be used, such as refrigerators, heat pumps, cooking appliances, LED lights and so on, are supposed to be as energy efficient as possible, smart and they will be equipped with an IP address for monitoring and control through the internet.

Inside the buildings the main voltage level will be $360V-400V$ DC. Also, a micro-grid where USB can be plugged in to charge equipment directly will be part of the system. The building micro-grid will be connected to the $700/1400V$ main DC network of the Green Village.

The first test container is already in place. This container is meant for the development of a well-controlled DC micro-grid of $380 V$ at container level that will be expanded to the Green Village level later on. The test container will also be used for testing and measuring equipment and implementing new technology for experimental reasons.

This innovative power system of course requires the development of new power electronics that can be used to such a grid and contribute to its high performance and reliability.

1.4 Goal and Methodology of the Project

The main goal of this project is:

- to investigate and determine a DC-DC buck (step-down) conversion topology that can be used for the connection of the power consumers (electronic appliances) to the $380V$ DC bus of the test container micro-grid and

- to design, develop and test an inrush current limiting circuit that will be placed between the main bus and the buck converter and eliminate the inrush current that results from the charging of the filter capacitors during the turn-on of the load

The DC-DC buck converter that will connect the loads to the main bus aims to convert the 380V voltage level to a lower voltage level appropriate for the optimum device operation, so that less power consumption is achieved and there is a near peak efficiency at all load conditions. Moreover, it will secure isolation between the load side and the mains in order to avoid problems in the load side affecting the rest of the system. The converter itself should have high efficiency in order not to add to the system losses and make use of a small number of components so that it has a small size, it is light and has reduced cost.

All in all, the converter topology has the following specifications:

- high efficiency (>95%)
- isolation
- reduced number of components

The Inrush Current Limiter (ICL) is necessary in order to secure the good operation of the system and protect the equipment and components of the circuit from damage due to high currents. The high inrush current is caused due to the fact that the input capacitors of the converter and the load of the circuit are initially empty acting as short circuits when the power is first applied. The ICL implemented in this project consists of a MOSFET and some passive elements that drive the MOSFET in such a way that the inrush current of the circuit can be limited by controlling the gate charge characteristic of the MOSFET.

In order to achieve the goals of this project, the following methodology was followed:

- the Femtograd system, which is a 380V DC bus system and it is the electricity system used by the test container, is first studied
- the operation of the buck and boost converter is described, so that some insight of their working principles can be obtained
- the control methods of DC-DC converters are investigated
- the Femtograd system is simulated
- the behavior of some electronic devices is investigated by testing them under DC and AC power, including inrush current measurements
- different buck converter topologies are studied and a selection is being done

- the ICL is designed, simulated, built and tested

A close collaboration with the company “Femtogrid” was required.

1.5 Structure of the Report

This report is structured in the following way:

Chapter 2 describes the electricity system of the test container. This electricity system, initially, is exclusively based on the Femtogrid system, which is a 380V DC bus system, implementing a parallel architecture. A detailed description of the Femtogrid system is also given in the 2nd chapter.

In chapter 3, the two basic power electronic topologies, i.e. the boost and buck converters, are described and their operation modes are explained. The boost and buck converters are the main power electronic components of the Femtogrid system.

In chapter 4, the most popular control methods of DC-DC converters are discussed. A literature study revealed some important information, advantages and disadvantages of these methods.

Chapter 5 explains how the modeling of every component (solar panel, power optimizer, buck converter) of the Femtogrid system was done. For building the models of the components, the software package Simulink/Matlab was used. The converters’ models are based on their state-space equations.

In chapter 6, the behavior of some common electronic appliances, in terms of power consumption and efficiency, is investigated under DC and AC power supply. Moreover, the inrush current of the devices is measured when they are supplied with DC power. The results from the experiments executed at the laboratory are presented here and conclusions are drawn based on these results. A comparison is done for the devices’ behavior under DC and AC power.

In chapter 7, four high efficiency, isolated buck converter topologies are described. One of them is selected and proposed for the buck converter design of the system discussed in this report.

In chapter 8, a circuit for limiting the inrush current of the system during sudden power up is proposed. This circuit makes use of a MOSFET and some passive elements. A prototype was simulated, built and tested. The simulation and experimental results are presented in this chapter.

In chapter 9, conclusions are drawn based on all the above analysis and some suggestions are made for further study.

In the section of the Appendices, the datasheets of the components of the FemtoGrid system are given, as well as some datasheets of power electronics used for the experiments. Additionally, the Simulink models of the system components and some curves of the experimental results taken from the ICL testing are presented.

Chapter 2: Test Container Micro-Grid

This chapter describes the test container micro-grid. It is explained that at a first approach, this micro-grid is based on the Femtogrid system, which is discussed here in detail.

2.1 Test Container

The first step towards the Green Village development is the construction of a test container at the TU Delft campus (Figure 2.1.1). This test container is meant to be used for testing equipment and performing measurements regarding the DC power grid and climate control of the Green Village. To that end, the test container is equipped with a 380V DC micro-grid. Main power sources are the solar panels placed on the roof of the container and a small DC wind turbine that is also on the roof.

At a first approach, the test container is fully equipped with the Femtogrid system. The container DC micro-grid is connected to the AC grid via an inverter and a rectifier. Surplus generated electricity is fed to the AC grid via the inverter. While if there is lack of power, the extra power needed is provided to the system from the AC grid via the rectifier. In this first stage no electricity storage is foreseen.

Actually, there are two containers placed next to each other, forming one common space. The roof of the one container is used for placing the solar panels and the wind turbine. The other one is used for the climate control system.

Considering the test container roof area, 6 solar panels were placed on the roof, as well as a small wind turbine. The power source devices used are the following:

- *Solar Panel Suntech STP 280-24Vd, Peak Power 280W*
- *Wind turbine Jetpro JPS-200, Peak Power 200W*

So, the maximum total power that can be produced is *1880W*. If more power is required, that is supplied to the system from the AC grid via the rectifier.



Fig. 2.1.1: Test container

2.2 Femtogrid System

As it was mentioned before, the test container's electricity system is based on the Femtogrid system. The Femtogrid system is a 380V DC bus system and apart from the solar panels and the wind turbine, it basically consists of 4 components:

- Power Optimizers
- DC cables
- Inverter 2400
- Monitoring

The solar panels use the PV300 Power Optimizer, which is mounted behind each solar panel. Each Solar Power Optimizer contains a DC-DC boost converter which converts the input voltage to the 380V of the main bus. Moreover, the Power Optimizer improves the performance of the individual solar panel by tracking its maximum power point. The solar panels are connected in parallel in the Femtogrid system. This parallel system architecture improves the overall performance for solar installations for suboptimal situations. By suboptimal situations are meant situations in which less power is produced than it is technically possible, like for example when there is partial shading, dirt, suboptimal angle to the sun or inferior solar panel quality. By connecting the solar panels in series the performance would be even

worse, because the overall power is eliminated by the solar panel that produces the smallest current. As a result, Femtograd system achieves a better efficiency and it is more flexible compared to the traditional systems which use serial string inverters that optimize the maximum power point of a string of solar panels.

For the communication between the Femtograd system and the AC grid, the Femtograd Inverter 2400 is used. This is a single phase isolated inverter and is designed to withdraw a maximum power of $2550W_{dc}$ from the solar panels. It is “simpler” compared to the traditional serial string inverters, as in the Femtograd system the Maximum Power Point Tracking (MPPT) is not performed by the inverter but by the Power Optimizers. The main task of the Inverter 2400 is to convert the voltage from $380V_{dc}$ to $230V_{ac}$. The Inverter also contains a voltage controller that ensures a voltage of $380V$ at the DC side. What is more, it communicates with each PV300 Power Optimizer and transfers the data to the Monitoring Box by using a wireless ZigBee network. Then the data can be transferred to the Monitoring Portal of the user. The Inverter 2400 also secures the safe operation of the system as it separates the Femtograd system from the grid.

The connection between the system components is done by the Femtograd DC cables. In order to ensure a safe system an integrated safety (black) wire of $48V$ is used besides the traditional red and blue wires. This safety line feeds the Power Optimizers from the Inverter.

The Monitoring system consists of a Monitoring Box and a Monitoring Portal. The Power Optimizers and the Inverter contain a ZigBee chip which gives them the opportunity to communicate the system data. Then the data are transmitted through the Monitoring Box to a personal website, the Monitoring Portal. As a result, the user is able to monitor the individual performance of each solar panel and collect information about fault detection and troubleshooting (Femtograd).

Figure 2.2.1 presents the connection between the different components of the Femtograd system, without taking into account the wind turbine.

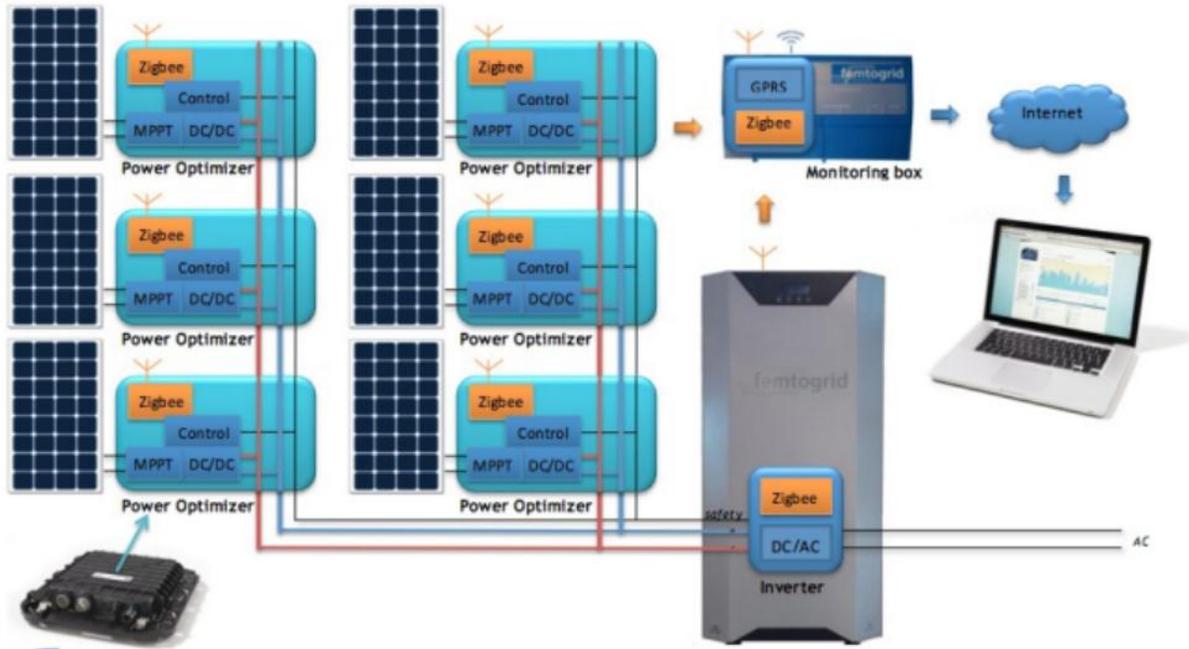


Fig. 2.2.1: Femtogrid system (Femtogrid)

As it was explained in the previous chapter, a buck converter with an ICL that will be used for the connection of each power consumer to the main bus of the test container should be constructed, so that optimum system operation and safety are guaranteed.

Figure 2.2.2 presents the block diagram of the test container's electricity system. In this figure, all the power electronics that will be used are shown.

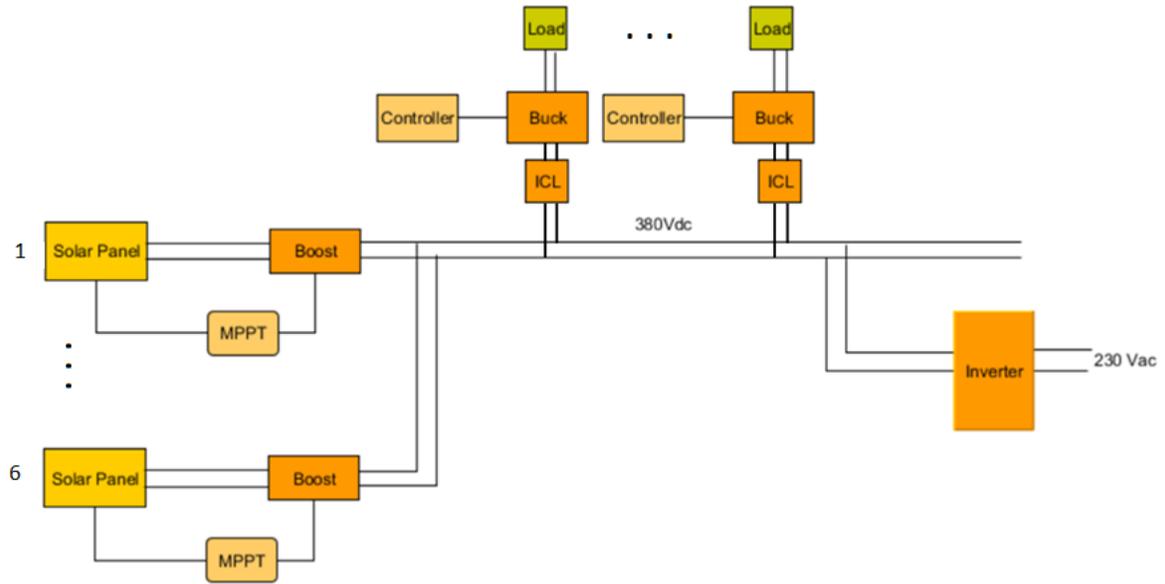


Fig. 2.2.2: Test container's electricity system block diagram

Chapter 3: DC-DC Converters

The DC-DC converters are widely used in regulated switch-mode DC power supplies and in DC motor drive applications. Although there are many different DC-DC converter topologies, two are the basic ones, i.e. the step-up (boost) converter and the step-down (buck) converter. The rest are derived from these two basic topologies.

In this chapter, the boost and buck converters are described, as well as their operation modes. These two converters are the basic power electronic components of the container’s micro-grid system.

3.1 Boost Converter

The boost converters are used in many applications that require the boosting up of the voltage. Normally, a solar panel will only produce 16V in full, nearly normal sunlight. As a result, a boost converter is generally used in order to step up the output voltage of the solar panel to the suitable voltage required by the electronic equipment.

The boost converter is a medium of power transmission to perform energy absorption and injection from the solar panel to the DC bus. It consists of four components, which are an inductor, an electronic switch, a diode and an output capacitor. The boost converter circuit can be implemented as shown in Figure 3.1.1.

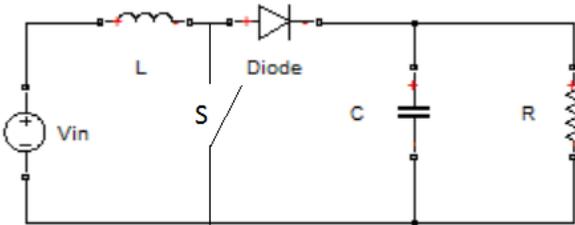


Fig. 3.1.1: Electronic circuit of boost converter

The process of energy absorption and injection constitutes a switching cycle. The average output voltage can be controlled by the switching on and off time duration. Under constant frequency, the adjustment

of the on and off time duration is called Pulse Width Modulation (PWM). The duty cycle D is defined as the on-time of the switch over the switching period: $D = \frac{t_{on}}{T}$ and it is always: $0 \leq D \leq 1$.

A boost converter can operate in two modes known as the Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The operation mode depends on the energy absorption and injection in combination with the relative length of the switching period.

3.1.1 Boost Converter Operation Modes

3.1.1.1 Continuous Conduction Mode (CCM)

During the CCM, the boost converter operates in two modes, which are depicted in the Figures 3.1.1.1.1 and 3.1.1.1.2. Figure 3.1.1.1.3 presents the waveforms of the boost converter in CCM. The key principle of the boost converter operation is the tendency of the inductor to resist changes in current.

Mode 1 appears when the switch S is turned on. The diode is reverse biased, thus isolating the output stage. The current provided by the voltage source, flows through the inductor and the switch and as a result, energy is stored in the inductor. The load is supplied by the capacitor current. During Mode 1, the inductor current increases as can be shown in Figure 3.1.1.1.3.

At $t=DT$, the switch is turned off and Mode 2 begins. The diode now conducts and the output stage receives energy from the inductor as well as from the input. The inductor current reduces because the impedance is higher. This results in the reversion of the polarity of the inductor voltage leading to a higher voltage to charge the capacitor. After $(1-D)T$, the switch is turned on again (Chan, Masri).

According to the volt-second balance, in steady state, the time integral of the inductor voltage over one time period must be zero,

$$V_{in}t_{on} + (V_{in} - V_{out})t_{off} = 0$$

Dividing both sides by the period T , the voltage ratio is obtained:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - D}$$

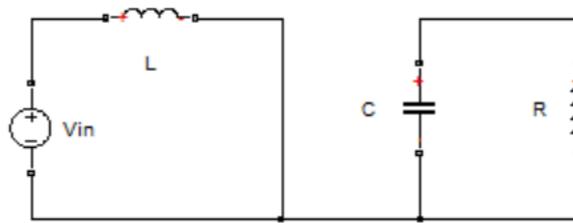


Fig. 3.1.1.1.1: Boost converter in Mode 1

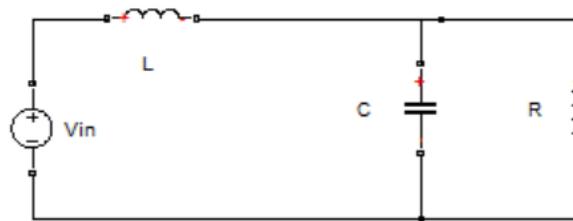


Fig. 3.1.1.1.2: Boost converter in Mode 2

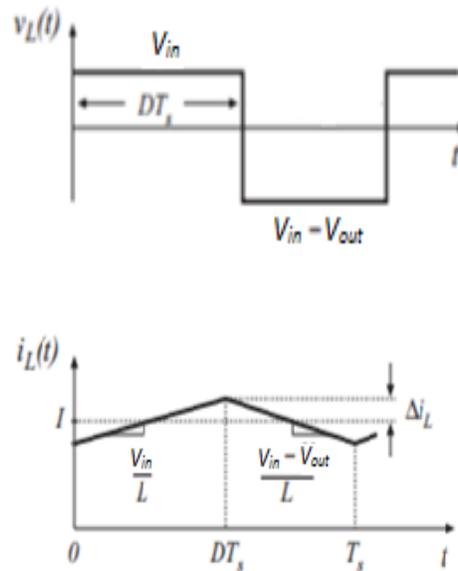


Fig. 3.1.1.1.3: Boost converter waveforms in CCM: inductor voltage and inductor current (Wattanasan, Principles of Steady-State Converter Analysis)

The converter operates in CCM when the inductor is not fully discharged in between the charging states and the inductor current flows continuously and never falls to zero. With this requirement, the boundary value for the inductance is calculated to be:

$$L_{min} = \frac{(1 - D)^2 DR}{2f}$$

(3.1.1.1.1)

where L_{min} is the minimum value of the inductance for operation in CCM, R is the resistance of the load, D is the duty cycle and f is the switching frequency.

Moreover, it is required that the output voltage ripple be very small. Hence, for a well-designed converter the peak output voltage ripple should be much smaller in magnitude than the output voltage DC component. So, it was assumed that $v_{out}(t) = V_{out}$.

3.1.1.2 Discontinuous Conduction Mode (DCM)

When the inductor current is clamped to zero for a time interval during one period, the boost converter operates in DCM. Operation in DCM adds one more mode to the two modes described before, during which the inductor current is zero. Both switch and diode are in the off-state, as depicted in Figure 3.1.1.2.1. Now the boost converter waveforms are described by Figure 3.1.1.2.2.

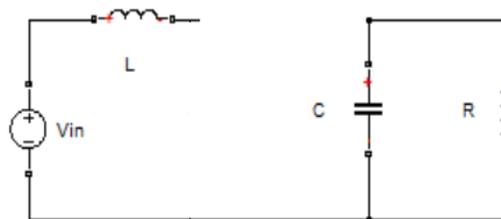
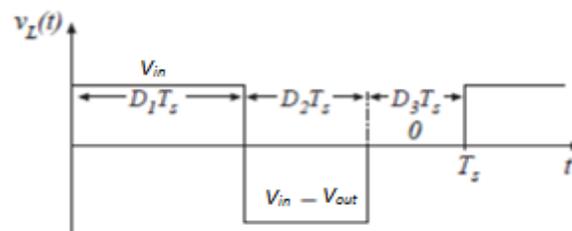


Fig. 3.1.1.2.1: Boost converter in Mode 3



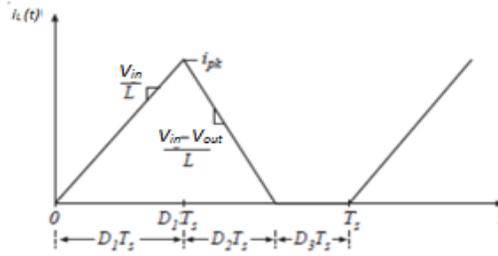


Fig. 3.1.1.2.2: Boost converter waveforms in DCM: inductor voltage and inductor current (Wattanasan, The Discontinuous Conduction Mode)

For steady state, by taking the time integral of the inductor voltage over one time period equal to zero, follows:

$$V_{in}D_1T + (V_{in} - V_{out})D_2T = 0$$

$$\frac{V_{out}}{V_{in}} = \frac{D_1 + D_2}{D_2}$$

(3.1.1.2.1)

where D_1 is the duty cycle of the first interval and D_2 the duty cycle of the second interval.

It should be noticed that the duty ratio of the second interval (D_2) is not an independent variable, but rather has algebraic dependence on the other variables (L, f, R, D_1).

One more equation is needed in order to determine the unknown variables V_{out} and D_2 . This equation is found from the capacitor charge balance (Wattanasan, The Discontinuous Conduction Mode). According to this balance, the time integral of the capacitor current over one period should be equal to zero. So:

$$I_c = I_D - \frac{V_{out}}{R} = 0$$

From Figure 3.1.1.2.3, the peak value of the inductor current is found to be:

$$i_{pk} = \frac{V_{in}}{L} D_1 T$$

The diode current is identical to the inductor current during the second subinterval, while it remains zero for the rest of the time, as the diode is reverse biased (Figure 3.1.1.2.3). So, the peak value of the diode current is the same as the peak value of the inductor current. With the help of the above equation, the DC component of the diode current is calculated:

$$I_D = \frac{V_{in} D_1 D_2 T}{2L}$$

As a result, the second equation needed is:

$$\frac{V_{in}D_1D_2T}{2L} = \frac{V_{out}}{R}$$

(3.1.1.2.2)

By solving the system of the equations (3.1.1.2.1) and (3.1.1.2.2), the following results are obtained:

$$M = \frac{V_{out}}{V_{in}} = \frac{V_C}{V_{in}} = \frac{1}{2} + \frac{1}{2} \sqrt{1 + \frac{2D_1^2R}{Lf}}$$

(3.1.1.2.3)

$$D_2 = \frac{2Lf}{D_1R} M$$

(3.1.1.2.4)

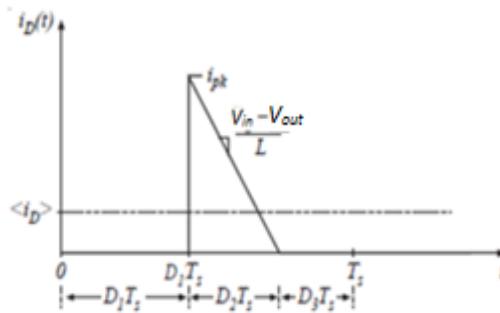


Fig. 3.1.1.2.3: Diode current waveform of boost converter in DCM (Wattanasan, The Discontinuous Conduction Mode).

As it was explained before, the minimum inductance for CCM operation is given by the equation (3.1.1.1.1). Thus, any value smaller than this critical value, will result in DCM operation.

3.2 Buck converter

The buck converter is the other basic topology of DC-DC converters. It produces a lower average output voltage than the DC input voltage. Its main application is in regulated DC power supplies and DC motor speed control.

The design of the buck converter is similar to that of the boost converter. Similarly to the boost converter, the buck converter is a power transmission medium that consists of four components, i.e. an electronic switch, a diode, an inductor and an output capacitor. The electronic circuit of the buck converter is presented in Figure 3.2.1.

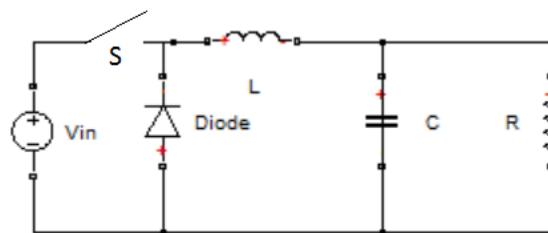


Fig. 3.2.1: Electronic circuit of buck converter

The duty cycle of the buck converter needs to be controlled so that the average output voltage can be controlled.

A buck converter can work in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) depending on the energy absorption and injection in combination with the relative length of the switching period.

3.2.1 Buck Converter Operation Modes

3.2.1.1 Continuous Conduction Mode (CCM)

CCM operation happens when the inductor current flows continuously through the circuit. In CCM, the buck converter operates in the two modes which are presented in Figures 3.2.1.1.1 and 3.2.1.1.2. Figure

3.2.1.1.3 shows the buck converter waveforms. It is important to mention that the inductor’s tendency to resist changes in current is the basic reason that determines the converter’s operation.

Mode 1 appears when the switch is in on position. Then, the switch conducts the inductor current and the diode becomes reverse biased. This results in a positive voltage $v_L=V_{in}-V_{out}$ across the inductor, which causes a linear increase in the inductor current and energy is stored in the inductor. The voltage over the load is decreased because of the voltage drop that induces the inductor in the input voltage.

At $t=DT$, the switch turns off and mode 2 begins. The voltage source is not connected to the circuit, however current continues to flow because of the inductive energy storage. This current flows through the diode and decreases while the inductor is getting discharged. After $(1-D)T$, the switch is turned on again.

In steady state, the integral of the inductor voltage over one period must be zero. Then:

$$(V_{in} - V_{out})t_{on} - V_{out}t_{off} = 0$$

so the voltage ratio for the buck converter will be:

$$\frac{V_{out}}{V_{in}} = D$$

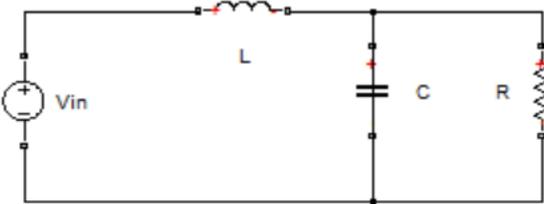


Fig. 3.2.1.1.1: Buck converter in Mode 1

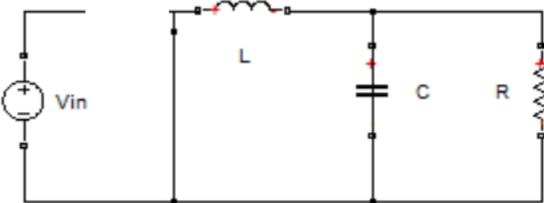


Fig. 3.2.1.1.2: Buck converter in Mode 2

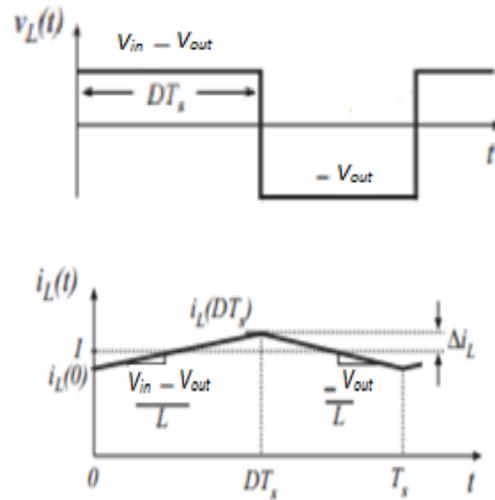


Fig. 3.2.1.1.3: Buck converter waveforms in CCM: inductor voltage and inductor current (Wattanasan, Principles of Steady-State Converter Analysis)

The requirement that the inductor current never falls to zero in CCM, determines the boundary condition for operation in CCM. The critical value of the inductance turns out to be:

$$L_{min} = \frac{(1 - D)R}{2f}$$

(3.2.1.1.1)

where L_{min} is the minimum value of the inductance for operation in CCM, R is the resistance of the load, D is the duty cycle and f is the switching frequency (Chander, Agarwal, & Gupta, 2010).

Furthermore, the output voltage ripple is required to be very small. Therefore, for a well-designed converter, the output voltage ripple should be very smaller in magnitude than the output voltage DC component. Thus, it was assumed that $v_{out}(t) = V_{out}$.

3.2.1.2 Discontinuous Conduction Mode (DCM)

The buck converter operates in DCM when the inductor gets completely discharged before the commutation cycle finishes. Figure 3.2.1.2.1 presents the converter mode for the third time interval during which the inductor current is clamped to zero. In this mode, both switch and diode are in the off-state. The buck converter waveforms in DCM are described by the Figure 3.2.1.2.2.

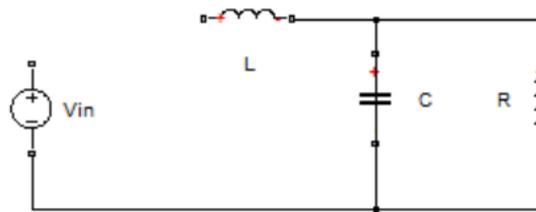


Fig. 3.2.1.2.1: Buck converter in Mode 3

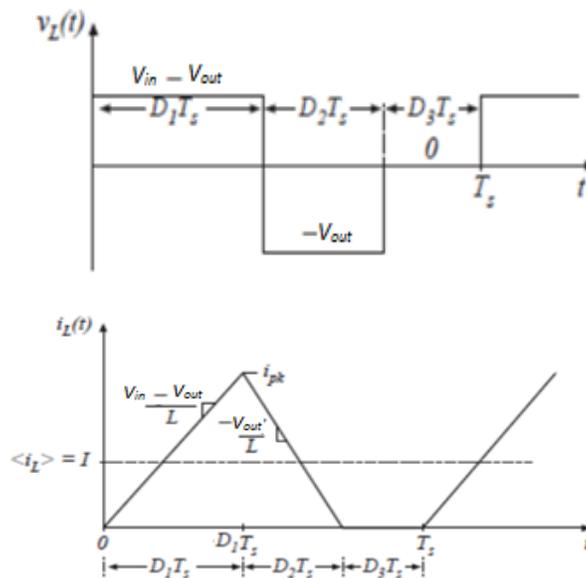


Fig. 3.2.1.2.2: Buck converter waveforms in DCM: inductor voltage and inductor current (Wattanasan, The Discontinuous Conduction Mode)

The same procedure, as in case of the boost converter, is followed here in order to determine the necessary relationships for DCM operation.

Equating the integral of the inductor voltage over one time period to zero yields:

$$(V_{in} - V_{out})D_1T + (-V_{out})D_2T = 0$$

$$\frac{V_{out}}{V_{in}} = \frac{D_1}{D_1 + D_2}$$

(3.2.1.2.1)

where D_1 is the duty cycle of the first interval and D_2 the duty cycle of the second interval.

It is repeated here that the duty ratio of the second interval (D_2) is not an independent variable, but rather has algebraic dependence on the other variables (L, f, R, D_1).

The second equation needed is obtained by making use of the capacitor charge balance.

$$I_c = I_L - \frac{V_{out}}{R} = 0$$

From Figure 3.2.1.2.2, the inductor current peak value is found to be:

$$i_{pk} = \frac{V_{in} - V_{out}}{L} D_1 T$$

Then the DC component of this current is:

$$I_L = (V_{in} - V_{out}) \frac{D_1 T}{2L} (D_1 + D_2)$$

As a result, the following equation is obtained.

$$\frac{V_{out}}{R} = (V_{in} - V_{out}) \frac{D_1 T}{2L} (D_1 + D_2)$$

(3.2.1.2.2)

Finally, solving the system of the equations (3.2.1.2.1) and (3.2.1.2.2) yields:

$$M = \frac{V_{out}}{V_{in}} = \frac{V_C}{V_{in}} = \frac{2}{1 + \sqrt{1 + \frac{8Lf}{D_1^2 R}}}$$

(3.2.1.2.3)

$$D_2 = \frac{2Lf}{RD_1} M$$

(3.2.1.2.4)

As it was explained before, the minimum inductance value required for operation in CCM is given by the equation (3.2.1.1.1). Any value smaller than this critical value, will result in DCM operation.

3.2.2 Synchronous Buck Converter

The synchronous buck converter is a modified version of the basic buck converter, where the diode has been replaced by a second switch, which in most applications is always turned on when the top switch is turned off (complementary switching).

The synchronous buck converter has some advantages compared to the traditional buck converter. At first, in low voltage applications the efficiency can be increased. This happens because the switch appears lower voltage drop in the on-state than the forward voltage drop of the diode. Secondly, the synchronous buck converter allows bidirectional power flow. When power flows in the “reverse” direction, it acts like a “boost” converter (Hirschmann, Richter, Dick, & De Doncker, 2007).

However, there are also some disadvantages in the use of the synchronous buck converter, like the increased cost and complexity. Attention must be paid to prevent the so called “shoot-through” fault. As “shoot-through” is defined the condition when both switches are turned on at the same time either fully or partially. This would result in destructive current flow through the switches and should be avoided.

Chapter 4: Control Methods of DC-DC Converters

The DC-DC converters (both buck and boost) require a control system that will determine their duty cycle, so that they will perform the right power conversion and provide the load with the appropriate voltage level. The control of the DC-DC converters can be done by several control methods. Each method appears its own advantages and disadvantages. A literature study was executed in order to examine the existing control methods.

4.1 PID Controllers

Buck and boost converters are nonlinear systems due to their inherent switching operation. Several linear and nonlinear control techniques have been used so far to control these converters. Classical control theory is based on the design of PID (Proportional-Integral-Derivative) family controllers. PID voltage-mode (VM) and PI current-mode (CM) controllers are applied for DC-DC converters using standard frequency response techniques. It should be noted that the design of these controllers requires precise linear mathematical models. They fail to perform satisfactory under parameter variation, non-linearity, load disturbance, etc. and they are useful only for small signals models (Raviraj & Sen, 1997). In order to deal with these problems, nonlinear controllers, which are more robust and have faster dynamic response, are applied to the power converters. Such controllers are fuzzy logic controllers and sliding mode controllers (Ellabban & Van Mierlo, 2009).

4.1.1 PID Voltage Mode Control (PID VMC)

The PID VM Control (VMC) is widely used because it is easy to design and implement and has good community to disturbances at the references input. Figure 4.1.1.1 presents the block diagram of the VMC of a buck converter. As it can be seen from the figure, the voltage output is compared to a constant reference signal to form the error, which is then passed through the controller to generate a control signal proportional to the duty ratio. Finally, the PWM modulator creates the signal for driving the switch (q).

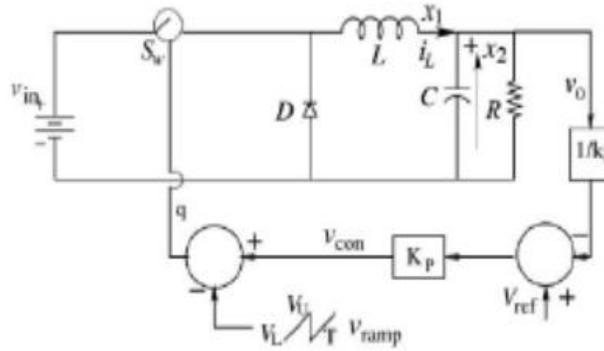


Fig. 4.1.1.1: Block diagram of voltage-mode control of buck converter (Himanshu, 2012)

4.1.2 PI Current Mode Control (PI CMC)

The PI CM control (CMC) is implemented as shown in Figure 4.1.2.1. In this control method, the PWM modulator is replaced by the inductor current feedback loop. At the beginning of the switching cycle, the clock signal sets the flip-flop ($q=1$), turning on the switch. The switch current rises linearly during this interval. The inductor current is compared with the control signal (i_{ref}). When the switch current is slightly greater than the reference current, the comparator output goes high and resets the flip-flop ($q=0$), turning off the switch. With the next clock signal, the switch is turned on again and the same procedure is repeated.

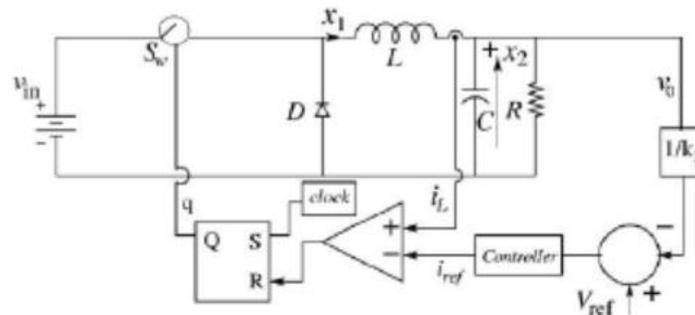


Fig. 4.1.2.1: Block diagram of current-mode control of buck converter (Himanshu, 2012)

4.2 Fuzzy Logic Controllers

The conventional control theory requires the mathematical model of the process that needs to be controlled. However, obtaining the mathematical model is difficult in many cases, like for example when the system is nonlinear or unknown or if it does not have constant parameters. Fuzzy logic control is based on the fuzzy set theory introduced by Zadeh in 1965 (Zadeh, 1965). Fuzzy controllers do not require an exact mathematical model. They are designed based on general knowledge of the plant, by making use of the knowledge and experience of an expert and they are especially useful for approximate systems. Some advantages of the fuzzy logic control are:

- it can work with less precise inputs,
- it does not require fast processors,
- it needs less data storage in the form of membership functions and rules than conventional look up table for nonlinear controllers and
- it is more robust than other nonlinear controllers.

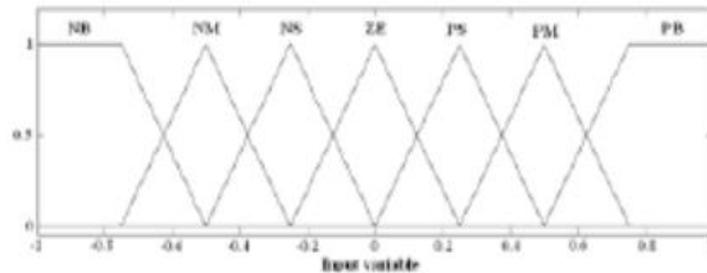


Fig. 4.2.1: Fuzzy sets (Ellabban & Van Mierlo, 2009)

The fuzzy controller has two inputs. The first input is the error in the output voltage ($e(k)=V_{ref}-V_o(k)$) and the second input is the change of the error ($ce(k)=e(k)-e(k-1)$). Each input is composed by seven fuzzy sets as shown in Figure 4.2.1. The two inputs are multiplied by two scaling factors g_0 and g_1 respectively and fed into the fuzzy controller, which gives as output the change of the duty cycle ($\delta d(k)$). The duty cycle at the k^{th} sampling time, is determined by:

$$d(k) = d(k - 1) + g_2 \cdot \delta d(k)$$

where g_2 is the linear gain of the $\delta d(k)$.

The duty cycle is then sent to a PWM module that creates the switching signal for the buck converter. Table 4.2.1 presents the rule base of the fuzzy controller.

Table 4.2.1: Rule base for fuzzy controller (Ellabban & Van Mierlo, 2009)

e/ce	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

There are several variations of this fuzzy logic controller presented in different studies. (Safarinejadian & Jafartabar, 2012) proposes a two-level hybrid fuzzy logic controller in order to decrease the settling time and a fuzzy PD+I controller in order to minimize the steady state error. (Seshachalam, Tripathi, Chandra, & Kumar, 2006) describes a fuzzy logic controller based on the sliding mode concept with reduced rule base. With this concept reduced chattering is achieved. A fuzzy logic controller with an adaptation algorithm for regulation of the output voltage of the controller despite the load changes has been proposed by (Elmas, Deperlioglu, & Huseyin Sayan, 2009). Finally, (Rabbani, Mesbah Maruf, Ahmed, Ashfanor Kabir, & Mahbub, 2012) presented a robust fuzzy PID controller. This controller was proved that performs better than the conventional PID controller while it appears to have excellent adaptation, simplicity and universality.

4.3 Sliding Mode Controllers (SMC)

The sliding mode controllers (SMC) is another kind of controllers that do not need accurate mathematical models of the process in order to operate but require the knowledge of parameter variation range to ensure stability and satisfy reaching conditions. They have first-order response irrespective of the order of the system. However, the fact that the worst-case inputs can be large, leads to chattering (Raviraj & Sen, 1997). This problem was solved by introducing a boundary layer around the sliding plane. SMC introduce to the system some advantages, like a fast dynamic response, high robustness to external disturbances and exclusive dependence of the behavior of the system on the parameters of the converter. Nevertheless, the SMC appear some drawbacks as well. First of all, the output voltage has a steady state error. Moreover, in many cases it is difficult to generate the reference values of some state variables, the state values can be large when the system is reaching the sliding function and finally the switching frequency should be bounded (Orosco & Vázquez, 2000).

There are many papers in the literature that deal with the SMC. Generally, it can be said that a typical SMC is described by the block diagram shown in Figure 4.3.1. It has two control modes: voltage mode

control and current mode control. In most cases, voltage mode control is preferred because constant output voltage is required. The state space description with control parameters the output voltage error and the output voltage error dynamics is used. In SMC, the system response in the phase plane is forced to follow a sliding line as shown in Figure 4.3.2, x denotes the state error which needs to be driven to zero and \dot{x} is its derivative. In the time domain, the response is exponential and depends only on the slope of the sliding line $x + c\dot{x} = 0$.

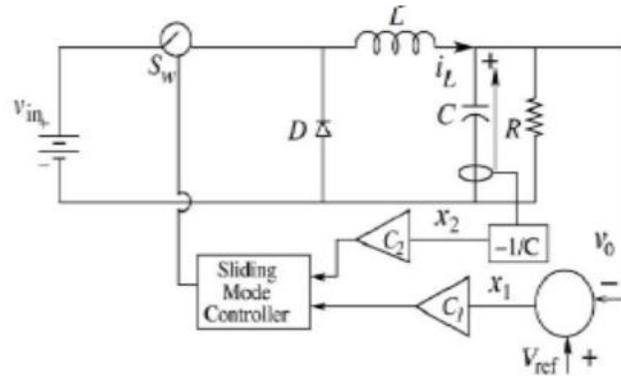


Fig. 4.3.1: Block diagram of sliding mode controller of buck converter (Himanshu, 2012)

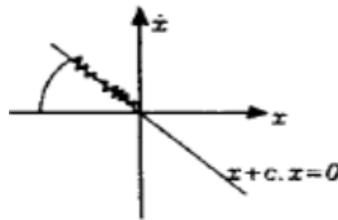


Fig. 4.3.2: Phase plane trajectory of sliding mode controller (Himanshu, 2012)

Some studies that discuss the SMC are presented here. (Akbar Hussainy, Ganguli Tandon, & Kumar, 2012) proposed a PWM based SMC in order to limit the switching frequency. (Ahmed, Kuisma, Tolsa, & Silventoinen, 2003) focuses on modeling a SMC circuit in Matlab/Simulink, implementing it to the buck converter and finally building up a prototype with SMC. It concludes that this control can stabilize the power supply and that the output voltage and inductor current can return to steady state when there is line and load variation with a very small overshoot and settling time. Also, the efficiency is found to be acceptable. A discrete sliding mode controller (DSMC) is proposed by (Orosco & Vázquez, 2000). The authors claim that the DSMC appear some advantages compared to the continuous SMC, such as flexibility in the creation of the sliding surface, the fact that the same control strategy can be used in different converters, the possibility to integrate advanced functions into the control algorithm and finally, the creation of an adaptive control. (Perry, Liu, & Sen, 2004) presents a sliding mode like control

(SMLC) technique and its fuzzy logic implementation. The paper concludes that the proposed control scheme has fixed switching frequency and appears zero steady state error.

4.4 Maximum Power Point Tracking Controllers (MPPT Controllers)

In most of the cases, when a DC-DC converter (normally boost converter) is connected to a photovoltaic (PV) generation system, a controller that implements a MPPT algorithm is used. By MPPT algorithm is meant the algorithm that tracks the unique point of the PV system at which maximum efficiency and output power is achieved. Throughout the years, many MPPT techniques have been developed. The MPPT methods will be further discussed in the next chapter.

4.5 Other Controllers

Apart from the control methods described above, there are many other control techniques discussed in the literature. For example, (Yang & Sen, 1999) proposed a current mode control technique, in which the inductor current and the diode current are feedback and combined in a specially non-linear way that makes the average inductor current proportional to the current control signal. Stability analysis revealed that the current control loop is inherently stable. The paper also used a closed-loop controller to achieve output voltage regulation.

A novel nonlinear average current control method with fixed frequency is presented by (Kancherla & Tripathi, 2008). The switch current is sensed and no current compensator is required. This control method is meant to overcome the problems of existing nonlinear control methods and to reject source and load disturbances in both CCM and DCM, while it offers very good ride through capability for source and load disturbances with a PI controller.

Finally, in (Yang, Chen, Chen, Hwang, & Lee, 2006) a hysteresis current controller for a buck converter suitable for a Li-Ion battery charger is presented. The charger operates in constant current/constant voltage dual mode, in order to decrease the damage of Li-Ion battery and improve the power efficiency of the charger. The study claims that the power efficiency of the charger can be up to 82% under the average power of 825mW. The proposed circuit is suitable for portable systems.

4.6 Conclusions

In this chapter, various control methods of DC-DC converters were studied. Although there are many methods that permit the voltage and/or current control of the DC-DC converters, it can be said that the most commonly used controllers are: the PID (PID VMC and PI CMC), fuzzy logic and sliding mode controllers or modified, improved or combined models of these controllers. For the control of the boost converter that follows the solar panels of a PV system, MPPT techniques are implemented. It is worth mentioning that the controllers can affect the current and voltage overshoot and settling time apart from their steady state values.

As it was explained in the previous sections, each control method appears some pros and cons. The PID controllers are based on the widely used classical control theory. They require precise linear mathematical models for their design and they are practically useful only for small signal models. Moreover, they are unable to perform satisfactory under large parameter or load variation.

As the power converters are nonlinear systems, other control methods such as fuzzy logic control and sliding mode control are preferred. These methods do not require accurate mathematical models of the process in order to perform satisfactory, are more robust and have faster dynamic response. The fuzzy logic controllers are designed based on the knowledge and experience of an expert and are ideal for approximate systems. However, as far as the sliding mode controllers are concerned, the knowledge of the parameter variation range is necessary. The sliding mode controllers have always first-order response and apply really well to power converters. Nevertheless, they also appear some restrictions. For instance, there can be a steady state error in the output voltage, the switching frequency needs to be bounded and sometimes it is difficult to obtain the reference values of some state variables.

All in all, a control method needs to be chosen for the power converters after considering the features of the methods and the under control system.

Chapter 5: Modeling of FemtoGrid System

The modeling of the FemtoGrid system is done by making use of the software package Simulink/Matlab. The models of the solar panel, power optimizer (including boost converter with MPPT) and buck converter were built. These models can be found in the Appendix B.

It should be noted that both the boost and the buck converters are designed to operate in DCM. This “FemtoGrid’s” choice was done in order to achieve a better efficiency. For low power applications, DCM is preferred in order to avoid the reverse recovery problem of the diode. Moreover, DCM operation can be considered a possible solution to the right-half plane (RHP) zero problem encountered in buck-boost and boost topologies.

In the following sections, the models of the different components of the system are described.

5.1 Solar panels

The energy source of the examined system is the solar modules. Each solar module or solar panel consists of several solar cells connected in series in order to increase the power and voltage produced by the module. This can be better understood if one notices that a typical PV cell produces less than 2W at 0.5V. Thus, series-parallel configurations of cells in a module are generally adopted.

A solar cell is basically a p-n junction fabricated in a thin wafer or layer of a semiconductor. The solar cells work on the principle of the photovoltaic effect. The photovoltaic effect is defined as the creation of a voltage or a corresponding electric current in a material upon exposure to light. In other words, when the solar module is exposed to sunlight, the photons with energy greater than the band-gap energy of the semiconductor are absorbed and create some electron-hole pairs proportional to the incident irradiation. Due to the influence of the internal electric fields of the p-n junction, these energy carriers create a photocurrent which is directly proportional to the solar insolation.

However, the current-voltage relationship and the power-voltage relationship are not linear and depend on the solar insolation, the cell temperature and the output voltage of the PV module. The I-V and P-V characteristics of a solar panel are shown in Figure 5.1.1.

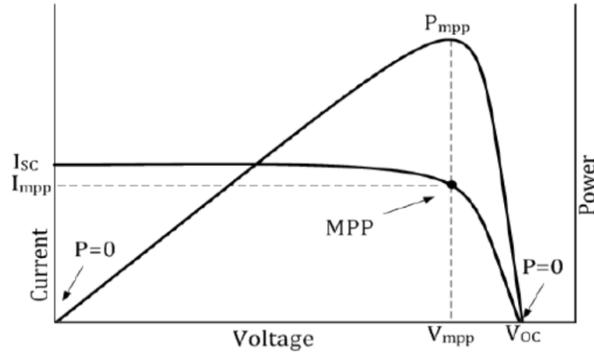


Fig. 5.1.1: I-V and P-V characteristics of a solar module

In the Femtogrid system, there is one Power Optimizer connected to each solar module. The Simulink model of the solar module is therefore created. First, the modeling of a single solar cell is described.

5.1.1 Solar Cell Model

The equivalent circuit of a PV cell is considered to consist of a current source connected in parallel with a diode, a parallel resistor expressing a leakage current and a series resistor describing an internal resistance to the current flow. The electrical circuit of the PV cell is shown in Figure 5.1.1.1.

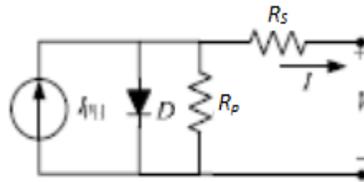


Fig. 5.1.1.1: General model of a photovoltaic cell (Tsai, Tu, & Su, 2008)

The voltage-current characteristic equation of the PV cell is (Tsai, Tu, & Su, 2008):

$$I = I_{PH} - I_S \left[\exp \left(\frac{q(V + IR_S)}{kT_C A} \right) - 1 \right] - \frac{V + R_S I}{R_p} \quad (5.1.1.1)$$

where I_{PH} is the light-generated current or photocurrent, I_S is the saturation current, q is the electron charge ($1.6 \cdot 10^{-19} C$), k is the Boltzmann's constant ($1.38 \cdot 10^{-23} J/K$), T_C is the cell's working temperature, A

is the ideality constant (usually $1 \leq A \leq 1.5$) which depends on the PV technology used, R_S is the series resistance of the cell and R_p the parallel resistance.

The light generated current (I_{PH}) depends linearly on the solar irradiation and is also influenced by the temperature according to the following equation:

$$I_{PH} = [I_{PH,n} + K_I(T_C - T_{Ref})]\lambda \quad (5.1.1.2)$$

where $I_{PH,n}$ is the photocurrent at the nominal conditions and it is assumed to be equal to the short-circuit current ($I_{PH,n} \approx I_{SC}$) at $25^\circ C$ and $1kW/m^2$, K_I is the cell's short-circuit current temperature coefficient, T_{Ref} is the cell's reference temperature and λ is the solar insolation in kW/m^2 . The short-circuit current and the cell's short-circuit current temperature coefficient are generally given in the manufacturer's datasheets.

The saturation current (I_S) is described by the equation:

$$I_S = I_{RS} \left(\frac{T_C}{T_{Ref}} \right)^3 \exp \left[\frac{qE_G \left(\frac{1}{T_{Ref}} - \frac{1}{T_C} \right)}{kA} \right] \quad (5.1.1.3)$$

where I_{RS} is the reverse saturation current at a reference temperature and a solar radiation and E_G is the band-gap energy of the semiconductor used in the cell.

5.1.2 Solar Module Model

As it was explained before, a solar module consists of several solar cells connected in series. If N_s is the number of the PV cells connected in series and N_p is the number of the PV cells connected in parallel in a solar array, where $N_p=1$ for a PV module, then the module current becomes as follows:

$$I = N_p I_{PH} - N_p I_S \left[\exp \left(\frac{q(V/N_s + IR_S/N_p)}{kT_C A} \right) - 1 \right] - \frac{N_p V/N_s + R_S I}{R_p} \quad (5.1.2.1)$$

The expressions for the photocurrent and the saturation current are given by the equations (5.1.1.2) and (5.1.1.3) respectively.

The reverse saturation current is approximated by the formula:

$$I_{RS} = I_{SC} / [\exp\left(\frac{qV_{OC}}{N_s k A T_c}\right) - 1]$$

(5.1.2.2)

As a result, the solar panel model is designed based on the equations (5.1.2.1), (5.1.1.2), (5.1.1.3) and (5.1.2.2).

5.2 Maximum Power Point Tracking

In general, PV generation systems have two major problems; the conversion efficiency of electric power generation is low (less than 17%) and the amount of electric power produced depends strongly on the weather conditions. As it was mentioned before, the I-V characteristic of the solar cell is nonlinear and varies with the irradiation and the cell temperature. From the Figure 5.1.1, it is obvious that there is a unique point on the I-V curve (or P-V curve) at which the PV system operates with maximum efficiency and produces its maximum output power. This point is called Maximum Power Point (MPP) and the power, voltage and current that correspond to that point are denoted as P_{MPP} , V_{MPP} and I_{MPP} respectively.

The location of the MPP can be found through calculation models or search algorithms. MPPT techniques are used to determine the V_{MPP} and/or I_{MPP} . It should be noted that under partial shading conditions, in some cases, there are multiple maxima, however overall there is only one MPP. Many MPPT techniques have been developed and implemented. The methods vary in complexity, sensors required, cost, range of effectiveness, popularity, hardware and in other aspects. Some of these methods are the Perturb and Observe/Hill-Climbing, Incremental Conductance, Fractional Open-Circuit Voltage, Fractional Short-Circuit Current and the Fuzzy Logic Control method (Esrām & Chapman), (Ali, Saied, Mostafa, & Abdel- Moneim). The method implemented from the Femtogrid power optimizer is the Perturb and Observe method.

5.2.1 Perturb and Observe Method

The Perturb and Observe method involves a perturbation in the operating voltage of the PV array (PV module in this system). In the case of a PV module connected to a power converter, perturbation in the

duty cycle of the converter causes a perturbation in the PV module current and consequently in the PV module voltage.

From Figure 5.1.1, it can be seen that incrementing (decrementing) the voltage increases (decreases) the power when operating on the left of the MPP, while decreases (increases) the power when operating on the right of the MPP. As a result, the subsequent perturbation should be kept the same if there is an increase in power, to reach the MPP, while if there is a decrease in power, the perturbation should be reversed. This process is repeated periodically until the MPP is reached. Then the system oscillates around the MPP. The step size is a trade-off between the size of the oscillations and the algorithm speed.

If the PV module is connected to a boost converter, the right side curve corresponds to a lower duty cycle (nearer to zero), while the left side curve corresponds to a higher duty cycle (nearer to unity). Similarly to the array voltage, depending on the sign of the power and voltage change, the algorithm decides if it will increase or decrease the duty cycle.

Two sensors (current sensor and voltage sensor) are usually required to measure the current and voltage of the PV, from which the power production is calculated. For some power converter topologies one voltage sensor is enough. Figure 5.2.1.1 presents the flowchart of the algorithm. According to that, first the voltage and current values are measured for a k th instant and the power is calculated. Then the $(k-1)$ th instant power and voltage are subtracted from the power and voltage of the k th instant. Depending on the sign of the result, the duty cycle increases or decreases by the step. The procedure is repeated until the MPP is reached (Alsadi & Alsayid, 2012).

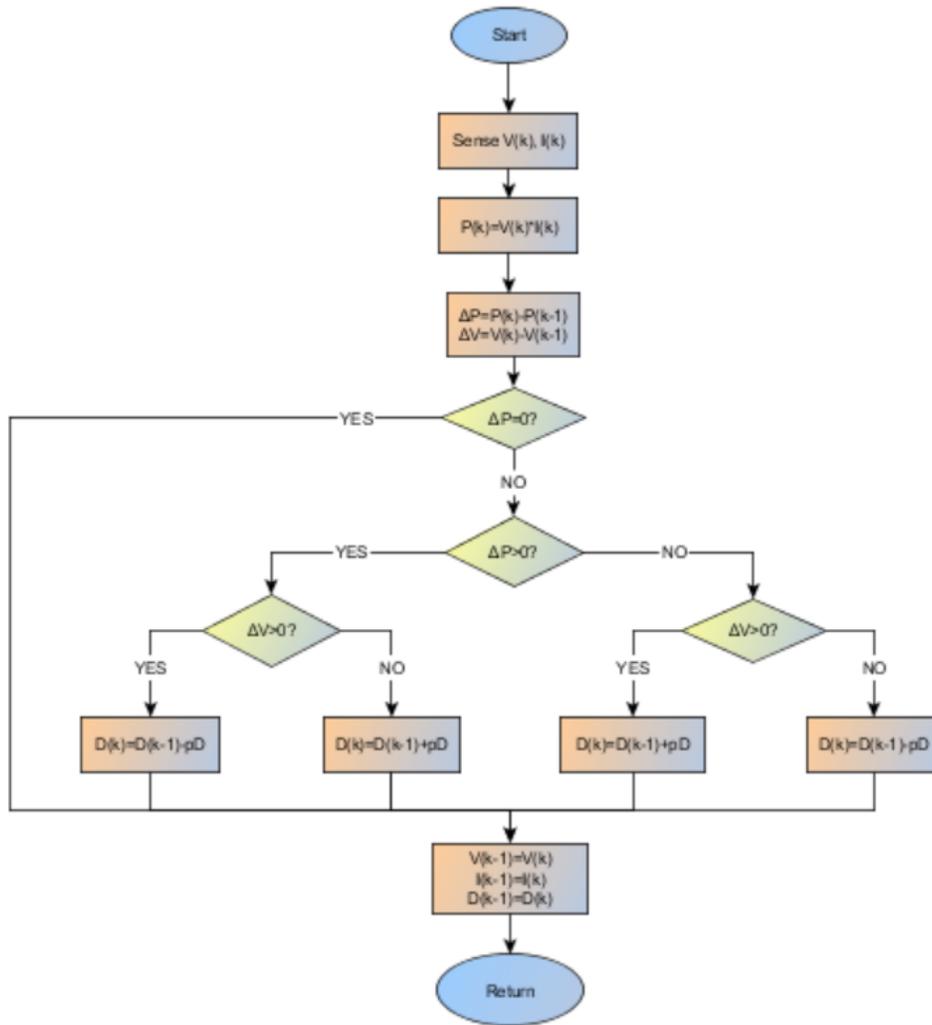


Fig. 5.2.1.1: Perturb and Observe flowchart

A major drawback of the Perturb and Observe method is that at steady state the operating point oscillates around the MPP, fact that causes the waste of some amount of the available energy. Another disadvantage of the method, is that it can fail under rapidly changing weather conditions. A situation that the method possibly fails is depicted in Figure 5.2.1.2 (Esrām & Chapman). Starting from the operating point A, with approximately constant weather conditions, a perturbation in voltage brings the operating point to B and the next perturbation will be reversed due to the fact that the power decreases. However, if the irradiance increases, the power curve will be changed from P_1 to P_2 and the operating point moves from A to C. Then the algorithm detects an increase in the power and the perturbation is kept the same resulting in the diverging of the operating point from the MPP. If the irradiance steadily increases, the operating point will continue diverging from the MPP. Some variations of the algorithm have been proposed by the bibliography for tackling with this problem (Hsiao & Chen,

2002), (Femia, Petrone, Spagnuolo, & Vitelli, 2005), (D'Souza, Lopes, & Liu, 2005), (Xiao & Dunford, 2004).

It should be mentioned here that the algorithm used for the MPPT in this report is described by the flowchart shown in Figure 5.2.1.1.

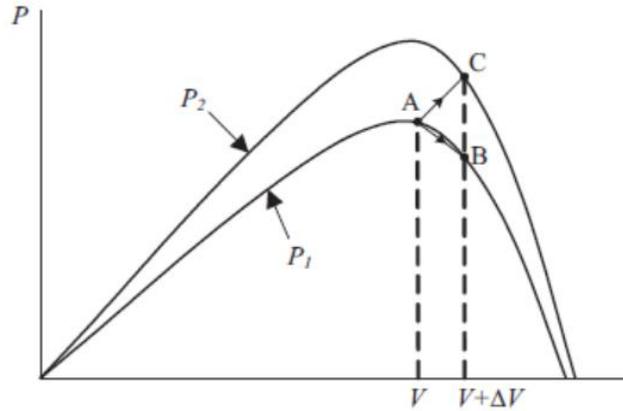


Fig. 5.2.1.2: Diverging of Perturb and Observe from MPP (Esram & Chapman)

5.3 Boost Converter

5.3.1 State-Space Model

As it was explained in the beginning of this chapter, FemtoGrid's power converters are designed to operate in DCM. Therefore, the boost converter is modeled for DCM operation based on its state-space equations. As state variables, the inductor current (i_L) and the capacitor voltage (v_C) were chosen. Input variable is the input voltage (v_{in}). Then, for the three modes of DCM described in Chapter 3, the following equations occur:

$$\begin{aligned} \dot{x} &= A_1x + B_1v_{in} \\ \text{for } t &\in [0, D_1T] \end{aligned} \tag{5.3.1.1}$$

$$\begin{aligned} \dot{x} &= A_2x + B_2v_{in} \\ \text{for } t &\in [D_1T, (D_1+D_2)T] \end{aligned}$$

(5.3.1.2)

$$\dot{x} = A_3x + B_3v_{in}$$

for $t \in [(D_1+D_2)T, T]$

(5.3.1.3)

with $x=[i_L, v_C]^T$.

The state-space equations are obtained by applying the Kirchhoff's voltage law for the inductor voltage and current law for the capacitor current in the circuits of Figures 3.1.1.1.1, 3.1.1.1.2 and 3.1.1.2.1.

Mode 1

$$\frac{di_L}{dt} = \frac{1}{L}v_{in}$$

$$\frac{dv_C}{dt} = \frac{1}{C}\left(-\frac{v_C}{R}\right)$$

Mode 2

$$\frac{di_L}{dt} = \frac{1}{L}(-v_C + v_{in})$$

$$\frac{dv_C}{dt} = \frac{1}{C}\left(i_L - \frac{v_C}{R}\right)$$

Mode 3

$$\frac{di_L}{dt} = 0$$

$$\frac{dv_C}{dt} = -\frac{v_C}{RC}$$

As a result, the state and input matrices are found to be:

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -1/RC \end{bmatrix}$$

$$A_2 = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix}$$

$$A_3 = \begin{bmatrix} 0 & 0 \\ 0 & -1/RC \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}$$

$$B_2 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}$$

$$B_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

5.3.2 Averaged model

The model described above is time dependent, because the converter is a periodic time-variant system due to its switching operation. The state-space averaging method can be used in order to make the model time independent.

According to that method, the state-space averaged model in DCM is given from the following equation:

$$\dot{\bar{x}} = [D_1A_1 + D_2A_2 + (1 - D_1 - D_2)A_3]\bar{x} + [D_1B_1 + D_2B_2 + (1 - D_1 - D_2)B_3]v_{in}$$

The notation \bar{x} is used to denote the average of x over an entire switching cycle.

However, the problem with this approach is that it averages just the matrix parameters and not necessarily the state variables themselves. To avoid this problem, a modified averaged model that would correctly predict the behavior in DCM is used (Sun, Mitchell, Greuel, Krein, & Bass, 2001).

This modified model yields:

$$\dot{\bar{x}} = [D_1A_1 + D_2A_2 + (1 - D_1 - D_2)A_3]M\bar{x} + [D_1B_1 + D_2B_2 + (1 - D_1 - D_2)B_3]v_{in} \quad (5.3.2.1)$$

where $M = \begin{bmatrix} \frac{1}{D_1+D_2} & 0 \\ 0 & 1 \end{bmatrix}$.

Hence the modified averaged model of the boost converter is:

$$\frac{d}{dt} \begin{bmatrix} \bar{i}_L \\ \bar{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{D_2}{L} \\ D_2 & \frac{1}{RC} \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{v}_C \end{bmatrix} + \begin{bmatrix} \frac{D_1 + D_2}{L} \\ 0 \end{bmatrix} v_{in}$$

The duty cycle of the second interval (D_2) is given by making use of the equations (3.1.1.2.3) and (3.1.1.2.4). The duty cycle of the first interval (D_1) is found by applying the Perturb and Observe algorithm.

5.4 Buck Converter

5.4.1 State-Space Model

The buck converter is also modeled for DCM operation and the model is based on its state-space equations. As state variables, the inductor current (i_L) and the capacitor voltage (v_C) were chosen. Input variable is the input voltage (v_{in}). The same general equations (5.3.1.1), (5.3.1.2) and (5.3.1.3) apply for the buck converter.

Using the circuits of Figures 3.2.1.1.1, 3.2.1.1.2 and 3.2.1.2.1 and applying the Kirchoff's laws, the state-space equations of the buck converter in DCM are found to be:

Mode 1

$$\frac{di_L}{dt} = \frac{1}{L}(-v_C + v_{in})$$

$$\frac{dv_C}{dt} = \frac{1}{C}(i_L - \frac{v_C}{R})$$

Mode 2

$$\frac{di_L}{dt} = \frac{1}{L}(-v_C)$$

$$\frac{dv_C}{dt} = \frac{1}{C}(i_L - \frac{v_C}{R})$$

Mode 3

$$\frac{di_L}{dt} = 0$$
$$\frac{dv_C}{dt} = -\frac{v_C}{RC}$$

As a result, the state and input matrices will be:

$$A_1 = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix}$$

$$A_2 = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix}$$

$$A_3 = \begin{bmatrix} 0 & 0 \\ 0 & -1/RC \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}$$

$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$B_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

5.4.2 Averaged model

Similarly to the case of the boost converter, the modified averaged model expressed by equation (5.3.1) is used here as well, for the reasons explained before.

This equation results in the expression for the modified averaged model of the buck converter in DCM.

$$\frac{d}{dt} \begin{bmatrix} \bar{i}_L \\ \bar{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(D_1 + D_2)}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{v}_C \end{bmatrix} + \begin{bmatrix} \frac{D_1}{L} \\ 0 \end{bmatrix} v_i$$

The duty cycle of the second interval (D_2) is given by making use of the equations (3.2.1.2.3) and (3.2.1.2.4). While, the duty cycle of the first interval (D_1) should be determined by a controller.

Note: All the Simulink models are given in the Appendix B.

Chapter 6: Behavior of Electronic Devices under DC and AC Input

As explained in previous chapters, the buck converter will be used for connecting several electronic devices to the $380V_{dc}$ main bus. To this end, it is essential to examine the behavior of the electronic appliances that normally operate with an AC supply, under DC input. It is observed that some phenomena, like high inrush currents, appear when they start-up. Therefore, an inrush current limiter circuit should also be included in order to prevent possible problems caused by these phenomena. Moreover, the behavior of the same appliances under AC input will be discussed in order to make a comparison possible.

Experiments with six loads were done. A television, a monitor, an AC adapter, an energy saving lamp, an incandescent lamp and a LED lamp were the selected power consumers.

6.1 Power Supplies

Although nearly all common electronic equipment and appliances plug directly into wall outlets and draw 230 V AC , in fact, most of their circuitry is designed to operate at a much lower DC voltage. Such electronic equipment includes devices like laptops, monitors, mobile phones, computers, printers, audio/video/digital video disc (DVD) players, lamps, laboratory instruments etc. However, because of the existing infrastructure of the AC electrical grid, an AC/DC energy conversion stage is added to every product. The devices that perform that conversion are called power supplies. The power supplies are located inside the product (internal) or outside (external). The external power supplies are often called “AC adapters”.

Conventional electricity grids that contain renewable energy sources that produce DC, like solar panels, require DC/AC conversion. Additional power conversion stages and therefore conversion losses can be avoided if the main bus is DC. As a result, it would be preferable if the grid used DC instead of AC.

The power supplies for electronic devices can be broadly divided into Linear Power Supplies and Switched-Mode Power Supplies (SMPS). The linear power supplies were the mainstay of power conversion until the late 1970's, when the first commercial SMPS became available. Nowadays, linear power supplies are only used in specific applications requiring extremely low noise or in very low power applications, like audio applications or alarm panels. On the other hand, although more complex, the SMPS have dominated due to the advantages they appear compared to the linear power supplies, i.e.: reduced size and weight and improved efficiency (Bocock, 2007).

Note that incandescent light bulbs do not contain any power supplies. They emit light when a filament wire is heated to a high temperature by an electric current passing through it, until it glows. So, they are just a resistive load.

6.1.1 Linear Power Supplies

The circuit of the linear power supplies can be described by Figure 6.1.1.1. According to that circuit, the 230V AC input is reduced to a low-level AC voltage by the low-frequency (60 Hz) transformer. Then, the AC voltage is rectified by the bridge rectifier and filtered by the filter capacitor. A Series Pass Element (SPE) (usually a transistor that operates in its active region) is employed to provide the necessary regulation. A FEEDBACK & DRIVE block is connected to the output of the SPE to provide feedback and drive signals.

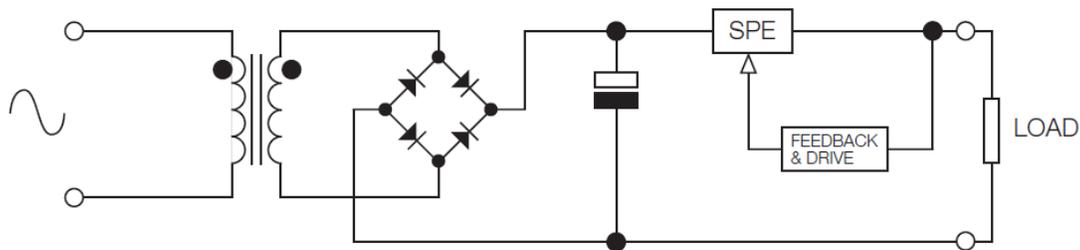


Fig. 6.1.1.1: Linear power supply circuit (Bocock, 2007)

Two are the major features of a linear power supply:

- A low-frequency transformer (60 Hz) is required. These transformers are quite large and heavy.
- There is a significant amount of power loss due to the transistor, resulting in an overall efficiency of 30-60% (Mohan, 2003).

6.1.2 Switched-Mode Power Supplies (SMPS)

Most of the power supplies used by the electronic devices today are SMPS. Figure 6.1.2.1 presents a typical SMPS circuit. This circuit is more complex than the linear power supply circuit and makes use of

DC-DC converters. DC-DC converters employ solid-state devices (transistors, MOSFETs, etc.) which operate as a switch (completely on or off) resulting in lower power dissipation than the linear power supplies (Mohan, 2003). As regards the circuit in Figure 6.1.2.1, L_1 is a common mode choke which is used for preventing electromagnetic interference (EMI) and radio frequency interference (RFI) from the power supply line. R_1 is the lumped equivalent impedance of the common mode choke, bridge rectifier, line cord and wiring. Its value is a few Ohms. The capacitor C_1 is used for EMI filtering and it is usually around $0.1\mu F$. So, it does not store much energy to present much of an inrush current problem. C_2 is a bulk storage capacitor used for smoothening out the DC output of the rectifier. It can be many hundreds of microfarads and can result in a high inrush current.

After the rectification and capacitor filtering of the AC voltage, an unregulated DC voltage appears ($230V_{ac} * \sqrt{2} = 325V_{dc}$) across the DC-DC converter. The DC-DC converter block converts the DC voltage from that level to another that is suitable for the device operation.

It is observed that AC adapters generally show the typical circuit presented in Figure 6.1.2.1 (Allinder, 2005), (Adragna & Gattavari, 2003) (Kraft & Wong, 2007) (16 W xDSL Modem AC-DC Adapter, 2009).

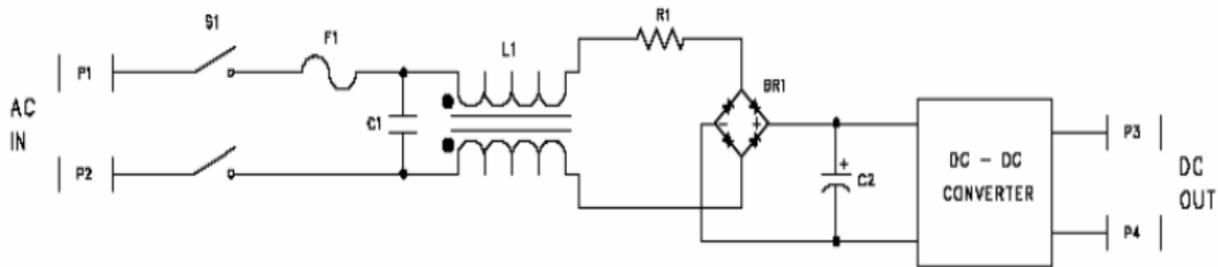


Fig. 6.1.2.1: Switched-mode power supply circuit (Understanding power supplies and inrush current)

SMPS have two major advantages compared to linear power supplies:

- Reduced power losses because the switching elements operate as a switch being completely on or off. Therefore, they appear a higher efficiency, which is in the range of 70-90% (Mohan, 2003).
- Reduced size and weight because they do not use a low-frequency transformer.

6.1.3 Applying DC to Power Supplies

As it was explained before, it would be convenient to implement a DC electricity grid and supply the electronic devices directly with DC power as they finally require DC for their operation. As a result, the question that comes into play is: Are the common electronic devices able to operate properly when supplied with DC instead of AC?

By taking into account the distinction made in the previous sections according to the power supply type each device is equipped with, devices that use SMPS should be able to operate with DC input while the ones that use linear power supplies should not. That is because linear power supplies are built with low-frequency transformers. The transformers require AC in order to create the varying magnetic flux that causes the voltage in the secondary. So, with DC input there is no transfer of energy to the secondary. On the other hand, when SMPS are supplied with DC, the input voltage passes unchanged the rectification stage. The device operates without problem as DC is required. As most of the common electronic devices are equipped with SMPS, they should be able to operate properly when supplied with DC (Dah-Chuan Lu & Agelidis, 2009). The following sections describe experiments that prove this statement.

6.2 Inrush Current

When an electrical device is first turned on, a maximum, instantaneous input current is drawn by the device. This high current is called inrush or surge current. The value of the inrush current can be many times larger than the steady-state current value. The inrush current is caused because of the charging of the input capacitors (C_2) during the initial application of power in most devices and the initially low resistance of the filaments in the case of an incandescent light bulb. If unrestricted, this current can exceed $100A$ at the peak of the AC cycle when the nominal line voltage is $240V_{ac}$ (Understanding power supplies and inrush current). Inrush current is of course also observed when the device is supplied with DC voltage and its value depends on the voltage level.

Figure 6.2.1 shows a simplified current waveform when the power is turned on. As it can be seen, the current begins to flow and reaches a peak value that is larger than the steady-state value. Then, the current starts to decrease until it reaches its steady-state value. The part of the waveform before steady-state is established, is the inrush current. The inrush current is characterized by its magnitude and its duration (settling time).

This high current severely stresses the converter’s fuse, input rectifiers and power switch and it can reduce significantly the reliability and life expectancy of the modules. In order to avoid these problems, some inrush current limiting techniques are adopted.

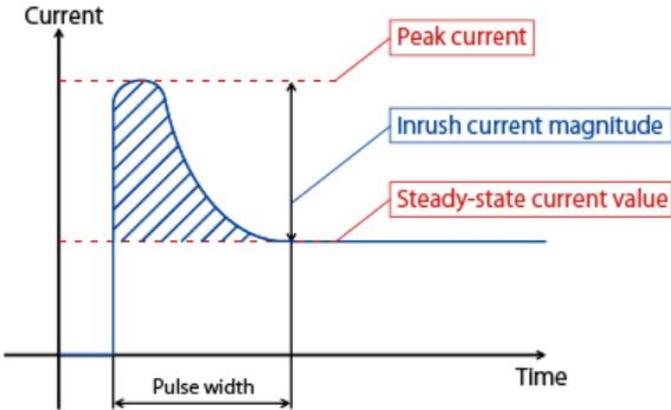


Fig. 6.2.1: Current waveform during the power up of a device

6.3 Experiments with Electronic Devices

6.3.1 DC Input

First, the experiments with the six different loads and DC power supply are discussed, as well as some important conclusions that can be drawn from their analysis.

6.3.1.1 Experimental Setup and Results

The power supply and measuring equipment used in the experiments are listed in Table 6.3.1.1.1. Table 6.3.1.1.2 presents the features of the devices that were tested. Fig. 6.3.1.1.1 displays the implementation of the circuit.

During the experiments, the loads were powered with different DC voltage levels starting from a voltage around $325V_{dc}$, which is the voltage level that corresponds to the $230V_{ac}$ that they normally operate. The voltage was slowly decreased until the level that the device stops its operation. The input current was measured for each voltage level with the help of a multimeter. Moreover, the magnitude and the duration of the inrush current were recorded.

In order to investigate the behavior of the adapter, a variable resistive load was used. The adapter was connected to that load and by changing the load's resistance a power consumption of the nominal $50W$ was achieved. The inrush current was then measured and recorded. Also, the current and voltage in the output were measured and therefore the output power was calculated. Then, the efficiency of the adapter was found by making use of the equation:

$$\eta = \frac{P_{out}}{P_{in}}$$

(6.3.1.1.1)

Table 6.3.1.1.1: Power Supply and Measuring Equipment for DC tests

Type of Equipment	Manufacturer	Model No	Specifications
Power Supply	Agilent Technologies	-	600V/12.6A/1560W
Current Probe	Yokogawa	PCB050	-
Differential Probe	Yokogawa	700924	-
Oscilloscope	Yokogawa	DLM2034	2.5GS/s 350MHz
Multimeter	Fluke	289	-
Photodiode	Vishay	BPW34	-

Table 6.3.1.1.2: Tested Devices for DC tests

Type of Device	Manufacturer	Model No	Specifications
Television	FINLUX	CT1408T	230V/50Hz/60W
Monitor	Iiyama	PLE 431S-S1S	12V/3.5A/42W
Adapter	TPV Electronics	ADPC12416AW	Inp:100-240V/~1.5A/50-60Hz Out:12V/4.16A
Energy Saving Lamp	-	-	220-240V/11W
Incandescent Lamp	Philips	-	230V/40W
LED Lamp	Philips	E27A60	220-240V/8W

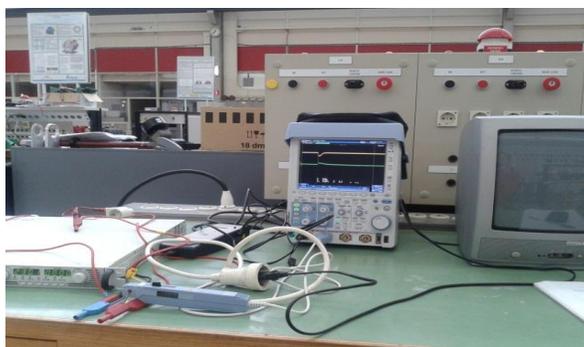


Fig. 6.3.1.1.1: Testing devices with DC voltage

The obtained measurements for the six different loads are tabulated in the Tables 6.3.1.1.3-6.3.1.1.8. Figures 6.3.1.1.2 a-g present the characteristic waveforms for the input voltage and current of the six devices for some voltage levels. In these figures the inrush current can be observed.

Figure 6.3.1.1.2.b explains what is measured as Δt .

Table 6.3.1.1.3: Television measurements with DC input

V(V)	Normal Operation		Standby Operation		Inrush Current	
	I(A)	P(W)	I _{standby} (A)	P _{standby} (W)	I _{max} (A)	Δt (ms)
125	0.418	52.25	0.023	2.85	6.9	2.65
130	0.400	52.00	0.023	2.99	9.1	3.00
140	0.370	51.80	0.022	3.08	11.8	4.50
150	0.341	51.15	0.022	3.30	10.6	4.00
180	0.284	51.12	0.025	4.50	14.9	4.50
200	0.255	51.00	0.018	3.60	12.4	2.90
230	0.220	50.60	0.015	3.45	21.9	3.30
250	0.203	50.75	0.015	3.75	22.4	4.20
325	0.156	50.70	0.013	4.23	31.5	3.04
400	0.130	52.00	0.012	4.80	39.8	9.24

Table 6.3.1.1.4: Monitor measurements with DC input

V(V)	Normal Operation		Standby Operation		Inrush Current	
	I(A)	P(W)	I _{standby} (A)	P _{standby} (W)	I _{max} (A)	Δt (ms)
60	0.470	28.2	0.030	1.80	6.1	2.75
70	0.390	27.3	0.025	1.75	6.0	2.70
80	0.330	26.4	0.025	2.00	7.5	3.25
100	0.267	26.7	0.021	2.10	9.6	3.10
150	0.170	25.5	0.015	2.25	14.1	3.40
200	0.130	26.0	0.013	2.60	19.4	2.70
240	0.111	26.6	0.012	2.88	22.5	3.35
325	0.082	26.7	0.012	3.90	33.0	2.55

Table 6.3.1.1.5: Adapter measurements with DC input

Input							Output			
Normal Operation		Standby Operation		Inrush Current		Normal Operation				
V _{in} (V)	I _{in} (A)	P _{in} (W)	I _{standby} (A)	P _{standby} (W)	I _{max} (A)	Δt(ms)	V _{out} (V)	I _{out} (A)	P _{out} (W)	η (%)
75	0.667	50	0.010	0.75	7.90	1.97	11.420	3.644	41.84	83.68
80	0.625	50	0.009	0.72	7.56	2.06	11.379	3.540	40.28	80.56
100	0.500	50	0.009	0.90	7.56	4.10	11.417	3.576	40.83	81.66
150	0.330	50	0.007	1.05	7.56	3.35	11.369	3.664	41.66	83.32
200	0.250	50	0.007	1.40	7.90	2.25	11.416	3.681	42.02	84.04
230	0.217	50	0.007	1.61	8.34	2.27	11.322	3.654	41.37	82.74
325	0.153	50	0.007	2.28	8.34	2.90	11.417	3.597	41.07	82.14

Table 6.3.1.1.6: Energy saving lamp measurements with DC input

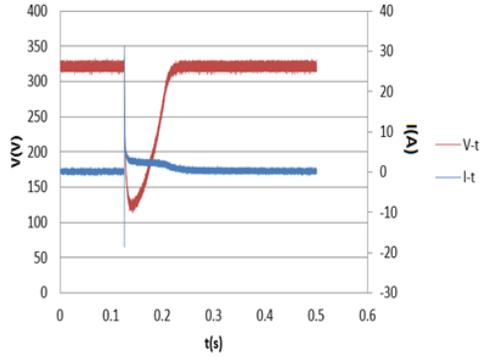
Normal Operation			Inrush Current	
V(V)	I(A)	P(W)	I _{max} (A)	Δt(μs)
70	0.045	3.15	3.3	111
80	0.043	3.44	4.5	123
90	0.040	3.60	4.8	118
100	0.038	3.80	5.4	115
150	0.033	4.95	7.2	133
200	0.033	6.60	9.3	129
230	0.032	7.36	10.5	147
325	0.030	9.75	16.8	181

Table 6.3.1.1.7: Incandescent lamp measurements with DC input

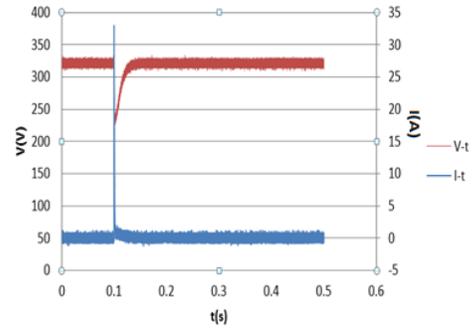
Normal Operation			Inrush Current	
V(V)	I(A)	P(W)	I _{max} (A)	Δt(ms)
40	0.078	3.12	0.362	8.17
50	0.085	4.25	0.463	8.73
60	0.091	5.46	0.567	8.43
70	0.098	6.86	0.679	7.81
80	0.104	8.32	0.780	7.85
100	0.116	11.60	1.010	7.98
150	0.142	21.30	1.520	4.78
200	0.164	32.80	2.020	3.57
230	0.176	40.48	2.370	3.97
325	0.212	68.90	2.840	3.80

Table 6.3.1.1.8: LED lamp measurements with DC input

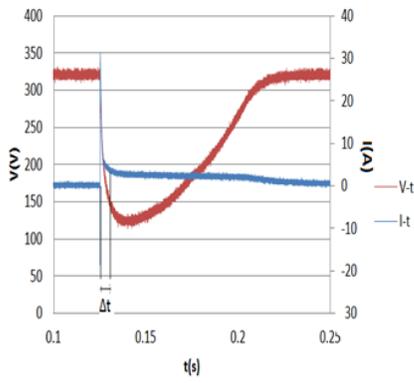
Normal Operation			Inrush Current	
V(V)	I(A)	P(W)	I _{max} (A)	Δt(ms)
50	0.023	1.150	0.23	1.500
60	0.002	0.138	0.32	1.510
70	0.002	0.140	0.38	1.485
80	0.002	0.128	0.46	1.410
100	0.004	0.370	0.80	1.145
150	0.033	4.950	1.12	1.155
180	0.038	6.840	1.20	1.150
200	0.038	7.600	1.46	1.147
230	0.035	8.050	1.71	1.435
325	0.030	9.750	3.03	1.145



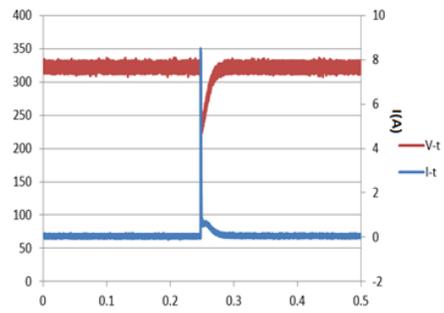
a. Input voltage and current waveforms of television with voltage supply of $325V_{dc}$.



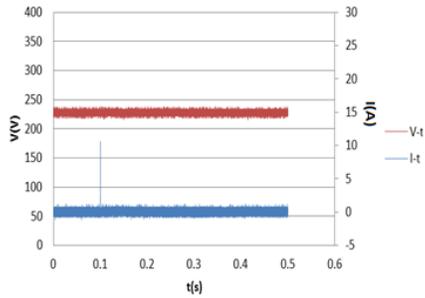
c. Input voltage and current waveforms of monitor with voltage supply of $325V_{dc}$.



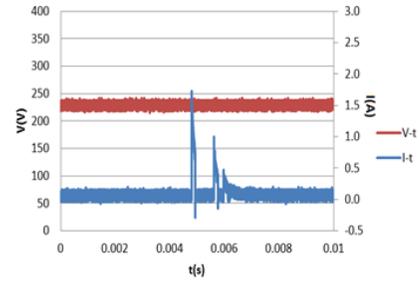
b. Zoom in of input voltage and current waveforms of television with voltage supply of $325V_{dc}$.



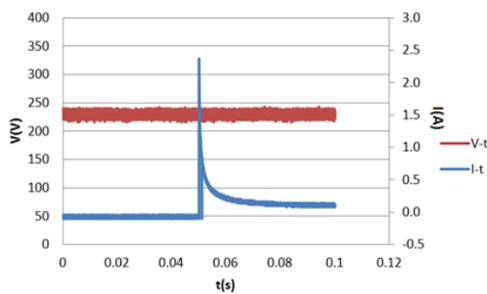
d. Input voltage and current waveforms of adapter with voltage supply of $325V_{dc}$.



e. Input voltage and current waveforms of energy saving lamp with voltage supply of $230V_{dc}$.



g. Input voltage and current waveforms of LED lamp with voltage supply of $230V_{dc}$.



f. Input voltage and current waveforms of incandescent lamp with voltage supply of $230V_{dc}$.

Fig. 6.3.1.1.2: Input voltage and current waveforms of the tested devices

Moreover, the efficiency of light emission of the lamps for different voltage levels was investigated. The experimental setup includes the photodiode described in Table 6.3.1.1.1 connected to an ammeter. The lamp was connected to a power supply and placed close to the photodiode. By shorting the photodiode's terminals, a photocurrent proportional to light intensity flows and can be measured by the ammeter. As shown in Figure 6.3.1.1.3, the short circuit current I_{sh} is extremely linear to the amount of incident light. The achievable range of linearity is 6 to 8 orders of magnitude, depending on the type of photodiode and circuit in which it is used (Corn). Therefore, the efficiency of light emission of the lamp can be found by dividing the photodiode's current values for the different voltage levels by the reference value. As reference value here is taken to be the short circuit current value for $325V_{dc}$ (that corresponds to the $230V_{ac}$ after rectification and capacitor filtering) for the energy saving and the LED lamps and the short circuit current value for $230V_{dc}$ for the incandescent lamp, as this lamp does not include a rectification stage (it is just a resistive load).

The Tables 6.3.1.1.9, 6.3.1.1.10 and 6.3.1.1.11 present the measured short circuit currents and calculated light emission efficiencies for the different voltage levels for the energy saving, the incandescent and the LED lamps respectively.

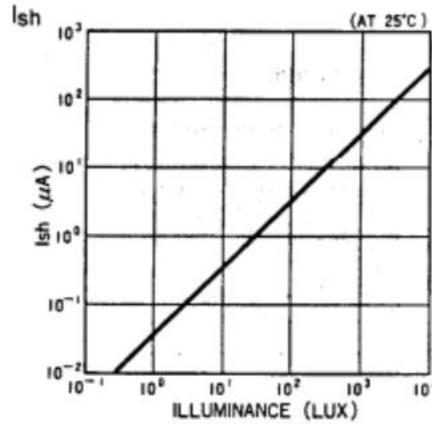


Fig. 6.3.1.1.3: Short circuit current vs illuminance of a photodiode (Corn)

Table 6.3.1.1.9: Light emission efficiency of energy saving lamp with DC input

V(V)	I _{sh} (μA)	η(%)
70	10.1	16.7
80	13.8	22.8
90	16.7	27.6
100	21.3	35.2
150	36.6	60.5
200	47.6	78.7
230	52.2	86.3
325	60.5	100.0

Table 6.3.1.1.10: Light emission efficiency of incandescent lamp with DC input

V(V)	I _{sh} (μA)	η(%)
40	1.3	0.18
50	3	0.41
60	6.8	0.93
70	13.4	1.84
80	23.3	3.2
100	55.7	7.7
150	216.9	29.8
200	500.4	68.7
230	727.4	100.0

Table 6.3.1.1.11: Light emission efficiency of LED lamp with DC input

V(V)	$I_{sh}(A)$	$\eta(\%)$
50	0.4	0.34
60	2	1.70
70	2.4	2.04
80	2.6	2.21
100	4.6	3.91
150	72.9	62.0
180	94.4	80.3
200	101.3	86.1
230	106.1	90.2
325	117.6	100.0

Note that the photodiode's current values given in the tables are the measured values after subtracting the current value that the ammeter displays when the lamp is off. By doing this, the influence of the ambient light is limited.

It should also be noted that all the measurements are subjected to inaccuracies because of several reasons. First of all, the waiting time between two measurements probably was not enough for the capacitor to get fully discharged in some cases. This results in a lower magnitude and duration of inrush current than the real ones. Another important factor is the observation error. Especially for the duration of the inrush current, the measurement cannot be completely precise as it was found by observing the current waveform in the oscilloscope. Finally, there are some errors because of the accuracy and the limitations of the measuring instruments.

6.3.1.2 Conclusions

Table 6.3.1.2.1: Results of DC measurements

	Minimum DC Voltage required for device operation (V)	Normal Operation Power Consumption (W)	Standby Operation Power Consumption (W)	Steady-state current at 325V (A)	Maximum Inrush Current (A)	Inrush Current Settling time (ms)	Efficiency (%)
Television	125	50.6-52.25	2.85-4.8	0.156	32	4	-
Monitor	60	25.5-28.2	1.8-3.9	0.082	33	3	-
Adapter	75	50	0.72-2.28	0.153	8.3	3	80.6-84
Energy Saving Lamp	-	9.75 (at full light emission)	-	0.03	17	0.18	-
Incandescent Lamp	-	40.48 (at full light emission)	-	0.212	3	8	-
LED Lamp	-	9.75 (at full light emission)	-	0.03	3	1.5	-

The table above summarizes the results taken from the measurements. Particularly, it presents the voltages the devices start to operate, the devices' power consumption in normal operation conditions and in standby operation conditions, the steady-state current at 325V, the maximum inrush current that can occur (at 325V), the inrush current settling time and the adapter's efficiency.

As it was observed, the inrush current can be many times higher than the steady state current. That is around 200 times higher for the television, 400 for the monitor, 55 for the adapter, 560 for the energy saving lamp, 13 for the incandescent lamp (this is not so high because the incandescent lamp does not contain an input capacitor, it is just a resistance) and 100 for the LED lamp.

The inrush current settling time is generally some ms, while in the case of the energy saving lamp it is in the order of a hundred of μ s.

The high inrush current leads to a voltage drop when the input voltage is relatively high (>200V), in the case of the monitor, the adapter and especially the television. This voltage drop gets higher as the inrush current becomes higher. When the input voltage is 325V, the voltage drop of the television is 210V and of the monitor and the adapter is 100V.

Finally, the light emission efficiency of the three lamps is plotted as a function of the input voltage and as a function of the input power, as shown in Figures 6.3.1.2.1 and 6.3.1.2.2 respectively.

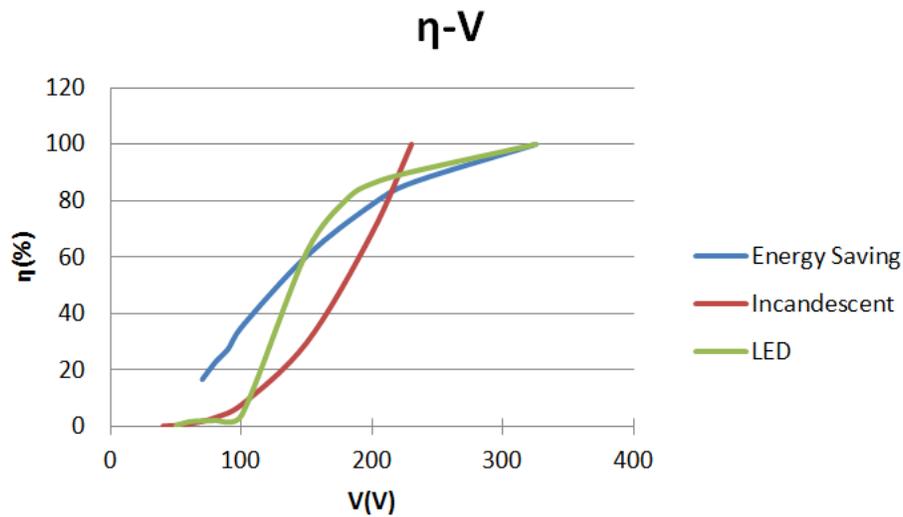


Fig. 6.3.1.2.1: Light emission efficiency versus input voltage of the three lamps with DC input

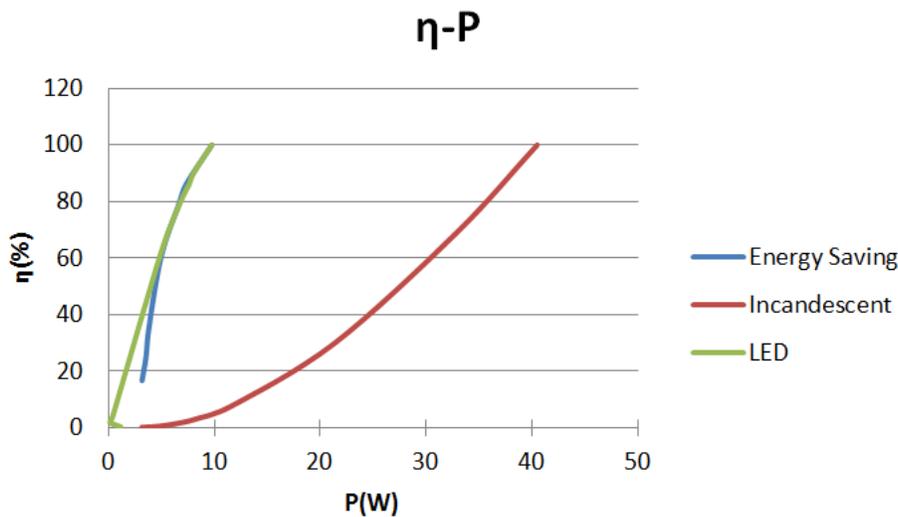


Fig. 6.3.1.2.2: Light emission efficiency versus power consumption of the three lamps with DC input

As it can be seen from the Figure 6.3.1.2.1, the LED lamp keeps a high light emission efficiency for a wide range of input voltages. For voltages higher than 180V, the light emission efficiency is more than 80%. However, if the voltage drops below 150V, the light emission efficiency decreases rapidly. The energy saving lamp has high efficiency for a narrower voltage range than the LED lamp, while for low voltages

its performance is better than the LED lamp. On the other hand, the light emission efficiency of the incandescent lamp drops immediately with the voltage decrease.

As far as the power consumption is concerned, the LED lamp and the energy saving lamp appear similar behavior, according to Figure 6.3.1.2.2. The incandescent lamp seems to consume much more power than the other two lamps. For full light emission the power consumption of the incandescent lamp is around $40W$, while of the energy saving lamp and the LED lamp is $9.75W$.

All in all, the LED lamp appears the best performance and should be preferred, however the input voltage should be kept quite high in order to secure good light emission.

6.3.2 AC Input

In this section, the experiments executed with an AC input power supply are presented as well as some conclusions based on the results.

6.3.2.1 Experimental Setup and Results

Besides the tests described in section 6.3.1, also tests with AC voltage supply were done, fact that makes it possible to compare the behavior of the different devices under DC and AC voltage. The equipment used for the experimental setup is described by Table 6.3.2.1.1.

A variable transformer (VARIAC), connected to the device under test, supplied the device with different voltage levels. Starting from around $230V_{ac}$, the voltage was decreased until the level that the device stops its operation. For each voltage level, the input current, the power factor and the power consumed were measured with the help of a power-meter and recorded. The devices used here are the same devices used for the DC tests (Table 6.3.1.1.2).

In order to test the adapter, similarly to the DC tests, that was connected to a variable resistive load and by changing the resistance, $50W$ power consumption was achieved. Then the input current and power factor were measured. Also, the output voltage and current were recorded and the efficiency was calculated according to the equation 6.3.1.1.1.

Table 6.3.2.1.1: Measuring equipment for AC tests

Type	Manufacturer	Model no	Specifications
VARIAC	-	2422530	U_p : KM 220V 50-400Hz U_s : KT 0-260V
Power-meter	Elcontrol	Nanovip Plus SN 27761	-
Current clamp	Elcontrol	MN13-EL	200A/1V Out: 30V
Multi-meter	Fluke	289	-
Photodiode	Vishay	BPW34	-

The measurements for the television, monitor, adapter, energy saving lamp, incandescent lamp and LED lamp are tabulated in the Tables 6.3.2.1.2-6.3.2.1.7 respectively.

Table 6.3.2.1.2: Television measurements with AC input

V(V)	Normal Operation			Standby Operation		
	I(A)	P(W)	$\cos\phi$	I_{standby} (A)	P_{standby} (W)	$\cos\phi_{\text{standby}}$
120	0.620	56.50	-0.75	0.042	3.14	-0.62
130	0.588	56.25	-0.74	0.040	3.21	-0.61
140	0.543	55.25	-0.73	0.039	3.19	-0.59
150	0.510	55.50	-0.72	0.038	3.26	-0.58
180	0.440	55.00	-0.69	0.035	3.28	-0.52
200	0.403	55.00	-0.68	0.034	3.31	-0.49
230	0.365	55.25	-0.65	0.033	3.39	-0.44
240	0.348	54.50	-0.66	0.032	3.48	-0.46

Table 6.3.2.1.3: Monitor measurements with AC input

V(V)	Normal Operation			Standby Operation		
	I(A)	P(W)	$\cos\phi$	I_{standby} (A)	P_{standby} (W)	$\cos\phi$
50	0.934	33.2	-0.70	0.062	2.02	-0.65
60	0.720	31.4	-0.72	0.054	1.98	-0.63
70	0.588	30.2	-0.72	0.044	1.79	-0.59
80	0.530	29.8	-0.70	0.044	1.98	-0.56
100	0.418	29.0	-0.68	0.034	1.85	-0.53
150	0.298	28.4	-0.62	0.032	2.01	-0.44
180	0.256	28.0	-0.61	0.031	2.10	-0.34
200	0.234	28.4	-0.60	0.031	2.19	-0.37
230	0.206	29.2	-0.57	0.034	2.35	-0.29
240	0.204	28.8	-0.58	0.035	2.48	-0.30

Table 6.3.2.1.4: Adapter measurements with AC input

Input				Output			
$V_{in}(V)$	$I_{in}(A)$	$P_{in}(W)$	$\cos\phi$	$V_{out}(V)$	$I_{out}(A)$	$P_{out}(W)$	$\eta(\%)$
70	1.100	50	-0.65	11.524	3.045	35.09	70.18
80	0.940	50	-0.65	11.519	3.306	38.08	76.16
90	0.840	50	-0.67	11.484	3.359	38.57	77.14
100	0.763	50	-0.66	11.472	3.419	39.22	78.44
150	0.533	50	-0.63	11.480	3.421	39.27	78.54
180	0.450	50	-0.61	11.485	3.451	39.63	79.26
200	0.425	50	-0.59	11.475	3.461	39.71	79.42
230	0.365	50	-0.59	11.492	3.284	37.74	75.48
240	0.360	50	-0.58	11.497	3.258	37.46	74.92

Table 6.3.2.1.5: Energy saving lamp measurements with AC input

$V(V)$	$I(A)$	$P(W)$	$\cos\phi$
70	0.054	2.67	-0.70
80	0.057	3.17	-0.68
90	0.057	3.51	-0.67
100	0.058	3.85	-0.67
150	0.059	5.85	-0.65
200	0.064	8.06	-0.63
230	0.062	8.69	-0.60
240	0.063	9.25	-0.61

Table 6.3.2.1.6: Incandescent lamp measurements with AC input

$V(V)$	$I(A)$	$P(W)$	$\cos\phi$
50	0.082	4.14	1
60	0.087	5.30	1
70	0.094	6.58	1
80	0.010	8.04	1
90	0.106	9.52	1
100	0.111	11.14	1
150	0.138	20.80	1
180	0.154	28.00	1
200	0.162	32.20	1
230	0.174	40.00	1
240	0.180	43.40	1

Table 6.3.2.1.7: LED lamp measurements with AC input

V(V)	I(A)	P(W)	cos ϕ
150	0.030	3.36	-0.74
180	0.038	4.71	-0.70
200	0.040	5.26	-0.66
230	0.042	6.25	-0.65
240	0.041	6.28	-0.65

Note that measurements for the LED lamp with input voltage lower than 150V couldn't be recorded because the power-meter was not able to detect so small currents. The same happens with the adapter measurements for standby operation.

It should be mentioned that the minus sign in the power factor of the television, the monitor, the adapter, the energy saving lamp and the LED lamp indicates that the current is lagging the voltage. The power factor of the incandescent lamp is 1 because this lamp is a completely resistive load.

Similarly to the case of the DC input described in the previous section, the light emission efficiency of the lamps can be calculated from the photodiode's short circuit current. The same experimental setup was used here. As explained before, the short circuit current I_{sh} is extremely linear to the amount of incident light. The reference current value now is the value that corresponds to 230V_{ac}. The results are presented in the Tables below.

Table 6.3.2.1.8: Light emission efficiency of energy saving lamp with AC input

V(V)	$I_{sh}(\mu A)$	$\eta(\%)$
70	11.3	19.1
80	13.8	23.3
90	17.6	29.7
100	20.7	35.0
150	37.2	62.8
200	49.2	83.1
230	59.2	100.0

Table 6.3.2.1.9: Light emission efficiency of incandescent lamp with AC input

V(V)	$I_{sh}(\mu A)$	$\eta(\%)$
50	2.5	0.4
60	4.5	0.8
70	9.5	1.6
80	18.5	3.1
90	31.5	5.3
100	46.5	7.9
150	178.5	30.2
180	308.5	52.2
200	407.5	68.9
230	591.5	100.0

Table 6.3.2.1.10: Light emission efficiency of LED lamp with AC input

V(V)	$I_{sh}(\mu A)$	$\eta(\%)$
70	0.3	0.2
80	1.8	1.3
90	6.7	4.9
100	7.6	5.6
150	77.6	56.9
180	110.5	81.1
200	121.7	89.3
230	136.3	100.0

Note that the photodiode's current values given in the tables are the measured values after subtracting the current value that the ammeter displays when the lamp is off. By doing this, the influence of the ambient light is limited.

Likewise to the case of DC measurements, the AC measurements are also subjected to inaccuracies because of several reasons, like the observation error and the limited measuring instruments accuracy.

6.3.2.2 Conclusions

Table 6.3.2.2.1: Results of AC measurements

	Minimum AC Voltage required for device operation (V)	Normal Operation Power Consumption (W)	Standby Operation Power Consumption (W)	Efficiency (%)
Television	120	54.5-56.5	3.14-3.48	-
Monitor	50	28-33.2	1.79-2.48	-
Adapter	70	50	-	70.1-79.4
Energy Saving Lamp	-	8.69 (at full light emission)	-	-
Incandescent Lamp	-	40 (at full light emission)	-	-
LED Lamp	-	6.25 (at full light emission)	-	-

The table above summarizes the results taken from the AC measurements. It presents the voltages that the devices start to operate, the devices' power consumption in normal operation conditions and in standby operation conditions and the adapter's efficiency.

Finally, the light emission efficiency of the three lamps is plotted as a function of the input voltage and the power consumption based on the measurements of the lamps. The corresponding graphs are shown in the Figures 6.3.2.2.1 and 6.3.2.2.2.

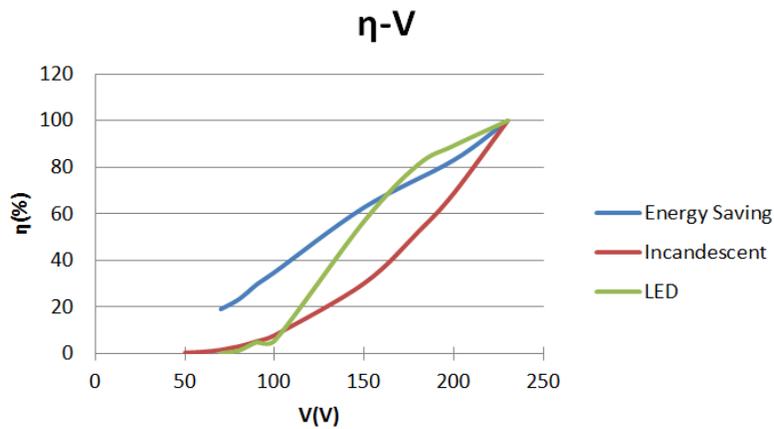


Fig. 6.3.2.2.1: Light emission efficiency versus input voltage

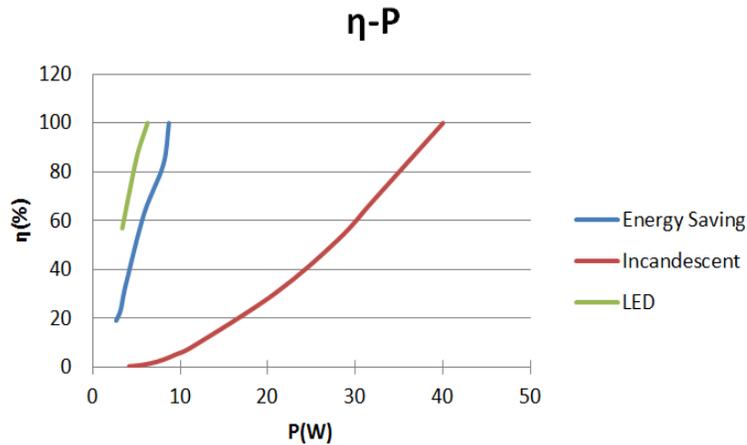


Fig. 6.3.2.2.2: Light emission efficiency versus power consumption

From the Figure 6.3.2.2.1, it can be seen that the LED lamp has a high light emission efficiency (>80%) for input voltages higher than 180V. If the input voltage drops below 150V, the light emission efficiency decreases sharply. As regards the light emission efficiency of the energy saving lamp, it decreases rather linearly when the input voltage decreases. For high voltages, that is lower than the LED's light emission efficiency, while for lower voltages it remains higher. Finally, the light emission efficiency of the incandescent lamp, drops rapidly.

As it is observed from the Figure 6.3.2.2.2, the LED lamp has the lowest power consumption compared to the other two lamps, while the incandescent lamp has by far the highest power consumption. For full light emission, the LED lamp consumes 6.25W, the energy saving lamp 8.7W and the incandescent lamp 40W.

All in all, the LED lamp appears the best performance in terms of light emission efficiency and power consumption and should be preferred. The input voltage should be kept rather high in order to get good light emission.

6.3.3 Comparison of Devices' Behavior under DC and AC

The following table compares the behavior of the tested devices when supplied with DC and AC power. It presents, both for DC and AC input, the minimum required voltage for the device operation, the normal and standby operation power consumption and the efficiency of the adapter. Finally, the maximum possible energy saving for the several devices and efficiency gain for the adapter are calculated for normal and standby operation.

Table 6.3.3.1: Comparison table for devices with DC and AC input

	Min Voltage required for device operation (V)		Normal Operation Power Consumption (W)		Standby Operation Power Consumption (W)		Efficiency (%)		Max Energy Saving with DC input/ Efficiency gain for adapter (%)	
	DC input	AC input	DC input	AC input	DC input	AC input	DC input	AC input	Normal Operation	Standby Operation
Television	125	120	50.6-52.25	54.5-56.5	2.85-4.8	3.14-3.48	-	-	10.4	18.1
Monitor	60	50	25.5-28.2	28-33.2	1.8-3.9	1.79-2.48	-	-	23.2	27.4
Adapter	75	70	50	50	0.72-2.28	-	80.6-84	70.1-79.4	13.9	-

As it can be seen from the table 6.3.3.1, energy can be saved if the television, monitor and adapter are supplied with DC instead of AC as these devices appear a lower power consumption in that case. This advantageous behavior of the devices under DC voltage is due to the less power conversion stages (the rectification stage is skipped) and therefore smaller power losses the loads appear when supplied with DC.

It should also be mentioned that the LED lamps appear to have the best performance compared to the other two lamps for both the DC and AC measurements, as they have the highest light emission efficiency and the least power consumption.

Note

Surprisingly, according to the measurements, the lamps appear less power consumption with AC than with DC input (Tables 6.3.1.2.1, 6.3.2.2.1). LED lamps and energy saving lamps are expected to consume

less power when supplied with DC, just like the other devices, as they are native users of DC power. It should be kept in mind that for the AC measurements, a power-meter was used. However, because the current level (around $40mA$ for LED) was below the instrument's detection level, many cable turns were made (14 turns). Probably, the measurements taken by the power-meter were not accurate enough, as the full range of measurement of the current coil of the power-meter is $200A$ and a lot of inaccuracy is added while trying to measure $0.5A$ with it, so a repetition of the experiments with a power-meter of a lower range is recommended.

Chapter 7: Design of Buck Converter

In this chapter some high efficiency buck converter topologies are discussed. In particular, their advantages/disadvantages, their operation, characteristic waveforms and simulation and experimental results presented in the literature, are explained. Finally, one of these topologies is selected for the design of the buck converter.

7.1 Buck Converter Topologies

A literature study was performed in order to choose the buck converter topology that will be used for the construction of the required converter. The prospective topology should fulfill the following criteria:

- it should be isolated, so that operation of the rest system is secured in the case that there is a fault in the load side, also safety is guaranteed
- it should have high efficiency (>95%)
- it should make use of as small number of components as possible, so it has small power losses, it is cheap and has reduced size

Based on these criteria, four topologies were chosen as the predominant ones and are described here.

7.1.1 LLC Resonant Converter

The LLC resonant converter can be implemented as shown in Figure 7.1.1.1 (Yang, Lee, Zhang, & Guisong, 2002). It consists of three passive components, i.e.: L_r , C_r and L_m . The secondary side is a center-tapped rectifier followed by a capacitive filter. The primary side is a Half-Bridge configuration in this case, but it could also be Full-Bridge or other topologies.

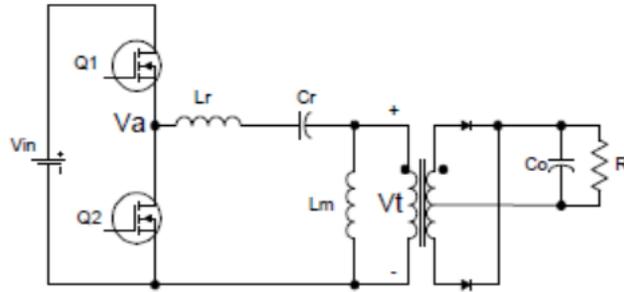


Fig. 7.1.1.1: LLC resonant converter (Yang, Lee, Zhang, & Guisong, 2002)

This kind of converter is normally used as the front-end DC/DC converter of Distributed Power Systems (DPS), which converts the $400V_{dc}$ to an isolated $48V_{dc}$. The most popular power level for this converter is $1kW$.

The LLC resonant converter has some important advantages:

- Zero Voltage Switching (ZVS) capability for zero to full load range and low MOSFET turn off current, therefore the switching losses are very low
- High efficiency for input voltages of $300V-400V$
- Low voltage stress on secondary rectifier as there is no secondary filter inductor
- The magnetic components can be integrated into one magnetic core easily and leakage inductance can be utilized.

It is important to mention that this circuit has two resonant frequencies:

$$f_1 = \frac{1}{2\pi\sqrt{L_r C_r}}$$

$$f_2 = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}$$

Figure 7.1.1.2 presents the DC characteristic of the LLC resonant converter. Q_s is given by the equation:

$$Q_s = \frac{\sqrt{L_r/C_r}}{R_l}$$

As a result, Q_s changes with the load variation. As it can be seen from the figure, the peak of the voltage gain moves when the load changes. For lighter load it moves towards f_2 , while for heavier load it moves towards f_1 . When the switching frequency is around f_1 , the gain is independent of the load and the voltage ratio is:

$$\frac{V_o}{V_{in}} = \frac{1}{2n}$$

where n is the transformer's turn ratio.

Additionally, it can be observed that the converter can operate either as buck or as boost converter, depending on the gain.

Therefore, the voltage gain depends on the load and the switching frequency as shown in Figure 7.1.1.2.

Furthermore, the load condition and the switching frequency will determine if the converter will operate at Zero Current Switching (ZCS) condition or ZVS condition.

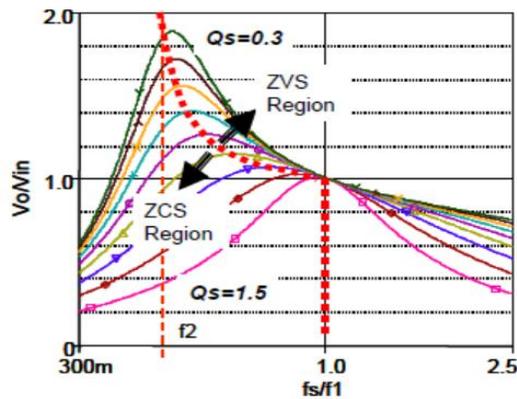


Fig. 7.1.1.2: DC characteristic of LLC Resonant Converter (Yang, Lee, Zhang, & Guisong, 2002)

In the paper (Yang, Lee, Zhang, & Guisong, 2002), it is assumed that the switching frequency is between f_1 and f_2 and ZVS is achieved. Figure 7.1.1.3 presents the waveforms of the resonant tank input voltage V_o , the series resonant inductor current I_{Lr} , the magnetizing inductor current I_{Lm} , the output current I_o and the transformer primary voltage V_t .

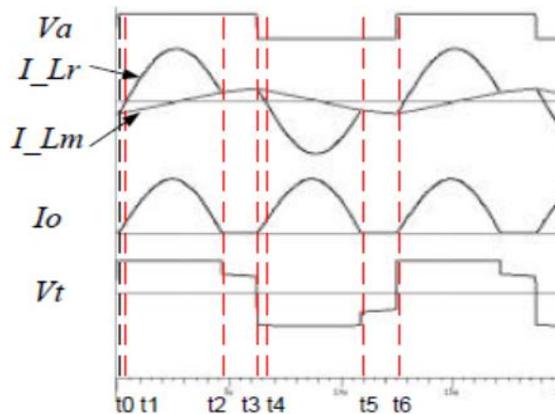


Fig. 7.1.1.3: Characteristic waveforms of LLC Resonant Converter (Yang, Lee, Zhang, & Guisong, 2002)

The operation of half switching cycle is described. The next half cycle is similar to the first one. The half switching cycle can be divided into three modes, which are depicted in Figure 7.1.1.4.

Mode 1 (t_0-t_1)

At t_0 , Q_2 is turned off. The negative resonant inductor current (I_{L_r}) flows through the body diode of Q_1 and creates a ZVS condition for Q_1 . While I_{L_r} flows through that body diode, it starts to rise. This forces the secondary diode D_1 to conduct and I_o begins to increase. The transformer sees an output voltage on the secondary side, while L_m is being charged with constant voltage.

Mode 2 (t_1-t_2)

This mode begins when the resonant inductor current becomes positive. Q_1 is on during this mode and D_1 conducts. The transformer voltage is clamped to V_o and L_m is linearly charged with output voltage, so it doesn't participate resonant. This mode ends when L_r current becomes equal to L_m current and I_o becomes zero.

Mode 3 (t_2-t_3)

During this operation mode, the two inductor currents (I_{L_r} and I_{L_m}) are equal and the output current is zero. The diodes D_1 and D_2 are reverse biased. The transformer secondary voltage is lower than the output voltage. During this mode, L_m is freed to participate resonant, so it forms a resonant tank in series with L_r and C_r . The mode ends when Q_1 is turned off.

From the waveforms, it can be seen that ZVS is achieved with this converter and this can be done for any load condition. Also, the turn off current of the switches is much smaller than the load current and therefore turn off losses can be reduced. All in all, the switching loss of this converter is very small.

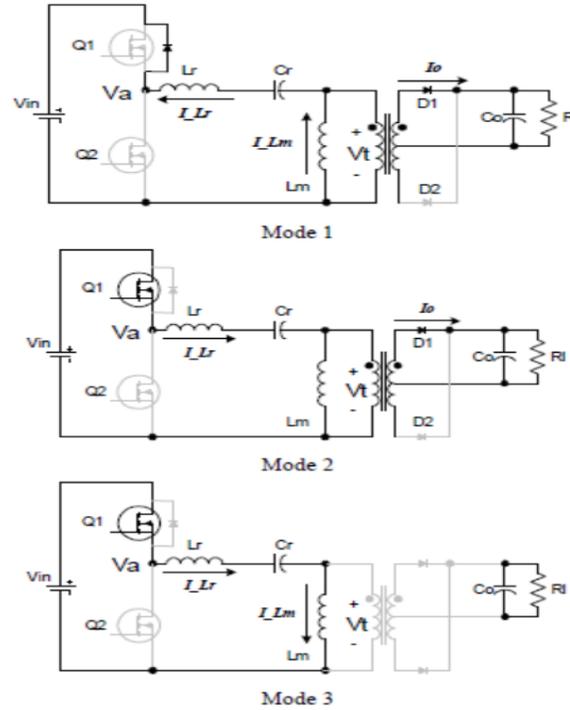


Fig. 7.1.1.4: Operating modes of LLC resonant converter (Yang, Lee, Zhang, & Guisong, 2002)

The paper also presents the simulation results of an LLC resonant converter with the specifications shown in Table 7.1.1.1.

Table 7.1.1.1: LLC resonant converter parameters

Parameter	Value
V_{in}	300-400V
V_{out}	48V
P_{out}	1kW
Switching frequency	150-200kHz
Primary switches	IXFN26N50 500V 21A MOSFET
Diodes	IXYSS20-015A 150V Schottky diode with forward voltage drop 0.65V
L_r	14 μ H
C_r	0.056 μ F
L_m	60 μ H
Transformer's turns ratio	16:4

The simulations revealed important information about the efficiency of this converter. Table 7.1.1.2 presents the loss breakdown of a PWM converter and the LLC resonant converter. Figures 7.1.1.5 and

7.1.1.6 show the efficiency comparison of the LLC resonant converter and an asymmetrical half bridge converter for different load conditions at 400V input voltage and for different input voltages at full load respectively. As it can be seen from the figures, the efficiency of the LLC resonant converter is more than 94% for voltages above 360V.

Table 7.1.1.2: Loss breakdown of PWM and LLC resonant converters

	PWM	LLC
Primary conduction loss	9.67	9.49
Primary switching loss	11.3	7.5
Secondary conduction loss	22.0	13.0
Secondary switching loss	?	0
Total	42.97+?	29.9

Note that secondary reverse recovery loss is not included in this analysis.

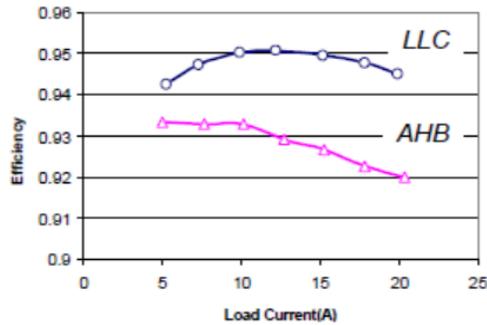


Fig. 7.1.1.5: Efficiency comparison with load change for 400V input voltage (Yang, Lee, Zhang, & Guisong, 2002)

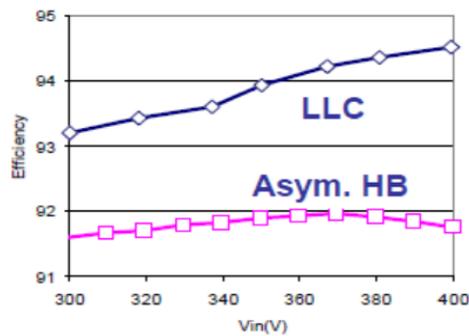


Fig. 7.1.1.6: Efficiency comparison with line change (Yang, Lee, Zhang, & Guisong, 2002)

7.1.2 ZVS Resonant Reset Dual Switch Forward DC/DC Converter

The second prospective buck converter topology is described by the circuit shown in Figure 7.1.2.1 (Gu, Gu, Hang, Wu, & Lu, 2004). This topology is a ZVS resonant reset dual switch forward converter with C_{oss1} , C_{oss2} and C_{oss3} being the parasitic capacities of the switches S_1 , S_2 and S_3 respectively. C_r is a resonant capacitor parallel to switch S_2 . C_r is much larger than C_{oss2} , so C_{oss2} can be neglected. L_m is the magnetizing inductance and L_s is the saturable inductance. L_s prevents the transfer of magnetizing current to the secondary side and assures ZVS for S_1 .

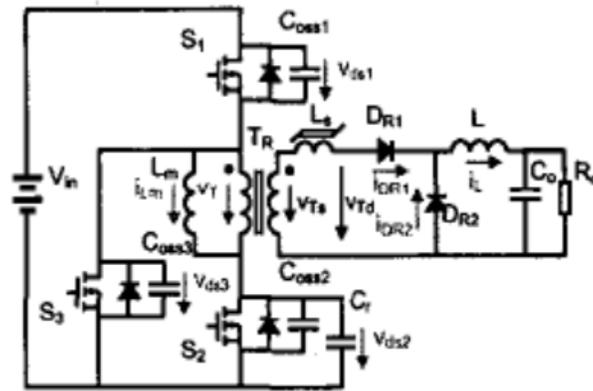


Fig. 7.1.2.1: ZVS Resonant reset dual switch forward converter (Gu, Gu, Hang, Wu, & Lu, 2004)

It is proved that this converter presents the following positive features:

- the duty cycle can be more than 50%
- voltage stress of the switches is reduced
- ZVS is achieved for all the switches
- high efficiency and power density are obtained

The switching period of this converter can be divided into eight operation modes. The operation waveforms and equivalent circuits of these modes are presented in Figures 7.1.2.2 and Fig. 7.1.2.3 respectively. The time period t_1 - t_3 is defined as the dead time t_{d1} and t_5 - t_7 as the dead time t_{d2} . t_5 - t_6 is the descending time of v_{ds1} and t_5 - t_8 is the blocking time of L_s . The eight operation modes of the converter are described here.

Mode 1 (t_0 - t_1)

During this time period, S_1 and S_2 are conducting. The primary side voltage of the transformer is V_{in} and the magnetizing current increases linearly. D_{R1} conducts while D_{R2} is reverse-biased.

Mode 2 (t_1-t_2)

At t_1 , S_1 and S_2 are turned off simultaneously. D_{R1} still conducts as the primary side voltage of the transformer (v_T) remains positive. The load current and magnetizing current charge C_{oss1} and discharge C_{oss3} . The voltage of C_{oss3} (v_{ds3}) decreases sharply and as a result v_T also decreases sharply (v_{ds2} can be ignored).

Mode 3 (t_2-t_3)

S_1 and S_2 are still off. D_{R1} is reverse-biased and D_{R2} is on. The inductance current i_L flows through D_{R2} and decreases linearly because of the effect of output voltage V_o . Resonance occurs between L_m and C_r . The resonant voltage across C_r varies according to sine wave. The transformer is reset by this resonant voltage and the current flows through the parasitic diode of S_3 .

Mode 4 (t_3-t_4)

At t_3 , S_3 is turned on under zero voltage condition. The voltage across C_r is sine wave because of the operation of the resonant tank of L_m and C_r . The resonant current circulates through S_3 .

Mode 5 (t_4-t_5)

The voltage of C_r reaches zero and magnetizing current circulates through the parasitic diode of S_2 . S_3 continues conducting. Now, v_T is zero so the magnetizing current is invariable.

Mode 6 (t_5-t_6)

At t_5 , S_3 is turned off. The magnetizing current charges C_{oss3} and discharges C_{oss1} , so v_{ds1} decreases rapidly. This current flows through the parasitic diode of S_2 , therefore v_{ds2} remains zero. v_T increases with v_{ds3} . D_{R1} remains off because L_s blocks the current from the transformer.

Mode 7 (t_6-t_7)

v_{ds1} decreases to zero, then the magnetizing current circulates through the parasitic diodes of S_1 and S_2 . The voltage applied to the primary side of the transformer is the input voltage V_{in} . The magnetizing current decreases inversely. The rectifier diode D_{R1} remains off and i_L is fully carried by D_{R2} .

Mode 8 (t_7-t_8)

S_1 and S_2 are turned on under zero voltage condition at t_7 . The voltage applied to the primary side of the transformer is still V_{in} . The magnetizing current circulates through S_1 and S_2 . D_{R1} remains off and D_{R2} on because of the blocking effect of L_s .

At t_8 , L_s enters saturation and the same procedure is repeated.

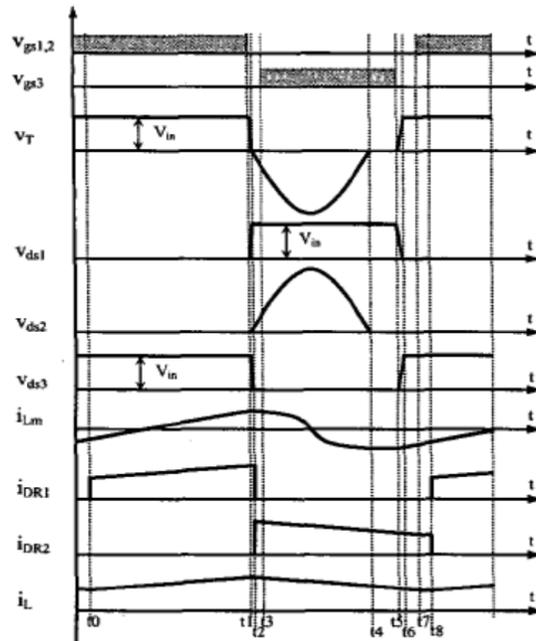
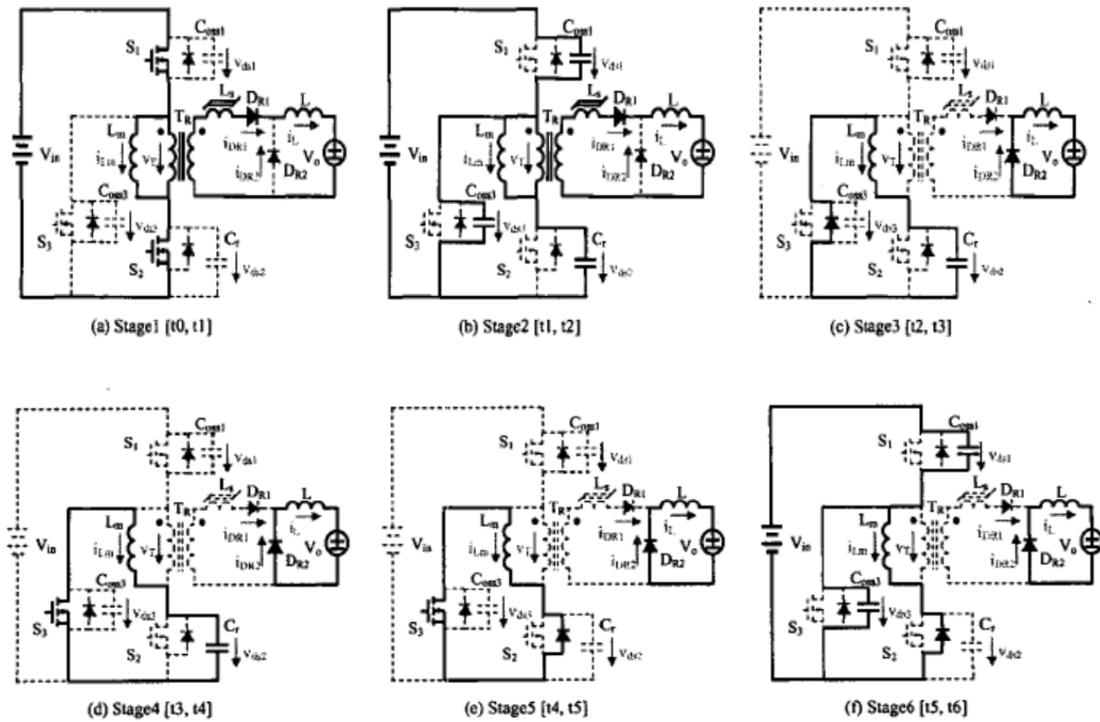


Fig. 7.1.2.2: Characteristic waveforms of the ZVS Resonant reset dual switch forward converter (Gu, Gu, Hang, Wu, & Lu, 2004)



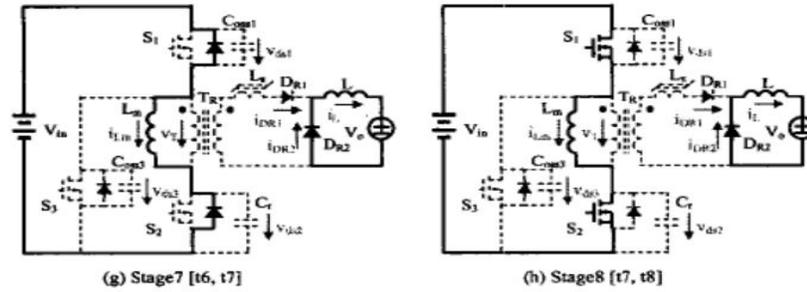


Fig. 7.1.2.3: Operating modes of ZVS Resonant reset dual switch forward converter (Gu, Gu, Hang, Wu, & Lu, 2004)

According to (Gu, Gu, Hang, Wu, & Lu, 2004), in order to assure ZVS for the three switches, the following should apply for the design of the converter:

- *Dead time t_{d2}*

An acceptable maximum value for t_{d2} must be determined. This period should be short. Normally, t_{d2} is approximately from 1% to 5% of the switching period.

- *Magnetizing inductance L_m*

$$L_m \leq \frac{nV_o t_{d2}}{2V_{in} f (C_{oss1} + C_{oss3})}$$

- *Saturable inductance L_s*

t_s is generally taken 1.2-1.5 times of t_{d2} .

The number of turns of the inductance is:

$$N = \frac{E_2 * t_s}{A_e * \Delta B}$$

where E_2 is the secondary voltage of the transformer, t_s is the blocking time of L_s , A_e is the cross sectional area of the saturable core and ΔB is the swing range of flux density in saturable core.

- *Resonant capacitance C_r*

$$C_r \leq \frac{(1 - D_{max})^2}{\pi^2 L_m f^2}$$

- *Dead time t_{d1}*

$$t_{d1} \geq \frac{V_{in} (C_{oss1} + C_{oss3})}{\left(I_m + \frac{I_o}{n}\right)}$$

The voltage ratio of this converter is:

$$\frac{V_o}{V_{in}} = \frac{D}{n}$$

According to the same study, a prototype was built in order to verify the performance of the converter. Its specifications and main parameters are presented in Table 7.1.2.1.

Table 7.1.2.1: Prototype's parameters

Parameter	Value	Parameter	Value
V_{in}	250-400V	S_3	IR830
V_o	54V	D_{R1}	HER1604PT
I_o	0-5A	D_{R2}	B20200
Switching frequency	100kHz	Transformer	n=50:20 $L_m=0.487mH$
$S_{1,2}$	STP11NM60	C_r	4400pF

Figure 7.1.2.4 shows the efficiency of the converter for various input voltages and load currents. It can be seen that the converter achieves high efficiencies (higher than 93%), with maximum efficiency 95.7%.

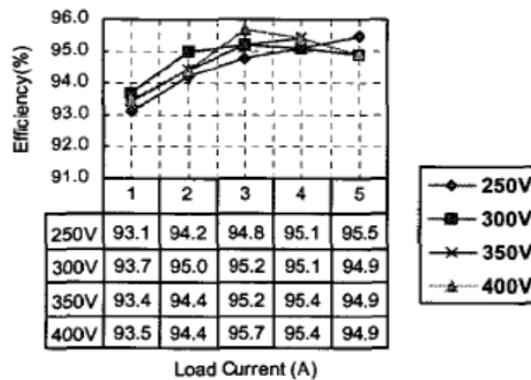


Fig. 7.1.2.4: Efficiency of ZVS Resonant reset dual switch forward converter at different conditions (Gu, Gu, Hang, Wu, & Lu, 2004)

7.1.3 Two Switch Forward Converter with Two Transformers and LLC Circuit

In the paper (Zhu, 2007) a novel two switch forward converter with LLC resonant circuit is proposed. This converter is a combination of a two switch forward converter and an LLC resonant circuit and can be described from the circuit shown in Fig. 7.1.3.1. As it can be seen, the proposed converter consists of two transformers, that their primary sides are connected in series while their secondary sides are connected in parallel through rectifier diodes. C_{r1} and C_{r2} are resonant capacitors, L_r is a resonant inductor, L_{m1} and L_{m2} are magnetizing inductors, like L_m in the case of the LLC converter, and the diodes D_3 and D_4 are clamping diodes.

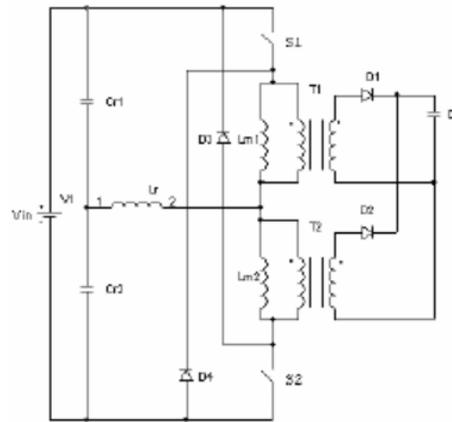


Fig. 7.1.3.1: Forward converter with LLC circuit (Zhu, 2007)

This converter combines the advantages of the common two switch forward converter and the LLC resonant converter. Therefore, it appears the following characteristics:

- high reliability due to no shoot-through issue
- high efficiency and high power density
- high switching frequency

However, the voltage of the switch at turn on although low it is not zero.

The operation of this converter consists of ten modes. For the following analysis, it is assumed that $C_{r1}=C_{r2}$, $L_{m1}=L_{m2}$, T_1 and T_2 are completely same, the inductance of primary side is large enough, C_1 is also large enough and S_1 and S_2 have inside capacitors and diodes connected in parallel. The switching frequency is a little higher than the resonant frequency of L_r and $(C_{r1}+C_{r2})$.

Figures 7.1.3.2 and 7.1.3.3 show the characteristic waveforms and the operating modes of the proposed converter.

Mode 1 (t_0-t_1)

At t_0 , S_2 turns on at low voltage. This time interval finishes when the reverse current of S_2 decreases to zero. Resonance occurs between L_r , L_{m1} , L_{m2} , C_{r1} and C_{r2} . The total equivalent inductance of resonance is $L_r+L_m/2$, as L_{m1} and L_{m2} are connected in parallel during this time interval. D_1 and D_2 are reverse-biased.

Mode 2 (t_1-t_2)

In this mode, the voltage on L_{m2} is clamped by the output voltage through T_1 , the current of L_{m2} increases linearly while the current of L_{m1} decreases linearly with the same slope. Resonance occurs between L_r and $C_{r1}+C_{r2}$. This interval ends when the current of L_r becomes zero.

Mode 3 (t_2-t_3)

This mode begins when the current of L_r is zero. The current direction of L_r now is opposite to the previous mode. The current increases to a maximum value and then decreases according to the resonance curve between L_r and $C_{r1}+C_{r2}$. This time interval finishes when the current of L_{m1} becomes zero.

Mode 4 (t_3-t_4)

S_2 remains on, D_4 turns off. The resonance between L_r and $C_{r1}+C_{r2}$ continues. The current of L_{m2} continues increasing linearly. Resonance occurs between L_{m1} and the capacitor of S_1 , through which the reverse voltage on S_1 decreases. The voltage of the switch decreases more slowly in this converter than in a common LLC converter, so longer time is needed to create low voltage condition.

Mode 5 (t_4-t_5)

At t_5 , S_2 turns off and S_1 remains off. D_3 now conducts, so the current of L_{m2} decreases. Resonance between L_{m1} and the capacitor of S_1 continues, so the voltage on S_1 decreases. The time interval finishes when S_1 turns on.

The next five modes are similar to the modes described above and they will not be further discussed here.

It should be noted that in modes 4 and 5, normally the lowest voltage of S_1 is not zero. It is given by the equation:

$$V_{S1} = V_{in} - 2(N * V_{out})$$

where N is the transformer's turn ratio.

In a typical design, V_{out} is a little lower than $V_{in}/(2N)$, so V_{S1} is a little higher than zero.

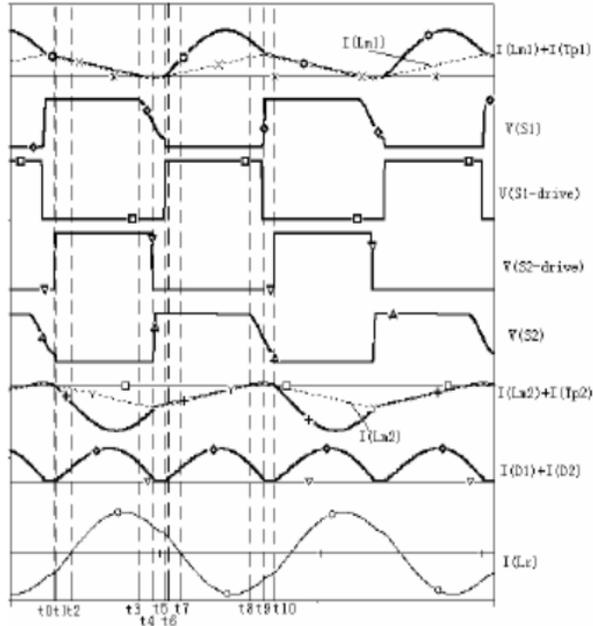
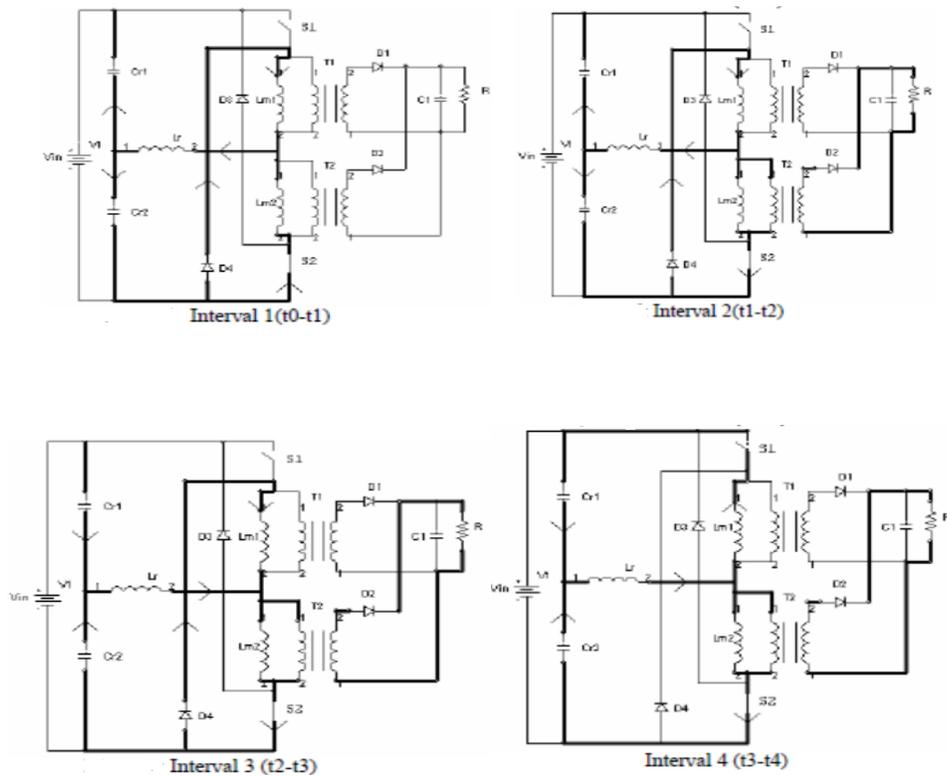


Fig. 7.1.3.2: Characteristic waveforms of two switch forward converter with LLC circuit (Zhu, 2007)



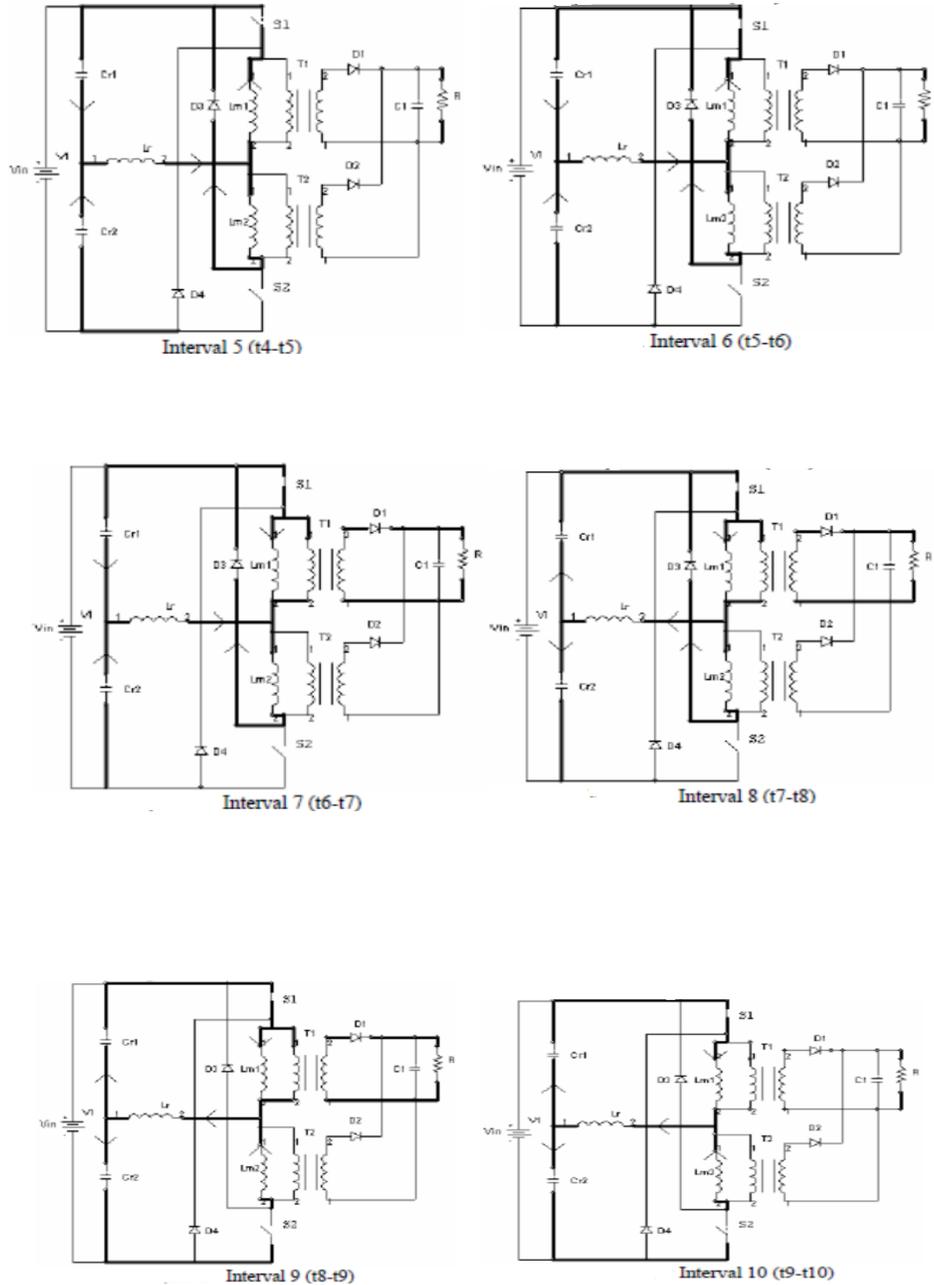


Fig. 7.1.3.3: Operating modes of two switch forward converter with LLC circuit (Zhu, 2007)

At the end of the paper, a comparison between the performance of a half-bridge LLC converter and the proposed converter is presented. The models used for the simulations have the specifications indicated in Table 7.1.3.1.

Table 7.1.3.1: Set of parameters used for simulations (Zhu, 2007)

Two switch forward converter with LLC circuit		LLC resonant converter	
Parameter	Value	Parameter	Value
V_{in}	400V	V_{in}	400V
S_1, S_2	IRFP460	S_1, S_2	IRFP460
L_{m1}, L_{m2}	400 μ H	L_m	200 μ H
L_r	30 μ H	L_r	30 μ H
C_{r1}, C_{r2}	46nF	C_r	92nF
D_3, D_4	MUR460		
Turn ratio	4:1	Turn ratio	4:1
Switching frequency	100kHz	Switching frequency	100kHz
Load	2.2 Ω	Load	2.2 Ω
D_1, D_2	Schottky, ideal	Diode	Schottky, ideal

The results of the simulations with the parameters given above, show that the LLC resonant converter performs better than the two switch forward converter with LLC circuit. The output voltage of the LLC converter comes out to be 47.62V, while the output voltage of the proposed converter is 46.95V. Moreover, the peak current and the resonance inductor current of the LLC converter are lower than the corresponding values of the proposed converter. Additionally, the voltage of switch at turn on is not zero but 90V. Finally, the total output power of the LLC converter is found to be 1030.9W and the efficiency 96.62%, while for the proposed converter the total output power is 1002.3W and the efficiency is 95.79%. However, the proposed converter does not have shoot-through issues as it can bear both switches keep on-state for enough time.

7.1.4 Phase Shifted Full Bridge Converter

Figure 7.1.4.1 shows the circuit of the phase shifted full bridge converter (PSFB) with a voltage doubler type rectifier stage proposed by (Lee, Kim, Han, & Moon, 2005).

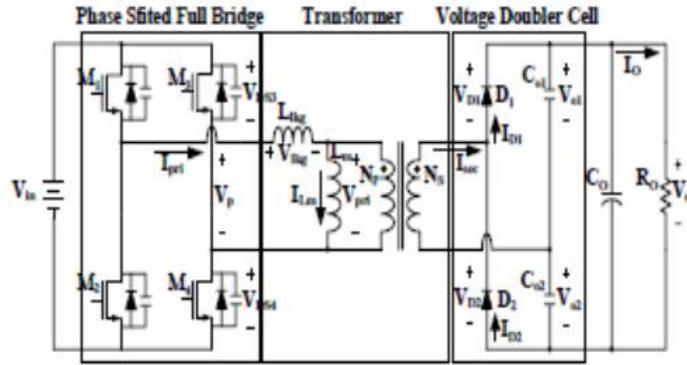


Fig. 7.1.4.1: Circuit diagram of the proposed phase shifted full bridge converter (Lee, Kim, Han, & Moon, 2005)

This converter was proposed to replace the conventional PSFB converter used in the plasma display panels (PDPs). It was proved that resolves many of the problems the conventional PSFB appears and therefore it has the following advantages:

- reduced voltage stresses of the secondary rectifier diodes, due to elimination of the output inductor
- high efficiency and power density
- low noise output voltage
- ZCS of the rectifier diodes
- ZVS of the primary switches

However, the current stresses of the rectifier diodes D_1 and D_2 are rather large, but they can be reduced with the right selection of the capacitance of the voltage doubler rectifier as it will be explained later.

Figure 7.1.4.2 shows the characteristic waveforms of the proposed converter and Figure 7.1.4.3 presents the different operating modes. The operation of the proposed converter can be divided into eight modes. However, because the operational principles of the two half cycles are symmetric, only the first four modes are described here.

The leading leg switches (M_1 and M_2) and lagging leg switches (M_3 and M_4) are turned on and off alternatively according to the duty ratio. $D_{eff}T_s$ is the operational conduction time and $D_{free}T_s$ is the phase shifted time. The phase difference between the two legs determines the duty cycle.

Mode 1 (t_0-t_1)

This time interval begins when ZVS condition of M_4 is achieved ($V_{DS4}=0$). The primary current (I_{pri}) rises with the resonance between the leakage inductor and the rectifier capacitor. The magnetizing current

(I_{Lm}) rises linearly. I_{D1} flows through the capacitor C_{o1} and therefore C_{o1} is being charged, while C_{o2} is being discharged.

Mode 2 (t_1-t_2)

At t_1 , M_1 is turned off. The output capacitor of M_1 is charged and the output capacitor of M_2 is discharged, therefore V_p is decreased to $0V$. V_{lkq} is also decreased. I_{pri} decreases with a slope of $-nV_{o1}/L_{lkq}$. The operation of the secondary side is similar to secondary side operation of Mode 1.

Mode 3 (t_2-t_3)

Mode 3 begins when the primary current (I_{pri}) becomes equal to the magnetizing current (I_{Lm}). These currents remain equal during this mode. D_1 becomes reverse-biased under ZCS condition. Both D_1 and D_2 are off with voltages V_{o1} and V_{o2} , respectively. M_2 is turned on at some instant during this time interval but V_p remains $0V$.

Mode 4 (t_3-t_4)

At t_4 , M_4 turns off and V_p decreases to $-V_{in}$. At the end of this time interval, the commutation between D_1 and D_2 is completed.

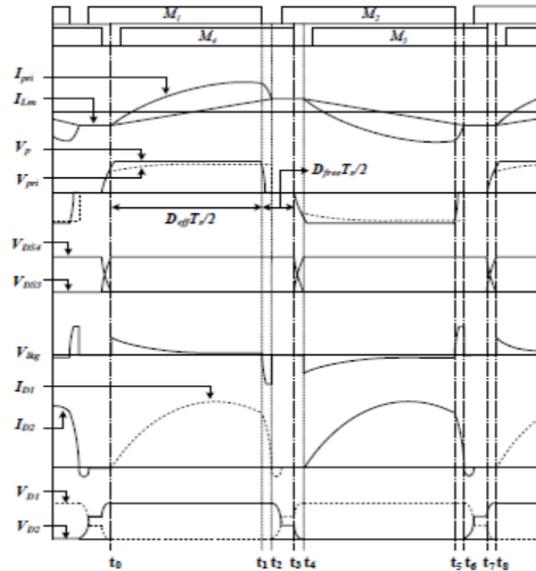


Fig. 7.1.4.2: Characteristic waveforms of the proposed phase shifted full bridge converter (Lee, Kim, Han, & Moon, 2005)

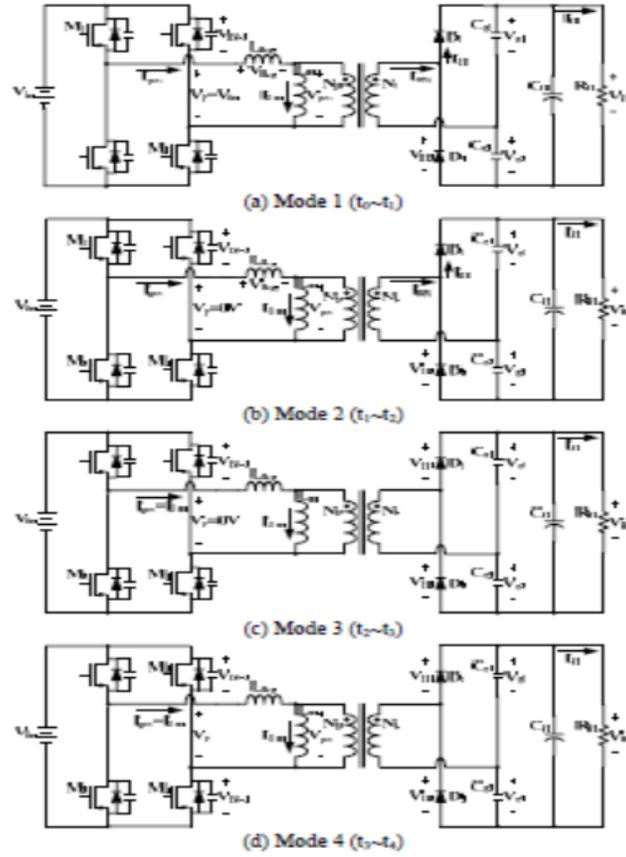


Fig. 7.1.4.3: Operating modes of the proposed phase shifted full bridge converter (Lee, Kim, Han, & Moon, 2005)

In order to find the DC conversion ratio, the following assumptions were made:

- The capacitors C_{o1} , C_{o2} and C_o are assumed to be large enough so that the voltages V_{o1} , V_{o2} and V_o are constant.
- L_m is so large that $I_{Lm}=0$.
- I_{pri} increases and decreases linearly.
- The time intervals (t_1-t_2) and (t_5-t_6) are so small that can be neglected.
- The dead time can also be neglected.

Then, the voltage conversion ratio yields:

$$\frac{V_o}{V_{in}} = \frac{1}{\frac{4L_{lk}g}{nR_oT_sD_{eff}^2} + \frac{n}{2}}$$

According to the paper (Lee, Kim, Han, & Moon, 2005), ZVS can be secured for all the switches regardless of load conditions. In order to guarantee the safe ZVS of lagging leg, the dead time should be:

$$\Delta t_{dead} = C_{oss} \frac{V_{in}}{|I_{Lm}(t_3)|/2}$$

where C_{oss} is the output capacitors of the switches.

As it was mentioned before, a disadvantage of this converter is that the current stresses of the rectifier diodes can be large. However, these stresses are limited because of the resonance between the leakage inductor and the capacitors of the rectifier side. The capacitance should be selected to satisfy the equation:

$$C_{o1} = \frac{n^2}{8\pi^2 L_{lkg} F_s^2 \left(\frac{F_r}{F_s}\right)^2}$$

where F_r/F_s is the normalized switching frequency.

Finally, a prototype of 450W was built in order to verify the performance of the converter (Lee, Kim, Han, & Moon, 2005). The parameters used are described in Table 7.1.4.1.

Table 7.1.4.1: Parameters of the PSFB prototype

Parameter	Value
Switching frequency	60kHz
Transformer's turn ratio	3.23:1
L_{lkg}	23 μ H
L_m	1.4mH
C_{o1}, C_{o2}	2.2 μ F/630V
C_o	1000 μ F/250V
M_1, M_2, M_3, M_4	FQP12N60
D_1, D_2	15ETH03

The results of the experiments verified the advantageous behavior of the proposed PSFB converter and showed that it has the characteristics predicted by theory, such as ZVS, ZCS and high efficiency. Figure 7.1.4.4 presents the measured efficiency of the proposed PSFB and the conventional PSFB converter. As it can be seen, the proposed converter maintains an efficiency higher than 95% for a wide load range. Its efficiency is above 96% for full load.

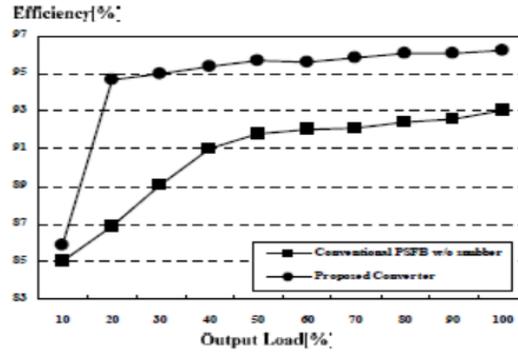


Fig. 7.1.4.4: Measured efficiency of proposed phase shifted full bridge converter (Lee, Kim, Han, & Moon, 2005)

7.2 Selection of Buck Converter Topology

The Table below summarizes the most important information regarding the four buck converter topologies described before. It presents the different components that comprise each topology circuit, the voltage ratio achieved according to the results of the papers, the advantages and disadvantages referred in the studies and the efficiencies achieved.

Table 7.2.1: Characteristics of the proposed buck converter topologies

Topology	Components	Voltage Ratio (V_o/V_{in})	Advantages	Disadvantages	Efficiency (%)
LLC Resonant Converter (selected topology)	2 switches, 1 T, L_r , L_m , C_r , C_o , 2 diodes	0.119	ZVS, low switching losses, low voltage stress, low turn off switching current, high power density	Possible shoot-through issues	94-96.62
ZVS Resonant Reset Dual Switch Forward Converter	3 switches, 1 T, L_m , L_s , L , C_r , C_o , 2 diodes	0.135-0.216	ZVS, low voltage stress, high power density	-	93.4-95.7
Two Switch Forward Converter with Two Transformers and LLC Circuit	2 switches, 2 T, L_r , L_{m1} , L_{m2} , C_{r1} , C_{r2} , C_1 , 4 diodes	0.117	High reliability (no shoot-through), high power density	Low voltage switching but no ZVS	95.79
Phase Shifted Full Bridge Converter	4 switches, 1 T, L_{lk} , L_m , L_c , C_c , 4D	-	ZVS, low voltage stress, low noise output voltage, ZCS of diodes, high power density, high efficiency for a wide load range	Large current stresses of diodes but possibility to be reduced	95-96.3

In order to make the selection of the topology, it should be noted that all the described topologies fulfill the criteria referred at the beginning of this chapter (isolation, high efficiency, small number of components). However, the half-bridge LLC resonant converter appears to have the best combination of characteristics. It makes use of the smallest number of components, it has small power losses, it achieves ZVS, low voltage stress and low turn off switching current. The shoot-through issue can be resolved by selecting sufficient dead time between the switching of the two switches. Finally, efficiency as high as 96.62% can be obtained if the parameter values of Table 7.1.3.1 are used. Therefore, the LLC resonant converter is the proposed buck converter topology for the test container's electricity system.

Chapter 8: Inrush Current Limiting Circuit

As it was explained in Chapter 6, the electronic devices and DC-DC converters contain large input capacitors for filtering the ripple current. When the devices are switched on, the loading of these capacitors results in high inrush currents as a result of the application of a high dv/dt to the filter capacitor. These filter capacitors initially act as short circuits resulting in high surge currents with fast rise times. The inrush current if not limited can cause dip in the input voltage and generate high di/dt and dv/dt that can damage the circuit components (Mallesham & Anand, 2006). The surge currents of some devices were measured and presented in Chapter 6.

This chapter presents the design of a circuit that can be used for limiting the inrush current. The proposed circuit was simulated and a prototype was built and tested. An improved version of the proposed inrush current limiter is also presented here.

8.1 Various Inrush Current Limiting Techniques

In order to avoid problems related to the surge currents, the power supply manufacturers have developed several inrush current limiting (ICL) techniques, some of them using passive and some other active elements.

The inductor is a passive device that can be used in series with the filter capacitor for limiting the inrush current. The disadvantage of this method is that the weight and volume of the circuit can be increased, because the size of the coil should be big enough to compensate the current value.

Instead of the inductor, a resistor can be used in series with the capacitor. However, the fixed impedance of the resistor will cause a permanent power loss to the circuit. In order to overcome this problem, many designers incorporate a parallel switch (usually a relay) with the resistor. This method can adjust the peak value of the inrush current and the settling time by using a control circuit which controls the switch's turn on and turn off. However, this method has a limitation due to the mechanical operation of the relay and additionally, it requires a control circuit.

Another very popular method for ICL makes use of the NTC thermistors. NTC thermistors have a negative temperature coefficient. In other words, the resistance of these devices decreases as current flows through them (current flow causes a temperature rise). So, initially the NTC thermistor has a high resistance, which limits the inrush current. As time goes by, the resistance value decreases and permits to the current to flow. The drawback of this device is that a "cool off" time is necessary after the power is removed in order for the thermistor to regain its high resistance. The NTC thermistor can be used in

combination with an active device in order to overcome the “cool off” time, but this adds to the complexity of the circuit.

Recently, the use of active inrush current limiters (AICL) is increasing. The AICL described and implemented in this project uses a MOSFET switch and some passive elements that can drive the MOSFET in such a way that the inrush current of the circuit can be limited by controlling the gate charge characteristic of the MOSFET. This ICL has been mainly used in low power circuits so far because of the large input impedance of the MOSFET and the limitation of rated voltage (Lee, Ahn, Shin, & Lee, 2012). For this reason, the study of effectiveness and reliability of this circuit to high voltage power supplies is still lacking. (Lee, Ahn, Shin, & Lee, 2012) presented a study on this topic by building an ICL prototype and conducting experiments with high voltage DC power supply. The results verified the effectiveness of the ICL.

8.2 Active Inrush Current Limiting Using a MOSFET

8.2.1 MOSFET

The Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) is a three-terminal device used for amplifying or switching electronic signals. The input terminal of the MOSFET, the gate (G), controls the current flow between the output terminals, i.e.: the drain (D) and the source (S) (Mohan, 2003). The output characteristics of drain current (i_D) as a function of drain-to-source voltage (v_{DS}), and V_{GS} as a parameter, for an n-channel MOSFET is presented in Figure 8.2.1.1.

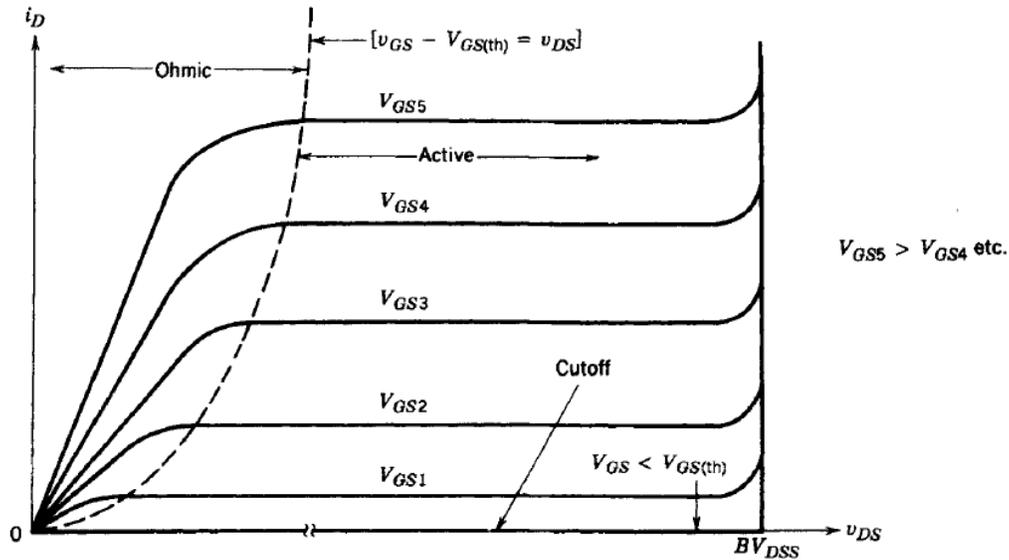


Fig. 8.2.1.1: Output i_D - v_{DS} characteristics of an n-channel MOSFET (Mohan, 2003)

The MOSFET can be used as a switch that controls the power flow to the load. As it can be seen from the Figure 8.2.1.1, the device passes from the cutoff through the active region to the ohmic region, during turn on. When it turns off, the procedure is reversed. The MOSFET is in off-state when the gate-source voltage is smaller than the threshold voltage ($V_{GS(th)}$). The drain-source voltage must be less than the breakdown voltage (BV_{DSS}), so that the breakdown of the MOSFET is avoided. When the MOSFET is driven by a large gate-source voltage, it is led to the ohmic region. In this region, the drain-source voltage is small and the following holds true:

$$v_{GS} - V_{GS} > v_{DS} > 0$$

In the active region, the drain current is only dependent on the gate-source voltage. As the drain current is independent of the drain-source voltage and considered saturated, this region is often called saturation or pentode region.

8.2.2 MOSFET Switching Characteristics

The MOSFET can be represented by the circuit shown in Figure 8.2.2.1. The capacitances that appear in the circuit are stray and depletion layer capacitances due to the inner structure of the MOSFET. The gate charge characteristic of the device will be explained by making use of this circuit.

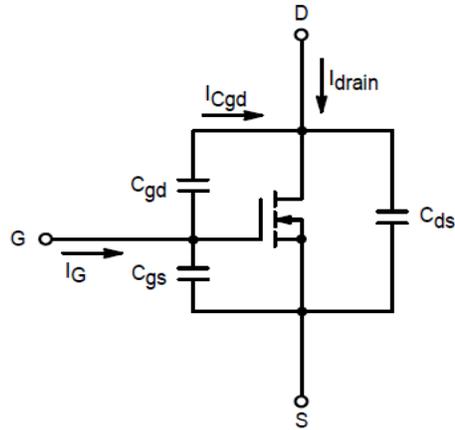


Fig. 8.2.2.1: Equivalent circuit of MOSFET (Mitter, 1995)

It is essential to mention that these capacitances are not constant but vary with the voltage across them as part of the capacitance is affected by the depletion layers. The capacitance C_{gd} has the most significant change because the voltage change across it is large. The change of C_{gd} can be in the scale of 10-100 (Mohan, 2003).

The following expressions can be obtained from the circuit above:

$$C_{iss} = C_{gs} + C_{gd} \tag{8.2.2.1}$$

$$C_{rss} = C_{gd} \tag{8.2.2.2}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{8.2.2.3}$$

C_{iss} is the equivalent input capacitance, C_{rss} is the reverse transfer capacitance and C_{oss} is the equivalent output capacitance. The values for these parameters can be found in the manufacturer's datasheets. The charge and discharge rate of the capacitances determines how fast the MOSFET switches on or off, as it determines the slew rate of V_{GS} and V_{DS} .

As it was explained before, C_{gd} has the most significant change, fact that affects the V_{DS} characteristic. By adding a big capacitor in parallel with the C_{gd} (C'_{gd}), the slope of the drain voltage transition can be controlled because the nonlinear capacitive effects of C_{gd} can be disregarded. This will allow the control of the inrush current as that depends on the dV_{DS}/dt .

Moreover, a large resistor R_G can be added in series to the gate for controlling the gate current (I_G).

Then, the circuit shown in Figure 8.2.2.1 is converted into the circuit presented in Figure 8.2.2.2.

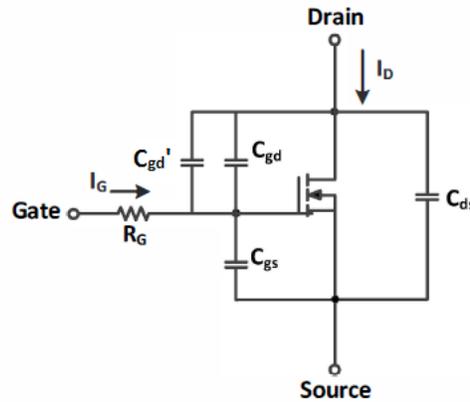


Fig.: 8.2.2.2: Revised MOSFET circuit with external capacitor and series resistance (Lee, Ahn, Shin, & Lee, 2012)

Given that: $C'_{gd} \gg C_{gd}$:

$$C_{iss} \approx C_{gs} + C'_{gd}$$

$$C_{rss} \approx C'_{gd}$$

$$C_{oss} \approx C'_{gd}$$

The gate charge characteristic of the circuit shown in Figure 8.2.2.2 is displayed in Figure 8.2.2.3.

Section I: In section I, a time delay appears. The turn-on time delay is defined as the time required for the gate-source voltage to reach the threshold value. During the turn-on delay time, the V_{GS} rises from 0 to the threshold value ($V_{GS(th)}$) because of the currents flowing through C'_{gd} , C_{gd} and C_{gs} . The gate current (I_G) is controlled by the gate resistor R_G . V_{GS} rises exponentially with its time constant being: $\tau = R_G(C'_{gd} + C_{gs})$. The V_{GS} rise seems to be linear because only part of the exponential curve is in section I.

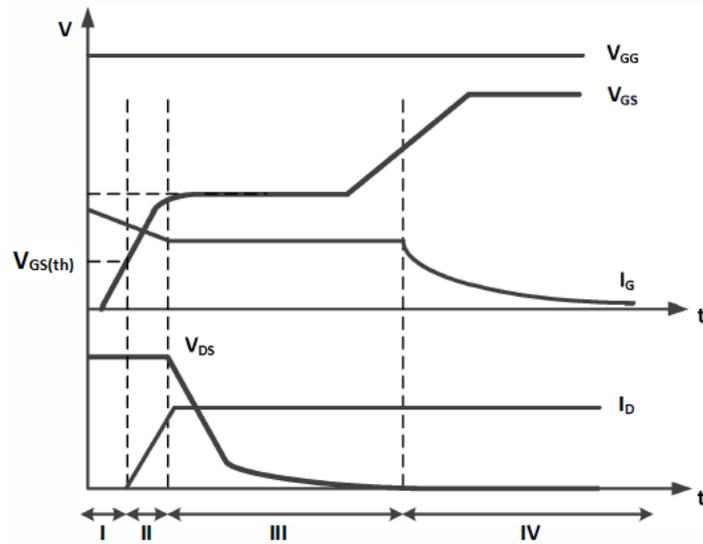


Fig. 8.2.2.3: MOSFET gate charge transfer curve (Lee, Ahn, Shin, & Lee, 2012)

Section II: V_{GS} continuous to increase. The value of I_D rises gradually as V_{GS} increases. The following equation describes the drain current rate of change:

$$\frac{dI_D}{dt} = g_{sf} \frac{dV_{GS}}{dt}$$

where g_{sf} is the transconductance. During this time interval, the drain voltage is almost constant.

Section III: In this section, the drain current is conducted and C_{gd} discharges continuously. Miller plateau region, where V_{GS} is clamped at its plateau value, is represented. If this section is increased, the slew rate of V_{DS} is decreased. By adding the C'_{gd} between the drain and gate, the charging time of the miller capacitance increases and as a consequence, the section III also increases. Therefore, the inrush current can be limited.

Section IV: V_{GS} rises to its gate voltage. The drain and source have the same potential in this region.

All in all, it can be concluded that by designing a proper driving circuit for the gate current and controlling the V_{DS} slew rate, inrush current limiting by using a MOSFET can be achieved.

8.3 Design of Inrush Current Limiter using MOSFET

For the design of the ICL, the circuit shown in Figure 8.2.2.2 will be used in combination with some other passive devices. The proposed ICL is presented in Figure 8.3.1. In this circuit, the inrush current is caused because of the C_{filter} which represents the input capacitor of the DC-DC converter.

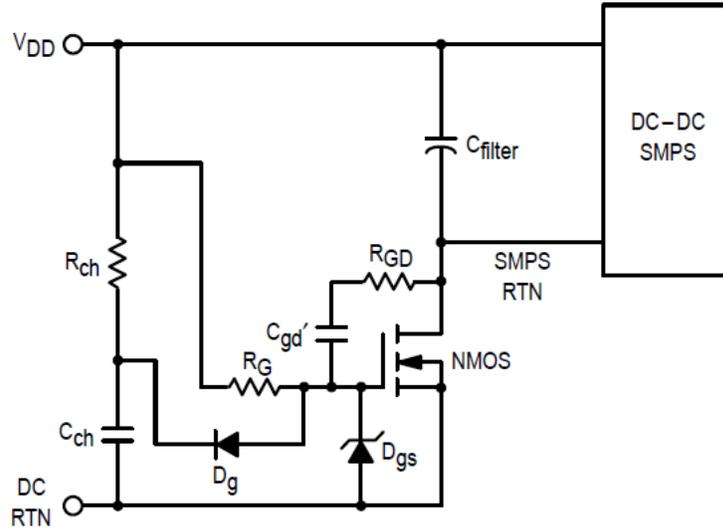


Fig. 8.3.1: Proposed inrush current limiter (Mitter, 1995)

As it can be seen from the figure above, the MOSFET is placed in the return path of the converter. Initially, the MOSFET is in off-state, before the DC bus voltage is applied. With the dv/dt control circuit of the MOSFET, V_{DD} voltage is applied to the load at a fixed rate. Consequently, the inrush current can be limited to a safe for the application value.

The C'_{gd} capacitor is connected in parallel between the gate and drain, as discussed above, and makes the control of the slope of the drain voltage possible. R_{GD} is a small resistor ($R_{GD} \ll R_G$) in series with C'_{gd} . It is added in order to damp any unwanted high frequency oscillations (Lee, Ahn, Shin, & Lee, 2012). The resistor R_G controls the charge rate of C'_{gd} . The diode D_g is used for providing faster turn off processes. The Zener diode (D_{gs}) protects the MOSFET, as it keeps the V_{GS} at a level below the breakdown voltage.

In some cases, when voltage is applied to the circuit, it is possible that the V_{GS} is higher than the $V_{GS(th)}$ and the MOSFET turns on. Then, the dv/dt control is lost. For this reason, a capacitor C_{ch} is inserted in order to keep the V_{GS} below the $V_{GS(th)}$, so that the device remains off and the control is not lost. The resistor R_{ch} determines the time constant for the charging of the C_{ch} capacitor.

So, when V_{DD} is applied to the circuit, the capacitance C_{ch} maintains the V_{GS} to a level below the $V_{GS(th)}$ so that the MOSFET does not turn on. The capacitance C_{ch} is charged depending on the $R_{ch}C_{ch}$ time constant. Then, the V_{GS} increases with the same rate up to a level that supports the inrush current. The

drain voltage decreases linearly with a slope that depends on the $R_G C'_{gd}$ time constant (Mitter, 1995). The drain current is constant in this section because the MOSFET is in the saturation region. The voltage across the C_{filter} increases with the same slope as V_{DS} decreases. This slope determines the maximum value of the inrush current. The waveforms that should be expected are presented in Figure 8.3.2.

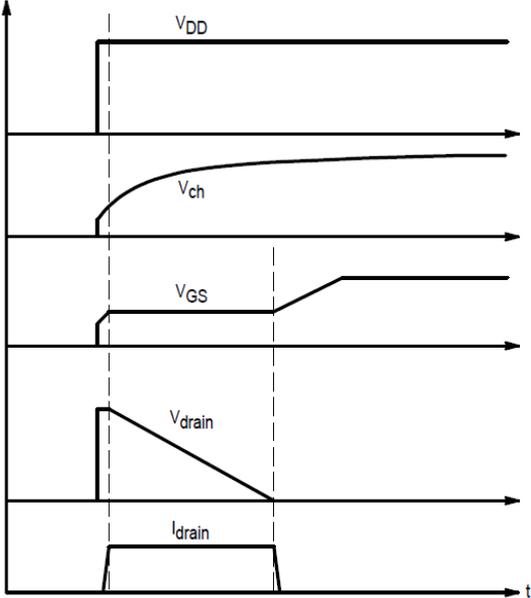


Fig. 8.3.2: Switching waveforms of circuit 8.3.1 (Mitter, 1995)

8.3.1 Design equations

The values of the components of the proposed ICL circuit are calculated based on the following equations, which result from the above analysis.

1. Time required to meet the inrush current requirement:

$$dt = C_{filter} \frac{V_{DD}}{I_{inrush}}$$

2. Gate-source plateau voltage required to supply the load current:

$$V_{plt} = V_{th} + \frac{I_{inrush}}{g_{fm(max)}}$$

3. C'_{gd} should be:

$$C'_{gd} \gg C_{gs} + C_{gd}$$

C_{gs}, C_{gd} can be calculated from the equations (8.2.2.1)-(8.2.2.3). The values of $C_{iss}, C_{rss}, C_{oss}$ are found from the MOSFET datasheet.

4. Gate current:

$$I_{gd} = C'_{gd} \frac{dV_{DS}}{dt}$$

5. Series gate resistance:

$$R_G = \frac{(V_{GG} - V_{plt})}{I_{gd}}$$

6. R_{GD} :

$$R_{GD} \ll R_G$$

7. Minimum time required for gate-source voltage to reach the value to support the initial inrush current:

$$t_{vgs(min)} = \frac{V_{plt}}{\left(\frac{dI_{inrush}}{dt}\right)}$$

8. The following equation should be satisfied so that line dropout does not happen:

$$R_G(C_{gs} + C'_{gd}) \geq \frac{-t_{vgs(min)}}{\ln \left| 1 - \frac{V_{pl}}{V_{GG}} \right|}$$

If this equation is not satisfied, either R_G or C'_{gd} should be changed to satisfy it.

9. Voltage across the charge capacitor:

$$V_{ch} = V_{thmin} - 1$$

10. Capacitor C_{ch} :

$$C_{ch} \approx \frac{C'_{gd}(V_{DD} - V_{ch})}{V_{ch}}$$

11. Delay time for the initial current:

$$t_{delay} \approx 5.3R_{GD}C'_{gd}$$

12. Resistor R_{ch} :

$$R_{ch} \geq \frac{1}{C_{ch}} \frac{t_{delay}}{\text{abs ln} \left| 1 - \frac{(V_{plt} - V_{ch} - V_{DG})}{V_{DD}} \right|}$$

8.4 Results

8.4.1 Experimental Results

In order to examine the performance of the proposed ICL, a prototype was built and tested. The values of the components that comprise the circuit were calculated based on the equations given in Section 8.3.1 and are tabulated in the following Table (Table 8.4.1.1).

Table 8.4.1.1: Components used

Parameter	Value	
MOSFET	IXFK 64N50P	
	C_{iss}	8700 pF
	C_{oss}	970 pF
	C_{rss}	90 pF
C_{ch}	20 μ F	
C_{gd}'	0.1 μ F	
R_{ch}	1 k Ω	
R_G	620 k Ω	
R_{GD}	100 Ω	
D_g	IN5408T036	
D_{gs}	W22C 9V1	
C_{filter}	10 μ F	

Figure 8.4.1.1 shows the built prototype of the ICL.

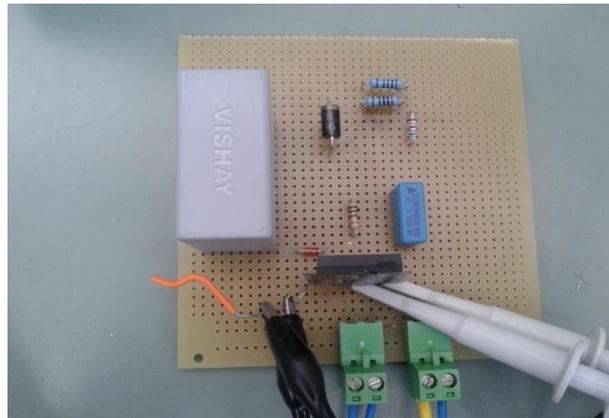


Fig. 8.4.1.1: Inrush current limiter prototype

The experimental setup used for testing the ICL prototype consists of the elements shown in Figure 8.4.1.2. The power supply provides the circuit with a high DC voltage of 360-400V and 250W load is connected to the ICL. The load consists of the parallel combination of the filter capacitor with a variable resistor, which is adjusted so that it has a resistance around 600 Ω . An electromechanical relay was used to switch on and off the ICL and the load. The behavior of the load during turn-on and turn-off was investigated by measuring the input current and input voltage of the load (i.e. across the filter capacitor) and the respective settling time. Additionally, the drain-to-source and gate-to-source voltages of the MOSFET were recorded.

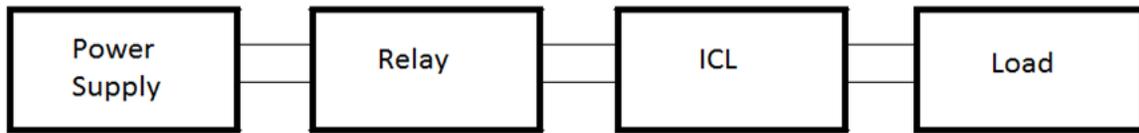


Fig. 8.4.1.2: Experimental setup

For comparative reasons, the input current and voltage of the load were also measured without the ICL during turn-on and turn-off of the load.

8.4.1.1 Without Inrush Current Limiter

Turn-on

The Table 8.4.1.1.1 and Figure 8.4.1.1.1 present the results taken from the experiments for the circuit without ICL during turn-on.

Table 8.4.1.1.1: Measurements without inrush current limiter during turn-on with $C_{filter}=10\mu F$

V (V)	I(A)	I_{max} (A)	I_{min} (A)	V_{max} (V)	V_{min} (V)	Settling time (μs)
360	0.633	199	-56	415	-12	60
370	0.651	208	-48	430	-28	50
380	0.670	208	-50	431	-28	50
390	0.680	216	-80	448	-31	60
400	0.700	216	-80	472	-40	70

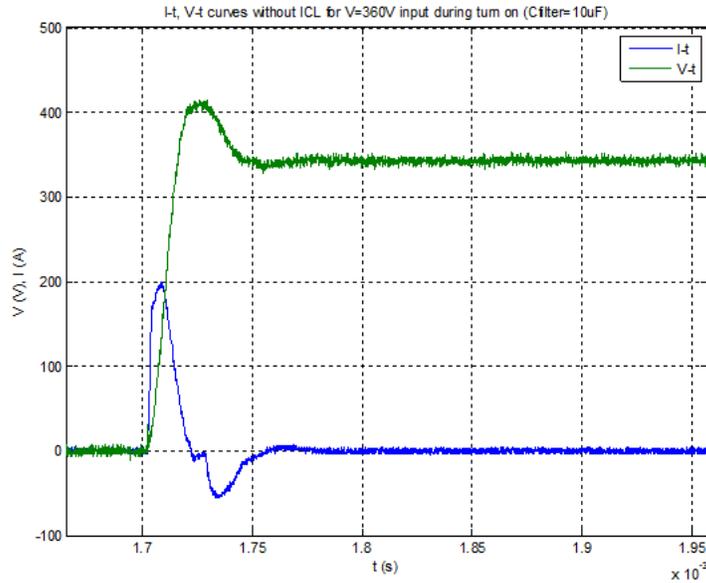


Fig. 8.4.1.1.1: $I-t$, $V-t$ curves without inrush current limiter for 360V input during turn-on and $C_{filter}=10\mu F$

As it can be seen, a high inrush current (more than 200A) with settling time around 60µs flows through the circuit when the load is switched-on.

Turn-off

The Table 8.4.1.1.2 and Figure 8.4.1.1.2 present the results taken from the experiments for the circuit without ICL during turn-off.

Table 8.4.1.1.2: Measurements without inrush current limiter during turn-off with $C_{filter}=10\mu F$

V (V)	V_{max} (V)	V_{min} (V)	Settling time (ms)
360	376	-16	20.7
370	392	-16	20.7
380	399	-16	22
390	408	-16	22
400	422	-16	24

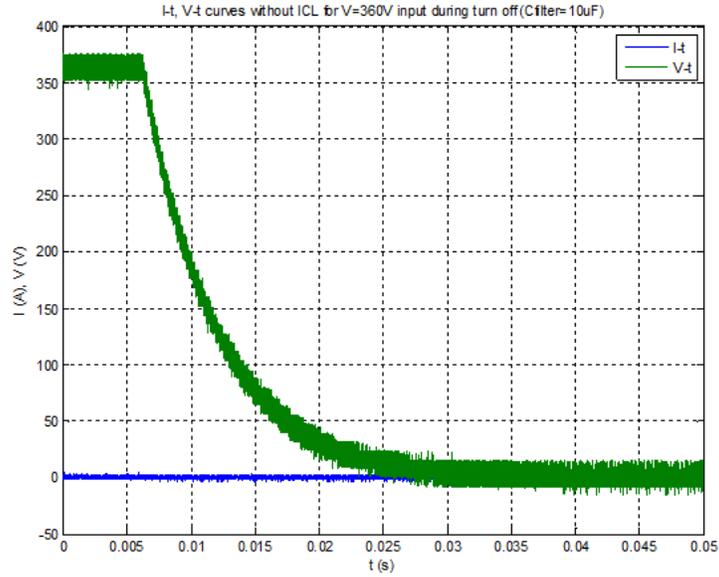


Fig. 8.4.1.1.2: I - t , V - t curves without inrush current limiter for 360V input during turn-off and $C_{filter}=10\mu F$

It can be observed that there is no high current problem at turn-off. The voltage settling time is around 20ms.

8.4.1.2 With Inrush Current Limiter

Turn-on

The Table 8.4.1.2.1 and Figures 8.4.1.2.1 and 8.4.1.2.2 display the measurement results for turn-on when the ICL is added to the circuit.

Table 8.4.1.2.1: Measurements with inrush current limiter during turn-on with $C_{filter}=10\mu F$

V (V)	I (A)	I_{max} (A)	I_{min} (A)	V_{max} (V)	V_{min} (V)	Settling time (μs)
360	0.637	144	-5	376	-29	800
370	0.656	150	-19	384	-16	700
380	0.670	155	-23	396	-14	800
390	0.686	157	-23	404	-17	700
400	0.708	156	-6	416	-12	700

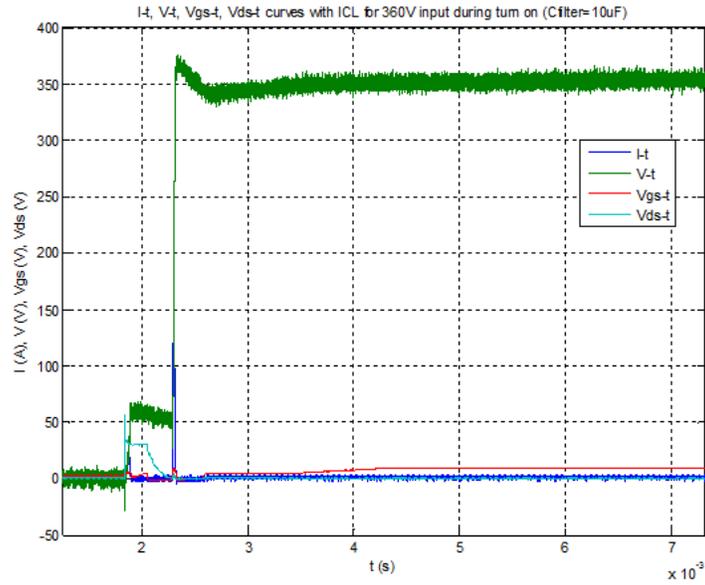


Fig. 8.4.1.2.1: $I-t$, $V-t$, $V_{GS}-t$, $V_{DS}-t$ curves with inrush current limiter for 360V input during turn-on and $C_{filter}=10\mu F$

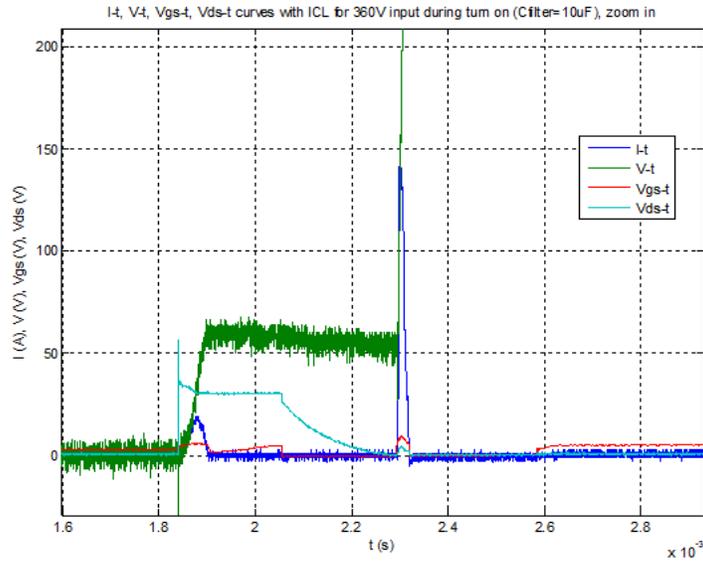


Fig. 8.4.1.2.2: $I-t$, $V-t$, $V_{GS}-t$, $V_{DS}-t$ curves with inrush current limiter for 360V input during turn-on and $C_{filter}=10\mu F$ (zoom in)

As it can be seen from the above measurements, a high inrush current (around 150A) seems to flow through the circuit with the ICL. The settling time is increased (700-800 μs) compared to the circuit without ICL. This should be expected as the goal of the ICL is to decrease the dv/dt by increasing the switching time.

Turn-off

The Table 8.4.1.2.2 and Figures 8.4.1.2.3 and 8.4.1.2.4 display the measurement results for turn-off of the circuit with the ICL.

Table 8.4.1.2.2: Measurements with inrush current limiter during turn-off with $C_{filter}=10\mu F$

V (V)	V_{max} (V)	V_{min} (V)	Settling time (ms)
360	374	-12	110
370	384	-12	110
380	395	-12	110
390	404	-12	112
400	414	-12	112

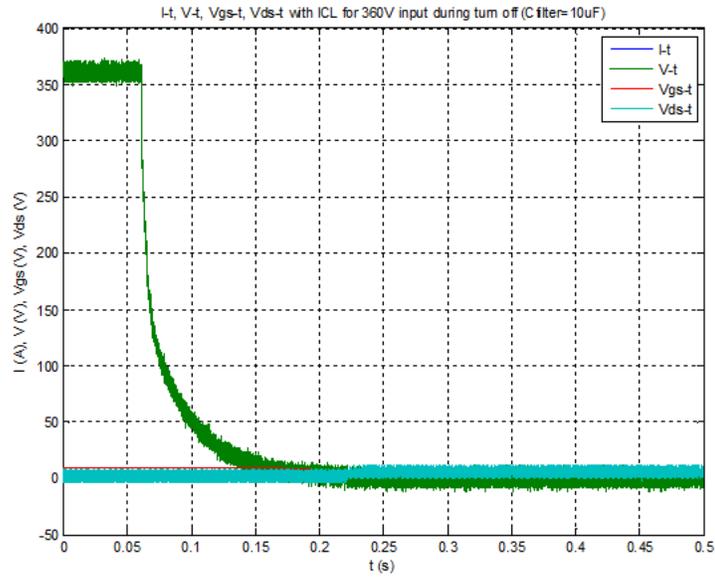


Fig. 8.4.1.2.3: $I-t$, $V-t$, $V_{GS}-t$, $V_{DS}-t$ curves with inrush current limiter for 360V input during turn-off and $C_{filter}=10\mu F$

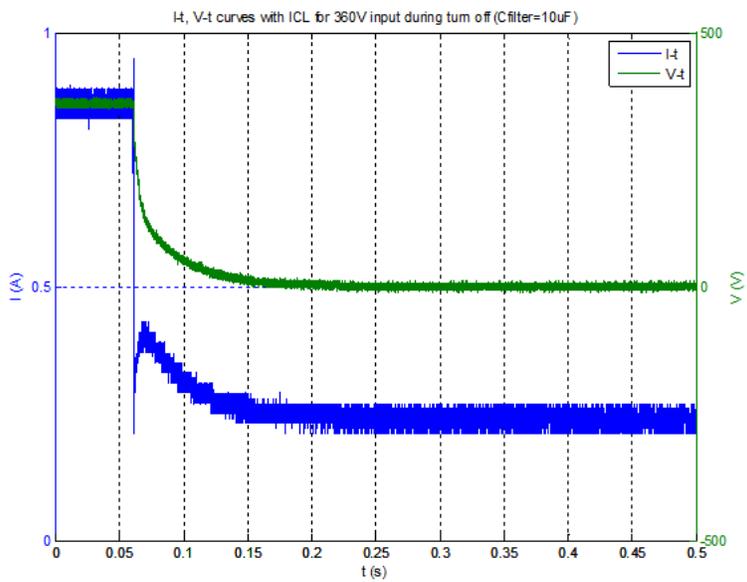


Fig. 8.4.1.2.4: $I-t$, $V-t$ curves with inrush current limiter for 360V input during turn-off and $C_{filter}=10\mu F$

As it was observed, there was no high current problem during turn-off. The voltage settling time was found to be *110ms* approximately.

8.4.2 Simulation Results

The experimental results showed that there are high inrush currents at turn-on even when the ICL circuit is used. In order to investigate in depth the behavior of the ICL, a model of the proposed circuit was made with the help of the simulation program NI Multisim. The model of the circuit is presented in Figure 8.4.2.1.

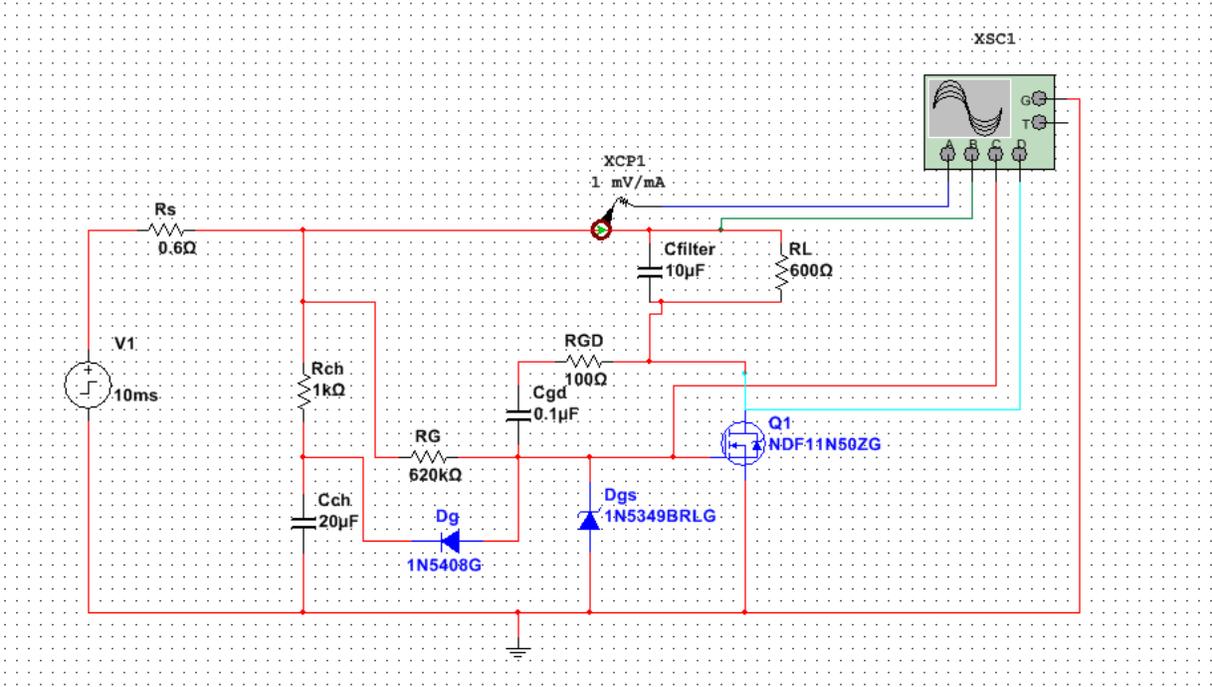


Fig. 8.4.2.1: Proposed Inrush Current Limiter

The following assumptions were made regarding the simulations:

- *0.6Ω* internal source resistance
- *100ns* voltage rise/fall time
- ideal capacitors and resistors

In order to examine the performance of this ICL, simulations with different values of filter capacitors were done. The input voltage was in the range of *360V-400V*.

First, the simulation results of the circuit without the ICL are presented for comparative reasons. Then, the circuit with the ICL is simulated.

8.4.2.1 Without Inrush Current Limiter

Turn-on

The Table 8.4.2.1.1 and Figure 8.4.2.1.1 display the simulation results for the circuit without ICL at turn-on.

Table 8.4.2.1.1: Simulation results of circuit without inrush current limiter during turn-on

V(V)	$C_{\text{filter}}=0.01\mu\text{F}$		$C_{\text{filter}}=10\mu\text{F}$		$C_{\text{filter}}=220\mu\text{F}$	
	$I_{\text{max}}(\text{A})$	Settling time (ns)	$I_{\text{max}}(\text{A})$	Settling time (μs)	$I_{\text{max}}(\text{A})$	Settling time (μs)
360	39	156	595	32	600	945
370	41	156	612	32	616	945
380	42	156	628	32	633	945
390	43	156	645	32	650	945
400	44	156	661	32	666	945

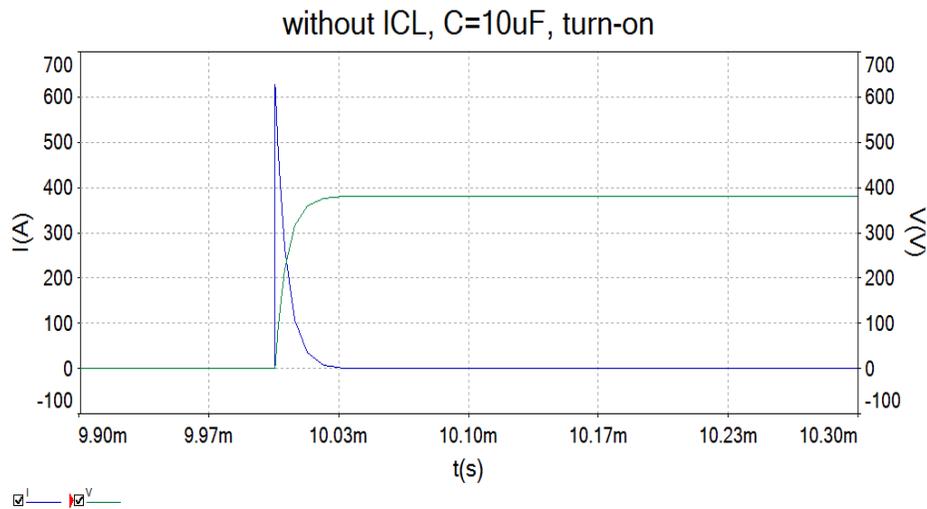


Fig. 8.4.2.1.1: $I-t$, $V-t$ curves without inrush current limiter for 380V input and $C_{\text{filter}}=10\mu\text{F}$ during turn-on

As it can be seen, there is a very high inrush current in this circuit. The magnitude of the inrush current and the settling time increase with the increase of the filter capacitance.

Turn-off

The Table 8.4.2.1.2 and Figure 8.4.2.1.2 display the simulation results for the circuit without ICL at turn-off.

Table 8.4.2.1.2: Simulation results of circuit without inrush current limiter during turn-off

V(V)	$C_{filter}=0.01\mu F$		$C_{filter}=10\mu F$		$C_{filter}=220\mu F$	
	$I_{min}(A)$	Settling time (ns)	$I_{min}(A)$	Settling time (μs)	$I_{min}(A)$	Settling time (μs)
360	-39	156	-595	37	-600	836
370	-40	156	-610	37	-616	836
380	-41	156	-627	37	-632	836
390	-42	156	-644	37	-649	836
400	-44	156	-660	37	-666	836

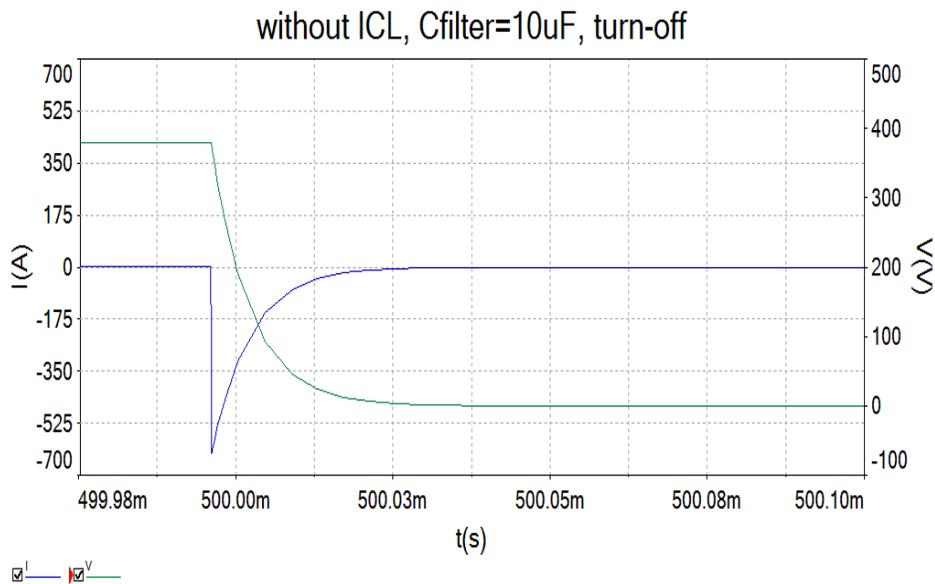


Fig. 8.4.2.1.2: $I-t$, $V-t$ curves without inrush current limiter for 380V input and $C_{filter}=10\mu F$ during turn-off

Here a large negative current is observed with almost the same magnitude as at turn-on. Also, the settling-time is in the same order of magnitude as at turn-on.

8.4.2.2 With Inrush Current Limiter

Turn-on

The following table and figures present the simulation results for the circuit with the ICL during the load turn-on.

Table 8.4.2.2.1: Simulation results of circuit with inrush current limiter during turn-on

V(V)	$C_{\text{filter}}=0.01\mu\text{F}$		$C_{\text{filter}}=10\mu\text{F}$		$C_{\text{filter}}=220\mu\text{F}$	
	$I_{\text{max}}(\text{A})$	Settling time (ms)	$I_{\text{max}}(\text{A})$	Settling time (ms)	$I_{\text{max}}(\text{A})$	Settling time (ms)
360	4.1	58	4.3	64	4.4	65
370	4.2	58	4.4	64	4.5	65
380	4.3	58	4.6	64	4.5	65
390	4.4	58	4.7	64	4.7	65
400	4.5	58	4.7	64	4.8	65

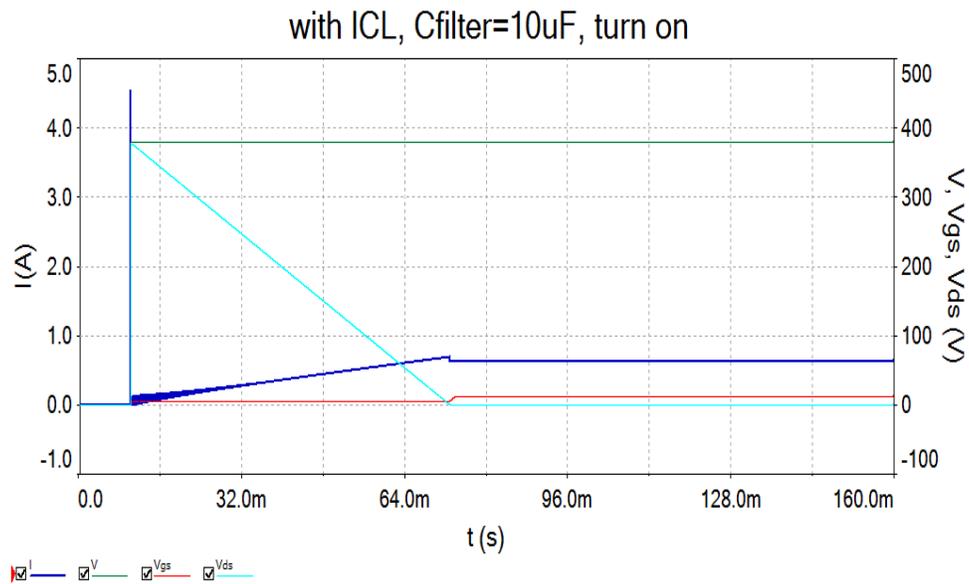


Fig. 8.4.2.2.1: $I-t$, $V-t$, $V_{gs}-t$, $V_{ds}-t$ curves with inrush current limiter for 380V input and $C_{\text{filter}}=10\mu\text{F}$ during turn-on

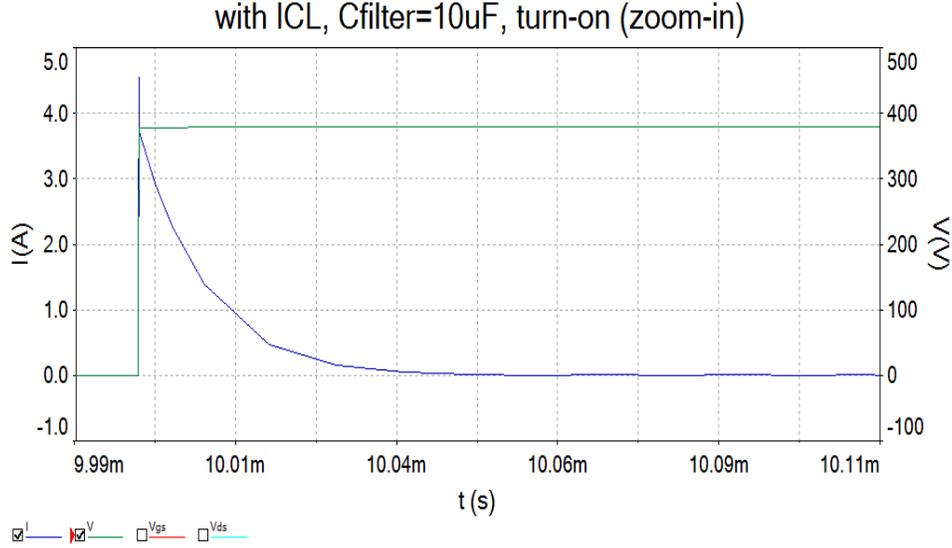


Fig. 8.4.2.2.2: $I-t$, $V-t$ curves with inrush current limiter for 380V input and $C_{filter}=10\mu F$ during turn-on (zoom-in)

As it can be observed from the simulation results presented above, the ICL achieves the goal it was designed for, namely limits the inrush current from a very high level to a safe for the circuit level during turn-on. In other words, the inrush current can be reduced from more than 600A without ICL to less than 5A when the ICL is used. The limiting of the inrush current is followed by an increase in the settling time as it was expected. The settling time in this circuit is around 60ms.

Turn-off

At the load turn-off, the following results were obtained.

Table 8.4.2.2.2: Simulation results of circuit with inrush current limiter during turn-off

V(V)	$C_{filter}=0.01\mu F$		$C_{filter}=10\mu F$		$C_{filter}=220\mu F$	
	$I_{min}(A)$	Settling time (ns)	$I_{min}(A)$	Settling time (μs)	$I_{min}(A)$	Settling time (ms)
360	-39	210	-578	120	-580	14
370	-40	210	-594	120	-600	14
380	-41	210	-610	120	-612	14
390	-42	210	-626	120	-630	14
400	-43	210	-643	120	-650	14

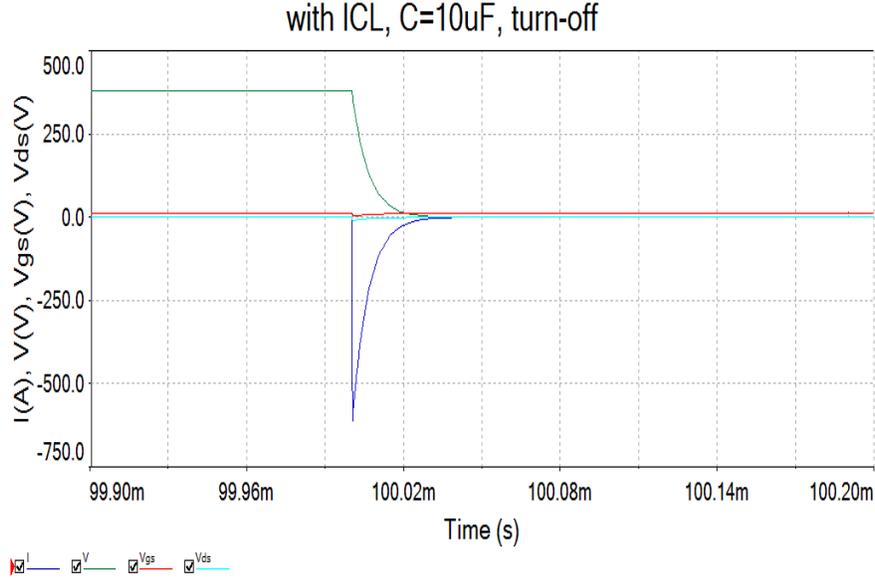


Fig. 8.4.2.2.3: $I-t$, $V-t$, $V_{gs}-t$, $V_{ds}-t$ curves with inrush current limiter for 380V input and $C_{filter}=10\mu F$ during turn-off

As it can be seen from the results above, the ICL has practically no effect on the circuit during the turn-off of the load as the current remains high, as absolute value, when the load is switched-off.

Design Changes

One of the reasons for this high current during turn-off was speculated to be the high dV/dt of the source. As it can be seen, the source voltage goes down from around 400V to 0V in 100ns. This causes the capacitor voltage also to be pulled down to 0 in about 100ns. So the capacitor discharges via the source causing a reverse current spike (as it can be seen in Figure 8.4.2.2.3).

In order to prevent the discharging of the filter capacitor through the source, a diode was added between the source and the ICL, as shown in Figure 8.4.2.2.4. At turn-off, the diode decouples the source from the rest of the circuit so that the discharging of the filter capacitor is done through the load resistance and the ICL only. Therefore, the expected current during turn-off should be smaller and the settling time is longer.

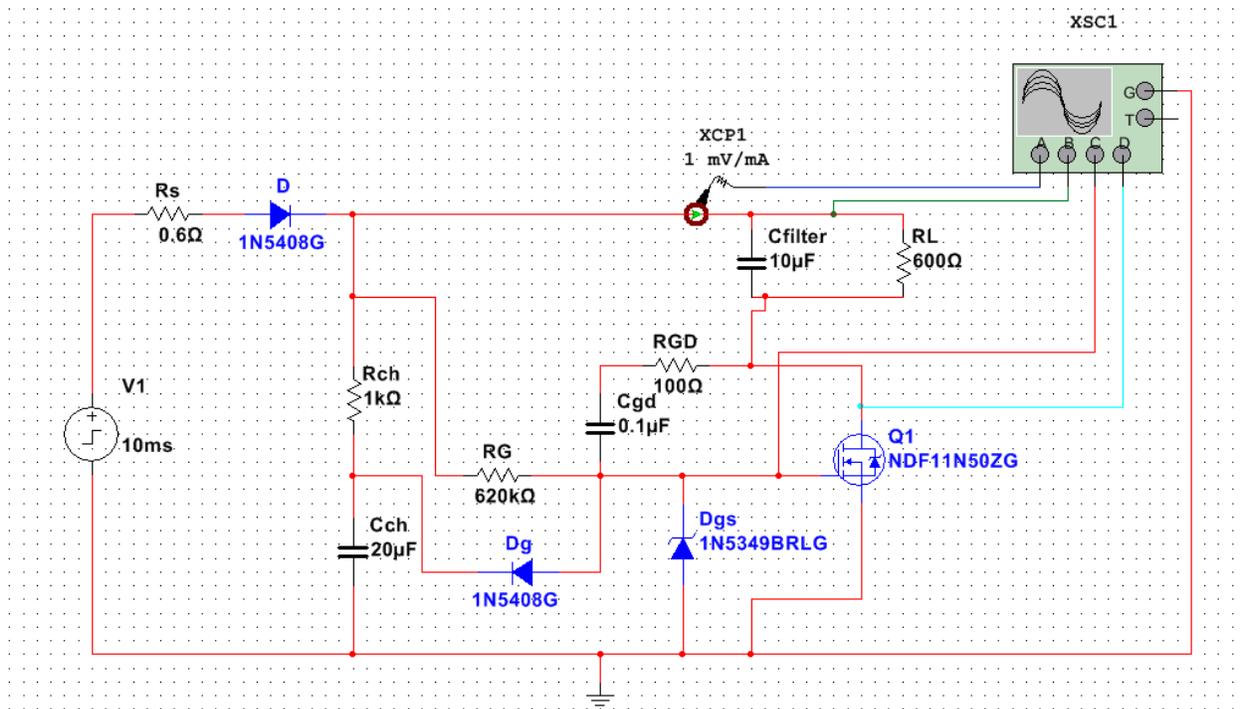


Fig. 8.4.2.2.4: Inrush Current Limiter with decoupling diode

The subsequent tables and figures present the simulation results of the circuit with the ICL and the decoupling diode.

Turn-on

The Table 8.4.2.2.3 and Figure 8.4.2.2.5 present the simulation results for the circuit with the ICL and the decoupling diode during turn-on.

Table 8.4.2.2.3: Simulation results of circuit with inrush current limiter and decoupling diode during turn-on

V(V)	$C_{filter}=0.01\mu F$		$C_{filter}=10\mu F$		$C_{filter}=220\mu F$	
	$I_{max}(A)$	Settling time (ms)	$I_{max}(A)$	Settling time (ms)	$I_{max}(A)$	Settling time (ms)
360	3.8	60	4	64	4	65
370	3.9	60	4.1	64	4.1	65
380	4	60	4.2	64	4.2	65
390	4.1	60	4.3	64	4.3	65
400	4.2	60	4.4	64	4.4	65

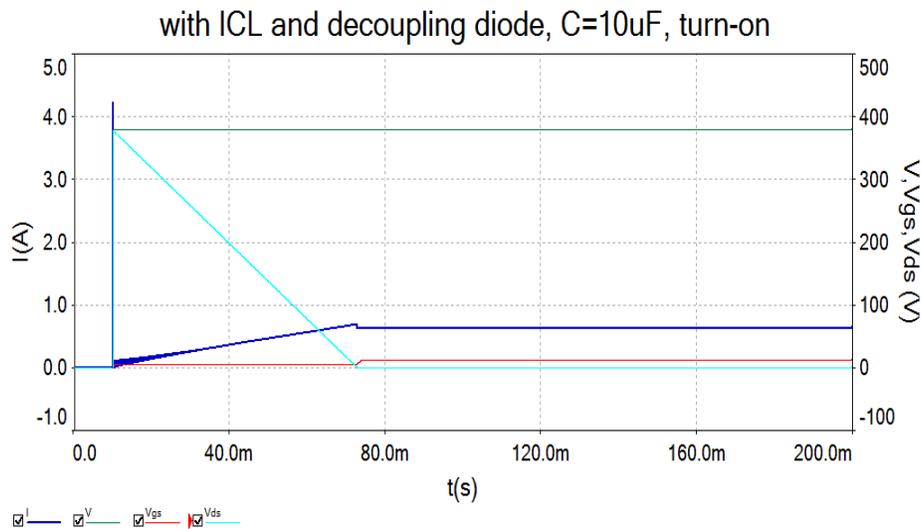


Fig. 8.4.2.2.5: $I-t$, $V-t$, $V_{gs}-t$, $V_{ds}-t$ curves with inrush current limiter and decoupling diode for 380V input and $C_{filter}=10\mu F$ during turn-on

According to the simulation results, the circuit continues to perform very well when the load is switched-on. In this circuit, the inrush current is less than 4.5A and the settling time about 60ms.

Turn-off

The following table and figure display the simulation results of the circuit with the ICL and the decoupling diode during the turn-off of the load.

Table 8.4.2.2.4: Simulation results of circuit with inrush current limiter and decoupling diode during turn-off

V(V)	$C_{filter}=0.01\mu F$		$C_{filter}=10\mu F$		$C_{filter}=220\mu F$	
	$I_{min}(A)$	Settling time (ms)	$I_{min}(A)$	Settling time (ms)	$I_{min}(A)$	Settling time (ms)
360	-0.072	140	-0.072	156	-0.073	590
370	-0.074	140	-0.074	156	-0.075	590
380	-0.075	140	-0.076	156	-0.076	590
390	-0.077	140	-0.078	156	-0.078	590
400	-0.079	140	-0.080	156	-0.080	590

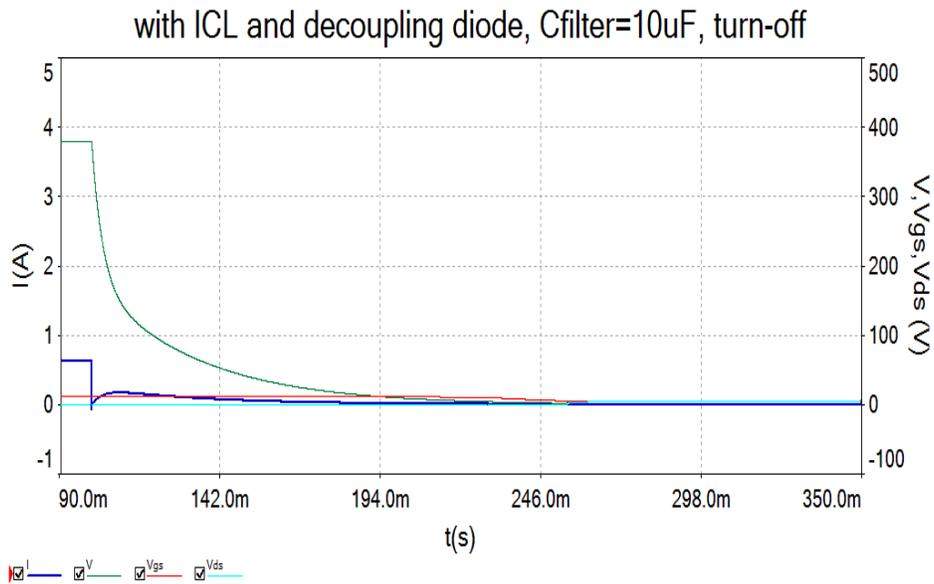


Fig. 8.4.2.2.6: $I-t$, $V-t$, $V_{gs}-t$, $V_{ds}-t$ curves with inrush current limiter and decoupling diode for 380V input and $C_{filter}=10\mu F$ during turn-off

As it can be observed from the simulation results, the maximum inrush current (as absolute value) during turn-off is less than 80mA. Therefore, the high current problem that suffered the circuit without the diode at turn-off has been solved. The settling time is increased as now the discharging of the filter capacitor is done via the load resistance and the ICL and not the voltage source. However, the current remains very low so it cannot damage the circuit.

Note

The results of the circuit with the decoupling diode are in correlation with the experiments as in most power supplies the voltage source is decoupled from the load and hence no negative current peak is seen during the turn-off in the experiments.

8.4.3 Conclusions

In this section the experimental and simulation results of the proposed ICL circuit were presented. Note that the circuit with the decoupling diode is considered for the comparison between the experimental and the simulation results. This is done because the voltage source used for the experiments is decoupled from the load, as no negative current peak is observed at turn-off. If decoupling is not provided by the power source, then a diode should be added.

The experiments showed that high inrush currents flow through the circuit at turn-on even when the ICL is used. On the other hand, the simulations demonstrated that the inrush current is limited to less than 4.5V at turn-on when the proposed ICL is used. At turn-off there is practically no inrush current according to the experimental as well as the simulation results when the decoupling diode is included. Therefore, it can be said that the ICL is able to fulfill the goal it was designed for.

The high inrush currents observed during the experiments are basically caused because of the arcing of the relay. The relay is a mechanical device consisting of movable contacts. When the contacts are moving an electric arc is produced. Due to the mass of the moving contact and any elasticity inherent in the mechanism and/or contact materials, the contacts will bounce when the relay closes or opens, for a period of milliseconds before coming to rest in the final state. This phenomenon is called “contact bounce”. The “contact bounce” can cause ringing when resonance occurs in the circuit (Appendix C). Additionally, it increases the switching arc which interacts with the connected circuit and leads to high frequency oscillations (Sluis, 2001). The oscillations are also increased because of the parasitic inductances (located in the source, load resistor, wiring) and capacitances of the circuit. The high frequency oscillations lead to very fast charging/discharging of the filter capacitor and therefore high dV/dt , which results in high inrush currents.

It is suggested that the experiments are repeated by using another switching device in order to take more accurate measurements. For instance, a solid state relay can be used. These relays do not contain moving parts, so there is no electric arc and therefore no high frequency oscillations that cause the high inrush currents.

Chapter 9: General Conclusions and Recommendations

9.1 Conclusions

This report proposed a DC-DC buck conversion topology with an inrush current limiting circuit that can be used for connecting power consumers to the main bus of a 380V DC micro-grid, such as the one implemented in the test container of the Green Village. The buck converter with the ICL is expected to increase the efficiency of the system and guarantee safety. It should secure the optimum operation of the devices with as less power consumption as possible and near peak efficiency. Additionally, protection is provided by isolating the load side from the rest of the system and eliminating the inrush current and voltage peak during turn-on and turn-off of the device.

Firstly, it was explained that the Green Village will make use of a DC electricity grid due to the various advantages it appears compared to the AC grid. For instance, the DC electricity grid requires reduced power conversion stages from production/storage to consumption and less conductor material. All in all, a DC system has higher efficiency, reliability, stability, faster recovery time and reduced cost.

The DC electricity grid used in the test container is based on the “Femtogrid” system, which is a 380V DC bus system implementing a parallel architecture, which results in an increased efficiency and flexibility. Moreover, the system’s inverter takes care of the safety of the system. Basic components of the system are the solar panels, the power optimizers (boost converter with MPPT) and the buck converter with ICL, which is the subject of this project.

The basic principles and operation modes of the boost and buck converters were explained and a literature study regarding the control methods of DC-DC converters was executed. The Perturb and Observe method is the MPPT control method used by the system’s power optimizer.

Then, the models of the components of the “Femtogrid” system (solar panel, power optimizer, buck converter) were built in Simulink/Matlab. The converters models were made based on their state-space equations.

Experiments were executed with common electronic devices in order to investigate their behavior with DC and AC power supply. As it was expected, the tests proved that common appliances can operate with DC voltage. It is interesting to notice that some devices even perform better when supplied with DC voltage. For example, the television and monitor, used in the experiments, appear to consume less power when operate on DC and the adapter has a better efficiency with DC input. This can be explained

if one considers the fact that the rectification stage of the device's power supply is skipped and as a result the device appears less loss.

The experiments also showed that the devices appear high inrush currents at turn-on, which when exceed a level, result in high voltage drops. The settling time is in the order of *ms* or *100-ds* of μs . These high inrush currents can severely stress and damage the components and the equipment of the system and therefore should be limited.

Furthermore, three lamps (energy saving, incandescent and LED) were tested and compared. The experiments showed that the LED lamp has the best performance compared to the other two for both DC and AC tests. LED lamps appear a better light emission efficiency and less power consumption. This explains why the Green Village will implement the LED technology.

The DC-DC buck converter topology proposed by this report for use in the electricity system of the test container is the LLC resonant converter. This topology was selected because it appears a very high efficiency (96.62%), it guarantees isolation, makes use of a small number of components, achieves ZVS, has low switching losses and low voltage stress, low turn off switching current and high power density.

The inrush current limiter (ICL) that aims to protect the buck converter and load from high inrush currents proposed here, consists of a MOSFET which is driven by a circuit of some passive components (capacitors and resistors). The driving circuit performs a dv/dt control to the MOSFET drain-source voltage, while at the same time, it takes care of keeping the gate voltage below the threshold value until the inrush current is reduced to a safe level so that the voltage control is not lost.

The proposed ICL was simulated and a prototype was built and tested. The simulations showed that the ICL is able to limit the inrush current to a safe for the circuit level (less than 4.5A) at turn-on. At turn-off, there is practically no current peak when a decoupling diode is added to the circuit.

According to the experimental results, high inrush currents were detected at turn-on. It is important to mention that an electromechanical relay was used as the switching device during the experiments because of lack of other choices. It is believed that these high currents are basically caused because of the high frequency oscillations produced by the electric arc that appears between the relay contacts and are increased by the "contact bounce" and parasitic inductances and capacitances of the circuit.

9.2 Recommendations

As it was explained before, the ICL should be able to limit the inrush current, however the experimental results showed high inrush currents that are believed to be caused because of the electromechanical relay that was included in the experimental setup. Therefore, it is suggested that the experiments are repeated by using a more accurate switch, a solid state relay for instance. With this type of relay no arc is produced as it has no moving parts.

Moreover, a control method for the buck converter should be decided. The Simulink models built here can be used in combination with models for the ICL, load and buck controller in order to simulate the overall test container's electricity system. By doing so, the performance of the buck converter with the ICL can be investigated in simulation level. The results taken from the integral model can verify the real measurements or reveal possible problems. What is more, a complete system model, including possible storage facilities, like batteries or super capacitors, could serve for examining the operation of the system and the dynamic behavior of the DC bus.

In addition, a buck converter prototype should be built and tested. This converter will have the following specifications: $380V_{in}$, $(100-300)V_{out}$, $250W$, $100kHz$. The LLC resonant converter topology was proposed here. The prototype should also be tested in combination with the ICL, the DC bus and the loads. Then, the dynamic behavior of the DC bus (voltage level variation) can also be investigated during turn-on and turn-off of the load. At a later stage, the converter can be placed in the test container and tested with the real circuit.

Finally, as shown from the experiments, the common electronic appliances used today, operate properly when supplied with DC voltage. What is more, some electronic devices have even a better performance with DC power supply. A repetition of the experiments done with the lamps with a power-meter of lower range than the one used in this project is recommended in order to verify their behavior.

Although the common electronic devices operate without problem with their current structure (made for AC), a future modification would be interesting. The rectification stage, that is now used by the power supplies for converting the input AC voltage to DC, and the filter capacitor (that causes the high inrush current problem), which is used for smoothening out the DC output of the rectifier, could be removed in a future DC world. Also, the DC-DC converter used by the power supply could possibly be removed, as the buck converter proposed in this project would provide the load with the necessary for its operation voltage level. Such modifications would result in less power losses, higher reliability, better efficiency and would reduce the inrush current problems that are caused because of the filter capacitors.

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Appendices

Appendix A: Datasheets

Appendix A (i): Solar Panel Suntech STP 280-24Vd Datasheet

STP280 - 24/Vd



280 Watt

POLYCRYSTALLINE SOLAR MODULE

Features



High module conversion efficiency
(up to 14.4%), through superior cell technology and leading manufacturing capability



Positive tolerance
Guaranteed positive tolerance from 0~5% ensures power output reliability



Suntech's TruPower™
Suntech's TruPower™ process neutralizes the initial LID effect



Excellent weak light performance
Excellent performance under low light environments (mornings, evenings, and cloudy days)



Withstand high wind and snow loads
Entire module certified to withstand high wind loads (2400 Pascal) and snow loads (5400 Pascal) *



Suntech current sorting process
All Suntech modules sorted and packaged by amperage, maximizing system output by reducing mismatch losses by up to 2%



Certifications and standards:
IEC 61215, IEC 61730, conformity to CE



Trust Suntech to Deliver Reliable Performance Over Time

- World's No.1 manufacturer of crystalline silicon photovoltaic modules
- Unrivaled manufacturing capacity and world-class technology
- Rigorous quality control meeting the highest international standards : ISO 9001: 2008 and ISO 14001: 2004

Industry-leading warranty



- Warrants 6.7% more power than the market standard over 25 years
- 25-year transferrable power output warranty: 5 years/95%, 12 years/90%, 18 years/85%, 25 years/80% **
- Based on nominal power
- 5 years material and workmanship warranty



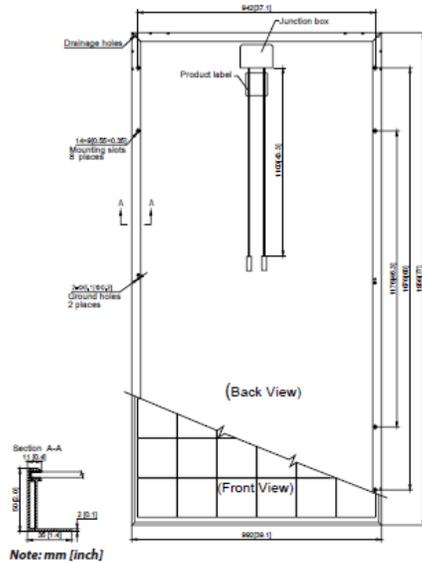
Specially designed drainage holes and rigid construction prevent frame from deforming or breaking due to freezing weather and other forces.



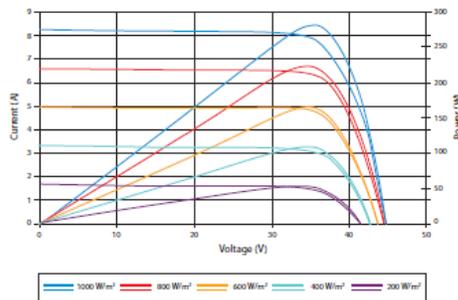
Latest IP67 rated junction box improves module performance stability. High performance connectors provide low resistance interconnection to ensure the full utilization of module power output.

* Please refer to Suntech Standard Module Installation Manual for details.
** Please refer to Suntech Product Warranty for details.

STP280 - 24/Vd



Current-Voltage & Power-Voltage Curve (280-24)



Excellent performance under weak light conditions: at an irradiance intensity of 200 W/m² (AM 1.5, 25 °C), 95.5% or higher of the STC efficiency (1000 W/m²) is achieved

Temperature Characteristics

Nominal Operating Cell Temperature (NOCT)	45±2°C
Temperature Coefficient of Pmax	-0.44 %/°C
Temperature Coefficient of Voc	-0.33 %/°C
Temperature Coefficient of Isc	0.055 %/°C

Dealer information

Specifications are subject to change without further notification

Electrical Characteristics

STC	STP280-24/Vd
Optimum Operating Voltage (Vmp)	35.2 V
Optimum Operating Current (Imp)	7.95 A
Open - Circuit Voltage (Voc)	44.8 V
Short - Circuit Current (Isc)	8.33 A
Maximum Power at STC (Pmax)	280 W
Module Efficiency	14.4%
Operating Module Temperature	-40 °C to +85 °C
Maximum System Voltage	1000 V DC (IEC) / 600 V DC (UL)
Maximum Series Fuse Rating	20 A
Power Tolerance	0/+5 %

STC: Irradiance 1000 W/m², module temperature 25 °C, AM=1.5;
Power measurement tolerance: ± 3%

NOCT	STP280-24/Vd
Maximum Power (W)	204 W
Maximum Power Voltage (V)	32.0 V
Maximum Power Current (A)	6.39 A
Open Circuit Voltage (Voc)	40.8 V
Short Circuit Current (Isc)	6.74 A

NOCT: Irradiance 800 W/m², ambient temperature 20 °C, wind speed 1 m/s;
Power measurement tolerance: ± 3%

Mechanical Characteristics

Solar Cell	Polycrystalline 156 × 156 mm (6 inches)
No. of Cells	72 (6 × 12)
Dimensions	1956 × 992 × 50 mm (77.0 × 39.1 × 2.0 inches)
Weight	27.0 kgs (59.5 lbs.)
Front Glass	4.0 mm (0.16 inches) tempered glass
Frame	Anodized aluminium alloy
Junction Box	IP67 rated
Output Cables	TUV (2Pfg1169:2007), UL 4703, UL 44 4.0 mm ² (0.006 inches ²), symmetrical lengths (-) 1100 mm (43.3 inches) and (+) 1100 mm (43.3 inches)
Connectors	RADOX® SOLAR integrated twist locking connectors

Packing Configuration

Container	20' GP	40' GP	40' HC
Pieces per pallet	21	21	21
Pallets per container	6	12	24
Pieces per container	126	252	504

Appendix A (ii): Wind turbine Jetpro JPS-200 Datasheet

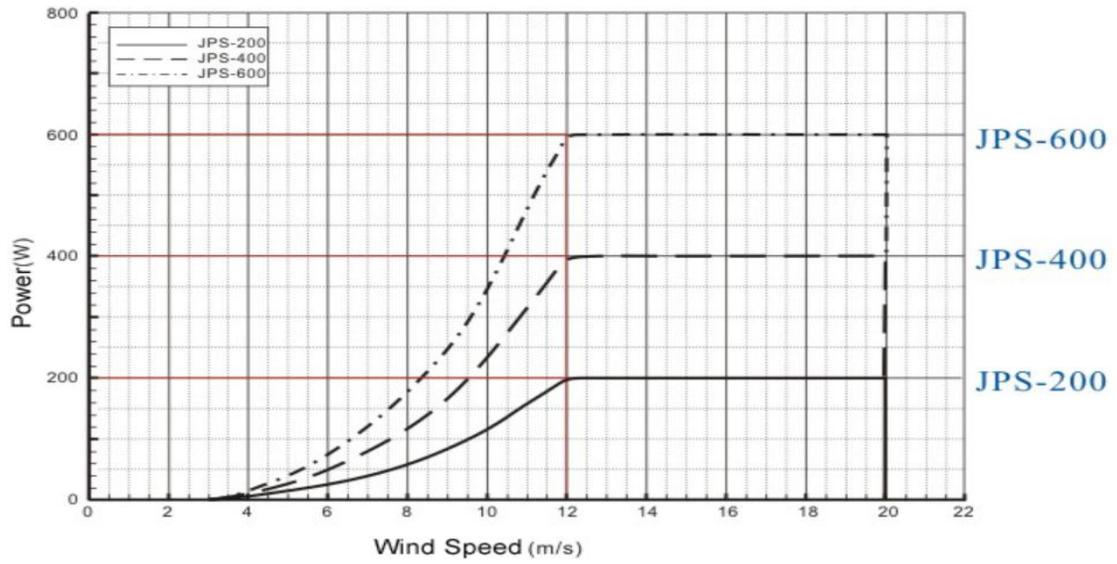


Our Products > JPS-200

Jetpro General Specifications

Shrouded Design	YES
Generators	Permanent Magnet Generator
Rated Power (W)	200
Voltage Output (Vdc)	12V/24V/48V
Rotor Diameter (m)	0.68
Number of Blades/set	5
Start-up Wind Speed (m/s)	3
Rated Wind Speed (m/s)	12
Cut-out Wind Speed (m/s)	20
Total Dimension (mm)	1026 X 912 X 330
Weight(kg)	10
Cascaded	N/A
YAW	Shroud Wind Force Automatic Adjustment
Brake	Electrical





Appendix A (iii): Technical Specifications of Femtogrid PV300 Power Optimizer

Solar Input (DC from PV modules)		
Maximum DC power	300	W
Nominal DC power	250	W
MPPT operating voltage range	8 - 42	Vdc
Maximum DC current	10	A
MPPT	decentralized per module	
Compatible with types of modules	mono- and polycrystalline	
Power Optimizer Output (DC in operation)		
Nominal DC power	250	W
Nominal output voltage (Femtogrid voltage)	380	Vdc
Maximum output current	0.8	A
Maximum efficiency	97.4	%
MPPT efficiency	>99	%
Efficiency, European related (Euro ETA)	95.7	%
Standard Compliance		
EMC: Immunity	EN61000-4-2/3/4/5/6/11	
EMC: Emission	EN55022/EN60601-1-2	
	EN55022/EN61000-3-3	
Safety	EN60950	
CE/RoHS/WEEE/REACH	Yes	
Safety class	Class II	
Degree of protection	IP65	
General		
Relative humidity (non-condensing)	0 - 95	% RH
Dimensions with bracket (WxLxH)	288x342x51	mm
Ambient temperature	-40/+65	°C
Weight	1.45	kg
DC connections	MC4	Type
Output connections	Custom made by Wieland for Femtogrid	Type
Switch-on power	0.5	W
Safetyline voltage ('neutral')	48	V
Femtogrid feed through current in-out	20	A

Appendix A (iv): Technical Specifications of Femtogrid Inverter 2400

Solar Input (DC from solar panels)		
Maximum DC power	2550	Wdc
Recommended PV Power range	500 - 3000	Wdc
Nominal DC operating voltage	360 - 400	Vdc
Minimum input voltage for rated output	380	Vdc
Maximum DC current	6.7	Adc
MPPT	@Femtogrid Solar Power Optimizer	
Isolated transformer	Galvanic isolation	
Mains output (AC)		
Maximum AC Power (@tamb 25°C)	2400	Wac
Nominal AC Power	2200	Wac
Nominal output voltage range (country specific)	184 - 265	Vac
Maximum output current (continuous)@230 V	10.5	Aac
Maximum efficiency	96	%
Efficiency, European related (Euro ETA)	94.6	%
Power factor	1	
Frequency (country specific)	45 - 55	Hz
Standard Compliance		
EMC: Immunity	EN61000-4-2/3/4/5/6/11	
EMC: Emission	EN55022/EN60601-1-2 EN55022/EN61000-3-3	
Grid connection standards	NEN-EN 50438/VDE0126-1-1	
CE/RoHS/WEEE/REACH	Yes	
Safety class	Class I	
Degree of protection	IP31	
Temperature protection	>80	°C
General		
Wireless communication	ZigBee	
Dimensions (WxLxH)	323x202x646	mm
Ambient temperature	0 - 40	°C
Weight	38	kg
DC connections	Custom made by Wieland for Femtogrid	Type
Output connections	Wieland	Type
Area of application	Indoor	

Appendix A (v): Technical Specifications of Femtogrid DC cables

Femtogrid DC Cable		
Type	Diameter over insulation	Outer diameter
3 x 2.5 mm ²	3.4 mm	9.1±0.2 mm

Properties Femtogrid DC Cable	
Flame retardent	EN 60332-1-2
Halogen free	EN 50267-2-1 and EN 60684-2
Temperature range	Ambient -40 °C to +90 °C
Max. conductor resistance @ 20 °C (Ω/km)	8.21
Colour of insulation	Red (+), blue (-) and black (0)
DC connectors	Custom made by Wieland for Femtogrid
Properties Femtogrid DC connectors	
Degree of protection	IP66/IP68
Housing material	Polyamide
Halogen free	Yes
Femtogrid feed through current in-out	Max. 20 A
Temperature range	Ambient -40 °C to +90 °C



Appendix A (vi): Technical Specifications of Vishay BPW34 Photodiode



www.vishay.com

BPW34, BPW34S

Vishay Semiconductors

Silicon PIN Photodiode



94 8283

DESCRIPTION

BPW34 is a PIN photodiode with high speed and high radiant sensitivity in miniature, flat, top view, clear plastic package. It is sensitive to visible and near infrared radiation. BPW34S is packed in tubes, specifications like BPW34.

FEATURES

- Package type: leaded
- Package form: top view
- Dimensions (L x W x H in mm): 5.4 x 4.3 x 3.2
- Radiant sensitive area (in mm²): 7.5
- High photo sensitivity
- High radiant sensitivity
- Suitable for visible and near infrared radiation
- Fast response times
- Angle of half sensitivity: $\varphi = \pm 65^\circ$
- Compliant to RoHS Directive 2002/95/EC and in accordance to WEEE 2002/96/EC



RoHS
COMPLIANT
GREEN
RE-ADDED**

Note

** Please see document "Vishay Material Category Policy":
www.vishay.com/doc?99902

APPLICATIONS

- High speed photo detector

PRODUCT SUMMARY			
COMPONENT	I_{ra} (μA)	φ (deg)	$\lambda_{0.1}$ (nm)
BPW34	50	± 65	430 to 1100
BPW34S	50	± 65	430 to 1100

Note

- Test condition see table "Basic Characteristics"

ORDERING INFORMATION			
ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
BPW34	Bulk	MOQ: 3000 pcs, 3000 pcs/bulk	Top view
BPW34S	Tube	MOQ: 1800 pcs, 45 pcs/tube	Top view

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage		V_R	60	V
Power dissipation	$T_{amb} \leq 25\text{ }^{\circ}\text{C}$	P_V	215	mW
Junction temperature		T_J	100	$^{\circ}\text{C}$
Operating temperature range		T_{amb}	- 40 to + 100	$^{\circ}\text{C}$
Storage temperature range		T_{stg}	- 40 to + 100	$^{\circ}\text{C}$
Soldering temperature	$t \leq 3\text{ s}$	T_{sd}	260	$^{\circ}\text{C}$
Thermal resistance junction/ambient	Connected with Cu wire, 0.14 mm ²	R_{thJA}	350	K/W



www.vishay.com

BPW34, BPW34S

Vishay Semiconductors

BASIC CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Breakdown voltage	$I_R = 100\text{ }\mu\text{A}$, $E = 0$	$V_{[BR]}$	60			V
Reverse dark current	$V_R = 10\text{ V}$, $E = 0$	I_{r0}		2	30	nA
Diode capacitance	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$, $E = 0$	C_D		70		pF
	$V_R = 3\text{ V}$, $f = 1\text{ MHz}$, $E = 0$	C_D		25	40	pF
Open circuit voltage	$E_0 = 1\text{ mW/cm}^2$, $\lambda = 950\text{ nm}$	V_{oc}		350		mV
Temperature coefficient of V_{oc}	$E_0 = 1\text{ mW/cm}^2$, $\lambda = 950\text{ nm}$	$TK_{V_{oc}}$		- 2.6		mV/K
Short circuit current	$E_A = 1\text{ klx}$	I_k		70		μA
	$E_0 = 1\text{ mW/cm}^2$, $\lambda = 950\text{ nm}$	I_k		47		μA
Temperature coefficient of I_k	$E_0 = 1\text{ mW/cm}^2$, $\lambda = 950\text{ nm}$	TK_{I_k}		0.1		%/K
Reverse light current	$E_A = 1\text{ klx}$, $V_R = 5\text{ V}$	I_{rs}		75		μA
	$E_0 = 1\text{ mW/cm}^2$, $\lambda = 950\text{ nm}$, $V_R = 5\text{ V}$	I_{rs}	40	50		μA
Angle of half sensitivity		ϕ		± 65		deg
Wavelength of peak sensitivity		λ_p		900		nm
Range of spectral bandwidth		$\lambda_{0.1}$		430 to 1100		nm
Noise equivalent power	$V_R = 10\text{ V}$, $\lambda = 950\text{ nm}$	NEP		4×10^{-14}		W/ $\sqrt{\text{Hz}}$
Rise time	$V_R = 10\text{ V}$, $R_L = 1\text{ k}\Omega$, $\lambda = 820\text{ nm}$	t_r		100		ns
Fall time	$V_R = 10\text{ V}$, $R_L = 1\text{ k}\Omega$, $\lambda = 820\text{ nm}$	t_f		100		ns

BASIC CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

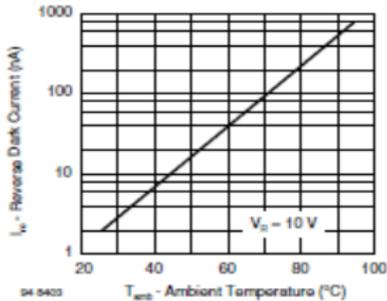


Fig. 1 - Reverse Dark Current vs. Ambient Temperature

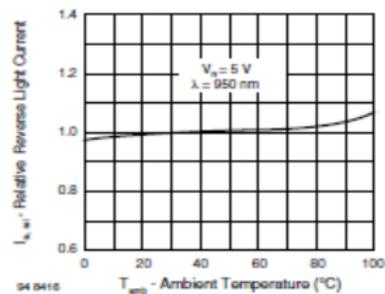
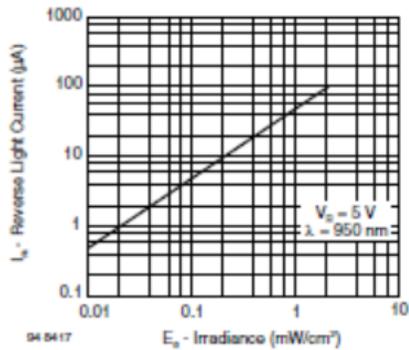
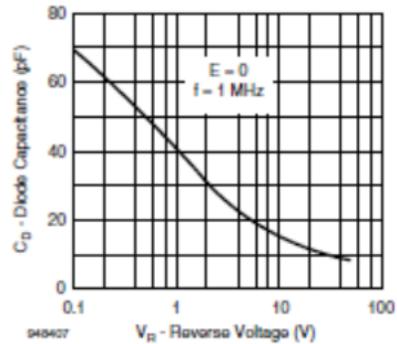


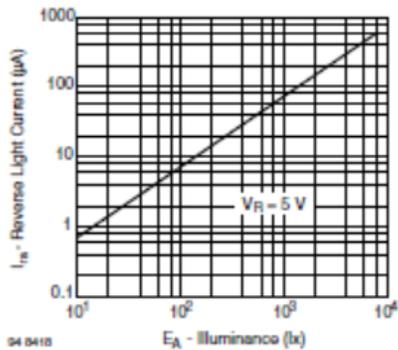
Fig. 2 - Relative Reverse Light Current vs. Ambient Temperature



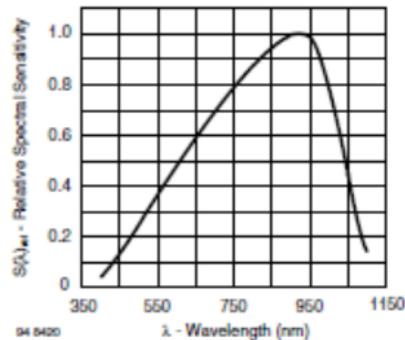
04 0417
Fig. 3 - Reverse Light Current vs. Irradiance



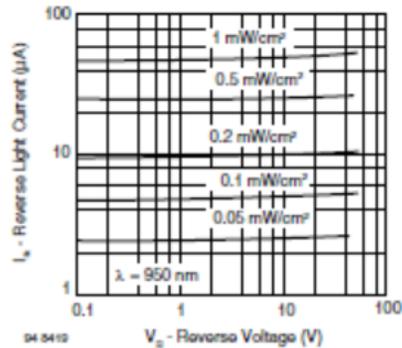
04 0427
Fig. 6 - Diode Capacitance vs. Reverse Voltage



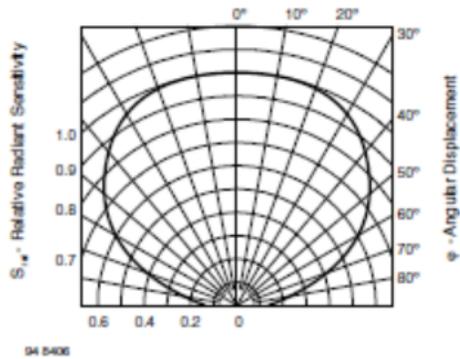
04 0418
Fig. 4 - Reverse Light Current vs. Illuminance



04 0420
Fig. 7 - Relative Spectral Sensitivity vs. Wavelength



04 0419
Fig. 5 - Reverse Light Current vs. Reverse Voltage



04 0426
Fig. 8 - Relative Radiant Sensitivity vs. Angular Displacement

Appendix A (vii): Technical Specifications of MOSFET IXYS

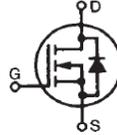


PolarHV™ HiPerFET Power MOSFET

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode

IXFK 64N50P
IXFX 64N50P

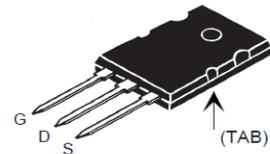
$V_{DSS} = 500 \text{ V}$
 $I_{D25} = 64 \text{ A}$
 $R_{DS(on)} \leq 85 \text{ m}\Omega$
 $t_{rr} \leq 200 \text{ ns}$



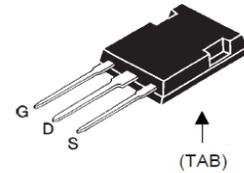
Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	500	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	500	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ\text{C}$	64	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	150	A
I_{AR}	$T_C = 25^\circ\text{C}$	64	A
E_{AR}	$T_C = 25^\circ\text{C}$	80	mJ
E_{AS}	$T_C = 25^\circ\text{C}$	2.5	J
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 4 \Omega$	20	V/ns
P_D	$T_C = 25^\circ\text{C}$	830	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
M_d	Mounting torque (TO-264)	1.13/10	Nm/lb.in.
Weight	TO-264	10	g
	PLUS247	6	g
T_L	1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
T_{SOLD}	Plastic body for 10 s	260	$^\circ\text{C}$

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8 \text{ mA}$	3.0		5.5 V
I_{GSS}	$V_{GS} = \pm 30 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 200 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$ $V_{GS} = 0 \text{ V}$ $T_J = 125^\circ\text{C}$			25 μA
				1000 μA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2\%$			85 $\text{m}\Omega$

TO-264 (IXFK)



PLUS247 (IXFX)



G = Gate D = Drain
S = Source Tab = Drain

Features

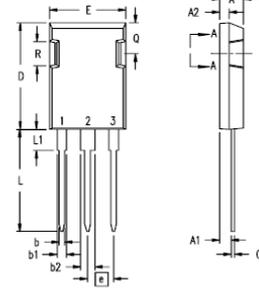
- ! International standard packages
- ! Fast recovery diode
- ! Unclamped Inductive Switching (UIS) rated
- ! Low package inductance
- easy to drive and to protect

Advantages

- ! Easy to mount
- ! Space savings
- ! High power density

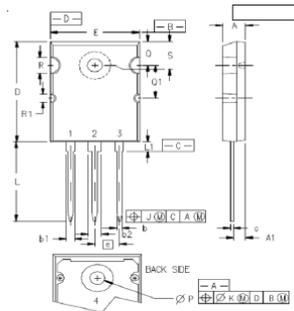
Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{ V}$; $I_D = 0.5 I_{D25}$, pulse test	30	50	S
C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$		8700	pF
C_{oss}			970	pF
C_{rss}			90	pF
$t_{d(on)}$	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.5 V_{DSS}$, $I_D = 0.5 I_{D25}$ $R_G = 2\ \Omega$ (External)		30	ns
t_r			25	ns
$t_{d(off)}$			85	ns
t_f			22	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.5 V_{DSS}$, $I_D = 0.5 I_{D25}$		150	nC
Q_{gs}			50	nC
Q_{gd}			50	nC
R_{thJC}			0.15	$^\circ\text{C/W}$
R_{thCS}		0.15		$^\circ\text{C/W}$

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{ V}$			64 A
I_{SM}	Repetitive			150 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			1.5 V
t_{rr}	$I_F = 25\text{ A}$, $-di/dt = 100\text{ A}/\mu\text{s}$ $V_R = 100\text{ V}$			200 ns
Q_{RM}			0.6	
I_{RM}			6.0	A

PLUS 247™ (IXFX) Outline


Terminals: 1 - Gate
 2 - Drain (Collector)
 3 - Source (Emitter)
 4 - Drain (Collector)

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.83	5.21	.190	.205
A ₁	2.29	2.54	.090	.100
A ₂	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b ₁	1.91	2.13	.075	.084
b ₂	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

TO-264 (IXFK) Outline


1 - GATE
 2, 4 - DRAIN (COLLECTOR)
 3 - SOURCE (EMITTER)

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215 BSC		5.46 BSC	
J	.000	.010	0.00	0.25
K	.000	.010	0.00	0.25
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
ØP	.122	.138	3.10	3.51
Q	.240	.256	6.10	6.50
Q1	.350	.346	8.38	8.79
ØR	.195	.187	3.94	4.75
ØR1	.085	.093	2.16	2.36
S	.243	.293	6.17	6.43

Fig. 1. Output Characteristics
@ 25°C

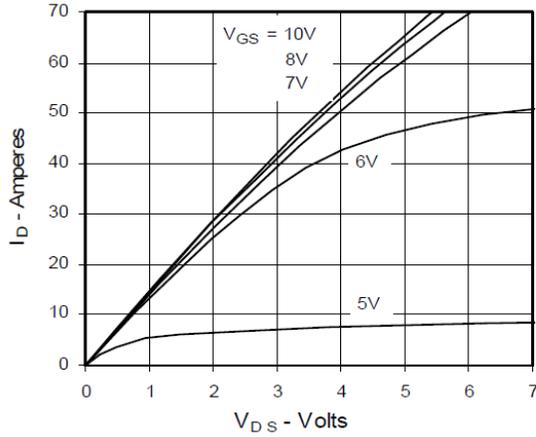


Fig. 2. Extended Output Characteristics
@ 25°C

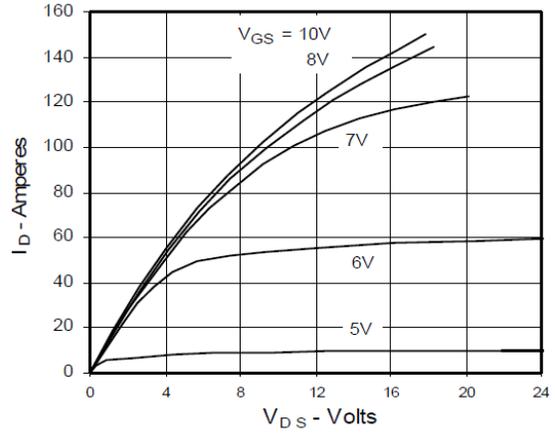


Fig. 3. Output Characteristics
@ 125°C

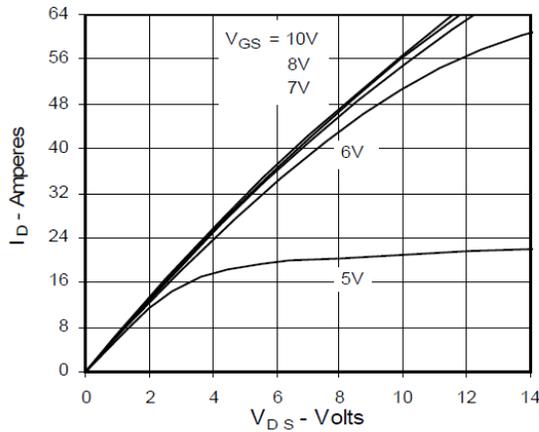


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25}
Value vs. Junction Temperature

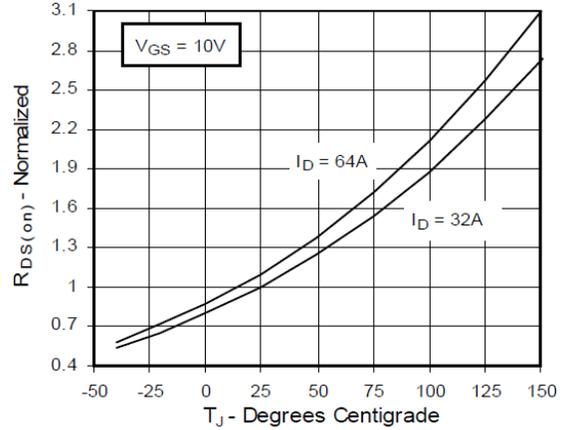


Fig. 5. $R_{DS(on)}$ Normalized to
0.5 I_{D25} Value vs. I_D

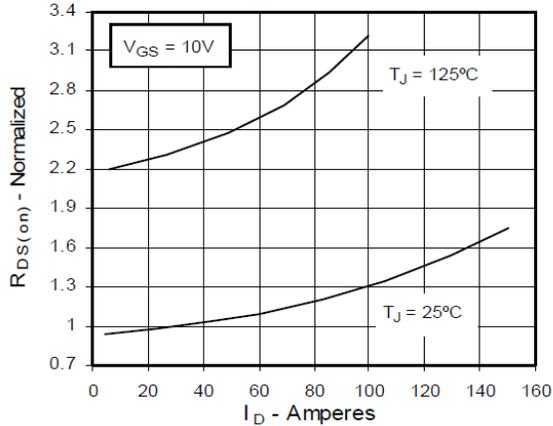


Fig. 6. Drain Current vs. Case
Temperature

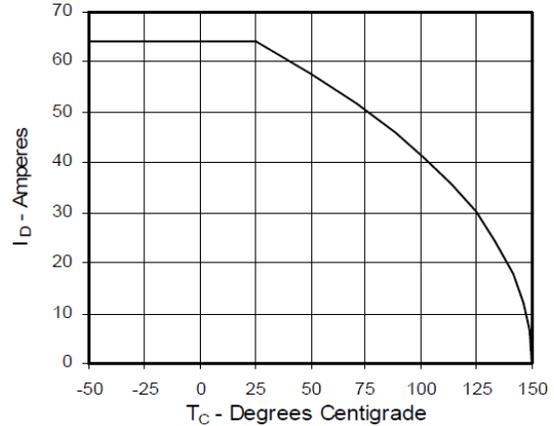


Fig. 7. Input Admittance

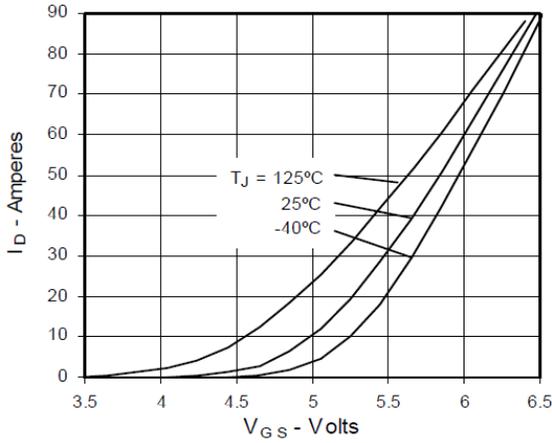


Fig. 8. Transconductance

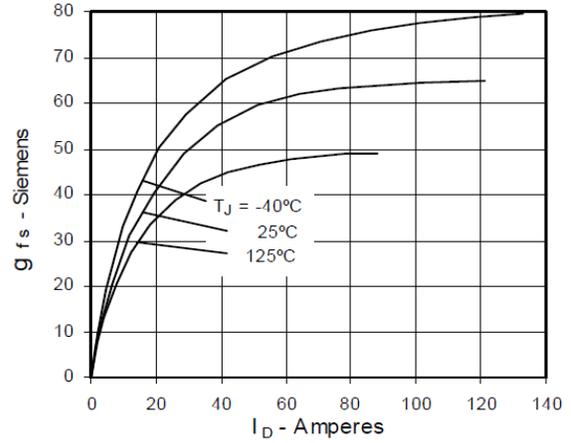


Fig. 9. Source Current vs. Source-To-Drain Voltage

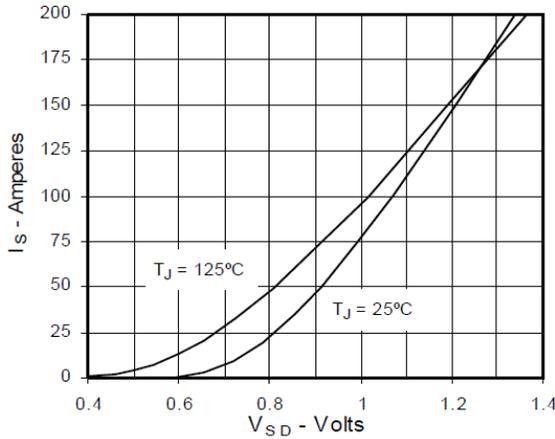


Fig. 10. Gate Charge

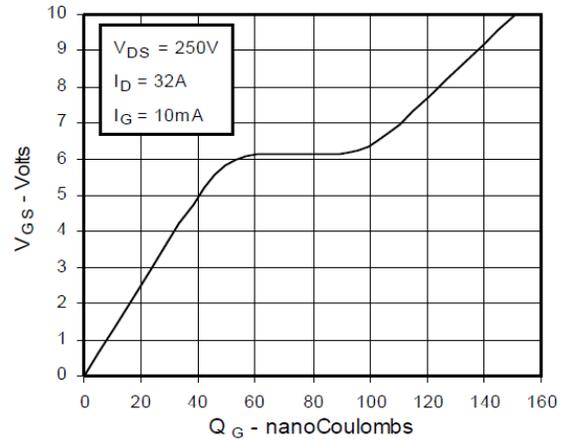


Fig. 11. Capacitance

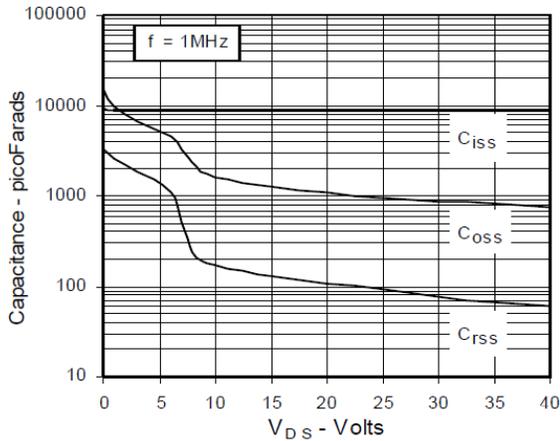
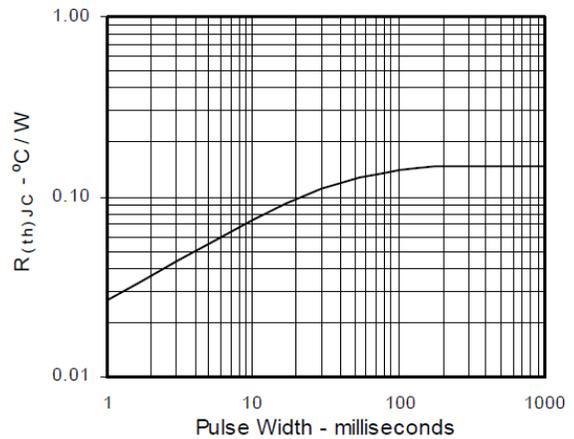
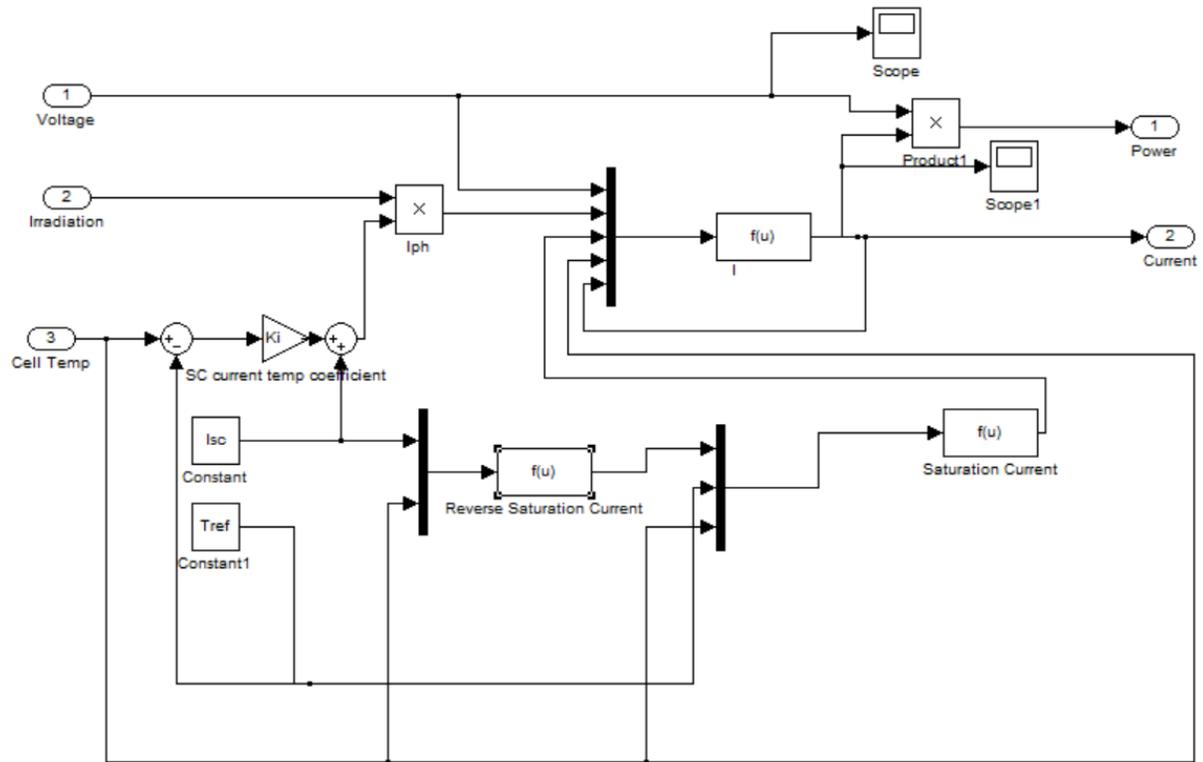


Fig. 12. Maximum Transient Thermal Resistance

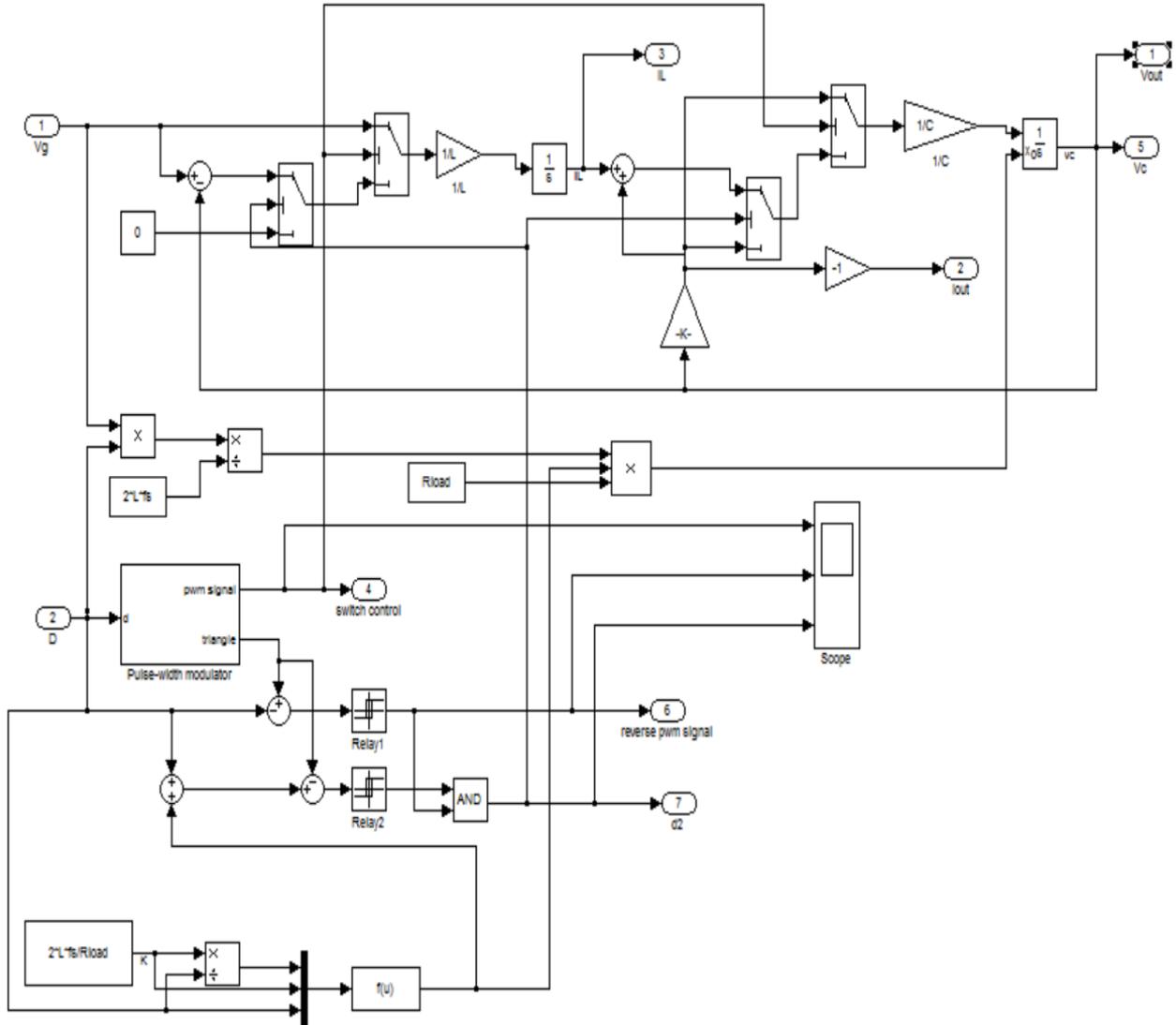


Appendix B: Simulink/Matlab Models

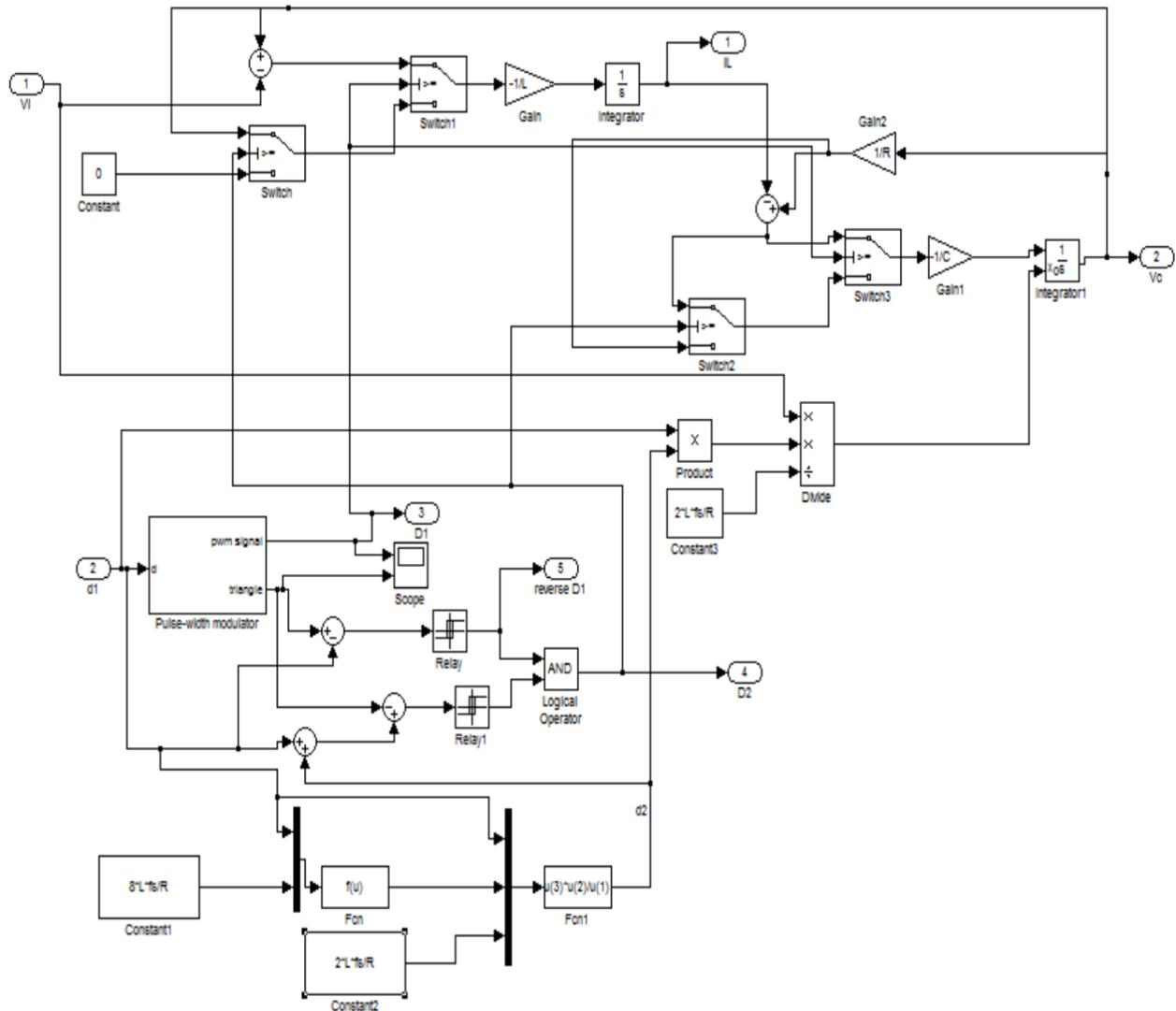
Appendix B (i): Simulink Model of Solar Panel



Appendix B (ii): Simulink Model of Boost Converter operating in DCM



Appendix B (iii): Simulink Model of Buck Converter Operating in DCM



Appendix B (iv): Matlab Code for Perturb and Observe Method

```
function D = MPPT(V,I)

Dinit=0.5;
Dmax=1;
Dmin=0;
pD=0.001; % duty cycle step

persistent Vold Pold Dold

if isempty(Vold) % initial values
    Pold=0;
    Vold=0;
    Dold=Dinit;
end

P=V*I;
DP=P-Pold; % calculate power change
DV=V-Vold; % calculate voltage change

if DP~=0 % if not at the MPP
    if DP>0 % check power change
        if DV>0 % check voltage change
            D=Dold-pD; % if power change positive and voltage change
            positive, decrease duty cycle by step
        else
            D=Dold+pD; % if power change positive and voltage change
            negative, increase duty cycle by step
        end
    else
        if DV>0 % check voltage change
            D=Dold+pD; % if power change negative and voltage change
            positive, increase duty cycle by step
        else
            D=Dold-pD; % if power change negative and voltage change
            negative, decrease duty cycle by step
        end
    end
else
    D=Dold; % if at the MPP, keep duty cycle same
end

if D>=Dmax | D<=Dmin % check if duty cycle value is valid
    D=Dold;
end

Dold=D; % keep old values
Vold=V;
Pold=P;
```

Appendix C: Ringing because of Relay “Contact Bounce”

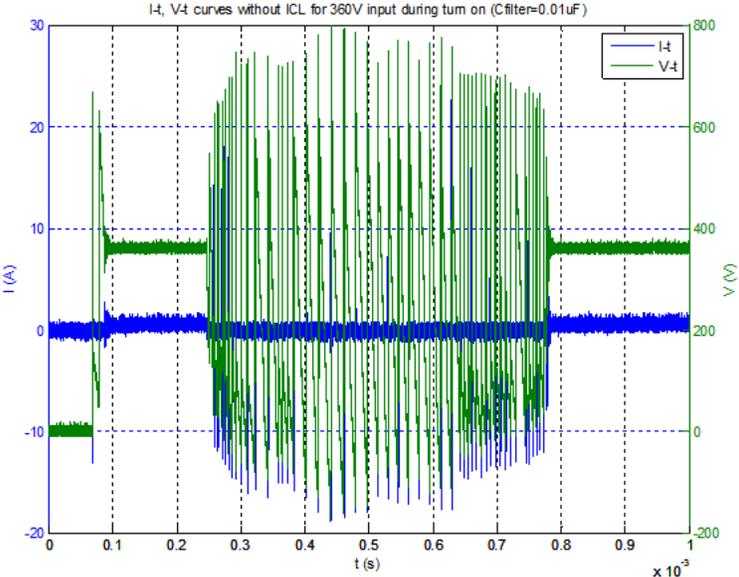


Fig. a: *I-t*, *V-t* curves without inrush current limiter for 360V input during turn-on and $C_{filter}=0.01\mu F$

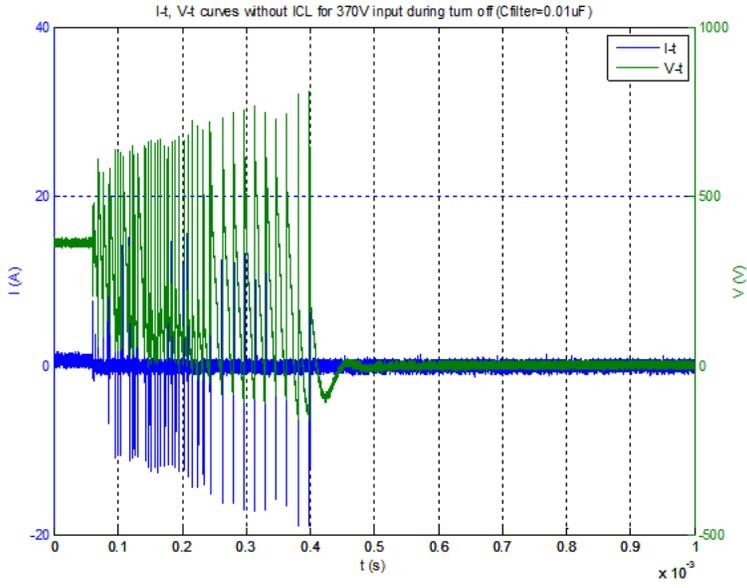


Fig. b: $I-t$, $V-t$ curves without inrush current limiter for 360V input during turn-off and $C_{filter}=0.01\mu F$

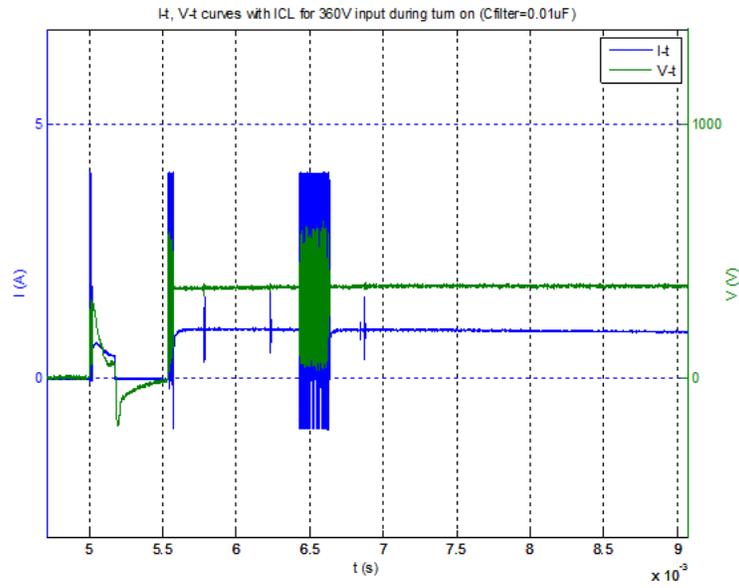


Fig. c: $I-t$, $V-t$ curves with inrush current limiter for 370V input during turn-on and $C_{filter}=0.01\mu F$

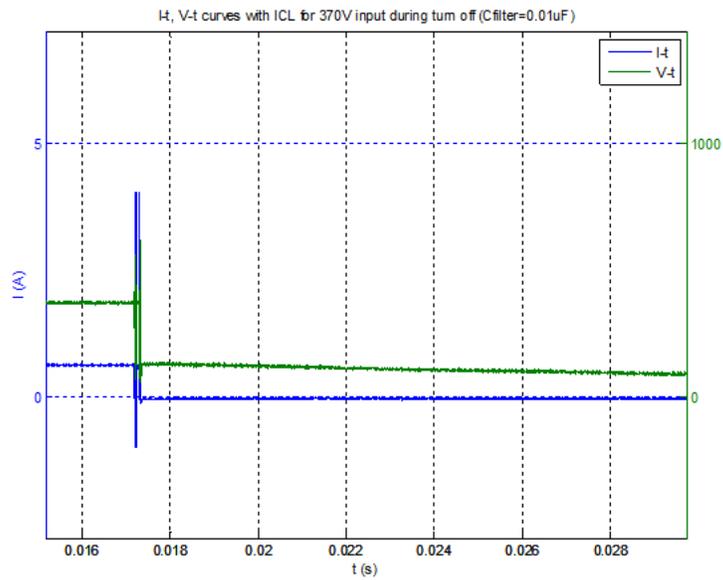


Fig. d: $I-t$, $V-t$ curves with inrush current limiter for 370V input during turn-off and $C_{filter}=0.01\mu F$