Low-Power Circuit Analysis and Design Based on Heterojunction Tunneling Transistors (HETTs)

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***Abstract*— The theoretical lower limit of subthreshold swing in MOSFETs (60 mV/decade) significantly restricts low-voltage operation since it results in a low ON-to-OFF current ratio at low supply voltages. This paper investigates extremely low-power circuits based on new Si/SiGe heterojunction tunneling transistors (HETTs) that have a subthreshold swing of <60 mV/decade. Device characteristics, as determined through technology computer aided design tools, are used to develop a Verilog-A device model to simulate and evaluate a range of HETT-based circuits. We show that an HETT-based ring oscillator (RO) shows a 9–19 times reduction in dynamic power compared to a CMOS RO. We also explore two key differences between HETTs and traditional MOSFETs, namely, asymmetric current flow and increased Miller capacitance, analyze their effect on circuit behavior, and propose methods to address them. HETT characteristics have the most dramatic impact on static random access memory (SRAM) operation and we propose a novel seven-transistor HETT-based SRAM cell topology to overcome, and take advantage of, the asymmetric current flow. This new HETT SRAM design achieves 7–37 times reduction in leakage power compared to CMOS.**

***Index Terms*— 7T SRAM, low-power, heterojunction tunneling transistors (HETT), tunneling transistor.**

I. Introduction

LOW-VOLTAGE operation is one of the most effective low-power design techniques because of its quadratic dynamic energy saving. Recently, a number of works [1]–[5] have shown aggressive supply voltage reduction to near or below the threshold voltage (Vth) of MOSFET devices with considerable reduction in power consumption. However, this power improvement has come at the cost of operation speed (typically <10 MHz). At such low supply voltages, the ON current drops dramatically because of the lack of gate overdrive, resulting in large signal transition delays. To regain this performance loss, it is possible to reduce the threshold voltage. However, this exponentially increases the OFF current, which is particularly problematic in applications that spend significant time in the standby mode [6]. For instance, lowering the supply voltage from 500 to 250 mV while enforcing iso-performance by reducing the Vth increases the leakage power by 275× in a commercial bulk-CMOS 45-nm technology, which is unacceptable.

To address this dilemma, there has been recent interest in new devices with significantly steeper subthreshold slopes than traditional MOSFETs [7]–[11]. A steep subthreshold slope enables operation with a much lower threshold voltage while maintaining low leakage. In turn, a low Vth enables low-voltage operation while maintaining performance. Hence, steep subthreshold slopes can provide power-efficient operation without loss of performance.

In this paper, we investigate circuit designs using the recently proposed Si/SiGe heterojunction tunneling transistor (HETT) [12]. The Si/SiGe heterostructure uses gate-controlled modulation of band-to-band tunneling to obtain subthreshold swings of less than 30 mV/decade with a large ON current of 0.42 mA/μm at $V_{ds} = 0.5$ V. Furthermore, Si/SiGe heterostructures are fully compatible with current MOSFET fabrication and can leverage the extensive prior investment in CMOS fabrication technology. Several industry and university teams have actively developed Si/SiGe HETT-type transistor structures, and initial devices have been experimentally demonstrated [13], [14].

We explore the key differences between HETTs and traditional MOSFETs that must be considered in the design of circuits using these new devices. Most significantly, HETTs display asymmetric conductance. In MOSFETs, the source and drain are interchangeable, with the distinction only determined by the voltages during operation. However, in HETTs, the source and drain are determined at the time of fabrication, and the current flow for $V_{ds} < 0$ is substantially less than for $V_{ds} > 0$ [in an N-type HETT (NHETT)]. Hence, HETTs can be thought to operate unidirectionally, passing logic values only in one direction, which has significant implications on logic and especially static random access memory (SRAM) design.

Our analysis shows that another effect is a large increase in gate-to-drain capacitance (i.e., Miller capacitance) in HETTs compared to MOSFETs. This excess Miller capacitance can cause undesirable artifacts in the switching behavior of HETTs which are not present in MOSFETs. These differences in device operation and characteristics require careful study to

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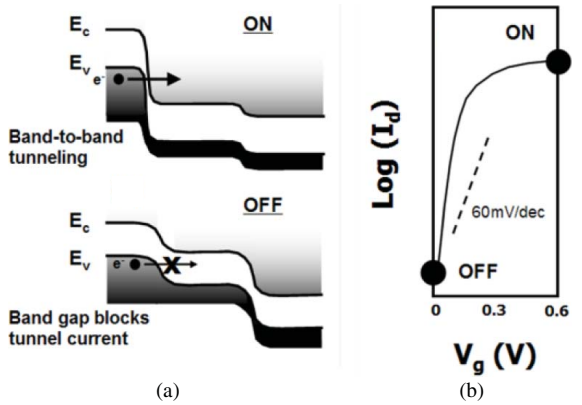

(a) (b)

Fig. 1. Tunneling FET device concept as depicted by (a) band diagrams in the source-to-drain direction and (b) qualitative current-voltage characteristics.

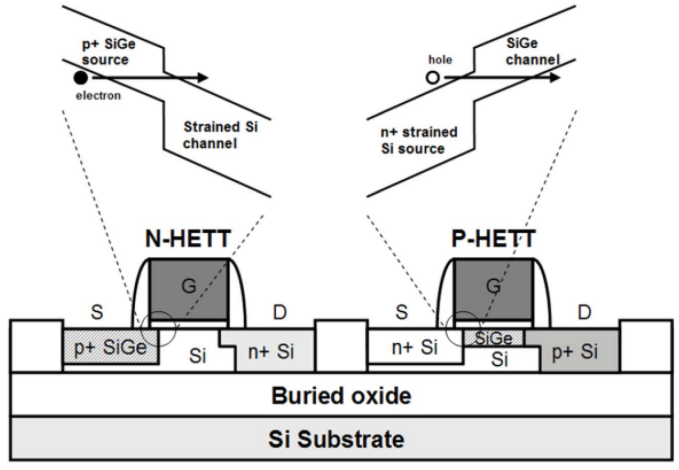

Fig. 2. CMOS-compatible implementation of complementary tunneling FETs with type-II source-to-body heterojunctions to improve device drive current.

understand their circuit design implications. To explore the potential impact of HETT on circuit design, we investigate the impact on logic and memory components in this paper since LSIs generally consist of logic and memory structures. We show that HETT-based logic circuits are capable of improving energy efficiency by 19× compared to CMOS when operated at a supply voltage of 0.23 V. We particularly study SRAM design, which is most impacted by the novel characteristics of HETTs. We show that the unidirectional characteristic of HETTs can actually be exploited in SRAM design to enable a novel 7T robust SRAM cell.

The remainder of this paper is organized as follows: 1) we briefly discuss HETT device operation and highlight the differences between the physics of HETT and MOSFET operation; 2) we introduce our modeling method for HETTs to enable circuit simulation of these devices, and examine dynamic and leakage power reduction in standard circuits compared to a commercial bulk CMOS 45-nm technology; 3) we discuss the impact of the unique characteristics of HETTs on circuit behavior and describe how to address these issues; and 4) we present the new HETT-based SRAM cell topology that takes advantage of the asymmetric current flow of HETTs and quantify robustness improvements and leakage power reductions compared with CMOS-based SRAM.

II. HETT Device Characteristics

The 60 mV/decade subthreshold slope limitation of conventional MOSFETs arises because of the thermionic nature of the turn-on mechanism. Tunneling transistors do not suffer from this fundamental limitation, since the turn-on in these devices is not governed by thermionic emission over a barrier.

Fig. 1 illustrates the basic concept of tunneling transistor operation. In an n-type tunneling transistor, the source is doped p-type, the channel is undoped or lightly doped, and the drain is n-type. As shown in Fig. 1, when the gate is biased positively, the device is turned on because electrons in the valence band of the p-type source can tunnel into the conduction band of the channel. If the Fermi level in the source is less than a few thermal voltages (kT) below the valence band edge, the bandgap acts as an "energy filter," precluding tunneling from the exponential portion of the Fermi–Dirac distribution. If the gate bias is reduced sufficiently so that the bottom of the conduction band in the channel rises above the top of the valence band in the source, the tunneling abruptly shuts off. Because of this filtering of the Fermi–Dirac distribution function by the bandgap, the subthreshold slopes can be significantly smaller than 60 mV/decade.

A potential problem with tunneling transistors is that a very narrow bandgap semiconductor must be used to obtain sufficiently high ON current. However, narrow bandgap materials also lead to higher OFF currents, and are often incompatible with standard CMOS processing. To avoid this problem, a type-II HETT can instead be employed. In such a case, the source-to-body contact has a staggered band lineup that creates an effective tunneling band gap E_{geff}, which is smaller than that of the constituent materials. Such a band structure can also be realized in the Si/SiGe heterostructure material system, and complementary N- and P-HETTs can be fabricated by reusing the masks for NFETs and PFETs, making this technology fully CMOS compatible. For optimized HETT drain, each device can require two more masks, and to get HETT optimized sources would take two more, resulting in 0–4 additional masks for HETT implementation depending on the degree of optimization. This is still far less than number of additional masks required for BiCMOS, which takes about eight extra masks. Fig. 2 shows a schematic diagram of a complementary Si/SiGe HETT technology.

For the circuit simulations in this paper, an optimized device structure was used. The simulated HETT devices have a gate length of 40 nm and a high-k gate dielectric with effective gate oxide thickness of 1.2 nm. For NHETT, the source consists of pure Ge, with 3% biaxial compressive strain, and Si channel with 1% biaxial tensile strain. The complementary P-type HETT (PHETT) design includes a strained Si source and pure Ge channel. Using band offsets from [15], the effective bandgap for this structure is 0.22 eV. For the transport calculations, a nonlocal tunneling model [16] with a two-band dispersion relationship within the gap was used. Effective masses are $0.17m_0$ near the conduction band and $0.105m_0$ near the valence band in the silicon channel, and $0.10m_0$ near

Algorithm 1 Sample Verilog-A Code for NHETT

```
module NHETT (s, g, d);
inout s, g, d;
electrical s, g, d;
real cap_gd_value, cap_gs_value;
parameter real width = 1;
analog begin
    cap_gd_value = $table_model (V(g)−V(s), V(d)−V(s),
    "./cgd_table.csv," "1S, 1S");
    cap_gs_value = $table_model (V(g)−V(s), V(d)−V(s),
    "./cgs_table.csv," "1S, 1S");
    I(g, d) <+ cap_gd_value * ddt (V(g)−V(d))* width;
    I(g, s) <+ cap_gs_value * ddt (V(g)−V(s))* width;
    I(d, s) <+ $table_model (V(g)−V(s), V(d)−V(s),
    "./ids_table.csv," "1S,1S") * width;
end
```

the conduction band and $0.055m_0$ near the valence band in the pure Ge source [17]. The device has a 2-nm gate overlap of the source and an abrupt source doping profile. A gate work function of ∼4.4 eV is used to set the OFF current to <1 pA/μm.

III. HETT Device Modeling

Since accurate analytical models for HETTs are not available, we first built a lookup-table-based model using Verilog-A to enable circuit simulations. This technique is a simple and accurate way of compact modeling for emerging devices [18] where analytical expressions for the $I-V$ characteristics are not well established.

A lookup-table model is built for $I-V$ and $C-V$ characteristics using technology computer aided design simulation data based on the device parameters described in the above section. The HETT is modeled as a three-terminal device (source, gate, and drain) and current is assumed to flow only between source and drain since gate leakage is negligible with high-k gate dielectrics. Two parasitic capacitors are modeled, C_{gd} and C_{gs}, which include inner fringing capacitance and overlap capacitance between gate and drain and between gate and source, respectively. Channel capacitance is negligible because the device has a fully depleted channel, and junction capacitance is also negligible due to its silicon-on-insulator-type substrate. As a result, we build three 2-D tables that are functions of two input voltages, V_{gs} and V_{ds}, for modeling HETTs: I_{ds} (V_{gs}, V_{ds}), C_{gd}(V_{gs}, V_{ds}), and C_{gs} (V_{gs}, V_{ds}). V_{gs} and V_{ds} are swept in 50-mV steps in general, but in the slightly reverse biased region (-0.2 V $< V_{ds} <$ 0 V) where I_{ds} transition is rapid V_{ds} steps are 10 mV for the I_{ds} tables.

Based on the three tables stored at comma-separated values (CSV) files, NHETT and PHETT are modeled using Verilog-A. Algorithm 1 shows a sample Verilog-A code for NHETT. $table_model function needs three types of inputs: variables; a data file which has a data table; and control signals for interpolation and extrapolation. In this sample, the degree of the splines used for the interpolation process is 1. To evaluate a point beyond the interpolation area, the S (spline) extrapolation method is used. In this model, the length of a device is fixed and the width is modulated by parameter "width."

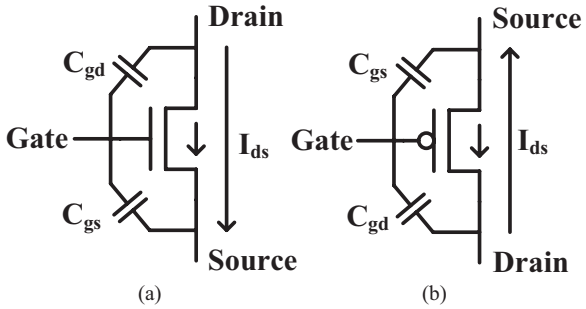

Fig. 3. Device symbols for (a) NHETT and (b) PHETT.

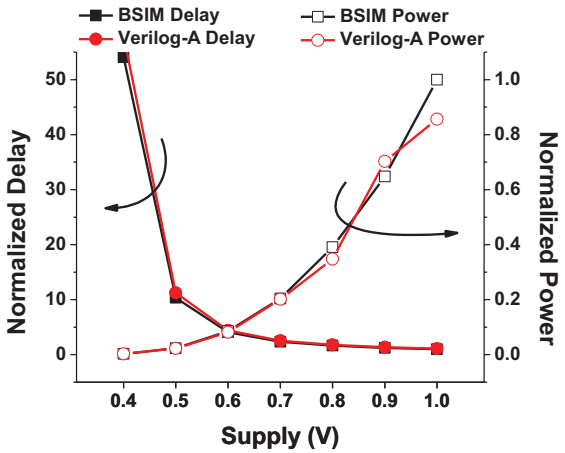

Fig. 4. BSIM versus Verilog-A for commercial 45-nm CMOS technology.

In Fig. 3, new symbols for NHETT and PHETT are presented. An arrow inside the conventional MOSFET symbol denotes the direction of forward biased current, which is from drain to source for NHETT and vice versa for PHETT.

To verify that the Verilog-A device modeling is accurate enough togenerate reasonable simulation results, conventional BSIM modeling and Verilog-A modeling are compared in Fig. 4. The tables of capacitance and current for commercial 45-nm CMOS technology are extracted from the BSIM model, and the Verilog-A model is built based on extracted tables. Fig. 4 shows the normalized delay and the normalized dynamic power consumption of an 11-stage ring oscillator (RO) from two models: BSIM and Verilog-A. The difference between the two simulation results is acceptable for investigating the basic characteristics of a futuristic device.

IV. HETT-Based Circuit Analysis

HETT device exhibited significantly lower subthreshold swing. For example, for V_g ranging from 0 V to 200 mV, NHETT has subthreshold swing of 25 mV/dec based on our simulations, whereas commercial bulk nMOS has 95 mV/dec for the LP and 93 mV/dec for the GP process. For the same range, PHETT has subthreshold swing of 27 mV/dec, whereas pMOS has 95 mV/dec for the LP and 100 mV/dec for the GP process. Such steep subthreshold swing and larger ON current of HETTs allow aggressive voltage scaling at

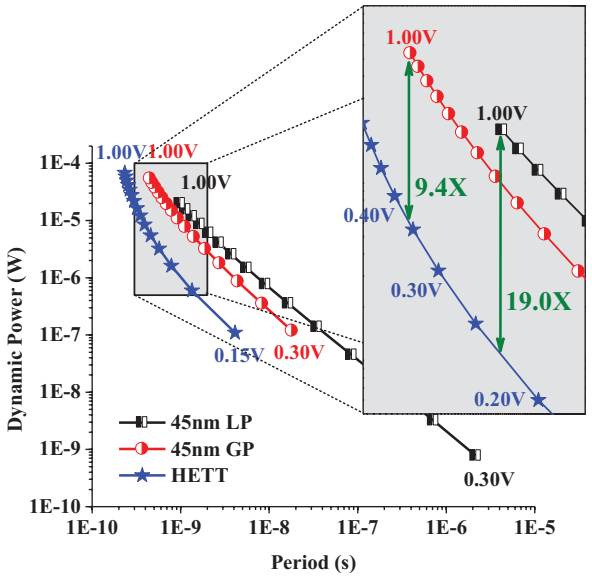

Fig. 5. Comparison of dynamic power with commercial bulk CMOS 45-nm LP, 45-nm GP, and HETT devices.

iso-performance, enabling dynamic power reductions. To quantify this power reduction, ROs are simulated with HETTs and compared with a commercial bulk CMOS 45 nm technology. In addition, the circuit design impact of HETT limitations is also addressed in this section. HETT-based SRAM design is discussed in Section V.

A. Dynamic Power Reduction

A 31-stage RO with minimum sized inverters is used to evaluate the dynamic power consumption. Leakage power is subtracted from total power to focus only on dynamic power in this section since the leakage power contribution was less than 10% (leakage is examined in more detail for SRAM in Section V). In addition, minimum sized inverters are used, since minimizing the size results in the least power for a given switching period.

Fig. 5 shows the dynamic power reduction of the 31-stage RO with HETT devices compared to the commercial bulk CMOS 45-nm technology. The CMOS technology has two types of logic devices: Low Power and General Purpose. The LP devices are designed for low power operation and exhibit lower leakage than GP devices. Iso-speed dynamic power consumption of LP devices is expected to be worse because the ON current in LP is smaller than in GP. With identical device sizes in both CMOS and HETT technology, supply voltage is lowered from 1.0 to 0.3 V in CMOS and from 1.0 to 0.15 V in HETT with 0.05 V steps. At 1.0 V, the GP-based RO has a period of 450 ps and 53.9 μW dynamic power consumption. To maintain the same period, the RO with HETT consumes only 5.74 μW at 0.355 V, achieving a 9.4× dynamic power reduction. For 45-nm LP, more dynamic power reduction is observed. At 1.0 V, the LP RO period is 980 ps and consumes 19.98 μW, while the HETT-based RO consumes 19× less power (1.05 μW) at 0.226 V within the same period.

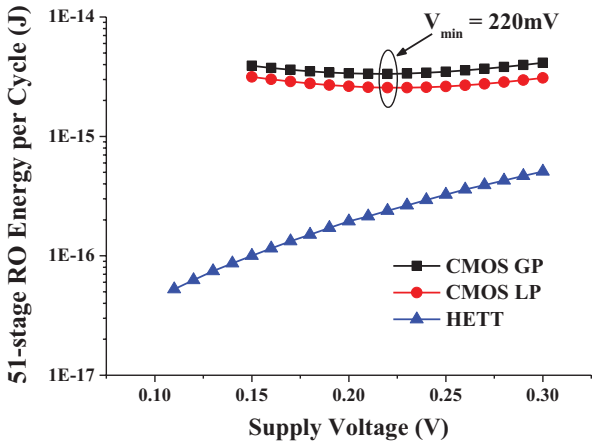

Fig. 6. Energy consumption per cycle and V_{min} of 51-stage RO with commercial bulk CMOS 45-nm LP, 45-nm GP, and HETT devices.

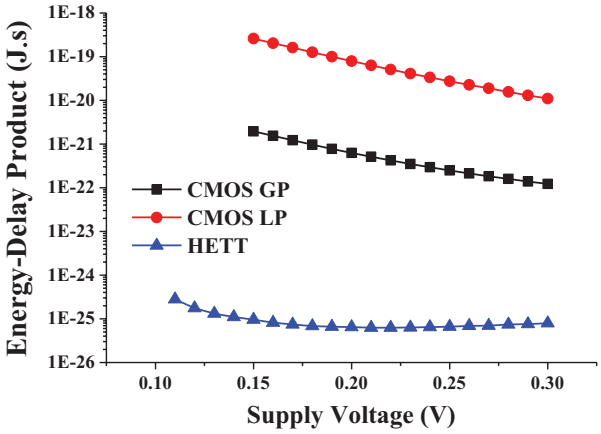

Fig. 7. Energy-delay product comparison with commercial bulk CMOS 45-nm LP, 45-nm GP, and HETT devices.

To compare optimal energy supply voltage (V_{min}), the total energy consumption per cycle for a 51-stage RO is compared in Fig. 6. V_{min} for bulk CMOS 45-nm GP and 45-nm LP devices was 220 mV. V_{min} for HETT device is <100 mV due to significant reduction of the leakage current. The HETT-based circuit was not functional below the supply voltage of 100 mV, at which point V_{min} was not yet reached. Fig. 7 shows the comparison of energy–delay product across supply voltages for a 51-stage RO. Significant reduction of the energy–delay product could be achieved with HETT devices. It is possible to implement logic with a mixture of CMOS and HETT, in which case the results will lie between those of the all-CMOS and all-HETT implementations. In case a design requires low leakage current, the designer would want to use HETTs as much as possible whereas where performance matters, CMOS would be preferred.

In HETT technology, power savings is obtained by using low-voltage operation. However, low-voltage operation also incurs higher sensitivity to process variations, which can offset some of the power saving gains seen by HETT. When reliable variation data is available for HETT technology, careful analysis is needed to understand the impact of these variations on power savings seen by HETT technology.

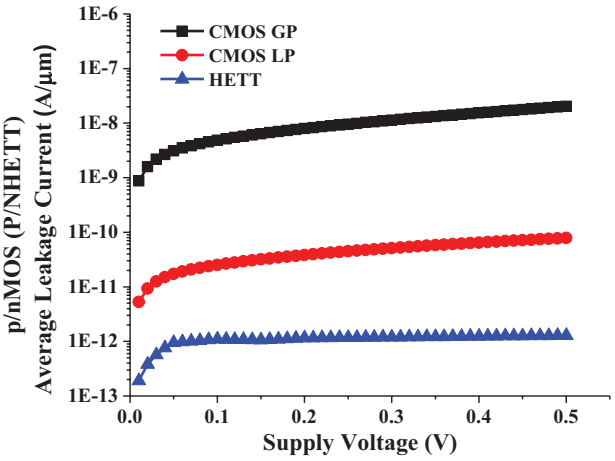

Fig. 8. Comparison of static power with commercial bulk CMOS 45-nm LP, 45-nm GP, and HETT devices. Average leakage current of pMOS/nMOS (or PHETT/NHETT) is plotted as a function of supply voltage.

B. Static Power Reduction

HETT devices exhibit lower leakage current due to their turn-on mechanism which is governed by band-to-band tunneling. Therefore significant static power reduction can be achieved with HETT devices. Fig. 8 shows the average leakage current of pMOS and nMOS (or PHETT and NHETT) as function of supply voltage. CMOS LP devices have approximately two orders of magnitude lower leakage than CMOS GP devices. HETT devices exhibit more than one order of magnitude lower leakage than CMOS LP devices.

C. Limitations of HETT-Based Circuits

1) Asymmetric Current Flow: HETT source and drain are determined during fabrication and current flow between the two nodes is not symmetric. Fig. 9 demonstrates this asymmetric current flow in an NHETT. We assume that the nominal voltage of HETTs will be <0.5 V, as HETTs target ultralow voltage applications and are well suited for this voltage regime [19], [20]. Fig. 9(a) shows the forward bias current with V_{gs} swept from 0 to 0.5 V. The drain current curves look similar to that of CMOS devices. However, the reverse bias current, where the voltage across the drain and source is negative, differs from that of CMOS devices as shown in Fig. 9(b). Note that I_{ds} is negative in Fig. 9(b). For most regions of V_{ds}, the drain current is several orders of magnitude smaller than the forward current. However, there are two cases where the reverse bias current becomes nonnegligible. First is when V_{ds} is approximately -0.5 V, at which point the drain current become nonnegligible regardless of V_{gs}. The second case occurs for positive V_{gs} combined with a small negative V_{ds}. PHETTs exhibit similar asymmetry in their current flow.

The asymmetric current flow does not restrict the use of traditional static CMOS logic circuits with pull-up network (PUN) and the pull-down network (PDN) because the current flow of each device in the PUN and PDN is unidirectional. By applying this current direction for logic circuit implementation with HETT, CMOS logic can be fully constructed with HETT. However, pass-transistor and transmission-gate operation is

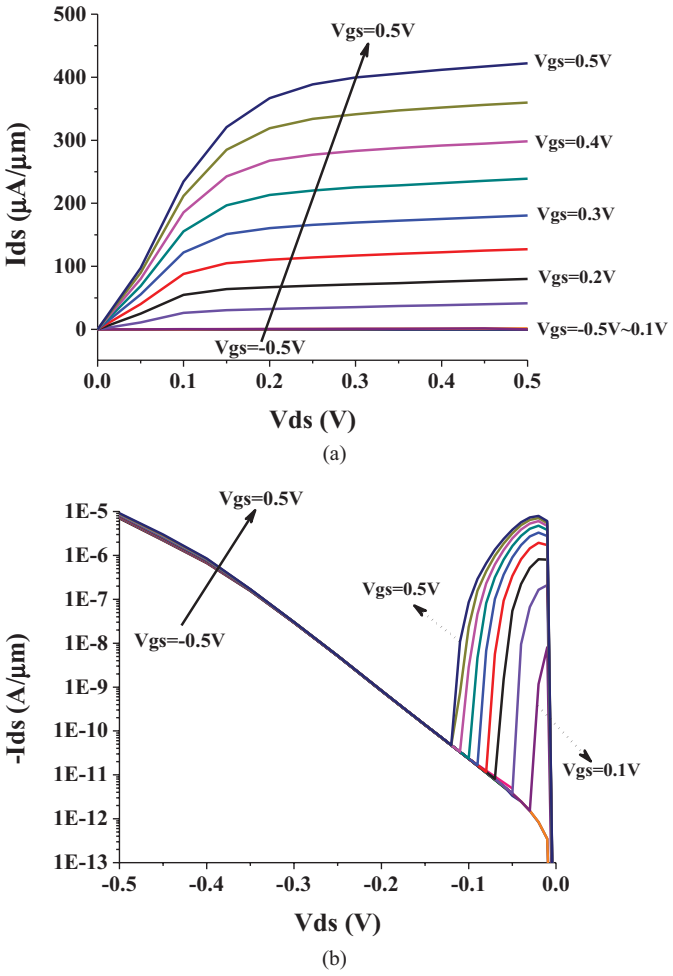

Fig. 9. (a) Forward bias and (b) reverse bias drain current of HETT device with $L = 40$ nm.

limited since it requires current flow in both directions. Fig. 10 details the limitation of HETT-based pass-transistor circuits. Because the drain and source of the device are fixed, there are two ways to implement a pass gate in a circuit: oriented left and right. In both cases, the current flow characteristics are classified again by two cases: passing logic "1" and passing logic "0."

A pass gate propagating logic "1" is shown in Fig. 10(a), where left and right configurations are both illustrated. Before the input at the gate of pass gate is switched at 2 ns, the output of the rightward pass gate stays near 0 V while the output of leftward pass gate is pulled up to ~150 mV. This is due to the fact that the reverse OFF current can be larger than the forward OFF current. When the input switches at 2 ns, the output of the rightward pass gate immediately switches to $\sim V_{DD}$ while the output of the leftward pass gate remains near 200 mV and increases very slowly. This clearly shows that the forward ON current can strongly drive the output but the reverse ON current cannot. For pass gate passing logic "0" [Fig. 10(b)], similar trends can be observed and only the leftward pass gate functions well. This directional current-driving capability renders pass gate logic useless for HETT-based circuits. The asymmetric current flow also limits the use of the standard

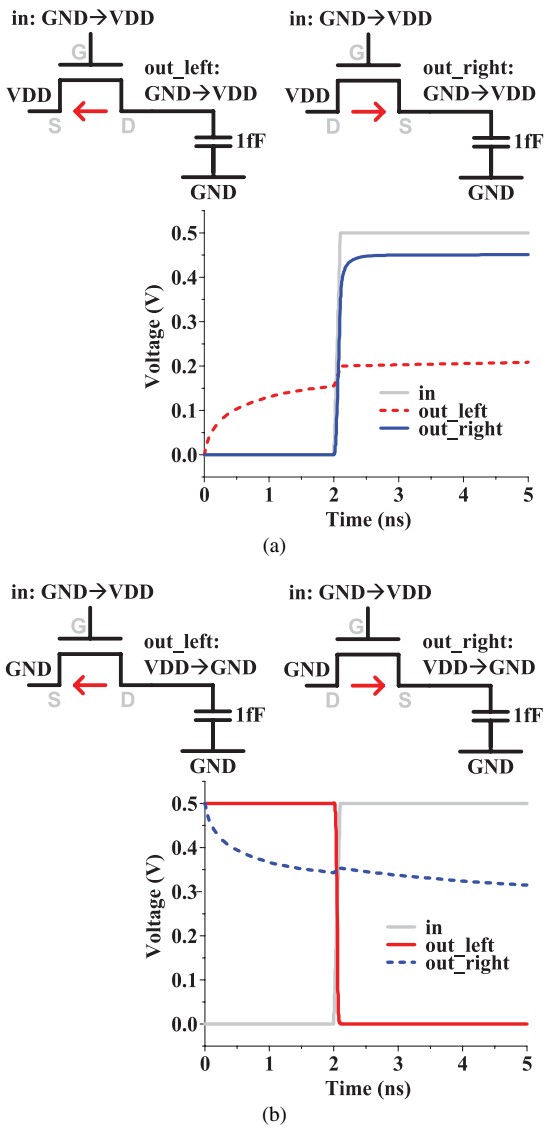

Fig. 10. Two orientations (left and right) for implementing NHETT-based pass gates (a) passing "1" and (b) passing "0."

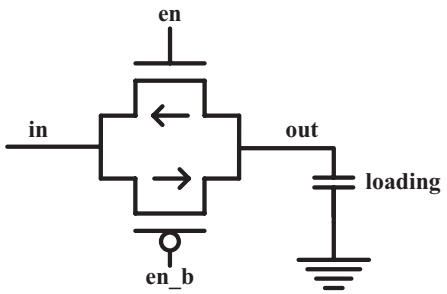

Fig. 11. Transmission gate for HETTs.

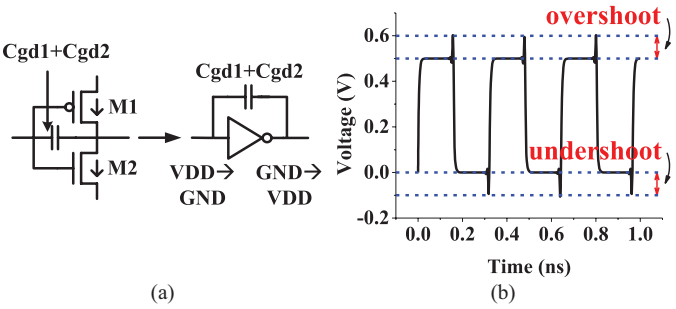

Fig. 12. (a) Miller capacitor acting as 2× larger capacitive loading. (b) Overshoot and undershoot caused by capacitive coupling.

6T SRAM cell and static latches/registers, where pass gates and transmission gates are used as key components. Latches and registers can be implemented without pass gates and transmission gates by using clocked CMOS logic. Alternative SRAM cell topologies will be discussed in Section VI.

To implement HETT-based logic circuits that include pass gates or transmission gates, two approaches can be taken. The first approach is to simply use CMOS devices for these gates. This can be accomplished easily since the HETT fabrication process is CMOS-compatible. The second approach is to mitigate the unfavorable effect of unidirectional current flow on pass-gate or transmission-gate operation by appropriately choosing the source and drain directions of NHETT and PHETT. However, since typical logic rarely uses pass gates or transmission gates, implementing these gates with CMOS will not have a significant impact on the overall design. As shown in Fig. 10, NHETT is better at passing logic "0" than logic "1" due to Vth drop at the output of a gate. For the same reason, PHETT is good at passing logic "1." Therefore, the current direction of NHETT must be from output to input, while the current direction of PHETT must be opposite (Fig. 11).

2) Increased Miller Capacitance: The capacitance between gate and drain is often referred to as the Miller capacitance, as it is impacted as the Miller effect [21]. During a voltage transition, the two terminals of the Miller capacitor are moving in opposite directions such that the voltage change across the capacitor is twice the absolute voltage change [Fig. 12(a)], hence this capacitance significantly impacts loading. In addition, it causes overshoots and undershoots during transitions due to capacitive coupling between the input and output of the gate [Fig. 12(b)], which results in additional capacitive loading and performance overhead.

The Miller capacitance in HETTs is larger than that in MOSFETs. This is due to the linking of the inversion layer in HETTs to the drain rather than the source, as is the case in MOSFETs. In HETTs with a large gate bias, what can be viewed as a parasitic inversion layer forms with carriers drawn from the drain side; this inversion layer is not the primary form of current conduction in the device, hence the term parasitic. Under this bias condition, C_{gd} becomes essentially equivalent to the entire channel capacitance due to the parasitic inversion layer. This principle is the same as that described in detail in [22] for carbon-nanotube-based tunneling FETs.

In Fig. 13, we find that the extracted C_{gd} of an NHETT is ∼2× larger than the C_{gd} of nMOS in a commercial bulk CMOS 45-nm technology. To evaluate the impact of this larger Miller capacitance in HETTs, the average overshoot and undershoot (as a percentage of the 0.5 V supply) are evaluated and shown in Fig. 14. If the electrical effort (from logical effort [23]) is larger than 4, overshoot effects in HETTs are comparable to that in commercial 45-nm CMOS technologies.

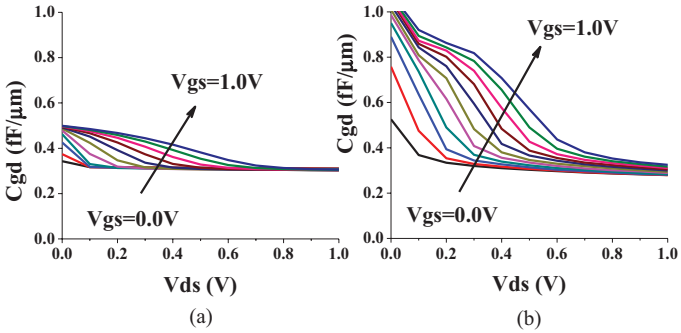

Fig. 13. C_{gd} comparison of (a) CMOS (nMOS) and (b) HETT (NHETT).

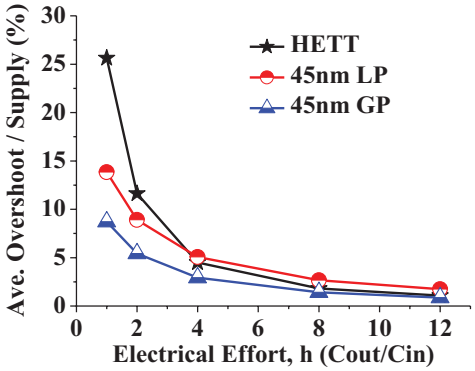

Fig. 14. Overshoot effects in HETT are not significant with electrical effort of 4 or larger despite the larger C_{gd}.

Hence we conclude that, for typical loads, the increased C_{gd} will not have any significant impact on circuit performance, although it should be considered for very lightly loaded gates.

V. 6T SRAM Design With HETT

The asymmetric current flow of HETT places restrictions on the use of the pass gate and the transmission gate. This limitation is not severe for logic circuits since the CMOS logic, which is the most widely used logic, is not affected by this property because the current is expected to flow only in one direction in the channel of each transistors. Moreover, any pass-gate logic can be easily converted to CMOS logic to prevent malfunctions with HETT. However, the impact of HETTs asymmetric current flow on SRAM is significant since standard 6T SRAM uses pass gates for access transistors, which is not trivial to replace. In this section, we first analyze the implications of asymmetric current flow on SRAM operation and go on to propose an alternative 7T HETT-based SRAM cell topology. We then compare the 7T performance and robustness to that of a CMOS-based 6T SRAM design.

A. CMOS Standard 6T SRAM

To understand the difference between HETT-based 6T SRAM and CMOS-based 6T SRAM, we trace the current flow paths in read and write operations. Fig. 15 shows a CMOS 6T SRAM cell storing "0." To read the stored value, bit lines (BIT, BIT_B) are precharged to V_{DD}. As a word line (WL) is driven high for read operation, NPDL pulls down the voltage at BIT

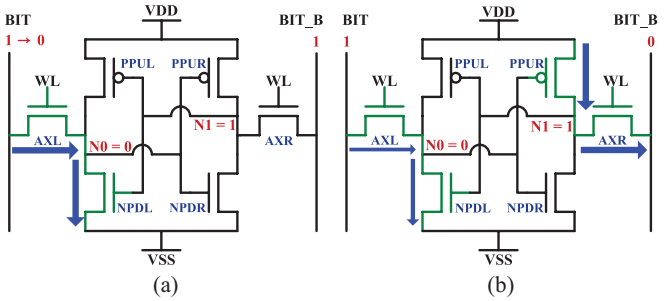

Fig. 15. Current flow paths in (a) read and (b) write operations in CMOS 6T SRAM.

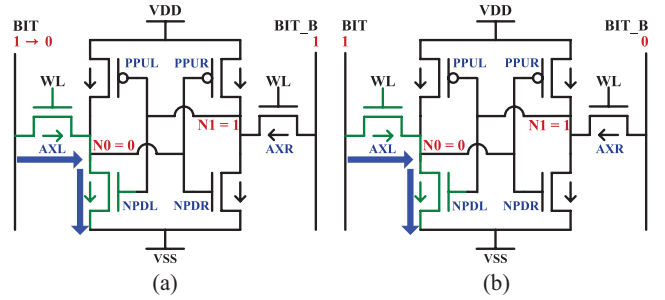

Fig. 16. Current flow paths in (a) read and (b) write operations in HETT 6T SRAM with inward direction access transistors.

as shown in Fig. 15(a). This pull-down current or voltage can be sensed by a sense amplifier to determine the stored value. For writing a value "1," as shown in Fig. 15(b), AXL pulls up the internal node N0 while AXR pulls down the internal node N1. However, since both access transistors are nMOS, which are better at pulling low, AXR plays the major role in write "1" operation. AXL aids in writing a "1" by pulling up N0 to a certain extent and making the bit flip more easily.

For this type of SRAM, read stability can be improved by increasing the sizing ratio of NPDL to AXL (or NPD to AX), which is commonly referred to as the cell β-ratio. As the cell β-ratio increases, NPDL in Fig. 15(a) holds the voltage at node N0 to ground more strongly during read, making it more stable. At the same time, this worsens the write ability of the cell by making it more difficult to change the voltage at node N0. However, as shown in Fig. 15(b), since the pull-down current path (AXR) plays the major role in writing, the size ratio of AXR to PPUR, or AX to PPU, is the critical one for writeability and can be improved by increasing this ratio. This implies that, up to a point, readability and writeability in CMOS 6T SRAM can be improved individually at the cost of larger area.

B. HETT Standard 6T SRAM With Inward Access Transistors

Due to its unidirectional nature, access transistors in HETT 6T SRAM can drive current either inward or outward. Fig. 16 shows a HETT 6T SRAM structure with inward current flow configuration and storing "0." Read operation for this SRAM is similar to that of a CMOS 6T SRAM. Bit lines are precharged and current flows through AXL and NPDL. Therefore, similar to CMOS 6T SRAM, a higher cell β-ratio is preferred for preventing read upset.

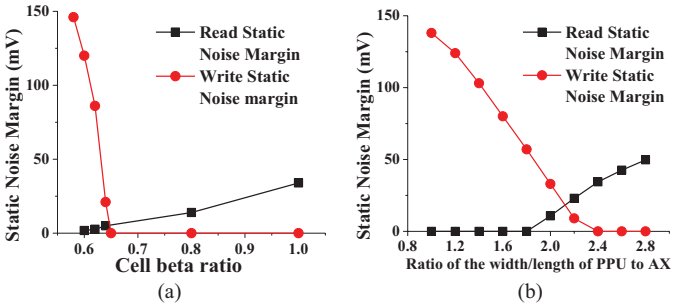

Fig. 17. SNMs of HETT 6T SRAM with (a) inward and (b) outward access transistors with $V_{DD} = 0.5$ V.

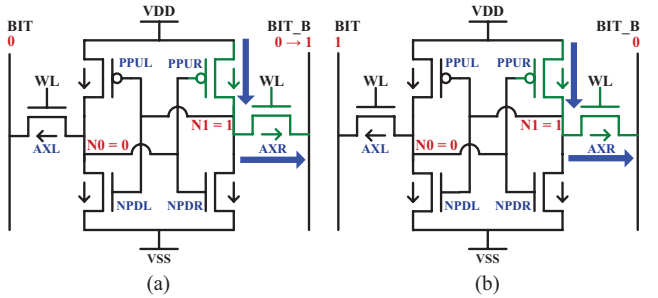

Fig. 18. Current flow paths in (a) read and (b) write operations in HETT 6T SRAM with outward direction access transistors.

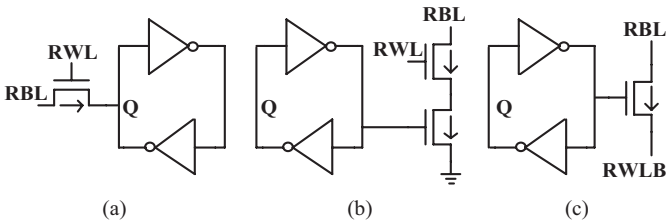

Fig. 19. Alternative write structures for HETT-based SRAM. (a) Two-side transmission gate write. (b) One-side transmission gate write. (c) Two-side NHETT pull-down write.

However, to write "1" to this cell, AXR cannot pull down the voltage at N1 since it can only conduct current inward, implying that AXL must pull up the voltage at N0 without differential aid, as shown in Fig. 16(b). Therefore, the write operation is performed only by one side and the stronger current path is removed in HETT 6T SRAM. Since we are relying on an n-type transistor to drive the internal node voltage high, writeability of this cell is substantially worse than a CMOS 6T SRAM. To overcome the poor writeability, AXL should be strengthened compared to NPDL, i.e., the cell β-ratio should be decreased. However, decreasing the cell β-ratio negatively affects the read margin.

This tradeoff between readability and writeability can be clearly seen if we plot the static noise margin (SNM) of read and write operation versus cell β-ratio, as shown in Fig. 17(a). SNM is the maximum dc. voltage of the noise that can be tolerated by the SRAM and it is widely used for modeling stability of SRAM cells [24]. SNM can be defined for three different operations: read, write, and standby (hold), but only read and write margins are compared here since they limit SRAM stability. In SNM analysis for HETT-based SRAMs, all simulations use $V_{DD} = 0.5$ V since HETTs are aimed at this voltage regime. For HETT 6T SRAM with inward access transistors with cell β-ratio of 1, the read margin is 34 mV but write margin is 0 V, meaning that write operation is impossible. As we decrease the cell β-ratio to improve writeability, the write margin becomes positive at a cell β-ratio of 0.64, but the read margin at this point has degraded to <3 mV, indicating that the cell is highly vulnerable to read upset at this design point. From this we conclude that HETT 6T SRAM with inward access transistors is not feasible.

C. HETT Standard 6T SRAM With Outward Access Transistors

HETT 6T SRAM with outward access transistors has a similar limitation. Fig. 18(a) shows a read operation where bit lines (BIT BIT_B) are predischarged and BIT_B is charged through AXR and must be sensed. For writing, AXR must drive internal node N1 to ground and flip the stored value without differential assistance from AXL. Since both of these operations involve PPUR and AXR, adjusting the ratio of PPUR to AXR strengths will improve one operation and worsen the other. This tradeoff can be clearly seen in Fig. 17(b). The read operation requires a PPUR to AXR ratio higher than 1.8, while the write operation malfunctions when the ratio is higher than 2.4. In the remaining design space, the SNM for read/write operations is limited to <50 mV, which is insufficient. Therefore, an alternative SRAM topology is needed to achieve robust low leakage SRAM with HETTs.

VI. Alternative SRAM Design With HETT

A fundamental tradeoff between readability and writeability limits the implementation of 6T HETT SRAM. This tradeoff can be avoided by separating read and write current flow paths at the cost of a few additional transistors. In this section, various possible read and write structures for HETT-based SRAM are compared. Then a 7T HETT SRAM is proposed and analyzed in detail.

A. Read Structures for HETT SRAM

In 6T SRAM, back-to-back inverters are the components that store the value, and two access transistors (AXL/AXR in Fig. 15) are used as read structure and write structure at the same time. To separate read and write paths, three possible read structures are shown in Fig. 19.

Fig. 19(a) shows a single HETT read structure where an additional HETT dedicated to read operation is attached to the back-to-back inverter pair. With this structure, inward NHETT configuration is preferred to outward configuration to minimize chance of read upset. The benefit of this separate read structure is that separate cell β-ratios can be obtained for read and write operations. By utilizing a weaker inward NHETT just for read operation, better read margin can be obtained while maintaining same write margin.

Fig. 19(b) shows the read structure widely used in CMOS 8T SRAM [26], where transistors are replaced with HETTs. This structure implements voltage sensing of the stored value, eliminating the current flow path through the back-to-back

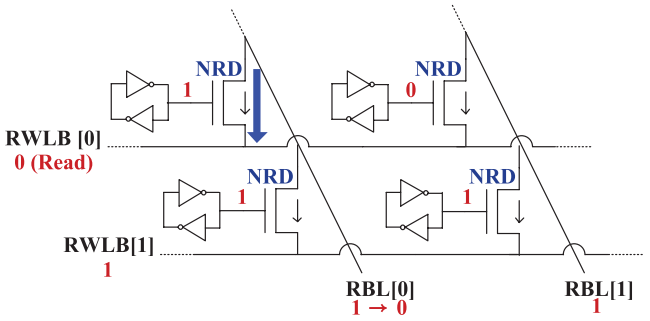

Fig. 20. Alternative read structures for HETT-based SRAM. (a) Single HETT read. (b) 8T read. (c) Reduced 8T read.

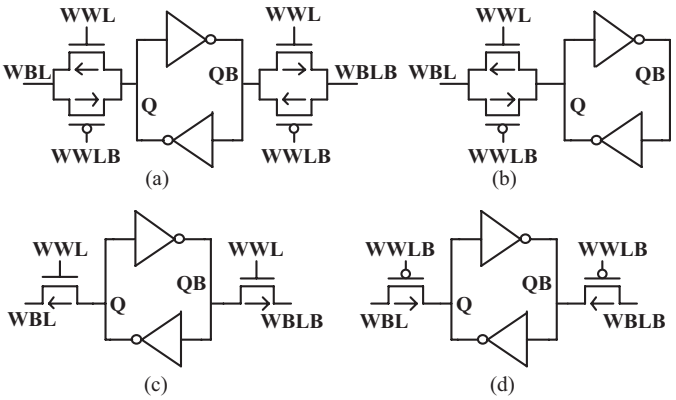

Fig. 21. Read operation in HETT 7T array. (a) Two-side transmission gate write. (b) One-side transmission gate write. (c) Two-side NHETT pull down write. (d) Two-side PHETT pull up write.

inverters. Therefore, the possibility of read upset is virtually eliminated at the cost of two additional transistors. In this structure, the bottom NHETT senses the stored voltage and the top NHETT selects the word to be read. However, by taking advantage of HETTs asymmetric current flow, voltage sensing and word selection can be done with one NHETT as shown in Fig. 19(c). Instead of grounding the source of the sensing (bottom) HETT, an inverted RWL is connected to the source so that only the selected word can drain current through the sensing HETT.

Fig. 20 illustrates how the NHETT of a reduced 8T read structure (NRD) in each cell is connected in the array structure. The source of NRD is connected to that of other cells in the same word (RWLB), while the drain is connected to that of other cells in same column (RBL). To read values in word [0] (top row of Fig. 20), bit lines (RBL [0], RBL [1]) are precharged and RWLB [0] is asserted (driven to ground), while all other RWLBs are set to V_{DD}. Since the source of the NRDs in word[0] are set to ground, cells that store value "1" can discharge the bit line, as depicted with the thick arrow in Fig. 20. With CMOS transistors, this read scheme does not work because, as RBL [0] is discharged, other cells storing "1" on the same bit line can start charging up RBL [0] as in the case of the bottom-left cell in Fig. 20. However, by leveraging the asymmetric nature of HETTs, this unwanted reverse-direction charging current is eliminated without the cost of an additional transistor. Therefore, reduced 8T read can achieve robust read operation as robust as 8T read with the same HETT count with a single HETT read.

B. Write Structures for HETT SRAM

Fig. 21 shows four of the possible HETT write structures. The tradeoff between readability and writeability originates from asymmetric current flow of access transistors (AXL/AXR in Fig. 16). Therefore, allowing bidirectional current flow by replacing access transistors with transmission gates [Fig. 21(a)] can eliminate this tradeoff. Although this scheme allows both read and write access through transmission gates, it requires eight HETTs which can be reduced by more advanced read and write structures. To reduce the HETT count, single-ended access can be used whereby transmission gate on one side can be eliminated [Fig. 21(b)]. However, this requires the PHETT in the transmission gate to be sized up by 1.55× since PHETT has a weaker current driving capability.

The nonuniform sizing of NHETT and PHETT in the transmission gate can result in irregular layout especially when the size difference is as high as 55%. To avoid this, an identical type of HETT can be used as access transistor, just as in standard 6T SRAM, but only for write operation. Fig. 21(c) shows a two-side NHETT pull-down write where the value is written by pulling down one of the storage nodes (Q and QB). For writing with NHETT, outward configuration is preferred. If we assume that the back-to-back inverters are minimum-sized for minimum cell area, the size of NHETT and PHETT should be identical. With this assumption, Fig. 17 shows that writing with outward minimum-sized NHETT is robust with a noise margin of 143 mV, whereas the inward NHETT has to be widened by 1.4× just to be functional. For the same reason, inward configuration is better with PHETT write [(Fig. 21(d)]. However, this scheme also requires 1.55× larger PHETT to achieve comparable write noise margin with NHETT write.

Two-side NHETT pull-down writing structure [Fig. 21(c)] also can benefit from the unidirectional current flow, which mitigates the half-select disturbance in a bit-interleaved array. The half-select disturbance accidently flips the internal data in half of the selected bit cells which share the same write WL with targeted bit cells for write operation [27]. With two-side NHETT pull-down write structure, if the write bit lines of the half selected bit cells are kept at V_{DD}, the amount of current flow via access transistors is limited to the leakage current level. Therefore, two-side NHETT pull-down write structures have improved immunity during half-select accesses.

C. 7T SRAM for HETT

Based on the previous discussion, 7T SRAM optimized for HETT is proposed as shown in Fig. 22. In this topology, readability/writeability tradeoffs in HETT-based 6T SRAM are overcome by utilizing separate read and write structures. The reduced 8T read enables extremely robust read with minimal additional number of HETT, and two-side NHETT pull-down write enables robust write with cell β-ratio of 1, where all

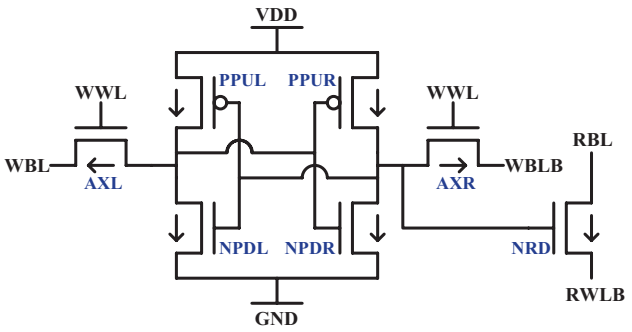

Fig. 22. Proposed HETT 7T SRAM structure.

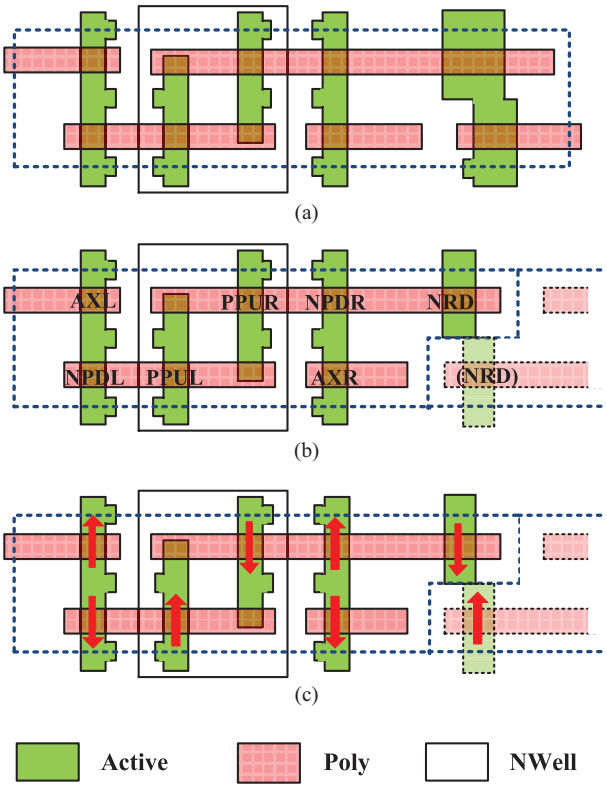

Fig. 23. (a) 8T layout. (b) Corresponding HETT 7T layout. (c) Current flow direction.

HETT sizes can be minimum. There have been several 7T SRAM cell structure published earlier; however [29]–[31] do not use decoupled read and [32] and [33] use two transistors as a decoupled read structure, and none of these prior artwork has used a single transistor decoupled read.

The HETT 7T SRAM is estimated to have <15% area overhead over a standard 6T, while the 8T SRAM exhibits 29% cell area overhead [26]. Fig. 23 shows that two read transistors (NRD in Fig. 22) from adjacent cells can be abutted in 7T SRAM, making the overhead for two 7T cells equal to that of one 8T cell. Moreover, as will be shown below, the 7T cell with all transistors at minimum size shows improved robustness over 6T at low voltage, hence if an upsized 6T were used to achieve iso-robustness, the area penalty would be much smaller than 15%.

For the proposed HETT 7T SRAM, memory cell array should be HETT-based to take advantage of the low

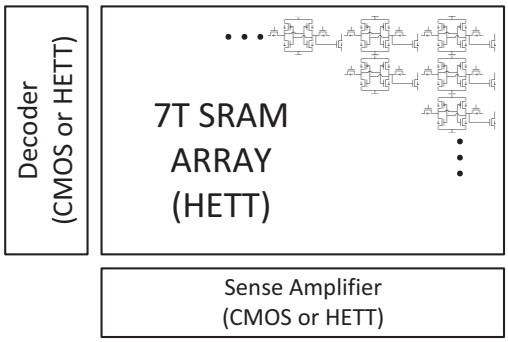

Fig. 24. Proposed usage of HETT-based 7T SRAM array.

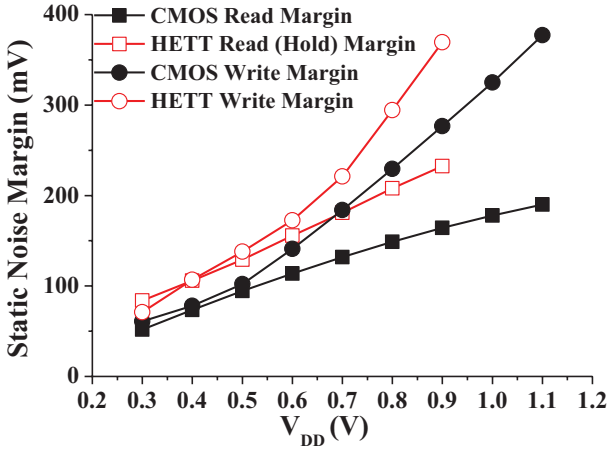

Fig. 25. Read/Write margin of 45-nm commercial bulk CMOS 6T SRAM and HETT 7T SRAM.

leakage current of the HETT devices. However, for peripherals such as decoder and sense amplifier, either CMOS or HETT can be used, as shown in Fig. 24, since the HETT fabrication process is compatible with that of logic CMOS. Depending on the user requirement, if read/write speed is critical for the user, CMOS peripheral circuits can be used, whereas if leakage current of the peripheral circuit is a primary concern, HETT-based peripheral circuits can be used. However, our discussion will mainly focus on memory cell itself.

A write operation in this 7T structure is equivalent to the HETT 6T SRAM with outward access transistors. However, since the read/write operations are performed by separate current paths, device sizes for all transistors other than NRD can be chosen to favor writeability.

We compare the SNM of HETT-based 7T SRAM to a 45-nm commercial bulk CMOS 6T SRAM cell provided by a foundry. We compared HETT-based 7T SRAM with CMOS 6T SRAM because large leakage-dominated memory structures, such as L3 caches, will most benefit from the low leakage of HETT SRAM and these arrays are commonly made with 6T SRAM cells. All HETT devices are set to equal (minimum) width for maximum density. Read and write margins of both types of SRAMs across a range of supply voltages are plotted in Fig. 25. The SNM for HETT is analyzed with supply voltages up to 0.9 V only because HETT is designed for low-voltage

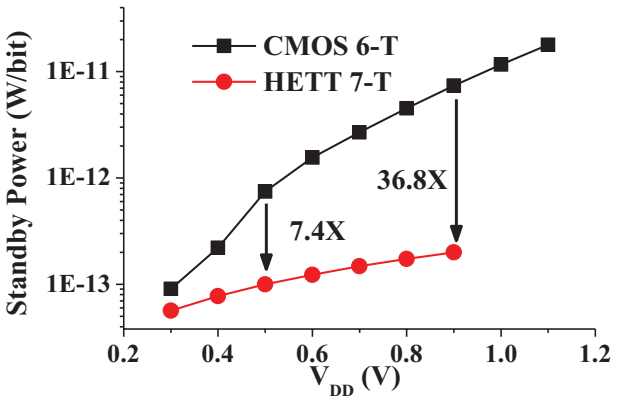

Fig. 26. Standby power of CMOS 6T and HETT 7T SRAM.

(∼0.5 V) operation. Write margins of HETT 7T SRAM are more than 30% higher than CMOS 6T SRAM for supply voltages of >0.4 V as shown in Fig. 25.

Since the read operation uses an additional read transistor in the HETT 7T SRAM and all other transistors are in standby (hold) state during read operation, the hold margin is equivalent to that in HETT 7T SRAM. Given this, HETT 7T read margin is 232 mV at $V_{DD} = 0.9$ V and 129 mV at 0.5 V, which is 41% and 37% higher than commercial bulk CMOS 6T SRAM, respectively. Such improvements in read/write margin can be observed for V_{DD} down to 0.3 V, suggesting that improved read/write robustness can be achieved with HETT 7T SRAM over traditional CMOS at low voltage.

Finally, HETT-based SRAM standby power is significantly reduced compared to that of CMOS 6T SRAM, as seen in Fig. 26. At a supply voltage of 0.9 V, standby power is reduced by 36.8× and at 0.5 V, by 7.4×. This clearly shows the promising low-leakage properties of HETT devices for future memory-dominated low-power applications.

VII. Conclusion

A circuit perspective of a new promising tunneling transistor, HETT, with steep subthreshold swing for extremely low power applications was presented in this paper. We investigated some unique electrical properties of HETT such as asymmetric current flow and increased Miller capacitance. A 9–19× dynamic power reduction is expected with HETT-based circuits due to their improved voltage scalability. We examined the limitations of HETTs as they relate to circuit operation. To overcome and exploit the inherent device asymmetry, a new HETT-based SRAM cell topology was presented with 7–37× leakage power reduction.

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