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An Approach to Improve Active Power Flow Capability by Using Dynamic Unified Power Flow Controller

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***Abstract*— Ever increasing power demand has made it essential to utilize the available transmission network resources. As a fact, steady state model of flexible alternating current transmission system (FACTS) devices have been used in many studies to improve power flow capability (PFC) in the transmission lines. In this paper, a dynamic model of unified power flow controller (UPFC) has been implemented to enhance the active power flow in transmission line. In addition, improving the bus voltages as well as reduction in the power losses also aimed with UPFC's presence. Both the controllers of shunt and series converters of UPFC are designed with PI controller. The performance of the proposed approach has been tested on IEEE 5–bus and IEEE 14–bus systems under PSCAD environment. The simulation results revealed that the proposed dynamic UPFC has effectively increased the active PFC in power system with the minimization of power losses.**

***Index Terms*-- Flexible AC Transmission Systems, PSCAD, Power Flow Capability, Power losses, Unified Power Flow Controller.**

I. INTRODUCTION

The expansion and up-gradation of power system has become essential to satisfy the ever growing power demand. Due to limited energy resources, deregulated electricity market, environmental constraints, time and capital required to build new transmission systems [1]. These issues have led the system planners to look for the new techniques for improving the power system performance. Therefore, keen attention has been paid to the application of Flexible Alternating Current Transmission System (FACTS) devices which are driven from modern power electronics components [2]. Over the last two decades FACTS devices have been extensively used to increase the amount of PFC through the transmission lines and enhance system controllability resulting in minimizing power losses in transmission network [3-5].

Many FACTS controllers such as: static VAR compensator (SVC), static synchronous compensator (STATCOM), thyristor-controlled series capacitor (TCSC), static synchronous series compensator (SSSC) and unified power flow controller (UPFC) are available [6]. Among them UPFC is the most versatile FACTS device. Since, it can individually or sequentially control all power system network parameters, including voltage magnitude, line impedance, and phase angle [7].

In past, several literatures focused on the steady state model of FACTS devices such as: SVC, STATCOM, TCSC and UPFC. These devices are implemented in power system network to enhance power flow capability (PFC), reduce power losses, and minimize cost and voltage deviation. Such functionalities are obtained by finding the optimal location, number and settings of these devices based on multi-objective optimization techniques like Evolutionary Programming (EP) [3], Harmony Search (HS) [8], Particle Swarm Optimization PSO [9-11], simulated annealing [12], Optimal Power Flow (OPF) [13], Differential Evolution (DE) [14]. However, in all these studies the steady state model of the FACTS devices have been adopted which are effective only for the planning and designing stage of power system networks. The models cannot be used to study real time operation of power system network. Therefore, it is essential to develop dynamic model of FACTS devices so that the real time analysis of power system network can be conducted.

This paper presents a real time approach to enhance the active power flow capability in power system network using dynamic UPFC. These are also intended with UPFC to enhance the bus voltage profiles and reduce power losses. A detail explanation of the controllers for both shunt and series converters of UPFC designed with PI controller are presented in this study. IEEE-5 and 14 bus systems are considered as case studies to justify the performance of the proposed dynamic UPFC model. PSCAD environment has been selected to conduct the simulation.

The rest of the paper is organized as follows: Section II focuses on UPFC's dynamic model. Section III presents the shunt and series converters controllers of UPFC. Section IV includes the simulation results obtained in PSCAD software for the two IEEE case studies. The significant points of this

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paper are summarized in the last section.

II. UPFC MODEL

The dynamic model of the UPFC build inside PSCAD is shown in Fig. 1. UPFC connects to the transmission line with shunt and series voltage source converters (VSC) which are coupled via a common DC link capacitor. Normally, the shunt VSC is considered as STATCOM and series one as SSSC [15]. Low pass AC filters are connected in each phase to prevent the flow of harmonic currents generated due to switching. The transformers are connected at the output of the converters to provide the isolation, modify voltage/current levels and also to prevent DC capacitor (C) being shorted due to the operation of various switches. Insulated gate bipolar transistors (IGBTs) with anti-parallel diodes are used as switching devices for both converters.

III. UPFC CONTROLLER

A. Shunt Controller

The controller of UPFC's shunt converter is presented in Fig. 2. The aim of shunt converter to draws a controlled current from the transmission line for the following reasons [15]:

- To keep the transmission line voltage at its reference value by providing or absorbing reactive power from the transmission line.

To maintain capacitance voltage level at its reference value on the DC link.

In order to control the bus voltage, sending-end voltage (Vs_measured) is measured instantly and subtracted from its reference value (Vs_reference) as per unit (pu) which reveals AC_voltage_error and pass it through a PI controller. The output of PI gives the magnitude of injected shunt voltage (Vmag_sh) in pu. Meanwhile, (Vdc_measured) is measured instantly and subtracted from its reference value (Vdc_reference) which reveals DC_voltage_error. The angle (angle_sh) is obtained after it went through another PI block. Phase Locked Loop (PLL) extracts the phase angle of sending-end voltage (a_s).The resultant angle of (a_s – angle_sh) and the magnitude (Vmag_sh) have used in 'sin ()' function to obtain the reference signals for Pulse Width Modulation (PWM). In PWM block, the reference signals are compared with carrier (triangle) signal which has a switching frequency of 3.5 KHz. The outputs of the comparators are given as firing signals to the converter switches.

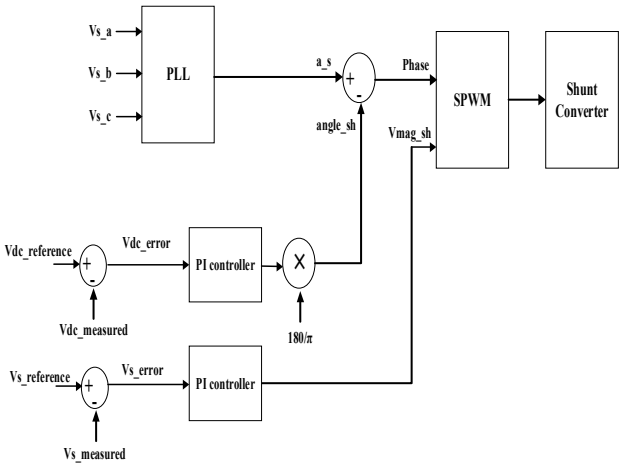

Fig. 2: Shunt controller of UPFC

B. Series Controller

The series converter controller of UPFC is illustrated in Fig. 3. The series converter controls the power flow across the line by injecting a voltage in series with the line current with controllable magnitude and angle.

The receiving end real and reactive power (Pmeasured and

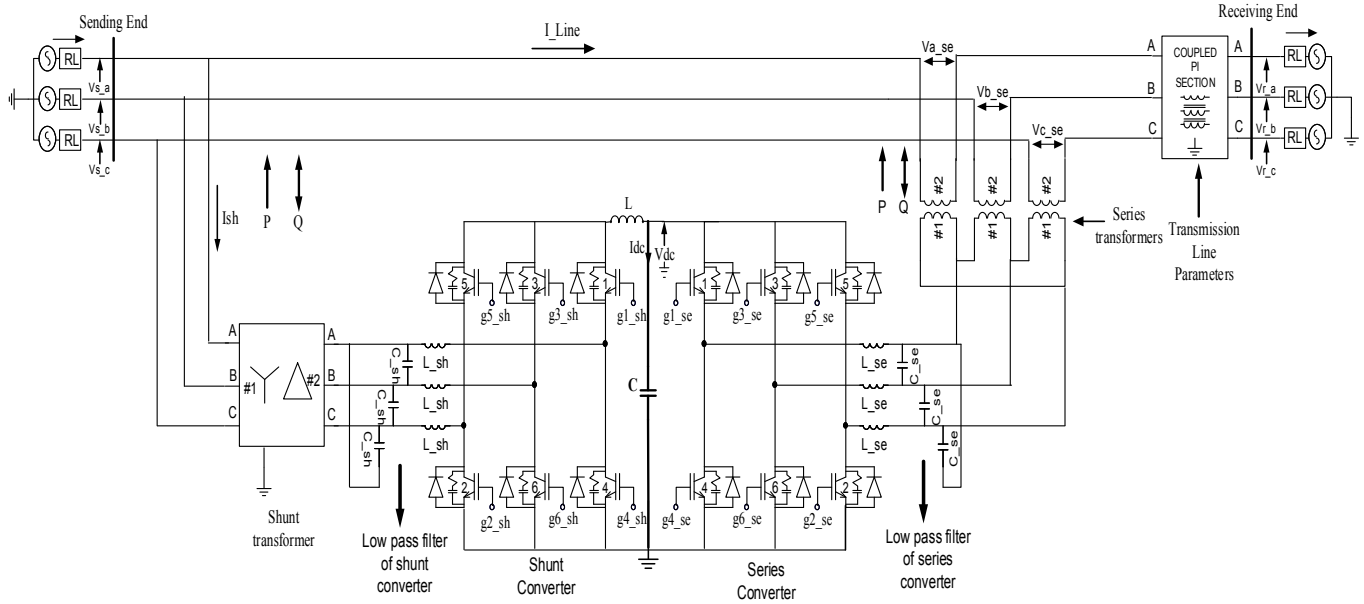

Fig. 1: Dynamic UPFC model

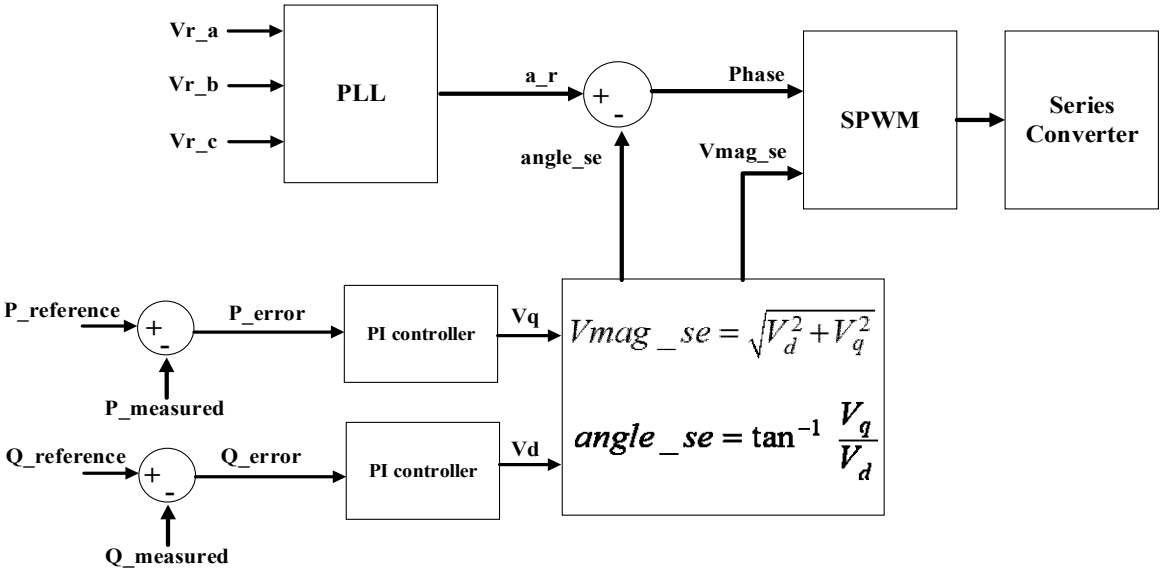

Fig. 3: Series controller of UPFC

Qmeasured) are measured and subtracted from their reference value (Preference and Qreference). These revealed the error signals (P_error) and (Q_error) which sent through two PI blocks. The outputs of the two PIs provided the orthogonal components of the injected voltage (Vq and Vd). Using these values the magnitude (Vmag_se) and phase angle (angle_se) of the series injected voltage have been calculated with the help of the following equations:

$$Vmag\_se = \sqrt{V_d^2 + V_q^2} \quad (1)$$

$$angle\_se = \tan^{-1}\frac{V_q}{V_d} \quad (2)$$

The phase angle of receiving-end voltage (*a_r*) is obtained through PLL. The angle obtained from (2) is subtracted from angle (*a_r*) of receiving-end voltage. The resultant angle and the magnitude of the voltage calculated from (1) are used in 'sin ( )' function block to obtain reference signals for PWM. In PWM, the reference signals are compared with carrier (triangle) signals. The switching frequency of the carrier has considered as 3.5 KHz. The firing signals of IGBTs are generated by comparing reference with carrier signals.

IV. Results and Discussions

In this section, IEEE 5 bus and IEEE 14 bus test systems are employed to evaluate the performance of the dynamic UPFC based on the active PFC enhancement. The proposed case studies are built inside PSCAD software by using the components available in PSCAD library.

A. IEEE 5 Bus Network

IEEE 5 bus system has to be tested with and without UPFC. In the analysis bus 1 has been taken as swing bus, 2 is generator bus (PV bus) and 3, 4, 5 are load buses (PQ buses).

The base values are: 100 MVA and 175 KV. The UPFC has been connected across line 2-3. A single line diagram of the network is presented in Fig. 4 along with the location of UPFC.

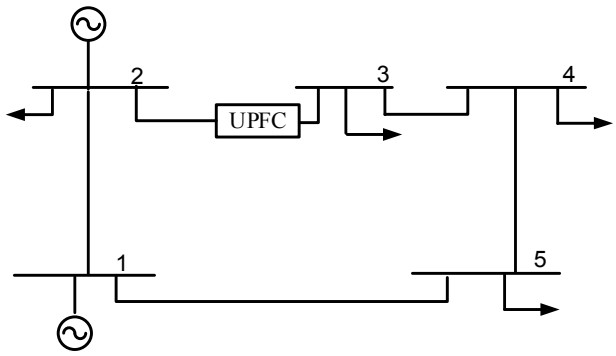

Fig 4: Single line diagram of IEEE 5 bus system

After placing the UPFC across line 2-3 an excellent improvement has been observed in the active power flow through the line. The real power flow has increased while the reactive power flow encountered a significant decrement. Without UPFC the receiving end real and reactive powers were 76 MW and 7.32 MVAR respectively where these power flows have become 77.6 MW and 6.7 MVAR respectively after UPFC has placed in the network. The simulation results of real and reactive powers are shown in Fig 5 and 6 respectively.

The voltage magnitudes before connecting UPFC were 0.9846 p.u and 0.935 p.u across sending and receiving ends respectively. While these have become 0.9956 p.u and 0.9458 p.u respectively after UPFC has connected to the line. The RMS values of voltage magnitudes for receiving and sending ends are illustrated in Fig. 7 and 8 respectively. Finally, all the bus voltages are represented in Fig. 9 for both UPFC and without UPFC cases. Overall it can be seen that UPFC helps to increase voltage profile of the whole system.

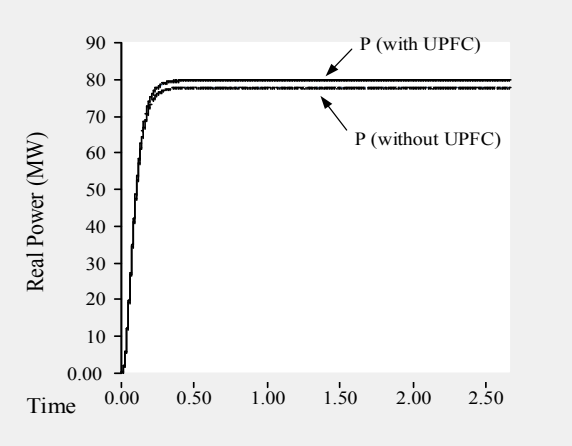

Fig. 5: Active power through line 2-3

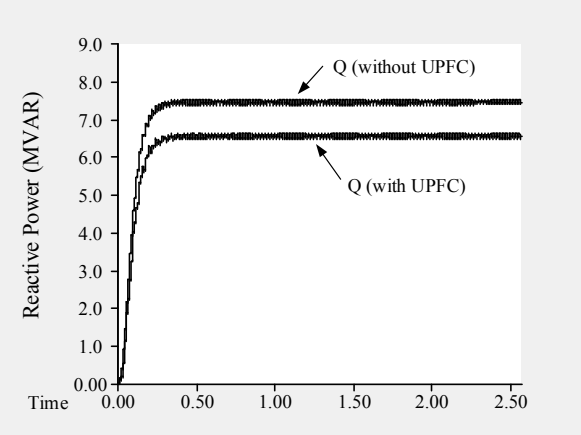

Fig. 6: Reactive power through line 2-3

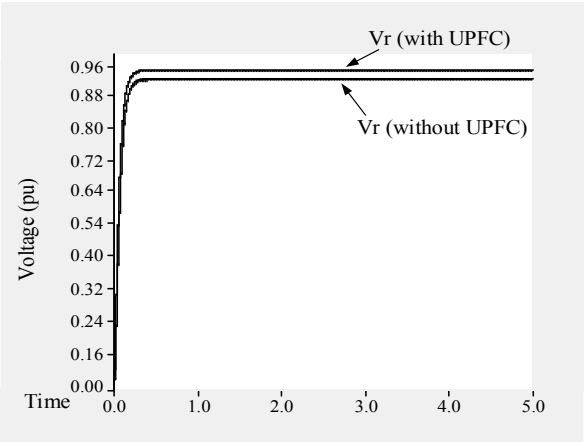

Fig. 7: Receiving end voltage across line 2-3

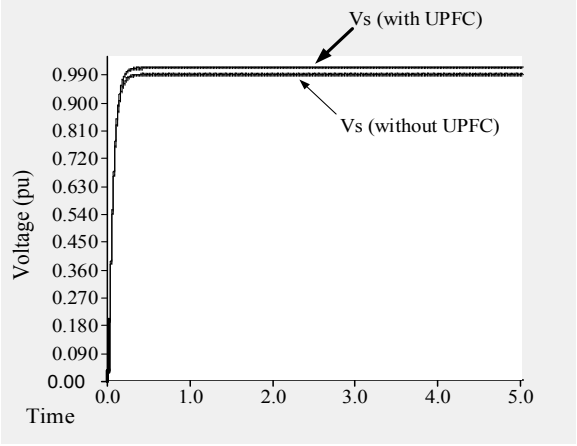

Fig. 8: Sending end voltage across line 2-3

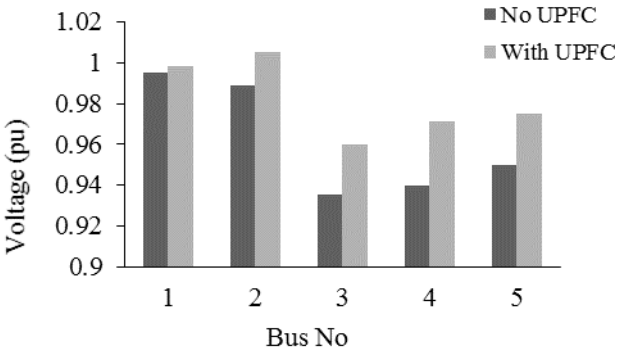

Fig. 9: Voltage profile across all the buses in IEEE-5 bus system

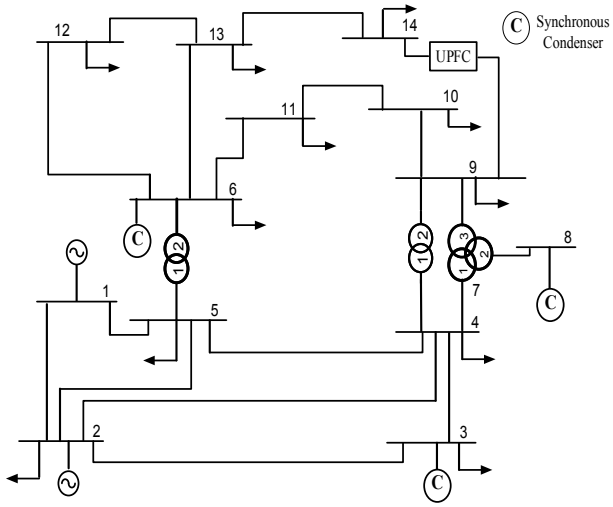

Fig 10: Single line diagram of IEEE 14 bus system

B. IEEE-14 Bus Network

It is a classical power system constitutes of 2 generator buses where bus 1 has considered as slack bus. To provide reactive power support it got three synchronous condensers at buses 3, 6, 8. It also has 11 load buses and 19 lines. The base case has been taken as 138 kV and 100 MVA. In this case study, UPFC has been placed across line 9-14 as shown in Fig. 10.

Improvement in active power flow has been observed when UPFC placed across line 9-14. According to the Fig. 11 real power of receiving end has got an increment of 0.665 MW (from 6.235 MW to 6.9 MW) with UPFC. In contrary, reactive power has experienced declination of approximately 0.293 MVAR (from 10.05 MVAR to 9.758 MVAR) which is depicted in Fig. 12.Referring to Fig. 13, receiving end voltage becomes 0.956 p.u with UPFC as per Fig. 14 which was

0.9446 p.u without UPFC. Similarly, with UPFC the sending end voltage has reached to 0.9931 p.u from 0.9886 p.u. All the bus voltages with respect to their bus numbers are plotted in Fig. 15. It has been observed that after UPFC has placed to the network all the bus voltages has improved when these are compared with without UPFC values.

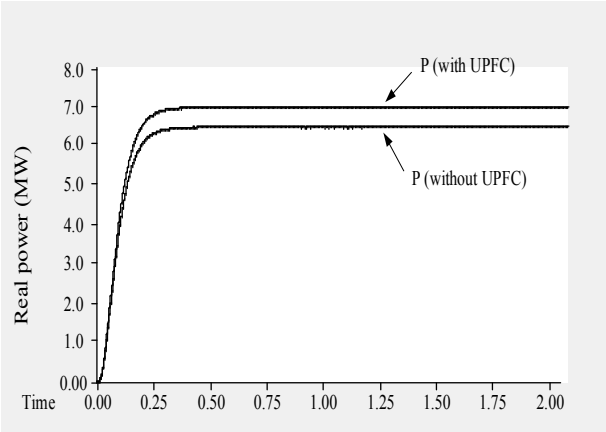

Fig. 11: Active power flow across line 9-14

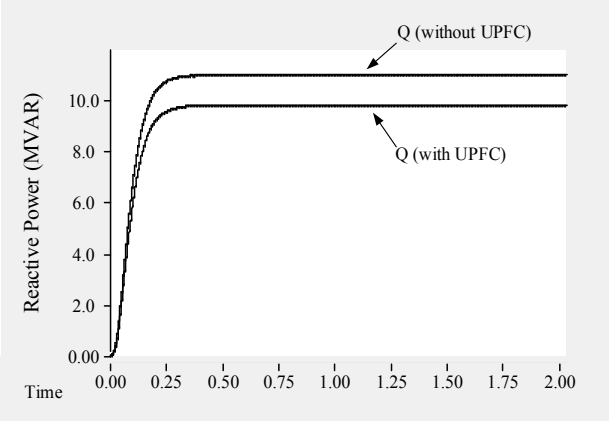

Fig. 12: Reactive power flow across line 9-14

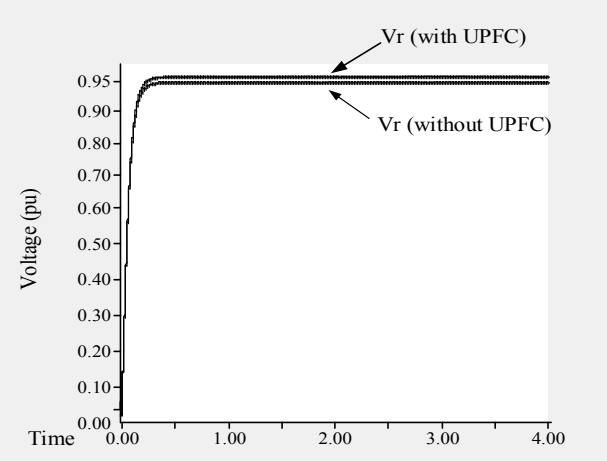

Fig. 13: Receiving end voltage across line 9-14

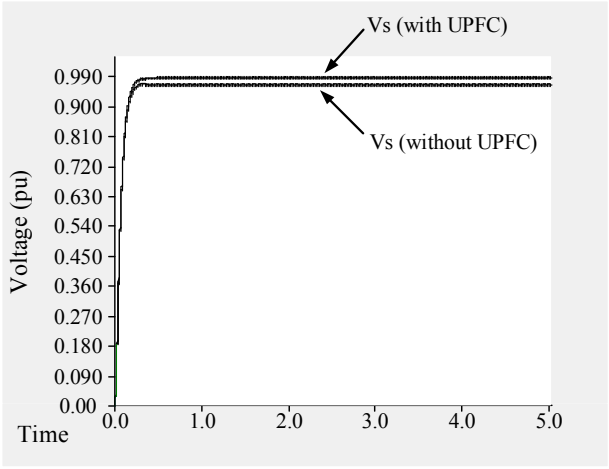

Fig. 14: Sending end voltage across line 9-14

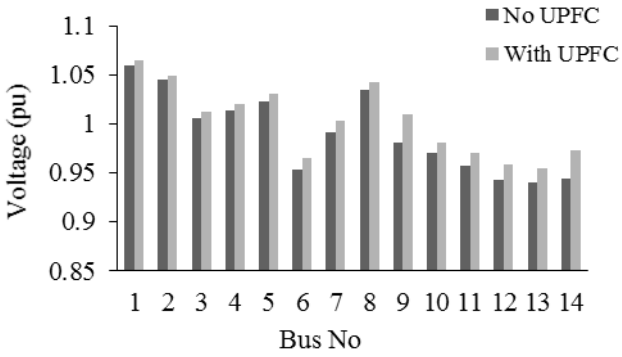

Fig. 15: Voltage profile across all the buses in IEEE-14 bus system

C. Power loss:

Another important effect of connecting UPFC to transmission network is that UPFC's presence not only increased the real power flow but also helped to reduce the power losses in the networks. In Table I, the power losses information has presented for both the case studies before and after connecting UPFC. According to the table, in IEEE 5 bus system before connecting UPFC the real and reactive power capacity losses were 6.2 MW and 4.502 MVAR respectively. While the real and reactive power capacity losses have reduced to 5.756 MW and 4.254 MVAR respectively when UPFC placed in the network. Similar way the real and reactive power capacity losses have reduced from 13.562 MW to 12.543 MW and 26.6206 MVAR to 24.15 MVAR respectively when UPFC has connected to IEEE 14 bus system.

V. CONCLUSION

In this study, with the objective of enhancing the active PFC of the power system network a dynamic model of UPFC has been implemented. It has been observed that after connecting UPFC active power flow has been improved by 2.10 % and 8.50 % in IEEE-5 and 14 bus systems

respectively. UPFC's influence has reduced the real and reactive power losses also by 7.161 % and 5.729 % respectively for IEEE-5 bus system. For IEEE -14 bus system also the power loss reduction percentage is similar. Overall, the dynamic UPFC has exhibited an excellent performance.

Table I
POWER LOSSES WITH AND WITHOUT UPFC

Case study	Power Losses without UPFC		Power Losses with UPFC	
	Real Power (MW)	*Reactive Power (MVAR)*	*Real Power (MW)*	*Reactive Power (MVAR)*
IEEE 5	6.2	4.502	5.756	4.254
IEEE 14	13.562	26.6206	12.543	24.15

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