Memristors: Devices, Models, and Applications

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I. THE HISTORY, THE DEVICE, AND THE OBJECTIVE OF THE SPECIAL ISSUE

The *three* basic electrical circuit elements, namely, capacitor, which was invented by Ewald Georg von Kleist in 1745, resistor, which was invented by Georg Simon Ohm in 1827, and inductor, which was invented by Michael Faraday in 1831, were constructed by experimental physicists to observe the lumped behavior of relevant measurable electrical parameters across the devices. In 1971, Leon Chua postulated the *fourth* basic circuit element while trying to establish a missing constitutive relationship between the electrical charge and the magnetic flux. Using Lewis Carroll's portmanteau naming technique, Chua named this hypothetical nonlinear device, *memristor* (memory + resistor) since it demonstrated the hysteresis property of the-then ferromagnetic core *memory* and also the dissipative characteristics of a *resistor*. Clearly, in such devices, the nonlinear resistance can be memorized indefinitely by controlling the flow of the electrical charge or the magnetic flux. In 1976, Leon Chua and Sung Mo Kang further extended the concept of memristor by proposing a broader class of *memristive devices* and systems.

This issue covers five important aspects of memristor technology: theory, device engineering, circuit modeling, digital and analog systems, and neuromorphic systems.

Though there were initial attempts to validate Chua's theoretical postulation of memristor by demonstrating the charge-controlled memristor behavior with the help of active and passive electrical circuit components, during these intervening years, practicing design engineers did not pay much attention to apply the memristors in commercial products because of the complexity involved in implementing memristors. As a result, the direct physical realization of memristor as the fourth basic circuit element remained unresolved, *de facto* forgotten for almost the past four decades. It was only in early 2008 when the Hewlett Packard (HP) researchers serendipitously observed the memristive behavior of nanoscale cross-point devices in their crossbar memory arrays and credited the seminal work of Leon Chua published in 1970s to the nanoscale phenomenon they witnessed, that the entire electrical and computer engineering community was galvanized by the reemergence of the *missing memristor as a* fundamental circuit element since it kicked open new vistas in multiple frontiers ranging from the abstruse chaos theory to nanoscale commercial products. This new technology is expected to bring about a slew of inventions in nonlinear dynamics of mem-impedance circuitry, programmable Boolean circuits, neuromorphic system design, transistorless multilevel nonvolatile digital memories, and so on. In less than two years since the HP paper appeared in *Nature*, the research output on memristors and memristive devices has grown exponentially with

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publications in all sorts of conferences and journals. For brevity, the terms *memristor* and *memristive device* have recently been renamed *ideal memristor*, representing the fourth element, and *generalized memristor*, respectively.

Further, due to the initial media coverage of the HP paper as a groundbreaking discovery, the newly acclaimed device swiftly garnered an unprecedented razzmatazz in national newspapers, weblogs, periodicals, archival proceedings, and business publications. This media deluge has created unreal speculations for investors and researchers alike. On the one hand, many investors are genuinely concerned whether the nascent memristor technology will ring the death knell of complementary metal–oxide–semiconductor (CMOS) transistors in the multibillion dollar chip industry or the resistive nonvolatile storage devices will completely drive out the traditional DRAM and flash memories. On the other hand, artificial neural net engineers, neurobiologists, and neuroscientists have started hypothesizing the possibility of integrating memristor-based multibillion synapses to fabricate biology-inspired chips that will navigate like lower order primates using their visual, auditory, and tactile sensory networks.

Recent publications point out that two-terminal memristors can be configured to perform the *implicative logic function*, once popularized by logicians like Bertrand Russell and Alfred Whitehead, in three steps in order to replace functionally complete NAND gates that have been traditionally implemented by three-terminal CMOS transistors. This has injected a new round of grievous concerns among researchers and investors whether CMOS is nearing its obsolescence far more quickly than prophesized by the International Technology Roadmap for Semiconductors (ITRS) roadmaps. Confusion also pervades among device engineers whether the host of solid-state technology devices with pinched hysteresis such as the phase-change memory, magnetoresistance memory, and resistive memory that have evolved in the last five decades should be considered as memristors, though the authors of papers on these devices were oblivious of the prior art in memristor technology. These memory devices were the offshoots of synergistic engineering research in materials, device scaling, and modeling of device transport using the quantum physics. The purpose of this special issue is to set aside numerous misunderstanding and misgivings about the history, theory, and development of the memristor technology by presenting in-depth original and review papers on the memristor and mem-impedance devices so that readers will gain right perspectives about this new device and will be motivated to foster innovations that will profoundly impact the semiconductor industry.

II. THE OUTLINE OF THE SPECIAL ISSUE

As a sequel to two National Science Foundation (NSF)-sponsored Symposia on Memristors, Memristive Devices and Systems (November 2008 and February 2010) which were held at the University of California Berkeley, this special issue on memristors in the PROCEEDINGS OF THE IEEE is designed to serve as a good pedagogical resource on memristor technology by complementing the lectures presented by some of the distinguished speakers in the above symposia. The lectures are now widely disseminated through YouTube video presentations and they will benefit interested viewers if they can cross-refer to archival journal papers contributed by the speakers in this special issue. We have made the following outline for the special issue to ensure that it provides balanced presentations on five important aspects of the memristor technology, namely, the theory, the device engineering, the circuit modeling, the digital and analog systems, and the neuromorphic systems. These articles will provide educators to adopt the special issue in advanced undergraduate and graduate courses for integrated circuit design as well as nanoelectronic devices. They will also serve as a good resource for practicing design engineers.

The first three articles provide the theoretical framework of memristors and memristive devices. At first, Chua (paper 1) recapitulates the mathematical treatment in his seminal work to demonstrate how any two-terminal circuit elements that maintain a functional relationship between the time integrals of current and voltage can be classified as memristor. More importantly, his paper provides differential calculus-based formalisms to show that various types of practical devices like phase-change memory, magnetoresistive memory, Josephson and junction devices belong to the memristor family. However, memristive properties transcend the domain of electrical circuits and can be attributed to various types of mechanical, chemical, and biological entities. Jeltsema and Dòria-Cerezo (paper 2) and Georgiou *et al.* (paper 3) provide additional theoretical perspectives by extending the port-Hamilton formalism and Bernoulli equations to account for memristive properties in other systems.

The next three articles discuss various types of physical structures that can be fabricated to realize memristors in integrated circuits. Wong *et al.* (paper 4) discuss the metal–insulator–metal structures that are now gaining wide attention since they can be easily adopted in conventional CMOS foundry to integrate 3-D nonvolatile memory chips as well as the synapses for neuromorphic computing. The next paper in this category, by Gergel-Hackett *et al.* (paper 5), discusses how to fabricate memristors on flexible polymer substrates to advance its applications in lightweight, inexpensive, flexible electronics products.

Device modeling is an important aspect of memristor research in order to simulate large applications using SPICE equivalent memristor circuit models. Depending on the materials

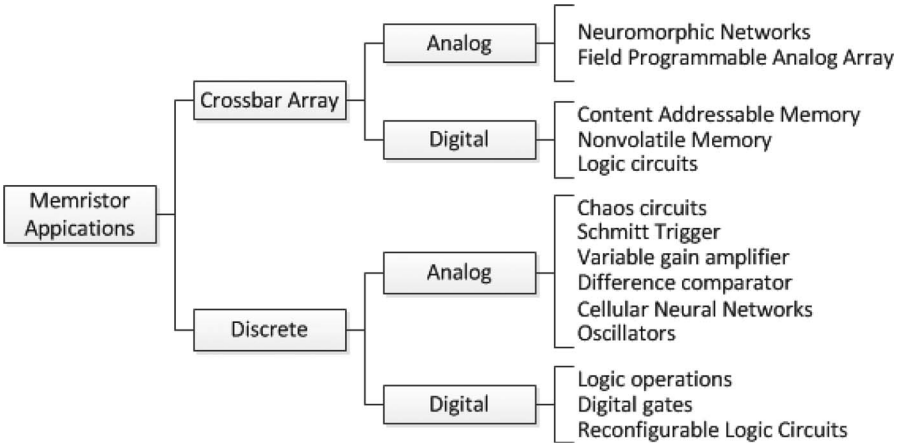

Fig. 1. ***Taxonomy of memristor applications.***

and transport mechanisms (shuttling of oxygen ions versus filament formation through metal ion migration), the device current–voltage characteristics and circuit models can vary widely. Dittmann *et al.* (paper 6) discuss transport models for various types of oxide-based memristors, while Eshraghian *et al.* (paper 7) have developed SPICE-ready circuit models so that system designers can accurately measure the static and dynamic behavior of memristor-based large systems.

In the memristor application frontier, the contributed papers can be divided into three important classes of applications, namely: 1) design of nonvolatile memristor memory system; 2) digital and analog systems; and 3) neuromorphic systems. Sacchetto *et al.* (paper 8) introduce multiterminal memristive nanowire devices in memory applications, while Shin *et al.* (paper 9) develop pattern-sensitive statistical model for nonvolatile resistive random access memory (RAM) memory array with self-adaptable sense resistance. Rose *et al.* (paper 10) discuss the advantages of introducing memristors in the reprogrammable digital systems such as field-programmable gate arrays (FPGAs) and programmable logic devices (PLDs) to replace bulky static random-access memory (SRAM)-based configurable memories. Finally, the brain-like computing capability of memristor-based complex spike-timing-dependent plasticity (STDP) learning networks is demonstrated by Ebong and Mazumder (paper 11), while a simple memristive bridge synapse circuit capable of learning is presented by Kim *et al.* (paper 12). Finally, Pershin and Di Ventra (paper 13) address the capability of memristors to perform quantum computation in addition to conventional neuromorphic and digital data processing.

III. A BIRD'S EYE VIEW OF APPLICATIONS OF MEMRISTORS WITH BIBLIOGRAPHIC INFORMATION

The aforementioned 13 papers are merely a small representative of the whole gamut of multifarious research activities currently underway in the field of memristors. To provide the overall perspectives of numerous applications of memristors, we will provide a short tutorial with appropriate categorization of memristor applications into 1) discrete device applications and 2) array devices applications. The discrete device applications use memristors in a manner that takes advantage of their nonlinear characteristics and their controllable resistance changes to enhance the performance of the desired application. Array device applications on the other hand not only depend on memristor properties but are also coupled with the ongoing trend to increase the device density by reducing the width of the wires in nanocrossbar structure. The quest for the terabit nonvolatile high-density memory using the crossbar structure is pushing the memristor cross-point cell area nearly to 100 nm^2. Fig. 1 provides the taxonomy of applications for memristors in both crossbar array and discrete device form. A comprehensive listing of these papers is provided here since only a few of these applications are covered in this special issue.

Some applications actually adjoin both clusters depending on the intended usages. From a research perspective, some papers focus on how unit cells would work: for example, STDP in [1], associative memory demonstration [2], and a feedback write scheme for a memristive memory in [3]. Strictly speaking, the illustration may actually be an example of a discrete application but the emphasis of work actually points to an array application. This is why memory applications and some examples of biomimetic circuits are under the array devices categories and not discrete devices, even though the cited papers themselves may point to the workings of a unit cell. Due to space

constraints, not all applications will be highlighted in detail, but we hope to provide readers with enough bibliographic content to inspire their exploration into key applications. The application examples that will be mentioned in more detail are: nonvolatile memory, biomimetic (neuromorphic) circuits, reconfigurable logic, chaos circuits, and logic gates.

Nonvolatile memory (NVM) work is the most mature of all the applications because NVM has been in the research phase for decades in various forms due to the recognition that flash memory would stop growing due to scaling limits [4]. Resistive random access memory (RRAM) can be arguably regarded as a subset of memristors. The accompanying article by Leon Chua provides the formal definition of memristors which encompasses the I–V characteristics of various classes of resistive and phase change RAMs. Before physical uncovering of memristors by HP, research and development of phase change RAM (PCRAM) had been ongoing for decades and PCRAM is expected to debut in commercial applications in the near future, with the milestones of memory chip demonstration at the 90-nm technology node [5] and the 45-nm 1-Gb phase change material (PCM) chip [6]. PCRAM relies on changing a PCM between a crystalline state (low-resistance state) and an amorphous state (high-resistance state) by use of electrical current. There have been many good reviews of the development of the technology, and more details can be found in [7] and [8].

Besides PCRAM, various other forms of hysteretic memories have been proposed and are being developed. First reports about resistance switching in metal–oxide–metal devices date back to 1962 in which Hickmott reported a hysteretic resistance change in $Al/Al_2O_3/Al$ structures after application of voltage pulses [9]. Later similar effects were observed in NiO [10], SiO [11], and As_2S_3 [12]. This early period of research was based mainly on relatively thick oxide films which in some cases needed the application of high voltages in the range of several hundred volts. The period lasted until the mid-1980s and has been comprehensively reviewed by Dearnaley *et al.* [13], Oxley [14], and Pagnia and Sotnik [15]. Obviously the activity faded because of the lack of progress in understanding and controlling the phenomena due to insufficient analytical tools and technological equipment at that time.

A new era in research on resistive switching started in the late 1990s, initiated independently by Asamitsu *et al.* [16] using manganites, Kozicki *et al.* [17] studying Ag–GeSe systems, and Beck *et al.* [18] investigating titanates and zirconates. A broad spectrum of mechanisms has been suggested as underlying mechanisms for the resistive switching in the metal–oxide systems. In 2006, Szot *et al.* were able to clarify the underlying effect as a motion of oxygen ions and a coupled electrochemical redox process on the nanometer scale at structural defects in the crystal lattice of the metal oxides [19]. In other words, the ion motion triggers a change of the stoichiometry on the nanoscale near one electrode. This leads to a redox reaction caused by a valence change of the cation sublattice and a drastic change in the electronic conductivity, known as an insulator–metal transition. For this reason, the expression valence change memory effect (VCM) was suggested for bipolar metal–oxide systems by Waser *et al.* [20]. The memristor devices presented by the HP group [21], [22] belong to this class of materials. Subsequently, a whole variety of observed switching phenomena could be classified into three different types of redox-based RRAM [20], [23]. In addition to the VCM effect just mentioned, there is a type of unipolar resistive switches which relies on a thermochemical memory (TCM) effect (also known as fuse-antifuse switches). Here, temperature gradient between a conducting filament and the surrounding material is the main driving force for the switching, while electrochemical effects play a secondary role. Already in 2004, Samsung presented an integrated memory circuit which utilized this effect that leads to a change of the stoichiometry due to a current-induced increase of the temperature [24]. A detailed review of the TCM area has recently been published by Ielmini *et al.* [25]. There is a clear link between the unipolar TCM and the bipolar VCM-type switching. By changing the current control of a metal–oxide cell, the type of switching can be altered [26]. Furthermore, it has been shown that apart from the field-accelerated movement of oxygen vacancies [27], [28], the thermal assistance plays a key role in explaining the nonlinearity of the switching kinetics of VCM-based devices [29]. A third type of resistive switches relies on the fact that one of the electrodes contains an electrochemically active metal such as Ag or Cu. These electrochemical metallization (ECM) memories (also called conductive bridge RAM) utilize the electrochemical oxidation of, for example, Ag metal to Ag^+ ions, the drift of these highly mobile cations in the ion conducting layer, and their discharge at the (inert) counter-electrode. This leads to a growth of Ag dendrites which form a highly conductive filament in the ON state of the cell. Terabe *et al.* have shown that the effect can be scaled down to the atomic level leading to the observation of Landauer conductance steps at room temperature [30], demonstrating the ultimate scaling potential of this type of resistive RAM. A fully CMOS integrated 2 M-bit memory has been presented by Qimonda researchers [31]. A comprehensive review of the ECM area including the related background in electrochemistry has recently been given by Valov *et al.* [32].

In most cases, all three types of redox-based RRAM show a filamentary-type of resistive switching [33]. However, there are some reports in the literature about resistive switching material combinations which show electrode-area-dependent

resistances [27]. Sawa [34] reported on a so-called homogeneous interface-type switching which is observed in heterojunctions between Nb-doped $SrTiO_3$ [35] and $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) with various metals. Generally, this type of switching cells shows a clear scaling of the device resistance with the area. For this type of devices, the change of the resistance is attributed to the field-induced change of the Schottky barrier at the interface. Moreover, it has been shown that filamentary as well as interface-type switching coexists in $SrTiO_3$ metal–insulator–metal structures [36]. The type of I–V characteristics of all redox-based RRAMs is a necessary condition to classify them under generalized memristors. Pershin and DiVentra have stated recently the additional sufficient conditions for a generalized memristor to be a proper RRAM [37].

Some of the problems faced by memristor memories in the crossbar structure are leaky crossbar devices, nonuniform resistance profile across the crossbar array, resistance drift, and low yield issues. Various methods are used to address the problems associated with the crossbar memory array: using correcting pulses to restore state after reading, thereby mitigating the effect of resistance drift during memory operation [38]; adding access diodes to isolate devices in order to reduce the leakage of crossbar memory elements [39]; implementing them as complementary resistive switches [40]; and using adaptive writing and erasing methods to combat low yield issues and the effects of nonuniform resistance profile across the crossbar array [3], [41], [42]. Many memory papers are available that address issues related to READ/WRITE issues in the memristor crossbar, and a sizeable amount contain discussions about realizing multibit [43] cells in memristor memories. A more detailed discussion of the RRAM is presented in [44]. A different memory structure, the content-addressable memory (CAM), has been shown to benefit from memristor implementation through better power management [45].

A conceptual extension of digital memory is digital logic, and memristors have been proposed and demonstrated for different digital logic applications. The first, an amalgamation of memory and logic, is the flip flop [46], and the second is logic gates [47], [48]. The use of memristors in a discrete fashion tailored to building of logic blocks like the flip flop is advantageous because it shows resiliency to power losses. In [46], the experimental nonvolatile synchronous flip flop had an error rate of 0.1% during 1000 power losses. The same advantages can be found in an FPGA implementation with memristors [49]. In a crossbar topology, a field programmable nanowire interconnect (FPNI) architecture can be used to increase density and reduce power consumption [50]. In FPNI architecture, the crossbar is used only for routing, and stark improvements over CMOS-only FPGAs have been demonstrated. A discrete FPGA architecture that uses memristors purely for interconnect purposes is dubbed mrFPGA and is presented in [51]. mrFPGA boasts ~5.5X area reduction, 2.3X speed increase, and 1.6X power reduction. Boolean logic gates have been investigated for crossbar implementation but their performance lags behind standard CMOS gates [52]; fast CMOS transistors in conjunction with crossbar array is necessary in order to have acceptable performance compared to CMOS [53]. Logic gates using implication logic [54–56] and threshold logic [57] have also been investigated for alternative means to realizing more compact circuits using memristors. Kim *et al.* [55] propose a novel stateful logic pipeline architecture based on memristive switches. The proposed architecture mapped to the FPNI fabric produces a field-programmable stateful logic array (FPSLA), in which general-purpose computation functions can be implemented by configuring only nonvolatile nanowire crossbar switches. CMOS control switches are used to isolate stateful logic units so that multiple operations can be executed in parallel. The proposed architecture has been mapped to the FPNI fabric to produce a FPSLA in which the functionality can be implemented by configuring only the nonvolatile switches in the nanowire crossbar layer. This low-register-cost fine-grain ultradeep constant-throughput pipeline poses new problems to the design automation research community.

Potential applications of discrete memristors comprise performance enhancement of analog circuits. In general, analog circuits, for the most part, suffer from a larger area consumption compared to digital circuits. By using memristors as potentiometers in the case of programmable amplifiers, some have shown added functionality with reduced area [58], [59]. Memristors have also been proposed in designing cellular neural networks (CNNs) [60], [61], recurrent neural networks [62], ultrawideband receivers [63], adaptive filters [64], oscillators [65], programmable threshold comparators, Schmitt triggers, and difference amplifiers [58]. Within analog processing domain, the two applications that have garnered widespread attention are use of memristors in chaos circuits and use of memristors for biomimetic circuits. These two will be expounded upon in the following paragraphs.

The chaos applications of memristors have a large application space ranging from secure communication to medical purposes like seizure detection. Current papers in this area strive to use memristor properties to invoke a chaotic response. In [66], second-order effects of a memristor are considered to show that by choosing certain parameters, the memristor connected to a power source can exhibit chaos. The second-order properties of the memristor are cited to allow the smallest chaotic circuit observed. Other circuits with memristors that exhibit chaos achieve chaos by adapting a modified Chua's circuit. By replacing the Chua diode with the

memristor [67–69], chaos can be observed. An experimental demonstration of chaos with analog components used to build the memristor is presented in [70]. An image encryption application using piecewise linear memristors is presented in [71].

There have been multiple displays of using memristors in biomimetic and neuromorphic circuits [1], [72]– [82]. In the neuromorphic circuit approach, observable biological behavior or processing is aimed to be replicated. A simple way to build neuromorphc circuit using memristors is to build processing elements or "neuron circuits" with standard CMOS while the adaptive synapses are implemented using the memristor crossbar. Memristors have enlivened the neuromorphic circuit area because they have the potential of synaptic integration that is lacking in CMOS. In literature, various groups have demonstrated through simulation how to achieve STDP with memristors [1], [73], [76], [78]. Experimentally, STDP has been shown to be viable for a-Si memristor [74] as well as a Cu_2O device [79]. Larger applications based on spiking neural networks have also been proposed. Querlioz *et al.* [81] show that memristors utilized in neuromorphic configuration for unsupervised learning can tolerate device variation. Memristor implementation of the ink drop spread (IDS) method has been shown to exhibit low latency and strong immunity to power failure [82]. The area for neuromorphic computing is ripe with multiple works on showing different applications occurring in parallel; a recent review of adaptive oxides with more details on materials is presented in [83].

Since Chua's original paper in 1971 [84] and Chua and Kang's subsequent paper in 1976 [85] memristors and memristive system research was stalled due to lack of known compact solid-state devices that can be utilized in monolithic fabrication. However, during the past few years many computer models have been introduced for computer-aided analysis of memristor circuits and memristive systems [86–92]. As more researchers in various application domains are becoming intrigued by the latent potentials of these fascinating devices, new applications are expected to usher in with the help of augmented design automation tools and precise computer models for memristors. ■

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