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Design and Implementation of Multiple-valued Inverter Circuits Using Threshold Control in Silicon and Carbon Nanotubes Transistors

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ABSTRACT

Nowadays, multi valued logic circuits have lower power consumption, lower data transfer and also the simpler operations than the binary logic circuits. The most multi valued logic circuits use less number of gates than the binary logic circuits. Thus using multi valued logic will reduce the connections and more information will be processed than a binary element. Thus by using multi-valued logic we have achieved better complexity in the VLSI and ULSI integrated circuits. Because of the carbon nanotube field effect transistor characteristics most of the ternary circuits are design and implemented by this technology, but in this paper we try to have the ternary inverter by using the conventional and silicon transistors (MOSFET). In this paper, we try to design multi-valued inverter circuits with threshold control in the field effect transistors (MOSFET and CNTFET). The simulation results shows that we have achieved a ternary inverter through MOSFETs in compare with the CNTFETs in different voltage and temperatures. The behavior of deviation percent of the average delay for different temperature to approve the denouements are achieved.

KEYWORDS: Carbon nanotube, multiple-valued logic, TVL invertor, CNTFET.

1. INTRODUCTION

The most of semiconductor technology which are used in the integrated circuits are try to replace the ancient and most common silicon technology to an improved carbon nanotubes technology as an intrinsic semiconductors to approach all the nanotube Benefits such as scale, speed, power and etc. Considering the primary examinations that have been done on Carbon nanotube field-effect transistors Single-walled and by observing similar behaviors to the behaviors of the typical semi conductive transistors (Metal oxide silicon field effect transistors), it can be said: the field-effect transistors able to replace with MOSFET in nano-scale electronics. Therefore, the Carbon nanotube field-effect transistors is a special MOSFET which is very important and the basis of diagram block of Integrated circuits. Micro circuits need this block to reach their minimum sizes. In fact, by replacing the Carbon nanotube field-effect transistors with MOSFET, transistor-makers will be able to use micro circuits as functional pieces where they have to use special molecules. And then, they can supply a new category of smaller chips with higher speed and much less consuming power than today's Silicon chips to the market. So, studying the Carbon nanotube field-effect transistors and understanding and comprehending its behavior are two vital subjects to technology and the future of electronics. Also, developing technology and exploring carbonic nanotubes, the Carbon nanotube field-effect transistors have less consuming power and less delay than the silicon ones, and even are made concisely in very smaller sizes up to nano sizes in a very special and unique shape [1, 2, 3, 4], By using CNTFETS, low power consumption, high performance, ballistic transport, off-current properties and very little storage space have been achieved[5, 6, 7, 8, 9, 10]. Nowadays, MVL circuits have lower power consumption, lower data transfer and also the simpler operations than the binary logic circuits. The most MVL circuits use less number of gates than the binary logic circuits. Thus using MVL will reduce the connections and more information will be processed than a binary element. Thus by using MVL we have achieved better complexity in the VLSI and ULSI integrated circuits. [11, 12, 13].

One of the important applications of the analog circuits is connecting the real world with digital circuits. Previously for digital calculations binary logic (0, 1) was usually used. But today great potential of MVL make it the best replacement for digital calculations.[14] Because of the simple implementing method of electronic circuits and less connection costs the ternary logic can be overcome all the digital and binary problems. [15, 16, 17] MVL systems in addition to the binary logical value (0, 1), have some more logical values. As an instance the ternary logic also have an additional value than (0, 1), which is 2 and the ternary have three different voltages 0V, VDD/2 and VDD, respectively.

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Because of the CNTFET characteristics most of the ternary circuits are design and implemented by this technology, but in this paper we try to have the ternary inverter by using the conventional and silicon transistors (MOSFET). In this paper, we try to design multi-valued inverter circuits with threshold control in the field effect transistors (MOSFET and CNTFET). In this paper we have presented a novel circuit design technique to implement a three-valued logic inverter by using carbon nanotube and silicon field effect transistors. By the results, we have achieved a ternary inverter through MOSFETs in compare with the CNTFETs in different voltage and temperatures.

2. Design and Implementation of a Ternary Value Inverter Circuit by Silicon Transistor

Figure 1 shows the ternary circuit design of an inverter by using MOSFET. this circuit power for VDD=2 ,3 ,4 and 5 volts and 0, 10 ,27 ,37 ,50 ,60 , 70 ,80 ,90 and 100° C temperatures are obtained. Simulation results result in that we have the worse power in 5 volts and the best one in 2 volts. Table 1 exhibit The Percent Deviation of the average power, Figure 2 shows that Percent Deviation of the average for voltage 5 V is less than the other voltages. Average Percent Deviation of the average power for VDD=2 ,3 ,4 and 5 volts are 10.007 ,9.177 ,8.14 and 6.731 respectively, Average Percent Deviation of the average power for voltage 5 V is less than the other voltages.

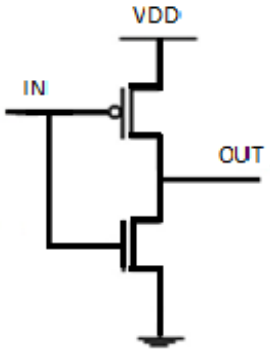

Figure 1 - inverter circuit design by MOSFET

Table 1 – The results for deviation percent of the average power of this circuit for VDD are 2, 3, 4; for voltage 5 ; and temperatures 0, 10,27, 37, 50, 60, 70, 80, 90 and 100° C

VDD/TEMP	0	10	27	37	50	60	70	80	90	100
2v	18.42	14.68	8.74	5.25	1.71	3.62	6.72	10.02	13.86	17.05
3v	16.69	13.6	7.91	4.12	0.37	3.27	6.34	10.02	13.29	16.16
4v	14.97	11.27	7.35	4.69	0.1	2.86	6.03	8.73	11.11	14.29
5v	12.14	9.89	6.08	3.49	0.35	2.03	4.47	6.91	10.16	11.79

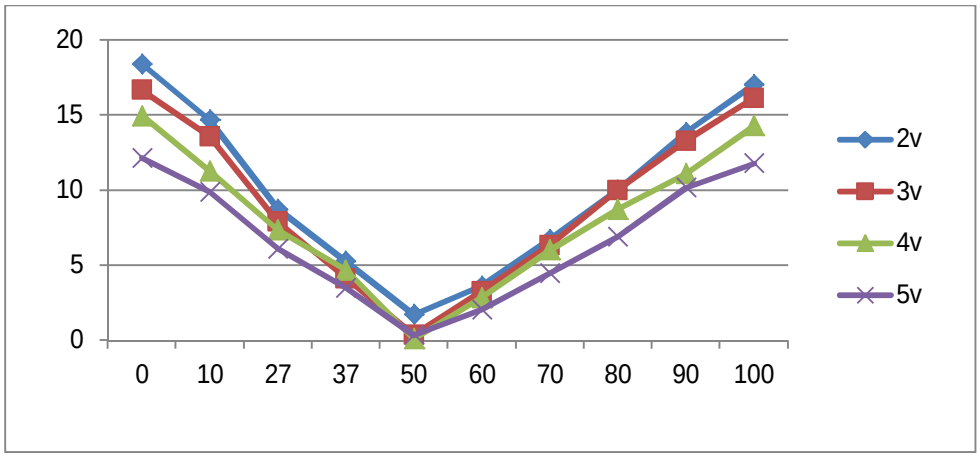

Figure 2 – The results for deviation percent of the average power of this circuit for VDD are 2, 3, 4; for voltage 5 ; and temperatures 0, 10,27, 37, 50, 60, 70, 80, 90 and 100° C

Table and Figure 3 show the Percent Deviation of the average delay values. For VDD= 2, 3, 4 and 5 volts the average Percent Deviation of the average are 9.87%, 23.19%, 22.90% and 9.14% respectively.

Table2 - The results for deviation percent of the average power of this circuit for VDD are 2, 3, 4; for voltage 5 ; and temperatures 0, 10,27, 37, 50, 60, 70, 80, 90 and 100° C

VDD/TEMP	0	10	27	37	50	60	70	80	90	100
2v	19.77	10.12	6.25	9.207	7.096	7.32	6.959	13	3.89	15.11
3v	14.22	11.51	7.033	87.55	13.31	11.06	19.42	4.799	33.49	29.54
4v	18.94	5.65	17.3	90.92	5.89	4.06	23.75	25.06	3.86	33.56
5v	10.23	17.81	8.042	7.067	0.649	6.38	3.9	15.07	21.92	0.37

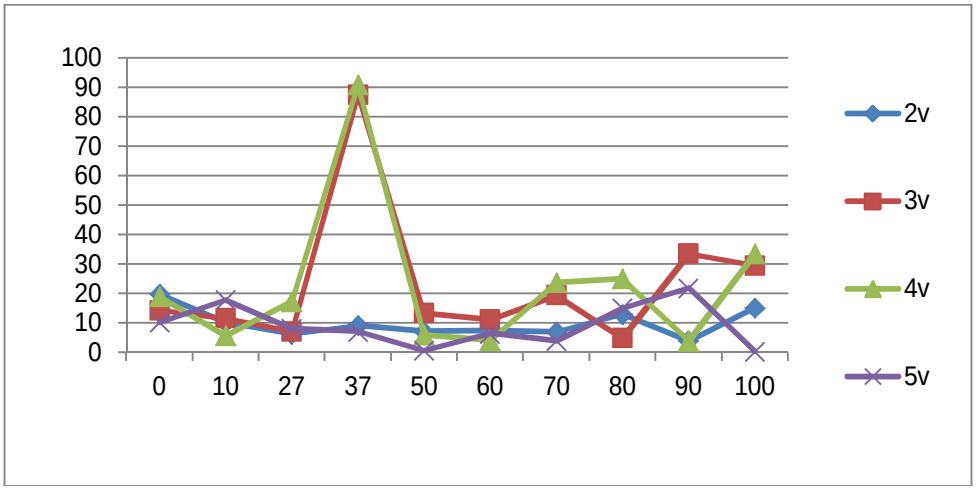

Figure 3 – The results for deviation percent of the average power of this circuit for VDD are 2, 3, 4; for voltage 5 ; and temperatures 0, 10,27, 37, 50, 60, 70, 80, 90 and 100° C

3. Design and Implementation of First Ternary Value Inverter Circuit by CarbonNanotubes Transistor

The second inverter circuit design by CNTFET is shown in Figure 4. In this circuit we have designed MVL circuit by using the threshold control of N-channel transistors. We have achieved zero for the Percent Deviation of the average power for all voltages and temperatures, thus the power Performance of these CNTFET circuit is better than MOSFET.

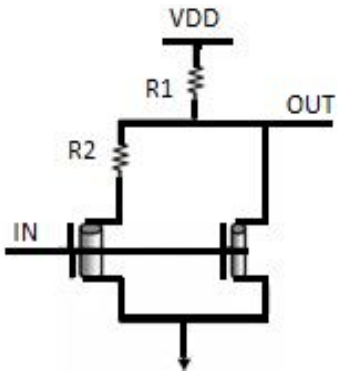

Figure4 - inverter circuit design by CNTFET N-channel

We have the best average delay circuit Behavior in the 0.9 volts. CNTFET has better circuit percent deviation of the average delay than MOSFET. Table 3 and Figure 4 shows the Results of Percent Deviation of the Average delay. The average percent deviation of the average delay for voltage 0.9 V is 1.495%, which is better than the average in 2 V. the average percent deviation for 2 V is 1.612%.

Table 3 – The results for deviation percent of the average delay of this circuit for VDD are 0.9 and 2 volts ; and temperatures 0, 10,27, 37, 50, 60, 70, 80, 90 and 100° C

VDD/TEMP	0	10	27	37	50	60	70	80	90	100
0.9v	0.071	2.93	0.607	3.69	1.066	0.013	0.188	2.26	0.524	3.605
2v	0.329	2.701	0.419	0.417	2.781	2.61	2.151	3.165	0.417	1.132

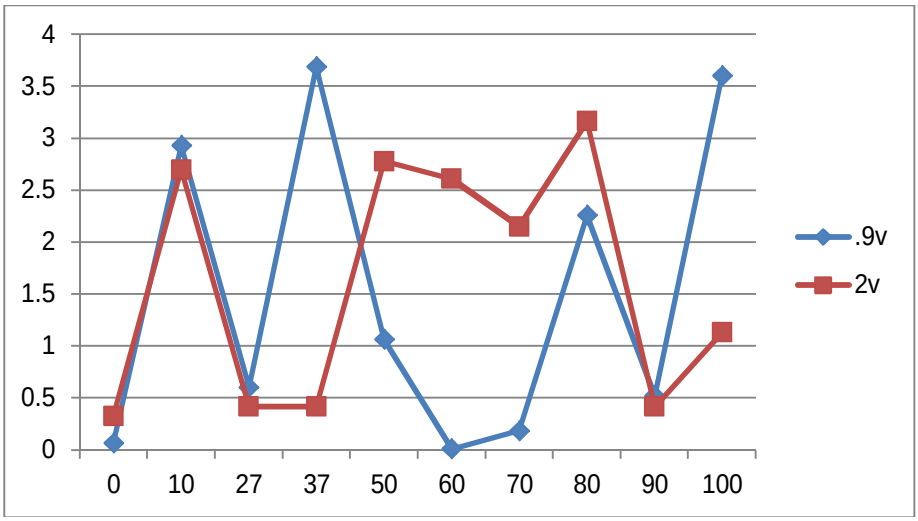

Figure 5 – The results for deviation percent of the average delay of this circuit for VDD are 0.9 and 2 volts ; and temperatures 0, 10,27, 37, 50, 60, 70, 80, 90 and 100° C

4. Design and Implementation of Second Ternary Value Inverter Circuit by Carbon Nanotubes Transistor

By using threshold control N-channel transistors and a P-channel transistor is design ternary logic for inverter circuit that is shown Figure 6.

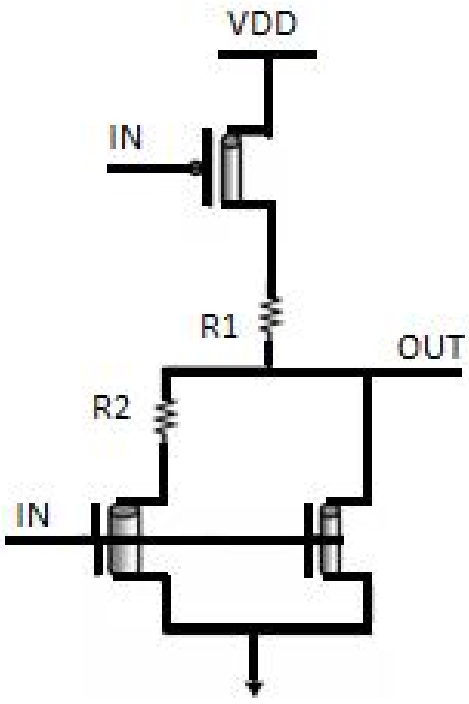

Figure 6 - inverter circuit design by CNTFET N-channel and P-channel

The minimum and maximum of the power consumption are achieved by 0.9 and 5 volt. According to Table 4 the deviation percent of the performance of average power is better than MOSFET, so the second circuit designed by CNTFET consumes less power, because the deviation percent of the average power at any temperatures is very low. The average deviation percent of the average power for all voltages has been calculated as follows: $3.004E^{-1}\%$,$2.332E^{-2}\%$,$9.92E^{-3}\%$,$9.35E^{-2}\%$ and 0%. The lowest average deviation percent achieved for the 3 V is.

Table4 –The results for deviation percent of the average power of this circuit for VDD are 0.9,2,3,4; for voltage 5; and temperatures 0, 10, 27, 37, 50, 60,70, 80, 90 and 100° C

VDD/TEMP	0	10	27	37	50	60	70	80	90	100
0.9v	0.158	0.158	0.158	0.158	1.53	0.158	0.158	0.158	0.158	0.21
2v	0.03	0.03	0.019	0.019	0.03	0.019	0.03	0.019	0.019	0.019
3v	0.006	0.01	0.011	0.011	0.011	0.011	0.011	0.006	0.011	0.011
4v	0.028	0.032	0.078	0.028	0.024	0.097	0.07	0.05	0.011	0.262
5v	0	0	0	0	0	0	0	0	0	0

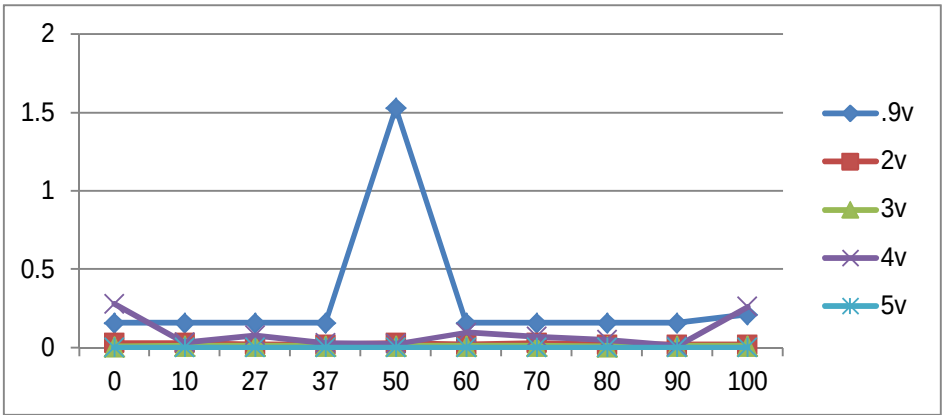

Figure 7 – The results for deviation percent of the average power of this circuit for VDD are 0.9, 2, 3, 4; for voltage 5 ; and temperatures 0, 10,27, 37, 50, 60, 70, 80, 90 and 100° C

You can see the behavior of deviation percent of the average delay for CNTFET2 circuit in Figure 7 and Table 5. When VDD equals 0.9, 2, 3, 4 and 5 volts the average deviation percent of the average delay is 1.738%, 1.030%, 2.927%, 6.156% and 0.4497% respectively.

Tables 5 – The results for deviation percent of the average delay of this circuit for VDD are 0.9, 2, 3, 4; for voltage 5 ; and temperatures 0, 10,27, 37, 50, 60, 70, 80, 90 and 100° C

VDD/TEMP	0	10	27	37	50	60	70	80	90	100
0.9v	0.105	1.65	1.02	0.15	0.898	5.65	0.63	2.98	1.43	2.87
2v	4.14	0.597	0.248	2.31	0.84	0.129	0.67	0.019	0.24	1.108
3v	3.12	0.65	1.42	12	2.05	2.42	0.797	0.86	4.07	1.88
4v	3.97	7.36	9.88	6.49	0.78	10.6	12.75	0.79	6.37	2.57
5v	0.023	0.624	0.582	0.228	1.87	0.209	036	0.226	0.28	0.095

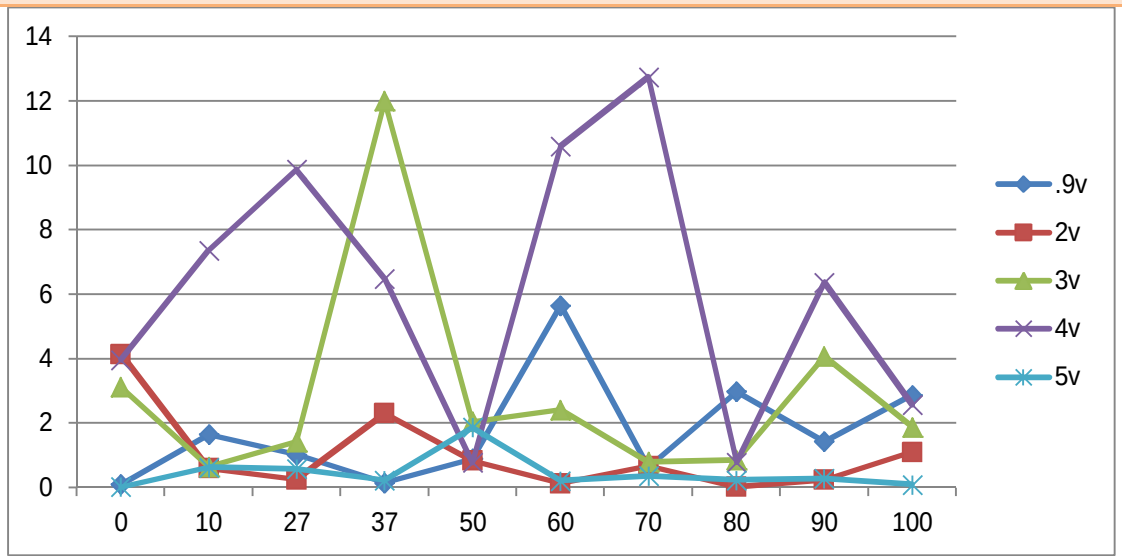

Figure 8 – The results for deviation percent of the average delay of this circuit for VDD are 0.9,2, 3, 4; for voltage 5 ; and temperatures 0, 10,27, 37, 50, 60, 70, 80, 90 and 100° C

5. The Comparing CNTFET Circuits

In this section, we're going to compare the behavior of CNTFET circuits at the same voltages. First, we are going to check the power of CNTFET circuits in 0.9 volts. According to Table 6 and Figure 8, it can be conclude that the performance of the deviation percent of the average power for CNTFET1 is less than CNTFET2. The average deviation percentage for the average power of CNTFET2 is 0.728%.

Table 6 – Results for the deviation percent of the average power of CNTFET1 and CNTFET2 circuits is as Follows: for VDD: 0.9 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

T/TEMP	0	10	27	37	50	60	70	80	90	100
CNTFET1	0	0	0	0	0	0	0	0	0	0
CNTFET2	0.16	0.16	0.16	0.16	1.58	0.16	1.58	1.58	0.16	1.58

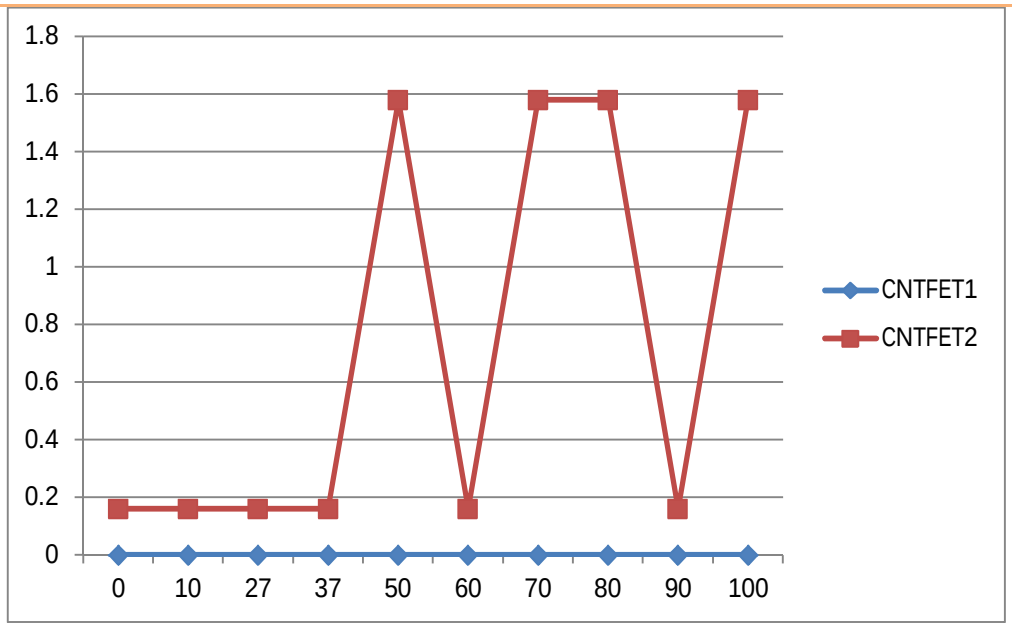

Figure 9 – Results for the deviation percent of the average power of CNTFET1 and CNTFET2 circuits is as follows: for VDD : 0.9 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

Table 7 and Figure 9 show the deviation percent for the average delay in CNTFET circuits in 0.9 volts, According to the deviation percent for the average delay is Less for circuit CNTFET1. We have achieved circuits 1.4943% and 1.7368% for the average deviation percent for the average delay for CNTFET1 and CNTFET2 circuits.

Table 7 – Results for the deviation percent of the average delay of CNTFET1 and CNTFET2 circuits is as follows: for VDD : 0.9 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

T/TEMP	0	10	27	37	50	60	70	80	90	100
CNTFET1	0.071	2.93	0.607	3.69	1.07	0.013	0.188	2.25	0.524	3.6
CNTFET2	0.10.5	1. 65	1.02	0.15	0.896	5.65	0.627	2.97	1.43	2.87

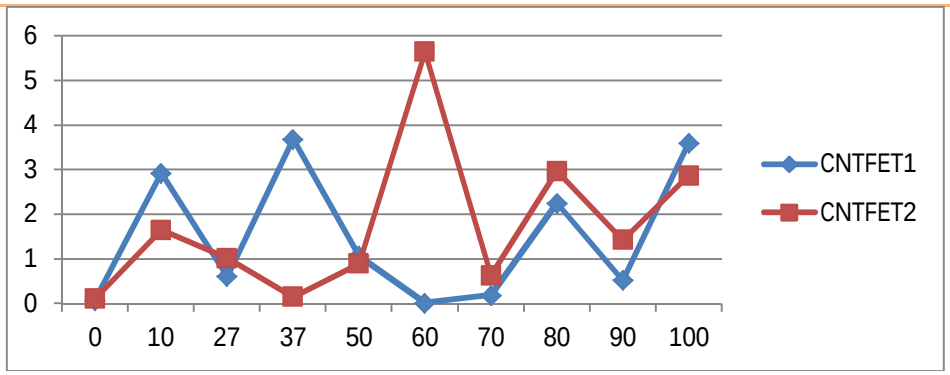

Figure 10 – Results for the deviation percent of the average delay of CNTFET1 and CNTFET2 circuits is as follows: for VDD : 0.9 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

6. **The Comparing CNTFET Circuits with MOSFET Circuit**

The performance of CNTFET1, CNTFET2 and MOSFET circuits is shown in table 8 and Figure 10. Considering them as the Minimum of deviation percent for the average power of CNTFET1 circuit, the maximum of deviation percent was also observed in MOSFET. The average deviation percent for the average power for CNTFET1, CNTFET2 and MOSFET circuits is respectively 0%, 0.023% and 9.984 %.

Table 8 - Results for the deviation percent of the average power of CNTFET1 and CNTFET2 circuits is as follows: for VDD : 2 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

T/TEMP	0	10	27	37	50	60	70	80	90	100
MOSFET	18.07	14.22	8.72	5.23	1.75	3.59	6.69	10	14.1	17.5
CNTFET1	0	0	0	0	0	0	0	0	0	0
CNTFET2	0.029	0.029	0.02	0.02	0.03	0.02	0.03	0.02	0.02	0.02

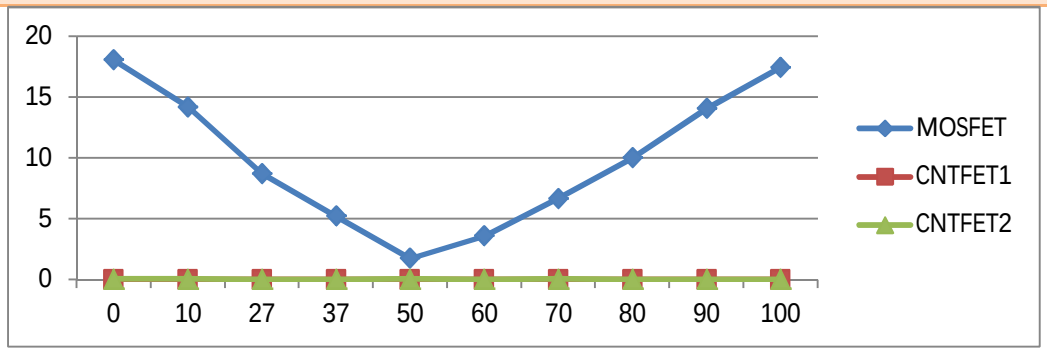

Figure 11 - Results for the deviation percent of the average power of CNTFET1 and CNTFET2 circuits is as follows: for VDD : 2 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

The average delay in MOSFET is higher than CNTFET. We have completely obtained the maximum and minimum of the deviation percent of the average delay for MOSFET and CNTFET1 in 2 V. this percent difference can been seen in table 9 and Figure11. We have obtained the maximum average of the deviation percent of the average delay for CNTFET1 as 1.6153% the minimum for CNTFET2 as 0.8213%, and for MOSFET, this average is 0.904%.

Table 9 - Results for the deviation percent of the average delay of CNTFET1 and CNTFET2 circuits is as follows: for VDD : 2 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

T/TEMP	0	10	27	37	50	60	70	80	90	100
MOSFET	19.82	10.13	6.25	9.29	7.13	7.28	6.96	13.06	3.95	15.17
CNTFET1	0.329	2.72	0.418	0.418	2.78	2.58	2.15	3.19	0.418	1.15
CNTFET2	4.11	0.599	0.25	0.23	0.856	0.132	0.654	0.019	0.243	1.12

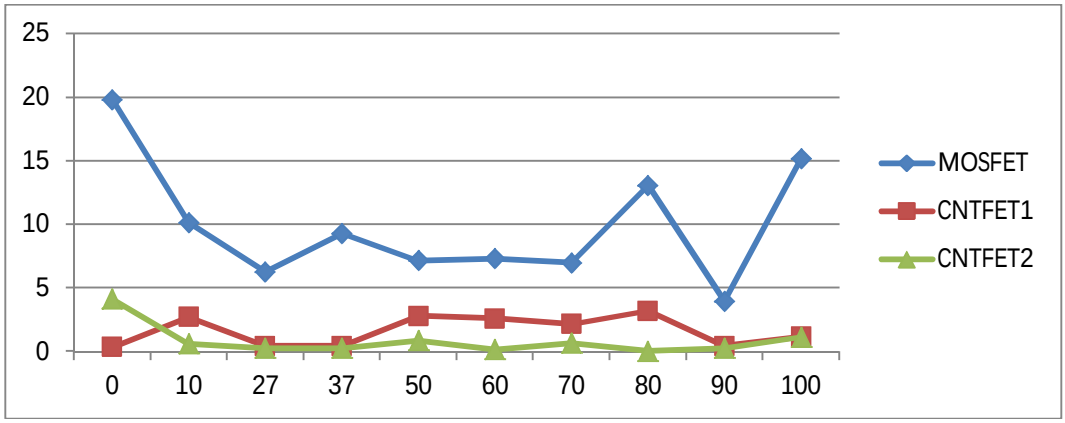

Figure 12-Results for the deviation percent of the average delay of CNTFET1 and CNTFET2 circuits is as follows: for VDD : 2 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

7. **The Comparing Second CNTFET Circuit with MOSFET Circuit**

In MOSFET, when VDD equals 3V (VDD=3V), as temperature increases the power decreases. The average deviation percent of the average power for CNTFET2 and MOSFET circuits has the values of $1.32E^{-2}$%and $0.9189E^{1}$%. The deviation percent for CNTFET2 circuit is less than MOSFET, as it can been seen in Table 10 and Figure 12.

Table 10 - Results for the deviation percent of the average power of CNTFET1 and CNTFET2 circuits is as follows: for VDD : 3 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

T/TEMP	0	10	27	37	50	60	70	80	90	100
MOSFET	16.69	13.6	7.95	4.12	0.36	0.013	0.188	2.25	0.524	3.6
CNTFET2	0.006	0.01	0.011	0.011	0.011	0.011	0.011	0.006	0.044	0.011

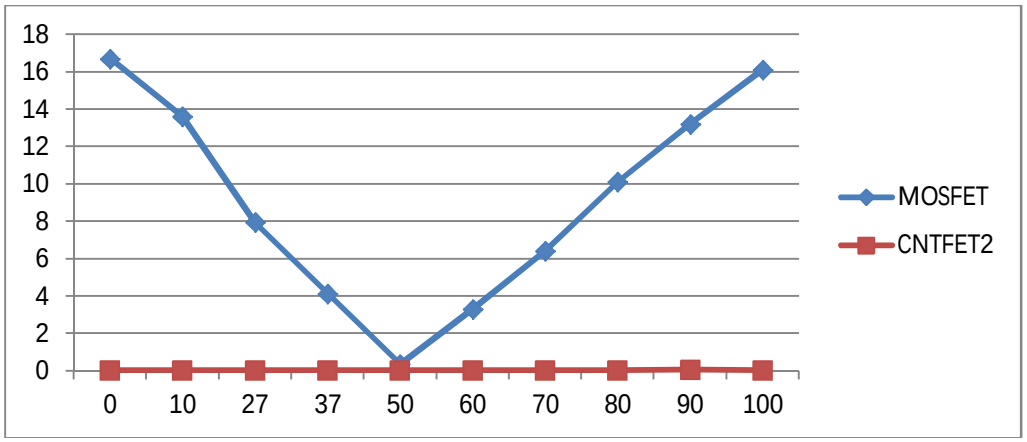

Figure 13 - Results for the deviation percent of the average power of CNTFET1 and CNTFET2 circuits is as follows: for VDD : 3 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

CNTFET2 in 3 volts performs better Than MOSFET. At any temperatures, the average deviation percent for the average delay for CNTFET2 circuit is 2.9105%, and also the average delay for MOSFET is 23.192%. Therefore, the best performance of the average deviation percent and delay in 3 V for MOSFET is.

Table 11 - Results for the deviation percent of the average delay of CNTFET1 and CNTFET2 circuits is as follows: for VDD : 3 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

T/TEMP	0	10	27	37	50	60	70	80	90	100
MOSFET	14.22	11.49	7.04	87.41	13.29	11.06	19.42	4.81	33.48	29.7
CNTFET2	3.12	0.48	1.42	12.02	2.04	2.42	0.797	0.858	4.06	1.89

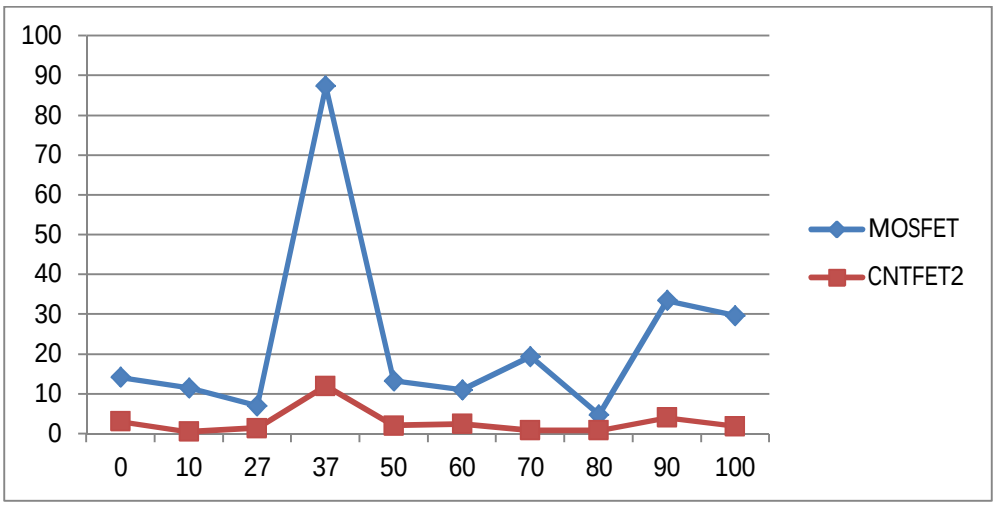

Figure 14 - Results for the deviation percent of the average delay of CNTFET1 and CNTFET2 circuits is as follows : for VDD : 3 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100°C

In Table 12 and Figure 14, we are showing the average deviation percent for Voltage 4 volts. The deviation Percent of the average power reduced more at CNTFET2 than MOSFET, so the power of CNTFET2 is better and less than MOSFET. As temperature increases, the power decreases. The average deviation percent of the average power for CNTFET2 and MOSFET circuits is 0.0932% and 8.1641%.

Table 12 - Results for the deviation percent of the average power of CNTFET1 and CNTFET2 circuits is as follows : for VDD : 4 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

T/TEMP	0	10	27	37	50	60	70	80	90	100
MOSFET	14.63	11.55	7.5	4.67	0.104	2.89	6.007	8.73	11.19	14.37
CNTFET2	0.28	0.033	0.078	0.028	0.025	0.097	0.069	0.051	0.011	0.26

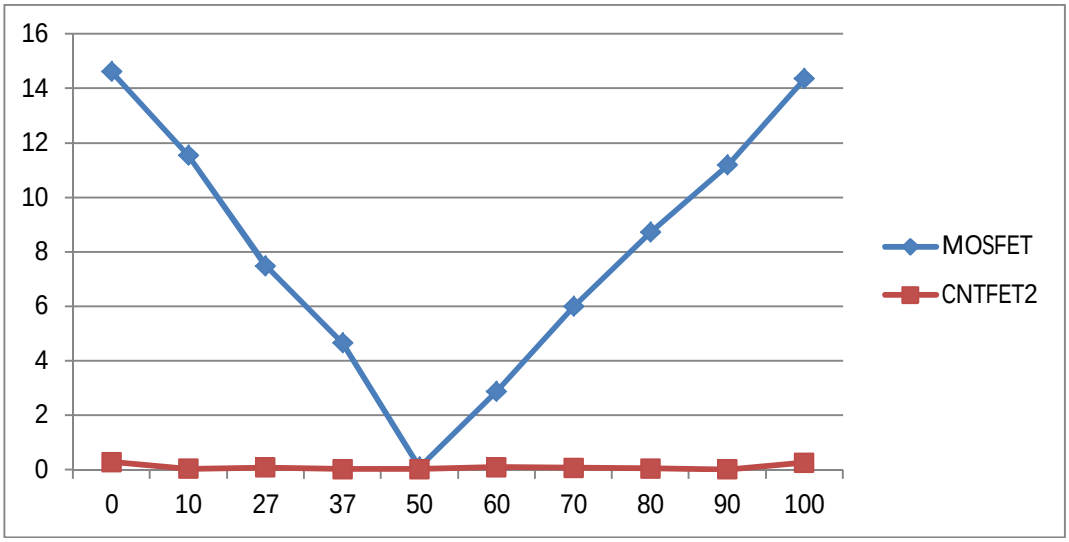

Figure 15 - Results for the deviation percent of the average power of CNTFET1 and CNTFET2 circuits is as follows : for VDD : 4 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

Table 13 and Figure 15 show the deviation percent for the average. Accordingly CNTFET2 circuit at any temperatures has less deviation percent and average deviation percent than MOSFET does, and the average deviation percent for is as follows: 6.312. The best delayed performance is in 4 volts for CNTFET2 circuit, rather than MOSFET circuit. The average deviation percent of the average delay for MOSFET is 23.056.

Table 13 - Results for the deviation percent of the average delay of CNTFET1 and CNTFET2 circuits is as follows : for VDD : 4 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

T/TEMP	0	10	27	37	50	60	70	80	90	100
MOSFET	18.96	5.97	17.31	91.04	5.96	4.07	23.64	24.93	3.94	34.74
CNTFET2	3.97	7.36	9.76	6.33	0.78	10.6	14.59	0.79	6.37	2.57

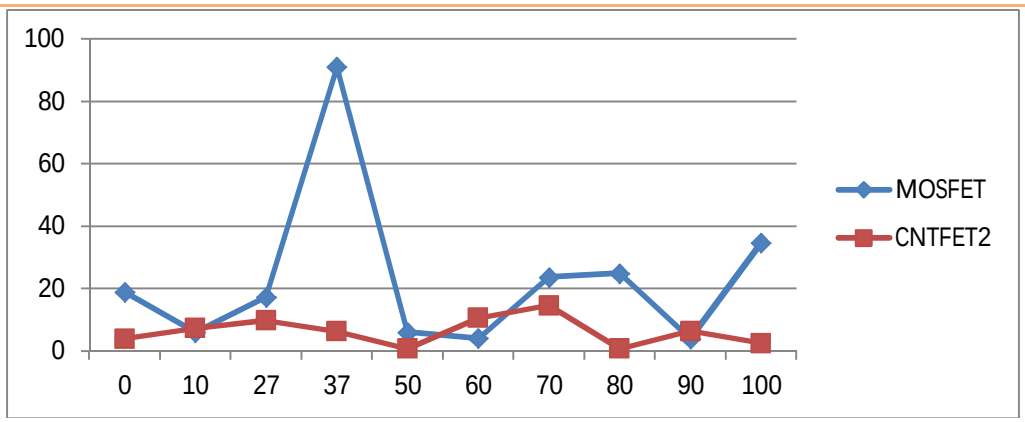

Figure 16 - Results for the deviation percent of the average delay of CNTFET1 and CNTFET2 circuits is as follows : for VDD : 4 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

For voltage 5, the power Diagram for CNTFET2 is linear, and at any temperatures it is 7.4W, that is better than MOSFET circuit. The deviation Percent for the average power for CNTFET2 circuit for all temperatures is zero, which is less than MOSFET circuit. According to Table 14 and Figure 15, based on their performance in the deviation percent for the average CNTFET2 circuit is better than MOSFET circuit. The average deviation percent for the average power for MOSFET is 6.735%.

Table 14 - Results for the deviation percent of the average power of CNTFET1 and CNTFET2 circuits is as follows : for VDD : 5 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

T/TEMP	0	10	27	37	50	60	70	80	90	100
MOSFET	12.1	9.89	6.19	3.5	0.35	2.03	4.63	6.95	10.04	11.67
CNTFET2	0	0	0	0	0	0	0	0	0	0

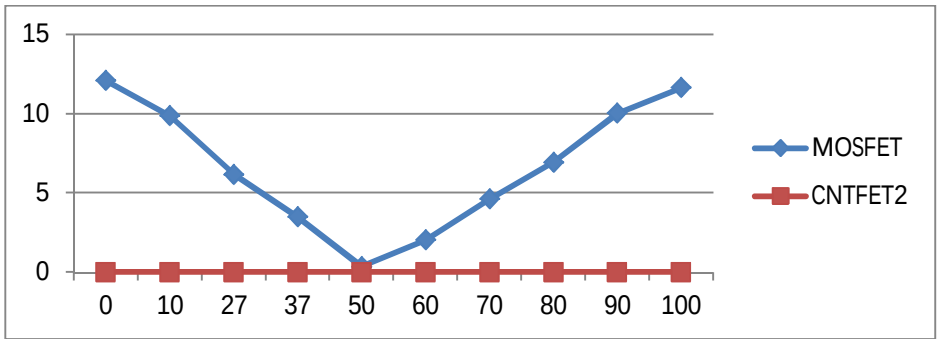

Figure 17 - Results for the deviation percent of the average power of CNTFET1 and CNTFET2 circuits is as follows : for VDD : 5 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

In table 15, the non-linear behavior of MOSFET circuit is shown. The deviation Percent for the average delay of this circuit is more than CNTFET2 circuit. The average deviation percent for the average delay for CNTFET2 circuit and MOSFET circuit is respectively 0.4504% and 9.126%. Thus, CNTFET2 circuit has the least delay and the minimum of deviation percent comparing to MOSFET.

Table 15- Results for the deviation percent of the average delay of CNTFET1 and CNTFET2 circuits is as follows : for VDD : 5 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C

T/TEMP	0	10	27	37	50	60	70	80	90	100
MOSFET	10.23	17.8	8.04	7.07	0.65	6.37	3.9	15.01	21.82	0.37
CNTFET2	0.023	0.619	0.59	0.23	1.87	0.21	0.36	0.226	0.28	0.096

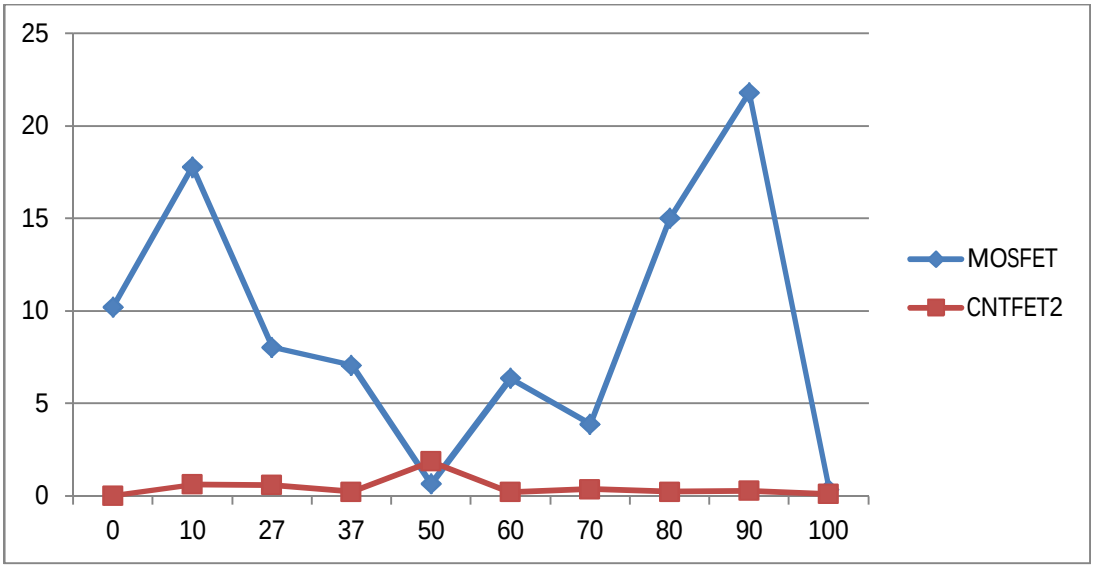

Figure 18 - Results for the deviation percent of the average delay of CNTFET1 and CNTFET2 circuits is as follows : for VDD : 5 volts in the temperatures 0, 10, 27, 37, 50, 60, 70, 80, 90 and 100° C 5. 5

8. CONCLUSION

In this paper we have presented a novel circuit design technique to implement a three-valued logic inverter by using carbon nanotube and silicon field effect transistors. By the results, we have achieveda ternary inverter through MOSFETs in compare with the CNTFETs in different voltage and temperatures. The behavior of deviation percent of the average delay for different temperature to approved the denouements are achieved. The simulation results show that the average deviation percent for the average delay for CNTFET2 circuit and MOSFET circuit is respectively 0.4504% and 9.126%. Thus, CNTFET2 circuit has the least delay and the minimum of deviation percent comparing to MOSFET. The average deviation percent of the average power for CNTFET2 and MOSFET circuits is 0.0932% and 8.1641%.

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The authors declare that they have no conflicts of interest in this research.

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