HIGH MOBILITY III-V MOSFET TECHNOLOGY

M. Passlack, R. Droopad, K. Rajagopalan, J. Abrokwah, and P. Zurcher

Freescale Semiconductor, Inc., 2100 East Elliot Road, Tempe, AZ 85284 USA
Tel: 480-413-4962, E-mail: m.passlack@freescale.com

R. Hill, D. Moran, X. Li, H. Zhou, D. Macintyre, S. Thoms, and I. Thayne

Nanoelectronics Research Centre, University of Glasgow, Rankine Building, Oakfield Avenue, Glasgow, G12 8LT UK

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Abstract

1 μm GaAs enhancement-mode MOSFETs have been manufactured with a threshold voltage, maximum drain current, maximum transconductance, on-resistance, drain conductance, subthreshold swing, and gate current of 0.28 V, 397 mA/mm, 428 mS/mm, and 2.3 Ω mm, 10 mS/mm, 100 mV/dec, < 60 nA, respectively. An off-state breakdown voltage of 18 V was measured for an oxide thickness of 18 nm. An effective channel mobility of ≅ 5,500 cm^2/Vs was measured on a 20 μm gate length device using the split C-V method. These devices are potentially suitable for RF power amplification, switching, and power control in mobile and wireless applications. The high MOSFET channel mobility is of interest for future CMOS applications.

INTRODUCTION

MOSFETs based on III-V semiconductors promise to combine III-V high frequency performance with scalability and integration known from silicon. GaAs MOSFET technology may find future use where high RF power is required at low voltage and high efficiency, i.e. wireless and mobile products. The technology may also have a unique advantage in regard to integration of RF power, switching, and power control functions. This is of interest where integration lowers cost and enables new functionality. For CMOS applications, novel device architectures, high-κ gate dielectrics, metal gates and high mobility channel materials will be required to continue CMOS device scaling according to Moore's Law and the ITRS.

Modern RF and CMOS applications prefer single supply operation using enhancement-mode (for a definition, see [1]) FETs. The GaAs enhancement-mode MOSFET, however, has remained elusive for decades [2]. Recent developments including the discovery of the low defect Ga_2O/GaAs interface [3], [4], the use of GdGaO/Ga_2O_3 dielectrics [5]-[7] and suitable epitaxial layer structures [8], and the invention of an implant free MOSFET design [9], [10] have finally delivered GaAs enhancement mode devices which realize their performance potential (Fig. 1).

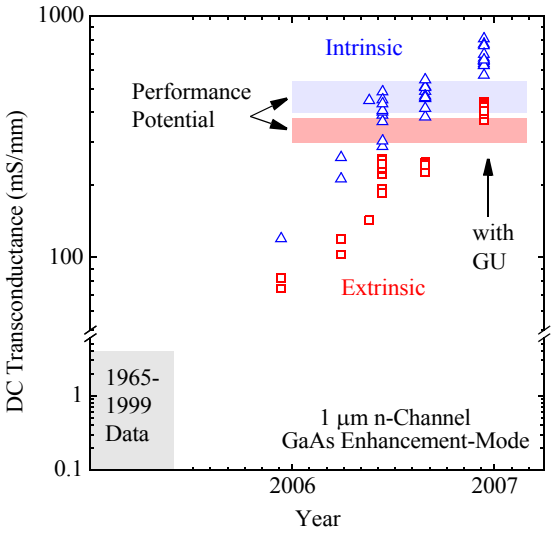

Fig. 1 Evolution of DC transconductance of GaAs based MOSFETs. (GU: Glasgow University)

In this extended abstract, we will illustrate the unique properties of the Ga_2O_3/GaAs interface, elucidate the operation of implant-free enhancement-mode MOSFETs, present recent 1 μm RF power MOSFET DC data, and benchmark these data against conventional 1 μm GaAs Schottky gate enhancement mode devices (HIGFET) designed for single supply operation.

WAFER GROWTH

MOSFET wafers have been fabricated by molecular beam epitaxy (MBE) using an ultra-high vacuum (UHV) dual chamber configuration manufactured by DCA Instruments. The MOSFET structure is grown on 3 in. semi-insulating GaAs substrate and consists of undoped GaAs and AlGaAs buffer layers, a bottom Si δ-doping with nominal concentration of $3x10^{12}$ cm^{-2}, an undoped bottom spacer layer including 3 nm of $Al_{0.2}Ga_{0.8}As$ and 2 nm of GaAs, a 10 nm undoped $In_{0.3}Ga_{0.7}As$ channel layer, a 2 nm undoped GaAs top spacer layer, a top Si δ-doping ($1x10^{12}$ cm^{-2}), a 2 nm undoped

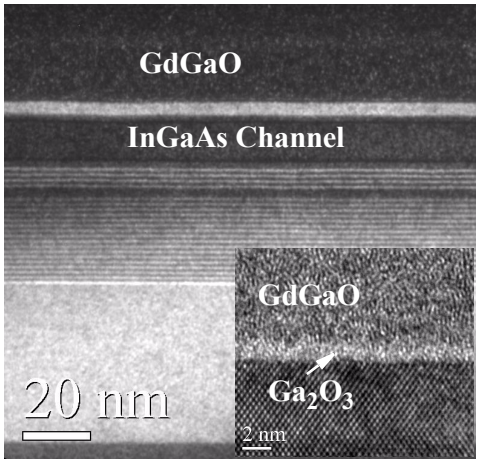

Fig. 2 Dark field TEM micrograph of a typical MOSFET structure with an InGaAs channel. The inset shows a high resolution TEM micrograph of the oxide/semiconductor interface.

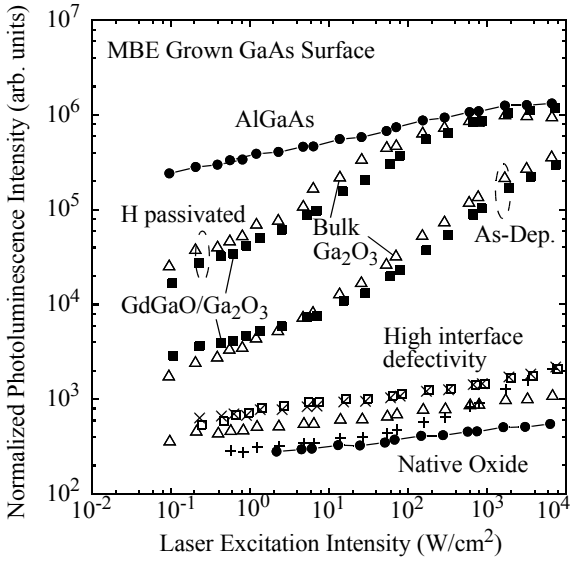

Fig. 3 Normalized GaAs photoluminescence intensity as a function of excitation intensity for AlGaAs (solid circles), Ga_2O_3 (open triangles), GdGaO/Ga_2O_3 (solid squares), high interface defectivity films, and native oxide (solid circles) on GaAs. All materials are deposited on MBE grown surfaces under UHV conditions (except for native oxide).

$Al_{0.45}Ga_{0.55}As$ barrier layer, and an amorphous GdGaO/Ga_2O_3 dielectric stack with a nominal thickness between 10 and 18 nm. The dielectric stack has a relative dielectric constant κ of 20 and a Ga_2O_3 template layer thickness of ≅ 1 nm [6]. Further growth details can be found in [11]. Fig. 2 shows a dark field TEM micrograph of a typical complete MOSFET layer structure. The inset shows a high resolution micrograph of the interface between the oxide and the semiconductor surface. The Ga_2O_3 template layer is clearly visible.

INTERFACE QUALITY

The electrical interface properties of the GdGaO/Ga_2O_3 dielectric stack on GaAs have been determined by a photoluminescence-intensity (PL-I) technique and by capacitance-voltage measurements [12]. The PL-I technique is uniquely suited to screen oxide/semiconductor interface quality. In this technique, the PL intensity is acquired by integrating over GaAs PL spectra as a function of laser intensity as shown in Fig. 3. The analysis domain (lines with solid circles) is defined by a known best interface with very low defectivity (AlGaAs on GaAs) and the lower boundary by a known worst interface (native oxide on GaAs). The four data curves close to the native oxide represent a large group of materials forming a high defectivity interface on GaAs. This group comprises more than 10 materials investigated over the years including oxides (e.g. Al_2O_3, Gd_2O_3, SiO_2), SiN, and Si. The only material departing from "native oxide" behavior is Ga_2O_3 (bulk Ga_2O_3, open triangles) which shows an interface defectivity adequate for MOSFET operation. The high quality Ga_2O_3/GaAs interface is preserved if the top oxide does not disrupt the template layer, as observed for the case of optimized deposition of GdGaO (solid squares). If appropriate hydrogen passivation techniques are applied, the interface quality of both bulk Ga_2O_3 and the dielectric stack further improve to the same extent confirming that a Ga_2O_3/GaAs interface is formed in both cases. The interface state density as a function of GaAs bandgap energy has been determined by quasi-static and high-frequency capacitance-voltage measurements and the midgap interface state density is typically 2-3x10^{11} cm^{-2} eV^{-1}.

IMPLANT FREE MOSFET

Cross sectional schematics of an n-channel III-V enhancement-mode MOSFET are shown in Fig. 4. As any MOSFET, the device features a gate oxide which separates the gate metal electrode from the conducting channel, two metallic contacts (Ohmic contacts source and drain) for current flow and a gate electrode to control the channel electron density under the gate contact and thus the current flow from drain to source. In case of a GaAs substrate, a typical epitaxial layer structure is described above.

In Fig. 4 (a), the n-channel MOSFET is depicted in off-state at a gate voltage V_G of 0 V with essentially no electrons under the gate and no current flow. When a positive voltage is

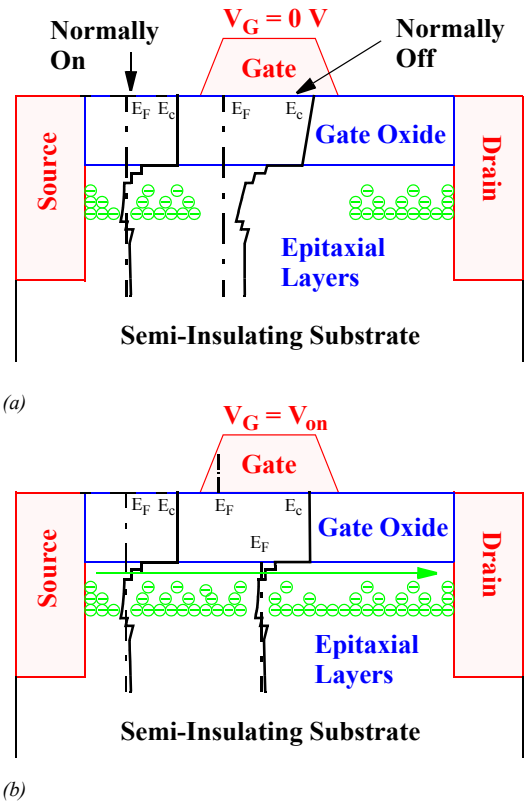

Fig. 4 Implant free (flatband) MOSFET in off-state (a) and on-state (b).

applied to the gate (Fig. 4 (b)), electrons start to appear under the gate, the device turns on and current starts to flow. Consequently the threshold voltage is larger than zero which is the criterion for enhancement mode operation of an n-channel device. The remarkable feature of the device is the absence of ion-implanted regions, yet the MOSFET works in enhancement-mode. This is possible because the surface potential in the regions between the Ohmic contacts and the gate differs from the surface potential under the gate, something which is impossible in conventional III-V technology where the high defectivity at the oxide-semiconductor interface pins the surface potential at the same energy along the entire semiconductor surface. Electrons are always present in between the Ohmic contacts and the gate, these regions are always on and in "flatband" condition (normally-on), but the region under the gate is depleted of electrons at zero gate voltage (normally-off) by virtue of a sufficiently high effective workfunction of the gate metal. Maximum current flow is obtained when the region under the gate is in "flatband" condition as well. Consequently, we termed this device "flatband" MOSFET in analogy to the Si inversion-type MOSFET where the conducting channel forms due to inversion.

High channel mobility is a prerequisite for "flatband-mode" operation. The resistance of the regions between the Ohmic contacts and the gate is inversely proportional to the channel mobility; low mobility as present in Si and Ge would lead to excessive and unacceptable parasitic resistance. Scaled performance of implant free, InGaAs channel MOSFETs with high In content for future CMOS applications is predicted in [13] using Monte-Carlo simulation.

MOSFET MANUFACTURING AND DC DATA

MOSFETs with 1 µm gate length have been manufactured using a two-level wrap-around gate design (where the gate encircles the drain) to simplify the device process flow, removing the need for isolation. The source-drain separation and the device width are 2.7 and 100 µm, respectively. Both the gate (Pt/Au) and ohmic contacts (Ni/Ge/Au) were defined by direct write e-beam lithography and patterned by the lift-off method. The GdGaO dielectric was removed by wet chemical etching prior to deposition of the ohmic contacts, which underwent rapid thermal annealing at 430 C for 60 s. Transmission line measurement (TLM) data obtained from process control structures alongside the devices gave a contact resistance of 0.41 Ω mm and a sheet resistance of 449 Ω/sq.

Fig. 5 gives typical output characteristics of a 1 µm gate length device with an oxide thickness of 10 nm. The device parameters threshold voltage, maximum drain current, maximum transconductance, on-resistance, drain conductance, subthreshold swing, and gate current are 0.28 V, 397 mA/mm, 428 mS/mm, and 2.3 Ω mm, 10 mS/mm, 100 mV/dec, < 60 nA, respectively. An off-state breakdown voltage of 18 V was measured for an oxide thickness of 18 nm. An effective channel mobility of ≅ 5,500 cm^2/Vs was measured on a 20 µm gate length device using the split C-V method. This mobility is comparable to the Hall-effect mobility reported earlier for a similar structure [14]. Hall-effect mobilities exceeding 12,000 cm^2/Vs were reported earlier for high-κ InP based NMOSFET structures designed for enhancement-mode operation [15].

In Table I, 1 µm GaAs power MOSFET performance is benchmarked against conventional enhancement mode power FET technology (HIGFET) for single supply operation (no negative voltage generator and drain–supply switch for power amplifier required). Beyond performance advantages in the power amplifier socket, different functions such as power amplification, RF switching, and power control can be potentially integrated on a GaAs MOSFET platform. Note that an increase of MOSFET threshold voltage of about 0.2-0.3 V over the data presented in this abstract (mainly to be obtained by increasing the effective gate metal workfunction) is required for single supply operation.

TABLE I

BENCHMARKING OF ENHANCEMENT MODE POWER MOSFET AGAINST HIGFET FOR SINGLE SUPPLY

	I_{max} (mA/mm)	R_{on} (Ω mm)	g_m (mS/mm)	I_G	Off-state Breakdown voltage (V)	Reference
GaAs MOSFET	398	2.3	426	< 60 pA [a]	18 [c]	this work, [16]
HIGFET	225-230	2.5	270-295	1 mA/mm [b]	18	[17], [18]

[a] all voltages measured [b] V_G=1.8V [c] 18 nm oxide thickness

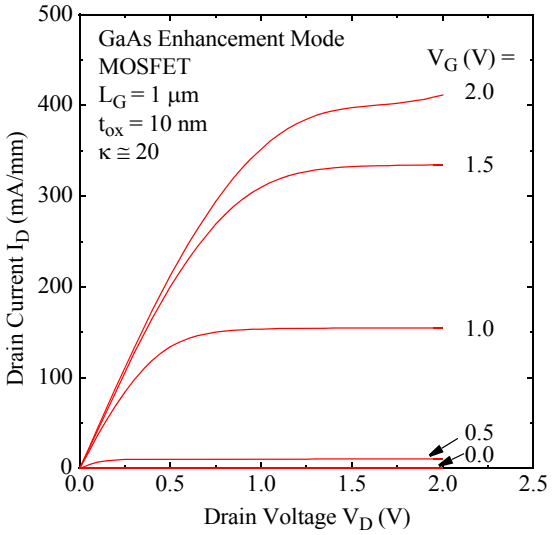

Fig. 5 Output characteristics of a 1 µm GaAs MOSFET.

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ACRONYMS

MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor
RF: Radio Frequency
CMOS: Complementary Metal-Oxide-Semiconductor
ITRS: International Technology Roadmap for Semiconductors
HIGFET: Heterostructure Insulated Gate Field Effect Transistor
MBE: Molecular Beam Epitaxy
UHV: Ultra High Vacuum
TEM: Transmission Electron Microscopy
PL: Photoluminescence
TLM: Transmission Line Method