New Single-Stage PFC Regulator Using the Sheppard–Taylor Topology

C. K. Tse, *Senior Member, IEEE,* and M. H. L. Chow, *Member, IEEE*

***Abstract*— This paper describes a new usage of the dc/dc converter developed by D. I. Sheppard and B. E. Taylor in 1983 for achieving high power factor and output regulation. This converter may be viewed as a cascade of a modified boost stage and a buck stage, with the two stages sharing the same active switch. Two possible operation regimes are described. In the first regime, the converter's input part, which is a modified boost converter, operates in discontinuous mode, and the output part, which is a buck converter, operates in continuous mode. In this regime, high power factor is naturally achieved, and the output voltage is regulated by duty-cycle modulation via a simple output feedback. In the second regime, the input part operates in continuous mode, and the output part operates in discontinuous mode, with duty-cycle modulation maintaining a high power factor and frequency modulation regulating the output. Some comparisons between the Sheppard–Taylor converter and conventional boost and buck cascade are given in the paper.**

***Index Terms*— Circuit topologies, power factor correction, switching regulators.**

I. Introduction

DEVELOPED in 1983, the Sheppard–Taylor converter [1] was primarily designed to provide nonpulsating input and output currents similar to the Ćuk converter. As shown in Fig. 1, the converter has two inductors that can shape the input current and feed the output load. In its original version, the converter was designed to operate with both inductance currents continuous, and only dc/dc voltage conversion was considered.

At first glance, this converter possesses a similar property to the normal boost–buck-cascade single-stage power-factor-correction (PFC) converter shown in Fig. 2. Essentially, the presence of a storage capacitor provides instantaneous power buffering which in turn allows output regulation to be achieved simultaneously with high power factor using only one switch control. Moreover, a closer inspection reveals that an extra useful feature is provided by the storage capacitor which, with a special switching arrangement, pushes up the input current during on time and pulls it down during off time. The on-time boosting of input current by an additional dc voltage is not provided by the normal boost converter. Not recognized in the past, this feature can be exploited for PFC

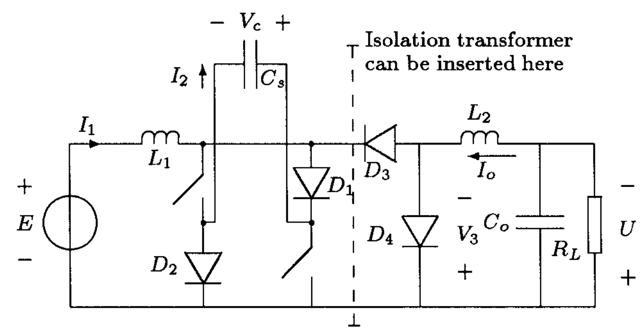


Fig. 1. The Sheppard–Taylor converter.

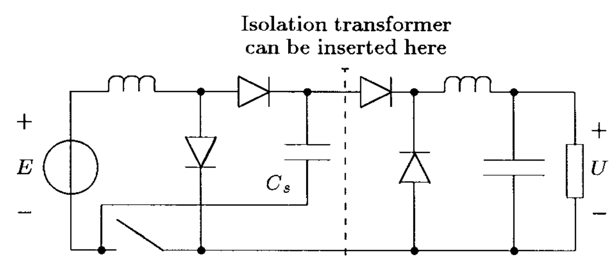


Fig. 2. The cascaded boost–buck single-stage PFC converter (Redl *et al.* [2]).

applications. In particular, two operating modes are possible for PFC applications.

1) With its input current in discontinuous mode, the converter naturally achieves high power factor, even without feedforward compensation. Compared to the discontinuous-mode boost converter, the Sheppard–Taylor achieves higher power factor and less harmonics for low-voltage stress ranges, and has extremely low third harmonics in a certain voltage stress range. (An objective comparison is given in Section II-D.)
2) Perfect input current shaping (sine current) can be achieved when the converter operates with its input current in continuous mode. Such is theoretically impossible with the boost PFC stage since the rate of change of the input current is always zero at the instant immediately after the zero crossing of the input sine voltage, as illustrated in Fig. 3.

Our objective in this paper is to study the use of the Sheppard–Taylor converter as a single-stage PFC regulator. By definition, a single-stage PFC regulator provides output voltage regulation and input power factor correction using one (or one set of synchronized) active switch(es) under the control

Manuscript received June 12, 1997; revised February 24, 1998. Recommended by Associate Editor, R. Steigerwald.

The authors are with the Department of Electronic Engineering, Hong Kong Polytechnic University, Hong Kong.

Publisher Item Identifier S 0885-8993(98)06474-6.

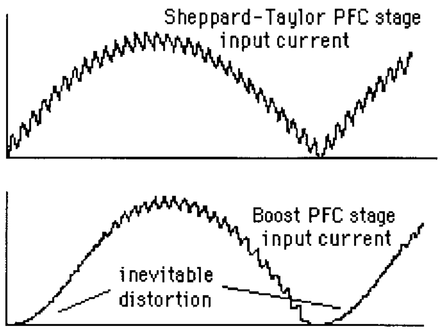


Fig. 3. The Sheppard–Taylor converter achieves “perfect” current shaping.

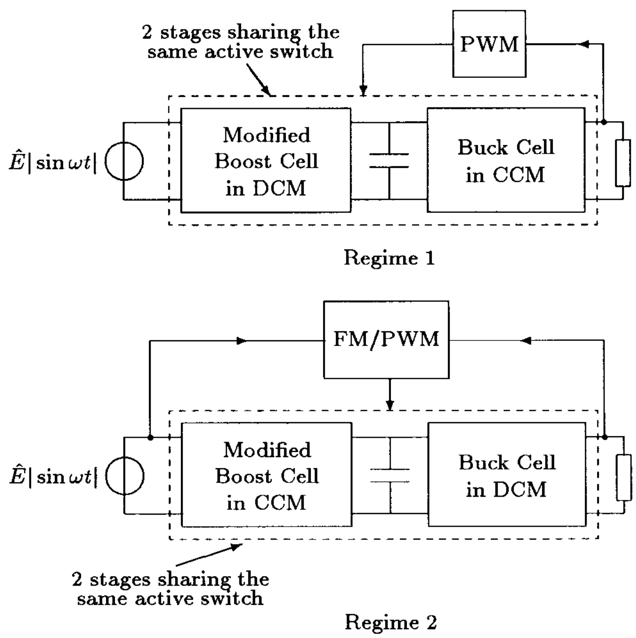


Fig. 4. Schematics of operating regimes.

of one driving signal. Such a circuit mandates the presence of an energy storage element which buffers the instantaneous difference between the constant output power and the input power which changes as the product of two sinusoids. Typical topologies consist of a cascade of a boost PFC stage and a dc/dc converter stage, with the two stages sharing the same active switch, e.g., SSIPP [2], BIFRED, and BIBRED [3], [4]. The Sheppard–Taylor converter represents yet another alternative with pros and cons. We will present two operating regimes of this converter that can result in a very high-input power factor and simultaneous output regulation. Referring to Fig. 1, the converter may be viewed as a cascade of a *modified boost converter* and *buck converter*. The switches are turned on and off synchronously. In the first regime, the modified boost converter operates in discontinuous mode while the buck converter in continuous mode. In the second regime, the reverse is arranged. Since high power factor is naturally achieved in the first regime, a simple feedback scheme suffices to regulate the output. In contrast, a feedforward-feedback scheme is necessary for the second regime to maintain both unity power factor and output regulation. Fig. 4 shows these arrangements.

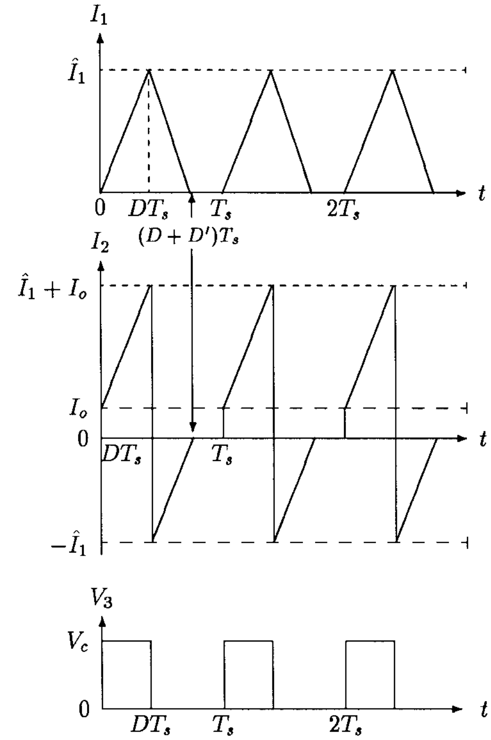


Fig. 5. Waveforms of I_1, I_2, and V_3 (Regime 1).

II. Regime 1—Operation with Discontinuous Input Current

The first operating regime takes advantage of the naturally high power factor of the discontinuous-mode converter [2], [5]. Referring to Fig. 1, the value of L_1 is relatively small so that the current through L_1 is maintained in discontinuous mode. The value of L_2, on the other hand, is large enough to keep the output current in continuous conduction. In the steady state, during the interval when the switches are on, both inductance currents flow through the switches and discharges C_s. When the switches are off, the current of L_1 flows through diodes D_1 and D_2 and charges up C_s, while the current of L_2 is forced into the freewheeling diode D_4. As soon as the current of L_1 vanishes, capacitor C_s is idle while the current of L_2 keeps freewheeling through D_4. The cycle ends at the instant the switches are turned on again. The aforementioned sequence of operations repeats itself every period T_s. Waveforms of I_1, I_2, and V_3 are shown in Fig. 5.

A. Derivation of Averaged Model for Regime 1

We now attempt to find an averaged model for the converter operating in the above-described regime, which will be viewed as a three-port circuit terminated by E, V_c, and I_o [6]. Our purpose is to find the averaged values of the port variables I_1, I_2, and V_3 as marked in Fig. 1. Referring to the waveforms of I_1, I_2, and V_3 shown in Fig. 5, we can write down the averaged values *over one switching cycle* as follows:

$$I_{1_{\rm av}} = \frac{1}{2}(D + D')\hat{I}_1 \tag{1}$$

$$I_{2_{\rm av}} = DI_o + \frac{1}{2}D\hat{I}_1 - \frac{1}{2}D'\hat{I}_1 \tag{2}$$

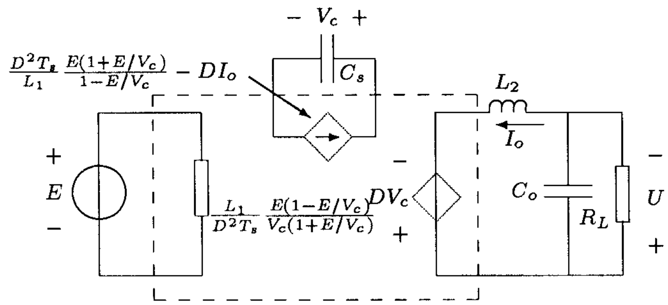


Fig. 6. Averaged model for the first operating regime—input part in discontinuous mode and output part in continuous mode.

$$V_{3_{\rm av}} = DV_C \tag{3}$$

where $\hat{I}_1$ is the peak current given by

$$\hat{I}_1 = \frac{DT_s(V_C + E)}{L_1}. \tag{4}$$

Also, since $\hat{I}_1$ is also equal to $D'T_s(V_C - E)/L_1$, we have

$$D' = \frac{V_C + E}{V_C - E} D. \tag{5}$$

Thus, (1)–(3) become

$$I_{1_{\rm av}} = \frac{E}{\left\{\frac{L_1(E/V_C)(1-E/V_C)}{D^2T_s(1+E/V_C)}\right\}} \tag{6}$$

$$I_{2_{\rm av}} = DI_o - \frac{D^2T_sE(1+E/V_C)}{L_1(1-E/V_C)} \tag{7}$$

$$V_{3_{\rm av}} = DV_C. \tag{8}$$

From the above expressions, we have an averaged circuit model for the Sheppard–Taylor circuit, as shown in Fig. 6.

B. Calculation of Input Power Factor and Harmonic Distortions for Constant-Frequency Operation

The input power factor of the proposed converter under no specific control action can be calculated as follows. Suppose the input voltage is a rectified sine wave, i.e., $E(t) = |\hat{E}\sin\omega t|$, where ω is normally $2\pi \times 50$ rad/s (or $2\pi \times 60$ rad/s in the United States and Japan). The input current waveform (in the averaged sense) is periodic with angular frequency 2ω

$$I_1(t) = \frac{D^2T_sV_CF(\omega t)}{L_1} \tag{9}$$

where

$$F(\omega t) = \frac{1 + \frac{\hat{E}|\sin\omega t|}{V_C}}{1 - \frac{\hat{E}|\sin\omega t|}{V_C}}. \tag{10}$$

Note that $2\pi/\omega$ is much greater than T_s. The value of V_C can be assumed constant. For the purpose of maintaining a constant output voltage, the duty cycle D will also be constant. Hence, the rms value of the input current is

$$\begin{aligned} I_{1,\rm rms} &= \sqrt{\frac{1}{\pi}\int_0^{\pi} \frac{D^4T_s^2V_C^2}{L_1^2}F(\theta)^2\,d\theta} \\ &= \frac{D^2T_sV_C}{L_1\sqrt{\pi}}\sqrt{\int_0^{\pi} F(\theta)^2\,d\theta} \end{aligned} \tag{11}$$

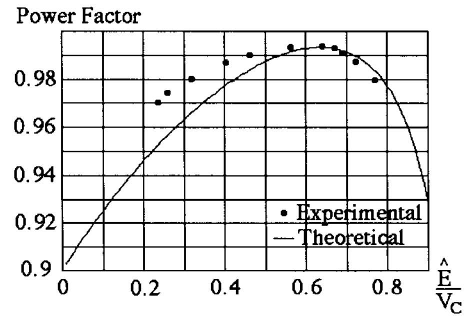


Fig. 7. Power factor versus $\hat{E}/V_C$ (Regime 1).

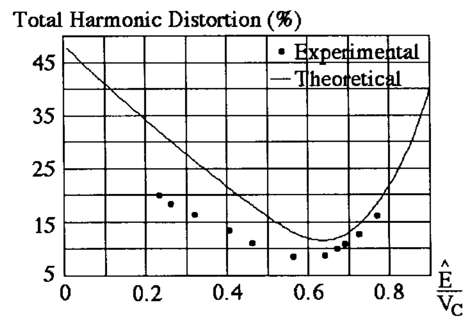


Fig. 8. THD versus $\hat{E}/V_C$ (Regime 1).

with θ being substituted for ωt. The power input is

$$\begin{aligned} P_{\rm in} &= \frac{\omega}{\pi}\int_0^{\frac{\pi}{\omega}} E(t)I_1(t)\,dt \\ &= \frac{1}{\pi}\int_0^{\pi} \hat{E}\sin\theta\frac{D^2T_sF(\theta)}{L_1}\,d\theta \\ &= \frac{D^2T_sV_C\hat{E}}{\pi L_1}\int_0^{\pi} F(\theta)\sin\theta\,d\theta. \end{aligned} \tag{12}$$

Hence, the input power factor of the system, with no feedforward control of power factor, is

$$\begin{aligned} \text{pf} &= \frac{P_{\rm in}}{E_{\rm rms}I_{1,\rm rms}} \\ &= \sqrt{\frac{2}{\pi}}\left(\frac{\int_0^{\pi} F(\theta)\sin\theta\,d\theta}{\sqrt{\int_0^{\pi} F(\theta)^2\,d\theta}}\right) \end{aligned} \tag{13}$$

where the involving definite integrals are functions of $\hat{E}/V_C$, the closed-form expressions of which are found in the Appendix. Fig. 7 shows a plot of the power factor versus the ratio $\hat{E}/V_C$ from which we can see clearly that the converter itself provides inherently high power factor. Also, the total harmonic distortion (THD) can be found as

$$\text{THD} = \sqrt{\frac{1}{(\text{pf})^2} - 1}. \tag{14}$$

Fig. 8 shows a plot of THD versus $\hat{E}/V_C$. We have also performed a Fourier analysis on the averaged input current. Fig. 10 shows the harmonic distortions up to the ninth harmonics.

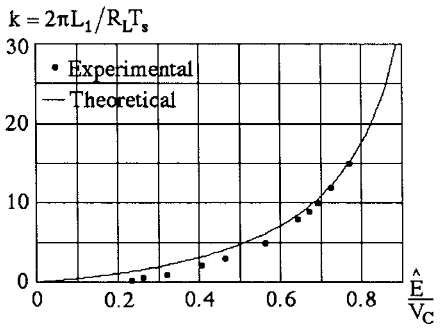


Fig. 9. Steady-state operating point (Regime 1).

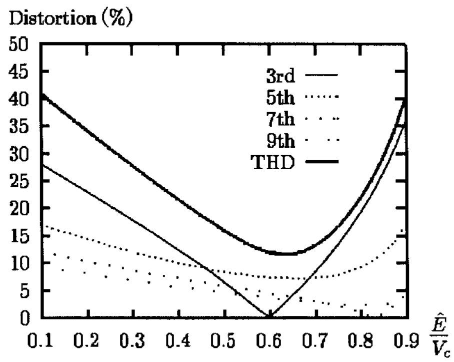


Fig. 10. Harmonic distortions versus $\hat{E}/V_C$ (Regime 1).

C. Steady-State Design for Regime 1

In order to choose a suitable set of component values for a specified operating point, we need to consider the steady-state operating condition. When the input is a rectified sinusoidal voltage of amplitude $\hat{E}$ and angular frequency ω, the current flowing into the storage capacitor C_s is given by (7). The average value of this current over a complete 50-Hz cycle is given by

$$I_2 = DI_o - \frac{D^2 T_s}{L_1 \pi} \int_0^{\pi} \frac{\hat{E}\sin\theta\left(1+\frac{\hat{E}}{V_c}\sin\theta\right)}{1-\frac{\hat{E}}{V_c}\sin\theta}\, d\theta. \tag{15}$$

This current must be equal to zero in the steady state. Hence, we have

$$\int_0^{\pi} F(\theta)\sin\theta\, d\theta = \frac{\pi L_1 I_o}{\hat{E} D T_s}. \tag{16}$$

Since V_c, U, I_o, and D are constant in the steady state, we can write $D = U/V_c$ and $I_o = U/R_L$. Thus, the steady-state equation is

$$\int_0^{\pi} F(\theta)\sin\theta\, d\theta = \frac{\pi L_1}{R_L T_s}\frac{1}{\hat{E}/V_c} = \frac{k}{2(\hat{E}/V_C)} \tag{17}$$

where k is defined by

$$k \stackrel{\text{def}}{=} \frac{2\pi L_1}{R_L T_s} \tag{18}$$

and the definite integral is a function of $\hat{E}/V_C$ (see Appendix). A graphical representation of (17) is shown in Fig. 9.

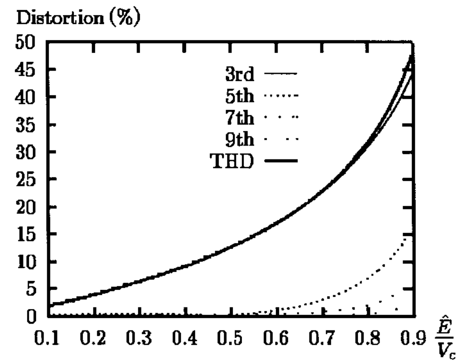


Fig. 11. Harmonic distortions versus $\hat{E}/V_C$ in boost–buck cascade with discontinuous input current.

TABLE I
COMPARISON OF THD OF SHEPPARD–TAYLOR CONVERTER (REGIME 1) AND CASCADED BOOST–BUCK CONVERTER

$\hat{E}/V_C$	Sheppard-Taylor	Cascaded-boost-buck
0.9	40%	48%
0.6	12%	17%
0.3	28%	7%

D. Comparison with Cascaded Boost and Buck Converter

In this section, we attempt to make an objective comparison of the Sheppard–Taylor converter and the standard cascaded boost–buck converter. We will focus on two main performance aspects, namely, harmonic distortions and device stresses.

1) Comparison of Harmonic Distortions: The harmonic distortions (up to the ninth harmonics) in the Sheppard–Taylor converter are shown in Fig. 10. For ease of comparison, we also plot the corresponding harmonic distortions in the cascaded boost–buck converter in Fig. 11. From the distortion curves, we make the following observations.

1) The Sheppard–Taylor converter achieves a minimum THD of 7% when $\hat{E}/V_C$ is about 0.64, whereas the cascaded boost–buck converter achieves arbitrarily low THD at the expense of small $\hat{E}/V_C$, i.e., high-voltage stress.
2) Some figures of THD for comparison are shown in Table I from which we clearly see that at low-input line, the Sheppard–Taylor converter is marginally better, whereas at high-input line, it is significantly worse.
3) The third-harmonic distortion is generally much less in the Sheppard–Taylor converter as can be seen from Fig. 10. However, the Sheppard–Taylor converter has comparatively richer higher harmonics.

2) Comparison of Device Stresses: The other aspect of comparison is the specific stresses (stresses per unit power) which measure how effectively the devices are exploited in the converter. For the Sheppard–Taylor converter, the rms current in the switch is given by

$$I_{\text{sw,rms}}\big|_{\text{Shep-Tay}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} [i_{\text{sw,rms}}(t)]^2\, dt} \tag{19}$$

TABLE II
COMPARISON OF STRESSES

Converter	Specific switch current stress	Maximum voltage stress
Sheppard-Taylor	$\sqrt{\frac{1}{3DE^2}\left[1+\frac{E}{V_C}+\left(\frac{E}{V_C}\right)^2\right]}$ A/W	V_C
Cascaded-boost-buck	$\sqrt{\frac{1}{3DE^2}\left[4-\frac{2E}{V_C}+\left(\frac{E}{V_C}\right)^2\right]}$ A/W	V_C+V_p where V_p is voltage reflected in the primary during core reset ($V_p = 0$ for non-isolated version)
DCM boost	$\sqrt{\frac{4}{3DE^2}\left[1-\frac{E}{V_C}\right]^2}$ A/W	V_C

$$= \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left[\frac{P}{DV_c}+\frac{(E+V_C)t}{L_1}\right]^2 dt} \tag{20}$$

$$= \sqrt{\frac{P^2}{V_C^2 D}+\frac{P(1+E/V_C)DT_s}{L_1}+\frac{(E+V_C)^2D^3T_s^2}{3L_1^2}} \tag{21}$$

where P is the power which is given by

$$P = EI_{1_{\rm av}} = \frac{E^2D^2T_s(1+E/V_C)}{L_1(E/V_C)(1-E/V_C)} \tag{22}$$

assuming constant E for simplicity. Thus, the switch current stress per unit power is

$$\left.\frac{I_{\rm sw,rms}}{P}\right|_{\rm Shep\text{-}Tay} = \sqrt{\frac{1}{3DE^2}\left[1+\frac{E}{V_C}+\left(\frac{E}{V_C}\right)^2\right]}. \tag{23}$$

Performing similar calculation for the cascaded boost–buck converter, we get

$$\left.\frac{I_{\rm sw,rms}}{P}\right|_{\rm boost-buck} = \sqrt{\frac{1}{3DE^2}\left[4-\frac{2E}{V_C}+\left(\frac{E}{V_C}\right)^2\right]}. \tag{24}$$

Thus, we see that the specific current stress in the Sheppard–Taylor converter is less than that in the cascaded boost–buck converter.

As regards maximum voltage stress, the two-switch Sheppard–Taylor converter has a voltage of V_C across the switch during off time, regardless of the presence of isolation transformer, i.e., for both Figs. 1 and 12. For the cascaded boost–buck converter, however, the maximum voltage stress depends on the exact configuration. For instance, in the single-switch nonisolated version, the maximum voltage stress is V_C, whereas in the single-switch isolated version, it is $V_C + V_p$, where V_p is the voltage reflected in the primary during core reset. In Table II, we tabulate the current and voltage stresses in the Sheppard–Taylor converter and the cascaded boost–buck converter. We also include in the table, for comparison, the stresses in a discontinuous-mode boost converter which appears in a two-stage configuration.

TABLE III
PARAMETER VALUES AND COMPONENTS FOR EXPERIMENTAL MEASUREMENT IN REGIME 1

Parameters	Components/Values
L_1	210 μH
L_2	735 μH
C_s	270 μF
C_o	1000 μF
T_s	1/100000 s
$\hat{E}/V_c$	0.234 – 0.768
U	50 V
Diodes	U1560
MOSFETs	IRFP450
L_1 Core	77206-A7
L_2 Core	77930-A7
Transformer	1:1

E. Experimental Demonstration

A simple prototypic demonstration is presented in this section. The circuit is constructed almost exactly as in Fig. 1, except that an isolation transformer has been included. The input to the circuit is a bridge rectifier and the circuit parameters are as shown in Table III. This set of values would ensure that the circuit operates in the expected regime, i.e., L_1 in discontinuous conduction mode (DCM) and L_2 in continuous conduction mode (CCM). The circuit has a TL494 voltage-mode control integrated circuit (IC) to maintain a fixed output voltage. The schematic experimental circuit is shown in Fig. 12. A series of data corresponding to different steady-state operating points are taken, which have been plotted in Figs. 7–9, alongside the theoretical curves.

To verify the operation of the converter, we show here some typical waveforms for a particular set of parameter values at $\hat{E} = 110\times\sqrt{2}$ V and $R_L = 50\ \Omega$. The measured V_C is 300 V, i.e., $\hat{E}/V_C = 0.52$. Figs. 13 and 14 show the inductor current waveforms, confirming operation in the expected regime. The input voltage and current waveforms are shown in Fig. 15. Note that the current waveform is actually a filtered version which has effectively removed the 100-kHz switching ripples. Finally, Fig. 16 shows the output voltage which is regulated at 50 V. The measured power factor for this particular case is 0.997.

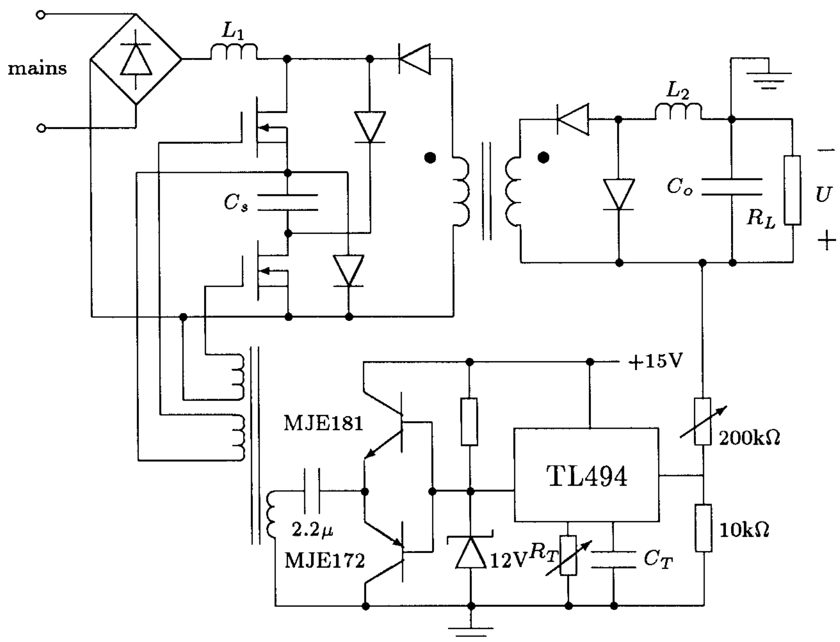


Fig. 12. Simplified schematic of experimental circuit for Regime 1. Details of compensation circuits in TL494 omitted for brevity.

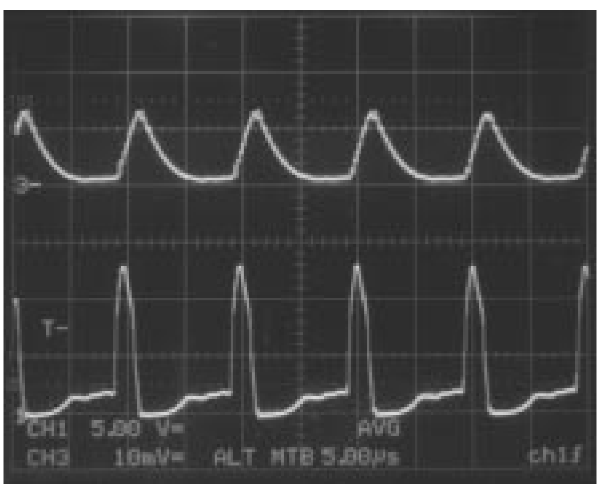


Fig. 13. Upper trace: current in L_1 (2 A/div; 5 μs/div). Lower trace: switch drive signal.

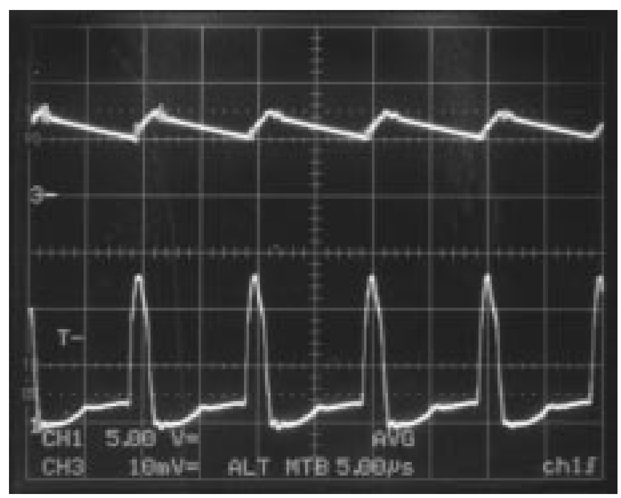


Fig. 14. Upper trace: current in L_2 (1 A/div; 5 μs/div). Lower trace: switch drive signal.

III. Regime 2—Operation with Continuous Input Current

With the input part (modified boost converter) operating in continuous mode, the Sheppard–Taylor converter can achieve unity power factor, provided that a suitable feedforward control is applied. Such is impossible with the standard boost topology, regardless of the control strategy. As we have mentioned in the Introduction, the boost converter always suffers a cusp distortion because for $E = \hat{E}|\sin \omega t|$, the input current satisfies $di_{\rm in}/dt = 0$ at $t = n\pi/\omega$ for all integers n. This situation is reflected in Fig. 3. (See Todd [7] and Chow and Tse [8] for a detailed analysis of the cusp distortion in the boost converter.)

Apart from achieving theoretical harmonic-free line current, the Sheppard–Taylor converter can simultaneously regulate the output voltage if the output part is made frequency dependent, for instance, under a discontinuous-mode operation. Again, such is impossible with the usual boost–buck cascade [2] (Fig. 2) because the normal boost PFC stage requires duty cycle of values approaching one during a considerable portion of the mains cycle, disallowing discontinuous mode of the output buck converter. Using the modified boost converter, unity power factor is achieved with duty cycles less than 0.5, thus making it possible for a discontinuous-mode operation of the output buck converter.

A simple and low-cost method to achieve unity power factor is to apply current-mode control which essentially forces the input current to follow the input voltage waveform. Such a control can be viewed as a special duty-cycle modulation scheme, as can be explained in terms of an averaged model described in the next section.

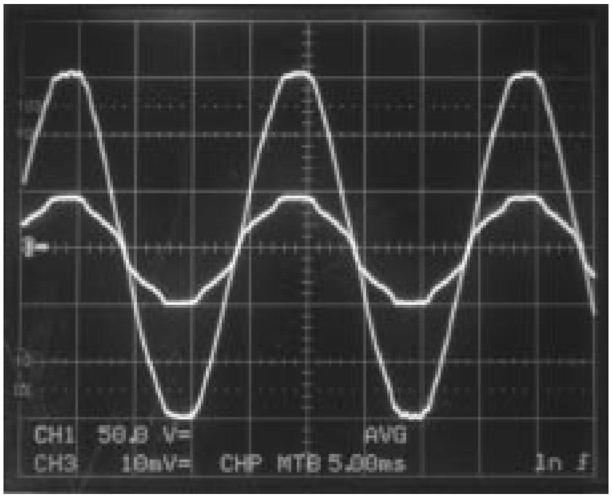


Fig. 15. Taller trace: input voltage (50 V/div; 5 ms/div). Shorter trace: averaged input current (1 A/div; 5 ms/div).

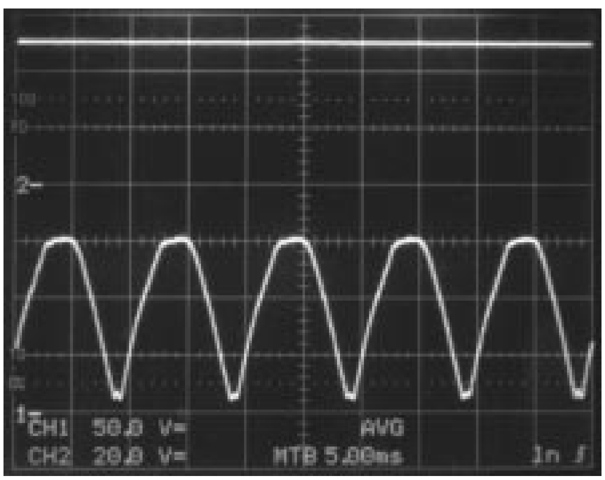


Fig. 16. Upper trace: output voltage (20 V/div; 2 ms/div). Lower trace: input voltage (50 V/div; 2 ms/div).

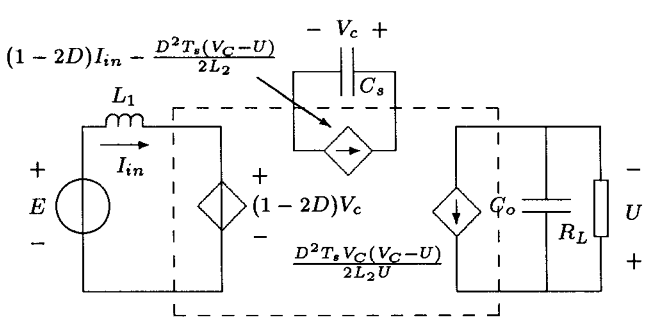


Fig. 17. Averaged model for the second operating regime—input part in continuous mode and output part in discontinuous mode.

A. Averaged Model for Regime 2

The procedure for deriving the averaged model for this operating regime follows closely the one outlined in the previous section. However, the model in this case will have a frequency-dependent current source driving the output load, as shown in Fig. 17. Note that in deriving this model, averaging is applied over the switching cycle.

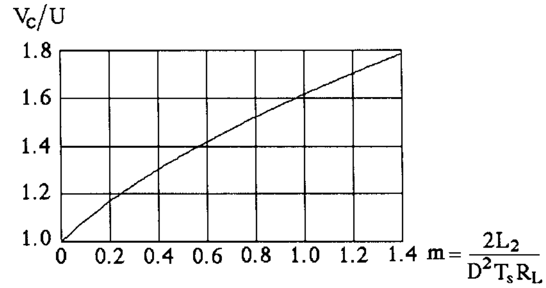


Fig. 18. V_C/U versus m from (31) (Regime 2).

B. Perfect Input Current Shaping Provided by the Modified Boost Converter

Our analysis starts with the same assumptions as made in the previous section. First, the input voltage is a rectified 50-Hz sine wave, i.e., $E = \hat{E}|\sin\omega t|$. Second, the voltage across C_s is nearly constant. As can be seen from the averaged model, in order for the input current to be proportional to the input voltage, i.e., $I_{\text{in}} = gE$, where g is a constant, the duty cycle has to be varied theoretically according to

$$\begin{aligned} D &= \frac{1}{2} - \frac{E - gL_1\frac{dE}{dt}}{2V_C} \\ &= \frac{1}{2} - \frac{(-1)^n(\hat{E}\sin\omega t - gL_1\omega\hat{E}\cos\omega t)}{2V_C} \end{aligned} \tag{25}$$

for $n\pi < \omega t \leq (n+1)\pi$, where $n = 0, 1, 2, \ldots$. Note that g controls the current amplitude and is usually adjusted via a feedback scheme.

An important observation is made here. The above equation shows that current shaping can be theoretically achieved for all t, provided D falls in the range zero–one. This requires that

$$\frac{\hat{E}}{V_C}\sqrt{1 + g^2L_1^2\omega^2} < 1 \tag{26}$$

which is a very weak condition and can be satisfied in most cases.

Remarks: Intuitively speaking, the input current in the boost converter fails to follow the sine wave because it cannot rise at $\omega t = n\pi$ in the absence of any dc voltage. This problem is resolved by the Sheppard–Taylor converter, where a dc voltage is always available from the storage capacitor C_s even at $\omega t = n\pi$.

C. Steady-State Design for Regime 2

Assuming that the input current is now under an appropriate control such that a sinusoidal waveform is maintained, the power input is given by

$$P_{\text{in}} = \frac{1}{2}g\hat{E}^2. \tag{27}$$

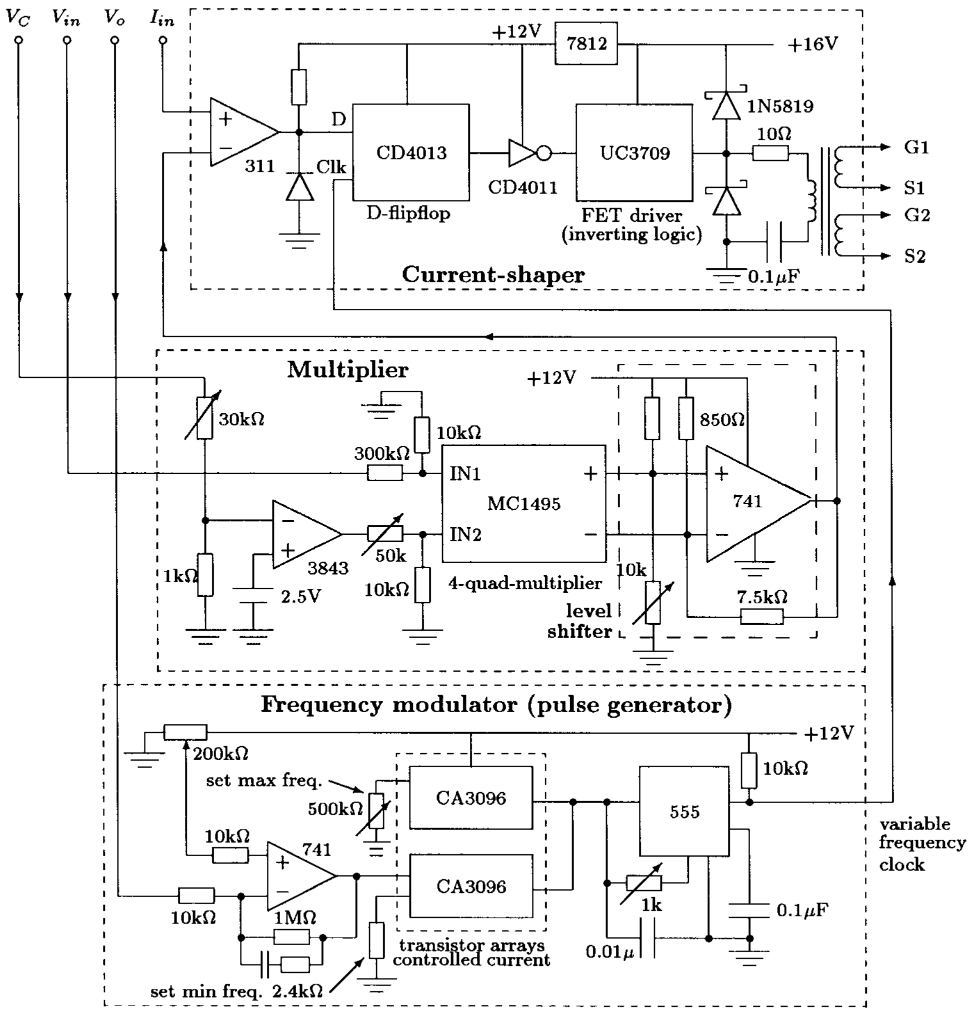


Fig. 19. Simplified schematic of the control circuit for Regime 2.

Suppose the output voltage is regulated at U. Then, g is set according to

$$g = \frac{2U^2}{R_L \hat{E}^2}. \tag{28}$$

Regulation of output voltage requires that $D^2 T_s$ be *nearly constant*, i.e., the frequency is adjusted in proportion to the square of the duty cycle. This implicit condition leads to

$$\frac{U}{R_L} = \frac{D^2 T_s V_C}{2L_2}\left(\frac{V_C}{U} - 1\right). \tag{29}$$

Hence, we obtain a steady-state equation as follows:

$$\frac{V_C}{U}\left(\frac{V_C}{U} - 1\right) = \frac{2L_2}{D^2 T_s R_L} \tag{30}$$

which can be solved to give

$$\frac{V_C}{U} = 0.5 + \sqrt{0.25 + m} \tag{31}$$

TABLE IV
PARAMETER VALUES FOR EXPERIMENTAL MEASUREMENT IN REGIME 2 OPERATION

Parameters	Values
L_1	8 mH
L_2	45 μH
C_s	270 μF
C_o	3300 μF
R_L	75 Ω
T_s	1/110000 s
$\hat{E}$	$110 \times \sqrt{2}$ V
U	60 V

where m is an important system parameter defined as

$$m \stackrel{\text{def}}{=} \frac{2L_2}{D^2 T_s R_L}. \tag{32}$$

Fig. 18 shows the relation between V_C/U and m. In practice, two constraints affect the selection of m.

1) The output buck stage is required to operate in discontinuous mode for the purpose of regulation. This

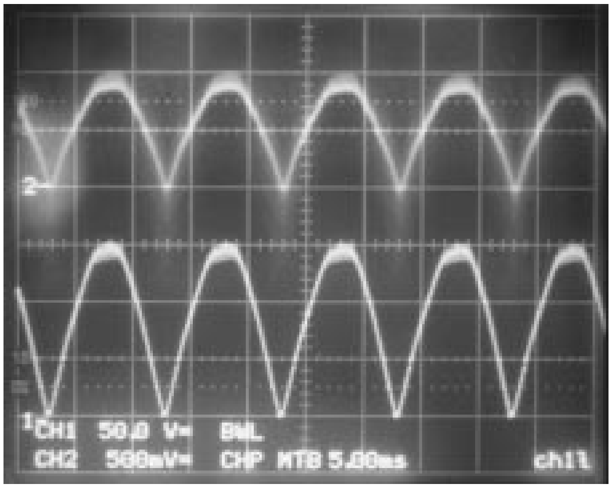


Fig. 20. Upper trace: rectified input current (0.5 A/div; 5 ms/div). Lower trace: rectified input voltage (50 V/div; 5 ms/div).

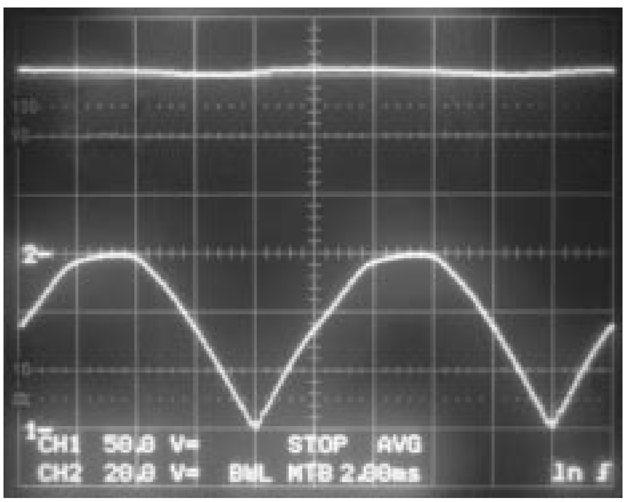


Fig. 21. Upper trace: output voltage (20 V/div; 2 ms/div). Lower trace: rectified input voltage (50 V/div; 2 ms/div).

necessitates satisfaction of the following inequality:

$$\frac{2L_2}{T_s R_L} < 1 - D_{\max} \Rightarrow m < \frac{1 - D_{\max}}{D_{\max}^2}. \tag{33}$$

For example, if D varies up to about 0.6, m must be below 1.11. Thus, a realistic choice of m is below one.

2) The input stage requires V_C be larger than $\hat{E}$. From (30), we have

$$\frac{\hat{E}}{U}\left(\frac{\hat{E}}{U} - 1\right) < m. \tag{34}$$

Combining inequalities (33) and (34) gives

$$\frac{\hat{E}}{U}\left(\frac{\hat{E}}{U} - 1\right) < m < \frac{1 - D_{\max}}{D_{\max}^2} \tag{35}$$

which defines the range of loads that can be regulated. Note that an alternative form of (35) can be derived using (28) as

$$\sqrt{\frac{2}{gR_L}}\left(\sqrt{\frac{2}{gR_L}} - 1\right) < m < \frac{1 - D_{\max}}{D_{\max}^2}. \tag{36}$$

Remarks: From (35), we see that a step-up application (i.e., $\hat{E} < U$) would impose no lower bound for m, while step down would require m be greater than $(\hat{E}/U)(\hat{E}/U - 1)$.

D. Experimental Demonstration

The experimental converter is constructed as in the previous case, but the inductance values are chosen to ensure that L_1 operates in CCM and L_2 in DCM. Table IV shows the parameter values of the experimental converter for this operating regime.

The control circuit consists of a simple current shaper for shaping the input current to a sinusoidal waveform, a simple frequency modulator for regulating the output voltage, and a multiplier circuit for power balancing (setting the amplitude of the sinusoidal input current waveform in accordance with the load power consumption). The operation of the input current shaper resembles that of a current-mode controller, which involves sensing the input current and comparing it with a mains voltage analog. The switches turn on by a clock signal and turn off when the input current hits the mains voltage analog. The clock that turns on the switches is frequency modulated. The required frequency modulation is performed by a simple 555 timer whose oscillation frequency is varied by a voltage-controlled current source which is, in turn, controlled by an error amplifier carrying information about the variation of the output voltage. Finally, the multiplier circuit sets the amplitude of the input current in accordance with the load power demand. A simplified schematic of the control circuit is shown in Fig. 19.

Fig. 20 shows the input current and voltage waveforms, confirming the power factor correction property. Note that the input current shown here has its switching frequency ripples removed by filtering. The output voltage is well regulated at 60 V$\pm$0.8 V, as shown in Fig. 21. The measured power factor in this case is 0.999, which verifies the almost "perfect" power factor correction provided by the Sheppard–Taylor topology.

IV. Conclusion

Single-stage PFC regulators have received much attention recently as motivated by the demand for simple low-cost circuit topologies for low–medium power switching regulators with high-input power factor. Typical structures of single-stage PFC converters consist of a cascade combination of two converters sharing one (or a set of) active switch(es), which is controlled by one drive signal. The SSIPP [2], BIFRED, and BIBRED [3], [4] are well-known examples. This paper adds to the list of single-stage PFC regulators the rarely known Sheppard–Taylor converter whose potential for PFC applications was not recognized in the past. In particular, this paper introduces two regimes of operation of the single-stage Sheppard–Taylor converter that can achieve high power factor and output regulation. Among the two regimes, the one with a CCM converter cascading a DCM converter (Regime 2 as in the paper) should represent a less practical mode of operation due to the undesirable mandatory frequency variation and the high peak value of the DCM output current. Nonetheless, when operating in the other way around (Regime 1 as in the paper), the converter provides a useful alternative topology.

APPENDIX

The closed-form expressions for the two definite integrals used in Sections II-B and C are

$$\int_0^{\pi} \frac{\sin\theta(1+p\sin\theta)}{1-p\sin\theta}\,d\theta = -2 - \frac{2\pi}{p} + \frac{2\pi}{p\sqrt{1-p^2}} + \frac{4\arctan\left(\frac{p}{\sqrt{1-p^2}}\right)}{p\sqrt{1-p^2}}$$

$$\int_0^{\pi} \left(\frac{1+p\sin\theta}{1-p\sin\theta}\right)^2 d\theta = \pi + \frac{4p^2\pi}{1-p^2}\sqrt{\frac{1}{1-p^2}} - \frac{8p^2\arctan\left(\frac{p}{\sqrt{1-p^2}}\right)}{\sqrt{1-p^2}(1-p^2)}$$

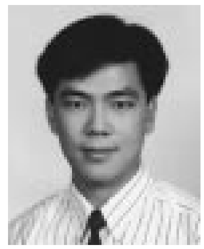
where, for brevity, p is used to denote $\hat{E}/V_C$.

ACKNOWLEDGMENT

The authors wish to thank K. C. Tsoi for assistance with the construction of the experimental circuits and the anonymous reviewers for constructive comments and helpful information.

REFERENCES

[1] D. I. Sheppard and B. E. Taylor, “A new converter topology imparts nonpulsating currents to input and output lines,” in *Proc. PCI/MOTOR-CON*, 1983, pp. 60–73.
[2] R. Redl, L. Balogh, and N. O. Sokal, “A new family of single-stage isolated power-factor-correctors with fast regulation of the output voltage,” in *IEEE PESC’94 Rec.*, pp. 1137–1144.
[3] M. Madigan, R. Erickson, and E. Ismail, “Integrated high-quality rectifier-regulators,” in *IEEE PESC Rec.*, 1992, pp. 1043–1051.
[4] M. M. Jovanović, D. M. C. Tsang, and F. C. Lee, “Reduction of voltage stress in integrated high-quality rectifier-regulators by variable frequency,” in *Proc. IEEE APEC*, 1994, pp. 569–575.
[5] C. K. Tse, “Zero-order switching networks and their applications to power factor correction in switching converters,” *IEEE Trans. Circuits Syst. I*, vol. 44, no. 8, pp. 667–675, 1997.
[6] C. K. Tse, Y. S. Lee, and W. C. So, “An approach to modeling dc/dc converter circuits using graph theoretic concepts,” *Int. J. Circ. Theor. Appl.*, vol. 22, pp. 371–384, July 1993.
[7] P. C. Todd, “UC3854 controlled power factor correction circuit design,” *Unitrode IC Product and Applications Handbook 95–96*, Nov. 1995, pp. 303–322.
[8] M. H. L. Chow and C. K. Tse, “Theoretical study of performance of continuous-mode boost converters for power-factor-correction applications,” in *Proc. IEEE PEDS’97*, May 1997, pp. 590–595.



C. K. Tse (M’90–SM’97) received the B.Eng. (Hons.) and Ph.D. degrees in electrical engineering from the University of Melbourne, Australia, in 1987 and 1991, respectively.

He is presently an Associate Professor with Hong Kong Polytechnic University, Hong Kong, and his research interests include circuit theory and power electronics. He has worked in software development with an Australian database company for some years and spent a short period of time with ASTEC International (Hong Kong) Limited as a Senior Engineer. He is the author of *Linear Circuit Analysis* (London, U.K.: Addison-Wesley, 1998).

Dr. Tse initiated the first Hong Kong IEEE Workshop on Switch Mode Power Supplies in 1993, for which he was the General Chairman and Technical Program Chairman in 1995 and 1997, respectively. He was also Technical Program Chairman of the Symposium on Power Electronics Circuits in 1994. He was awarded the L.R. East Prize from the Institution of Engineers, Australia, in 1988. He was the recipient of a President’s Award for Achievement in Research from the Hong Kong Polytechnic University in 1997. He is a Chartered Professional Engineer in Australia.

M. H. L. Chow (M’98) received the B.Sc.(Eng.) degree from the University of Hong Kong, Hong Kong, and the M.Sc. degree from the University of Surrey, Guildford, U.K., in 1980 and 1984, respectively.

In the course of his career, he has worked in short-wave radio design with Philips, Hong Kong, and in switch-mode power supplies design with Thomson, Singapore. In 1985, he started his teaching career at Hong Kong Polytechnic University, where he is currently a Senior Lecturer in the Department of Electronic Engineering. His main research interests are power electronics and analog circuit design.