On the Design of a Programmable-Gain Amplifier With Built-In Compact DC-Offset Cancellers for Very Low-Voltage WLAN Systems

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***Abstract*—Two circuit techniques adopted in the design of an embedded programmable-gain amplifier (PGA) for very low-voltage (LV) wireless local-area network systems are presented. A switched-current-resistor (SCR) technique minimizes the bandwidth variation and the transient in gain tuning by stabilizing, concurrently, the PGA's feedback factor and quiescent-operating point. Another technique, inside-opamp dc-offset canceller (DOC), embeds inside the PGA's opamp a subthreshold-biased G_m–C integrator for extracting its output dc-offset, while negatively feeding the correction (current) signal back to the opamp at an inherent low-impedance node. The resultant main benefits are: 1) the chip area, for realizing the large time constant in dc-offset extraction, is very small and 2) the lower cutoff of the PGA and the DOC-induced nonlinearity and noise are all suppressed by an amount of the loop gain in closed-loop formation. A 1-V three-stage 52-dB gain range PGA reinforcing such two techniques was designed and fabricated in a 3.3-V 0.35-μm CMOS process. It consumes 7.4 mW of power while measuring < 0.2-μs gain-switching transient and $+8.4$ dBm IIP3. The means of the lower and upper -3-dB cutoffs (averaged over 52-dB gain steps) are 2.25 kHz and 17.1 MHz, respectively.**

***Index Terms*—CMOS, constant bandwidth (BW), dc-offset canceller (DOC), low voltage (LV), programmable-gain amplifier (PGA), transient, wireless local-area network (WLAN).**

I. Introduction

THE rapid evolution of CMOS technology has accelerated the integration of mixed-signal systems, such as the wireless transceiver [1], on a single chip. Technology-scaling associated reliability and leakage-current issues, however, have driven the downsizing of threshold voltage continuously lagging that of the power supply [2], resulting in a continuous reduction of voltage head room for designing the analog parts. In the literature, techniques that help minimize the supply voltage requirement have been extensively investigated, ranging from elementary subcircuits like the bulk-input operational amplifier (opamp) [3] to building blocks like the sigma-delta modulator [4]. This paper, on the other hand, is focused on the design of a low-voltage (LV) embedded programmable-gain amplifier (PGA) with dc-offset cancellation for a receiver targeting the IEEE 802.11a/b/g wireless local-area network (WLAN) [5] applications. Two novel circuit techniques, namely switched current resistor (SCR) and inside-opamp dc-offset canceller (DOC), are proposed. These, in conjunction, not only enable the PGA to operate robustly under LV constraints, but also enhance the design efficiency and operation of the entire receiver as mentioned below.

With a zero-intermediate-frequency (IF) or low-IF receiver architecture, the signal levels arriving at the baseband are scaled to around the 0-dBm range for analog-to-digital conversion. The dynamic-range requirement from the antenna to the baseband is approximately 0 to 80 dB, with the majority of this gain achieved in the baseband. If the radio front-end offers typically a 0- to 30-dB gain range, the baseband channel-selection filter and PGA have to provide another 0 to 50 dB of controllable gain. In practice, although a cascade use of multiple PGAs can attain such a high gain range, the PGA has to feature an excess bandwidth (BW), roughly $10\times$ wider than that of the channel-selection filter to ensure stable selectivity against gain. Leaks of a high-performance opamp structure underneath a LV supply, however, will highly complicate the implementation.

On the other hand, the dc offset can easily saturate the PGA due to a large cascaded gain, requesting more local dc-offset removals [6], [7]. In a zero-IF receiver, the composite high-pass pole must be around tens of kilohertz to prevent the signal from deep damage, resulting in a large chip-area impact and inducing a long dc-offset transient in the gain change (critical for 802.11a and 802.11g, where the short preamble for gain settling is just 8μs).

The two techniques proposed here address these concerns. The SCR technique realizes a constant-BW transient-free gain control such that the BW requirement of the PGA can be largely relaxed to less than 20 MHz, while reducing the settling time in gain change and relaxing the opamp requirements as well as enhancing the stopband rejection. For the inside-opamp DOC technique, it implements efficiently a large time-constant integrator around the PGA to eliminate the dc offset and offers pole switchability to shorten the receiver setting time in case of dc-offset transients.

In this paper, in-depth treatments of the proposed techniques that are backed with detailed circuit analysis and simulation results are presented, profitably complementing the key concepts and experimental results that have been reported in part in [8].

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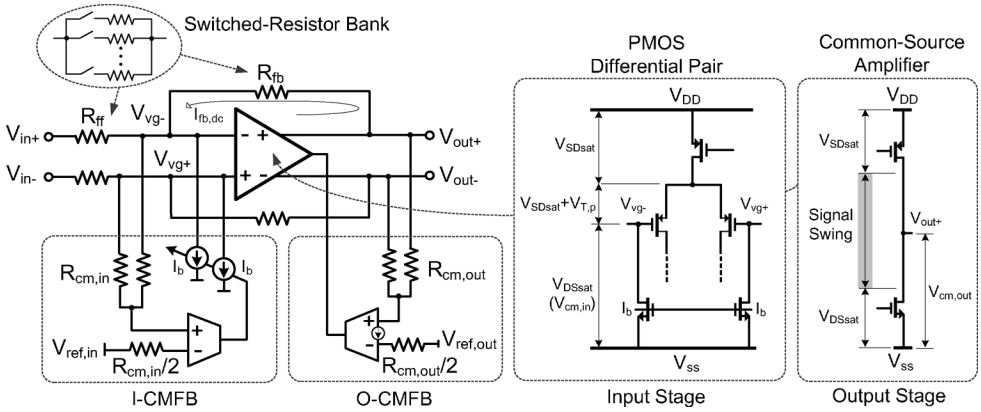


Fig. 1. LV switched-resistor PGA modified from biased inverting amplifier.

Section II presents the limitations of a conventional switched-resistor PGA in LV operation. Sections III and IV describe the SCR and inside-opamp DOC techniques, respectively. Section V shows the details of the design and simulation process of a PGA prototype, followed by the experimental results in Section VI. The conclusions and benchmarks are stated in Section VII.

II. Limitations of Conventional Switched-Resistor PGA in LV Operation

In terms of voltage headroom, technology scaling within the submicrometer scales will not imply a significant difference in the design of analog blocks as long as it is accompanied by a standard power supply ($V_{\rm DD}$). For instance, a standard inverting amplifier employing a switched-resistor bank for gain control becomes a PGA [9]. However, paving the way to the sub-1-V nanoscale processes, analog circuits are required to be operational underneath very LV headroom, rendering, to some extent, the classical switched-resistor PGA ineffectual. The key limitations are now briefly discussed.

One way to befit an inverting amplifier for a minimum $V_{\rm DD}$ is using a level shifter [10]. As depicted in Fig. 1, an extra input common-mode feedback (I-CMFB) explicitly biases the virtual ground ($V_{\rm vg+}$ and $V_{\rm vg-}$) to a common-mode voltage $V_{\rm cm,in}$, that is the minimum saturation voltage $V_{\rm DS,sat}$ (i.e., 0.1 V) necessary for a transistor to act as a current sink I_b. Taking into account this voltage requirement into the input stage (pMOS differential pair), the lowest possible $V_{\rm DD}$ (i.e., $V_{\rm DD} \geq |V_{T,p}| + 2V_{\rm SDsat} + V_{\rm DSsat}$) can be found, i.e., $\sim$ 1 V for $V_{T,p} = -0.65$ V. The second stage is a typical class-A amplifier, which delivers a high swing output by locking, explicitly, the output common-mode voltage $V_{\rm cm,out}$ to $V_{\rm DD}/2$. However, a large output swing requires a particular output common-mode feedback (O-CMFB). For instance, a resistive detector is required to extract $V_{\rm cm,out}$ and convert it to a current signal for the back-end current amplifier. Gain tuning can be attained via replacing either the feedforward $R_{\rm ff}$ or feedback $R_{\rm fb}$ resistor by a switched-resistor bank. The associated switch devices have to be realized with nMOS transistors and to be placed at $V_{\rm vg+}$ and $V_{\rm vg-}$ to gain enough overdrive voltage (V_{OD}) of roughly 0.3 V (i.e., $V_{\rm DD} - V_{T,n} - V_{\rm DS,sat}$). Two distinct reference voltages, $V_{\rm ref,in}$ (0.1 V) and $V_{\rm ref,out}$ (0.5 V), are required. $V_{\rm ref,out}$ should be buffered in order to be able to drive the O-CMFB that drains static current.

This PGA structure is basically LV compliant but suffers from two key drawbacks. First, independently of $V_{\rm DD}$, gain tuning through either $R_{\rm ff}$ or $R_{\rm fb}$ will vary the feedback factor, resulting in a gain-dependent output BW. Second, since the input impedance of the PGA is mainly governed by $R_{\rm ff}$, tuning $R_{\rm ff}$ without adopting a preceding buffer will draw a gain-dependent current from the previous stage that can be a mixer or a passive filter in a receiver. To avoid buffers and facilitate the concern of loading effects in designing a multistage PGA, $R_{\rm fb}$ should be tuned instead. The unequal common-mode levels of $V_{\rm cm,out}$ and $V_{\rm cm,in}$, however, induce another gain-dependent dc current $I_{\rm fb,dc}$ [i.e., $I_{\rm fb,dc} = (V_{\rm cm,out} - V_{\rm cm,in})/R_{\rm fb}$] in their feedback resistors, entailing a long settling time to re-stabilize the input–output (I/O) CMFBs and opamp at a new quiescent operating point.

III. Proposed LV Switched-Current-Resistor PGA

The proposed SCR PGA can robustly overcome the above-mentioned problems and is operational underneath a very LV $V_{\rm DD}$ of 1 V, or even below. Unless otherwise stated, a 1-V $V_{\rm DD}$ is assumed in the following description.

A. Basic Principles

Illustrated in Fig. 2 is the SCR PGA for a transient-free and constant-BW gain control. The former property is described first.

A set of switched resistors $[R_{{\rm fb},1} \cdots R_{{\rm fb},n}]$ is added in parallel with $R_{\rm fb}$ to achieve a tunable gain range between the maximum (i.e., $-R_{\rm fb}/R_{\rm ff}$) and the minimum [i.e., $-(R_{\rm fb}//R_{{\rm fb},1} \cdots //R_{{\rm fb},n})/R_{\rm ff}$]. In operation, when $[R_{{\rm fb},1} \cdots R_{{\rm fb},n}]$ are switched by the gain-control logic $[b_{c,1} \cdots b_{c,n}]$, a set of switched current sources $[I_{{\rm fb},1} \cdots I_{{\rm fb},n}]$ and grounded resistors $[R_{x,1} \cdots R_{x,n}]$ are switched correspondingly, such that $[I_{{\rm fb},1} \cdots I_{{\rm fb},n}]$ can replace the opamp to deliver the transient current, while $[R_{x,1} \cdots R_{x,n}]$ can sink the same current out from $V_{\rm vg-}$ as given by

$$I_{{\rm fb},n} = \frac{V_{\rm cm,out} - V_{\rm cm,in}}{R_{{\rm fb},n}} = \frac{V_{\rm cm,in}}{R_{x,n}}, \qquad \text{for } n = 1, 2, 3, \ldots . \tag{1}$$

Practically, equalizing the last two terms over process, voltage and temperature (PVT) variation is not complicated since $V_{\rm cm,out}$ and $V_{\rm cm,in}$ are mirrors of $V_{\rm ref,out}$ and $V_{\rm ref,in}$, respectively. They can be generated underneath one master $V_{\rm DD}$ (i.e.,

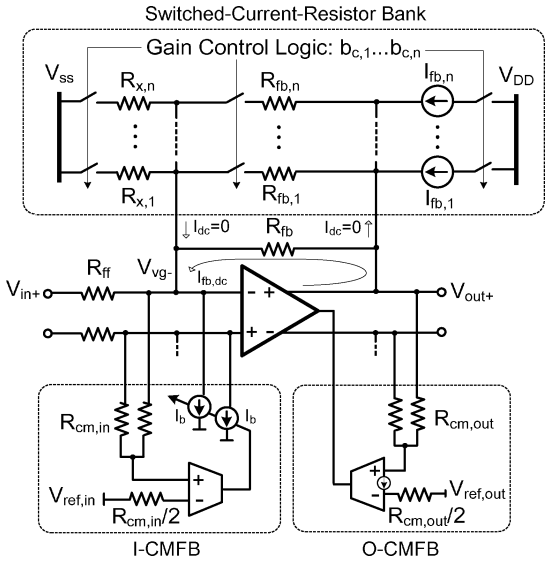


Fig. 2. Proposed SCR PGA (negative terminal is omitted for clarity).

$V_{\mathrm{ref,out}} = V_{\mathrm{DD}}/2$ and $V_{\mathrm{ref,in}} = V_{\mathrm{DD}}/10$), while $R_{\mathrm{fb},n}$ and $R_{x,n}$ can be synthesized using the same unit (poly) resistor R_u (i.e., $\alpha_n R_u = R_{\mathrm{fb},n} = 4R_{x,n}$, for $n = 1,\ 2,\ 3, \ldots$ where α_n is a positive integer representing a resistive ratio). Any PVT variation results in a common-mode disturbance on both terms. Yet, matching the first term of (1) to the rest involves an extra signal conversion such that the practically generated switched current sources $[I'_{\mathrm{fb},1} \cdots I'_{\mathrm{fb},n}]$ can track the PVT variations of $[R_{\mathrm{fb},1} \cdots R_{\mathrm{fb},n}]$, $[R_{x,1} \cdots R_{x,n}]$, $V_{\mathrm{ref,out}}$ and $V_{\mathrm{ref,in}}$. A LV resistor-to-current (R-to-I) conversion circuit serving this role is proposed next.

B. Proposed R-to-I Conversion Circuit

Fig. 3 shows the R-to-I conversion circuit for generating $V_{\mathrm{ref,out}}$, $V_{\mathrm{ref,in}}$, and $[I'_{\mathrm{fb},1} \cdots I'_{\mathrm{fb},n}]$ that approach the ideal $[I_{\mathrm{fb},1} \cdots I_{\mathrm{fb},n}]$ governed by (1). An error amplifier A_{error} in a feedback loop tracks the absolute value of R_3 underneath a fixed voltage V_z. The corresponding reference current $I_{\mathrm{fb,ref}}$ is therefore $\propto 1/R_3$. V_z is a mirror of V_x that is set to 0.1 V ($V_{\mathrm{DD}}/10$), enabling A_{error} to be realized simply by a p-channel differential pair. The R_3-tracked $I_{\mathrm{fb,ref}}$ is afterward mirrored to the switched current sources $[I'_{\mathrm{fb},1} \cdots I'_{\mathrm{fb},n}]$ through transistors M_1 to $[M_{b,1} \cdots M_{b,n}]$, which features the same ratios of $R_{\mathrm{fb},1}$ to $[R_{\mathrm{fb},1} \cdots R_{\mathrm{fb},n}]$. Normalizing $R_{\mathrm{fb},1}$ as the basic element among $[R_{\mathrm{fb},1} \cdots R_{\mathrm{fb},n}]$, $[I'_{\mathrm{fb},1} \cdots I'_{\mathrm{fb},n}]$ turns it in a function of R_3 as given by

$$I'_{\mathrm{fb},n} = \frac{V_z}{R_3}\left(\frac{R_{\mathrm{fb},1}}{R_{\mathrm{fb},n}}\right), \qquad \text{for } n = 1,\ 2,\ 3, \ldots . \tag{2}$$

The next step is make $I'_{\mathrm{fb},n}$ proportional to just $V_z/R_{\mathrm{fb},n}$. It can be done by substituting R_3 by $R_{\mathrm{fb},1}/4$, which concurrently equalizes the numerator of (2) to that of the second term in (1) (i.e., $4V_z = V_{\mathrm{cm,out}} - V_{\mathrm{cm,in}}$), yielding

$$I'_{\mathrm{fb},n} = \frac{4V_z}{R_{\mathrm{fb},n}}, \qquad \text{for } n = 1,\ 2,\ 3, \ldots . \tag{3}$$

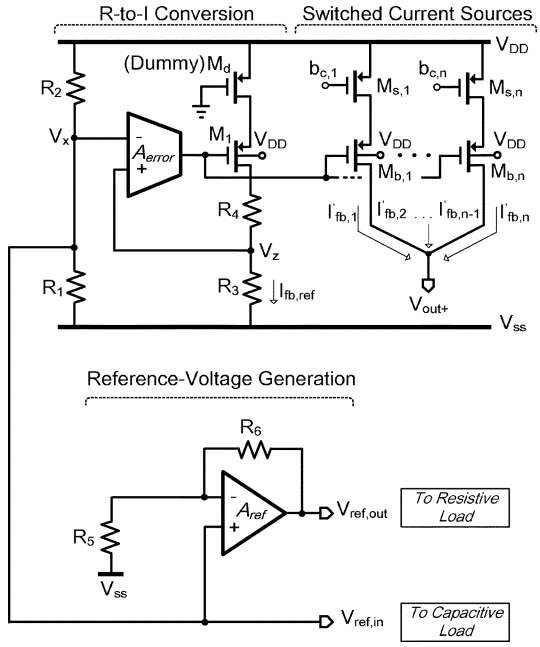


Fig. 3. R-to-I conversion circuit for reference voltage and switched-current-sources generations.

Substituting (3) back into the first term of (1), and replacing $R_{\mathrm{fb},n}$ and $R_{x,n}$ according to $\alpha_n R_u = R_{\mathrm{fb},n} = 4R_{x,n}$, will lead to the practical expression of (1), i.e.,

$$\frac{4V_z}{\alpha_n R_u} = \frac{V_{\mathrm{cm,out}} - V_{\mathrm{cm,in}}}{\alpha_n R_u} = \frac{V_{\mathrm{cm,in}}}{\frac{\alpha_n}{4} R_u}, \qquad \text{for } n = 1,\ 2,\ 3, \ldots \tag{4}$$

Recalling that V_z, $V_{\mathrm{cm,out}}$ and $V_{\mathrm{cm,in}}$ are, respectively, mirrors of $V_x(V_{\mathrm{DD}}/10)$, $V_{\mathrm{ref,out}}(V_{\mathrm{DD}}/2)$ and $V_{\mathrm{ref,in}}(V_{\mathrm{DD}}/10)$, the error voltage ($V_\Delta$) associated to V_{DD}, and the error resistance (R_Δ) associated to R_u, will have no effect on the balancing of (4) as given by

$$\begin{aligned} \frac{4\frac{(V_{\mathrm{DD}} \pm V_\Delta)}{10}}{\alpha_n (R_u \pm R_\Delta)} &= \frac{\frac{(V_{\mathrm{DD}} \pm V_\Delta)}{2} - \frac{(V_{\mathrm{DD}} \pm V_\Delta)}{10}}{\alpha_n (R_u \pm R_\Delta)} \\ &= \frac{\frac{(V_{\mathrm{DD}} \pm V_\Delta)}{10}}{\frac{\alpha_n}{4}(R_u \pm R_\Delta)} \end{aligned} \tag{5}$$

yielding in overall a PVT-insensitive operation.

The static and dynamic performances of the SCR technique are further improved by applying the following circuit practices.

1) The current mirror M_1 to $[M_{b,1} \cdots M_{b,n}]$, raises the precision by adding R_4 with $R_4 = R_3(V_D - V_z)/V_z$, level shifting the drain voltage (V_D) of M_1 to match that of $[M_{b,1} \cdots M_{b,n}]$.
2) The overall resistor matching, and the ground-noise rejection of A_{error} and A_{ref} (A_{ref} forms a noninverting amplifier for buffering $V_{\mathrm{ref,out}}$), are enhanced by selecting $R_1 = R_2/9 = R_3 = R_4/4 = R_5 = R_6/4$, resulting in a resistor spread of just 9.
3) $[I'_{\mathrm{fb},1} \cdots I'_{\mathrm{fb},n}]$ are switched through $[M_{s,1} \cdots M_{s,n}]$ rather than $[M_{b,1} \cdots M_{b,n}]$ such that $[M_{s,1} \cdots M_{s,n}]$ obtain the maximum overdrive voltage, leading to reduced device sizes and lower charge injection values. Moreover, since

only the current paths are opened, the gate-to-source capacitance of $[M_{b,1}\cdots M_{b,n}]$ are kept charged for a faster turn-on time [11].

4) Connecting the bodies of $[M_{b,1}\cdots M_{b,n}]$ to $V_{\rm DD}$ prevents the charge injection of $[M_{s,1}\cdots M_{s,n}]$ from coupling to their gates through their body-to-gate parasitic capacitance, yielding in simulation 200% to 300% (depending on the gain step) shorter transients.

C. Constant Feedback Factor

Another corollary of the SCR technique to the PGA is that the feedback factor $\beta_{\rm PGA}$, as given by

$$\beta_{\rm PGA}=\frac{1}{1+\left(\frac{R_{\rm fb}//R_{{\rm fb},1}\cdots//R_{{\rm fb},n}}{R_{\rm ff}//R_{x,1}\cdots//R_{x,n}}\right)} \tag{6}$$

will be stabilized upon the two conditions specified in (7) and (8) are satisfied concurrently

$$\frac{R_{\rm fb}}{R_{\rm ff}}=\frac{R_{{\rm fb},n}}{R_{x,n}}\le\frac{V_{\rm cm,out}-V_{\rm cm,in}}{V_{\rm cm,in}}\,,\qquad \text{for } n=1,\ 2,\ 3,\ldots \tag{7}$$

and

$$\beta_{\rm PGA}\le\frac{V_{\rm cm,in}}{V_{\rm cm,out}}. \tag{8}$$

It can be examined that both conditions can be fulfilled with no contradiction to the prerequisites defined in the previous section for a transient-free gain control. Moreover, since (7) and (8) depend on relative ratio rather than absolute value, $\beta_{\rm PGA}$ is robustly stabilized against gain over PVT. A constant $\beta_{\rm PGA}$ has the advantages of unvarying settling time and constant stopband rejection. Specific results of this claim are given in Section V-D.

D. Design Examples

1) A 1-V 24-dB-Gain-Range SCR PGA: For a 1-V $V_{\rm DD}$, $V_{\rm cm,in}=0.1$ V and $V_{\rm cm,out}=0.5$ V are accordingly set to respect the aforesaid concerns. To offer, for instance a gain range of -12 dB to 12 dB with a step size of 6 dB, we set $R_{\rm fb}=4R_{\rm ff}$ and $4R_{x,3-n}=R_{{\rm fb},3-n}=2^nR_{\rm ff}$ for $n=-1,\ 0,\ 1,\ 2$, resulting in a constant $\beta_{\rm PGA}$ of 0.2 while satisfying (1) for a transient-free gain adjustment. Without the technique, $\beta_{\rm PGA}$ will vary between 0.2 (at 12 dB) and 0.8 (at -12 dB), equivalent to a 4-fold BW difference. Of course, in practice, the constancy of $\beta_{\rm PGA}$ is related to the resistance ratio of $R_{\rm cm,in}$ to $R_{\rm ff}$ and $[R_{x,1}\cdots R_{x,n}]$. Under the same numerical conditions given above, (6) practically becomes

$$\beta'_{\rm PGA}=\frac{1}{5}\frac{1}{1+\frac{4}{5}\left(\frac{R_{\rm ff}//R_{x,1}\cdots//R_{x,n}}{R_{\rm cm,in}}\right)}. \tag{9}$$

How large $R_{\rm cm,in}$ could be? If $R_{\rm cm,in}$ is $5\times$ of $(R_{\rm ff}//R_{x,1}\cdots//R_{x,n})$, $\beta'_{\rm PGA}$ will vary between 0.177 (at 12 dB) to 0.198 (at -12 dB), leading to a BW variation of around 12%.

2) A 0.6-V 24-dB-Gain-Range SCR PGA: Again, $V_{\rm cm,in}$ of 0.1 V and $V_{\rm cm,out}$ of 0.3 V are the proper choices for a $V_{\rm DD}$ of 0.6 V. To attain the same gain range as in the former example, two identical PGAs in cascade are required because the maximum closed-loop gain, governed by (7), is 2 ($\sim$ 6 dB) in magnitude. Each PGA offers a gain range of -6 dB to 6 dB with a step size of 6 dB by setting $R_{\rm fb}=2R_{\rm ff}$ and $2R_{x,2-n}=R_{{\rm fb},2-n}=2^nR_{\rm ff}$ for $n=0,\ 1$. Comparing with the former case, a transient-free gain control is still achieved but with a larger value of $\beta_{\rm PGA}=1/3$. Although two identical PGAs in cascade reduce the BW by 35% (i.e., multiplied by a factor of $\sqrt{[2^{1/N}-1]}$, where N is the number of cascaded stages), a larger $\beta_{\rm PGA}$ will result in a 67% increment of BW if the same opamp specification is presumed, giving a net BW enlargement of 32%. Evidently, two PGAs imply a double of the power (i.e., a roughly fair tradeoff between power and $V_{\rm DD}$). The BW variation of this case is similar to the former example and its presentation is discarded for brevity.

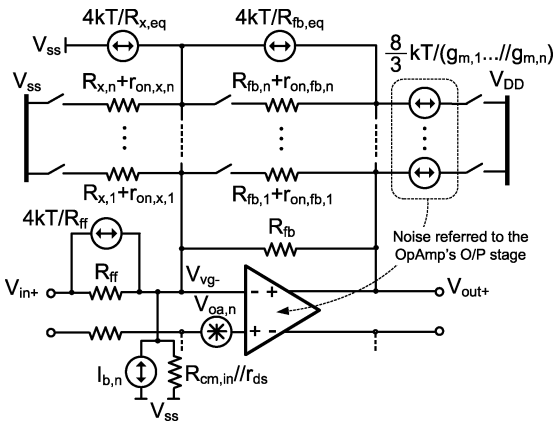


Fig. 4. Simplified noise model of proposed SCR PGA.

E. Linearity Considerations

For a fully differential circuit implementation with dc-offset cancellation, the even-harmonic distortion can be suppressed effectively such that only the odd harmonics are dominant. In determining the third-harmonic distortion (HD3) of a highly linear (poly) resistor in series with a nonlinear nMOS switch, it would be wise to assume that the terminal in the resistor side receives a sinusoidal signal, whereas that of the switch side is grounded, leading to the following expression of HD3 [12]:

$$\text{HD3}\approx\frac{3}{32}\left(\frac{V_{\text{out-},p}}{V_g-V_{\rm cm,in}-V_{T,n}}\right)^2\cdot\left(\frac{r_{\rm on}}{R_{\rm fb}}\right)^3 \tag{10}$$

where V_g is the transistor gate voltage, $V_{\text{out-},p}$ is the peak value of the output voltage and $r_{\rm on}$ is the transistor on-resistance. For example, with $V_g=1$ V , $V_{\text{out-},p}=0.5$ V, $V_{\rm cm,in}=0.1$ V, $V_{T,n}=0.52$ V, and $R_{\rm fb}=2.5$ kΩ for a minimum-gain level, $r_{\rm on}$ can be as large as 213 Ω (8.5% of $R_{\rm fb}$) for a HD3 of -80 dB. This indicates that explicitly biasing $V_{\rm cm,in}$ to a value close to one of the supply rails also helps improving the linearity due to an increase of V_{OD}.

F. Noise Considerations

The equivalent noise model of Fig. 2 is depicted in Fig. 4. Since the PGA in the whole receiver design will be preceded

by a high-gain channel-selection filter, its gain-dependent input-referred noise is fairly uncritical to the entire receiver's noise figure. Moreover, only thermal noise is critical since high-pass poles are created at dc for each stage, rejecting the flicker noise sufficiently (more details in Section IV). The mean squared output noise $v^2_{\rm noise}$ of the SCR PGA is given by

$$v^2_{\rm noise} = \left(\frac{4kT}{R_{\rm ff}} + \frac{4kT}{R_{x,\rm eq}} + \frac{4kT}{R_{\rm fb,eq}} + I^2_{b,n}\right) R^2_{\rm fb,eq} + v^2_{{\rm oa},n}\left(1 + \frac{R_{\rm fb,eq}}{R_{\rm ff}//R_{x,\rm eq}//r_{ds}//R_{\rm cm,in}}\right)^2 \quad (11)$$

where $R_{x,\rm eq} = (R_{x,1} + r_{{\rm on},x,1})// \cdots //(R_{x,n} + r_{{\rm on},x,n})$, $R_{\rm fb,eq} = R_{\rm fb}//(R_{\rm fb,1} + r_{{\rm on},fb,1}) \cdots //(R_{\rm fb,n} + r_{\rm on,fb,n})$, k is the Boltzmann constant, T is the absolute temperature, r_{ds} is the output resistance of the current source I_b. $v_{{\rm oa},n}$ is the equivalent input-referred noise voltage of the opamp which includes the uncritical noise contribution of $[I_{\rm fb,1} \cdots I_{{\rm fb},n}]$ that are injected at the output stage {i.e., $(8/3) \times [kT/(g_{m,1} \cdots //g_{m,n})]$, where $g_{m,1} \cdots //g_{m,n}$ are the transconductances of $[M_{b,1} \cdots M_{b,n}]$} and the excess noise coefficient γ is assumed to be 2/3. $I^2_{b,n}$ is the mean squared noise current of I_b as given by

$$I^2_{b,n} = \frac{16}{3} kT \frac{V_{\rm cm,out} - V_{\rm cm,in}}{V_{\rm cm,in}(R_{\rm fb,eq}//R_{\rm ff}//R_{x,\rm eq})}. \quad (12)$$

Equation (12) indicates that keeping the resistor spread small and increasing the level of $V_{\rm cm,in}$ are imperatives to lower $v^2_{\rm noise}$, but there remains a tradeoffs in stage gain range and linearity. Thus, LV low-noise PGAs normally consume higher power (i.e., by distributing the gain range over a wider number of stages).

IV. Proposed Inside-Opamp DOC

A high-pass pole with a large time constant can prevent the baseband signal from serious damage, but it will have a deep impact in terms of large chip area and long settling time. This paper introduces an innovative inside-opamp DOC to alleviate such drawbacks. The basic idea consists in embedding inside the opamp an integrator with specific purpose of sensing the imbalance of its differential outputs. The integrated correction signal is then converted into current and negatively fed back to the opamp at an inherent low-impedance node. The resulting advantages of such a configuration in terms of **switchability, compactness**, **noise**, **linearity**, and **convergent speed** are presented below.

A. Basic Principle 1—Switchability

Switchable DOC is commonly used to reduce the inconstant dc-offset induced transient time and glitch noise by properly switching the high-pass pole(s) to a lower/higher frequency (e.g., switched transconductors [13] and successive switching [14]). The quality of the operation is determined by the switchability of the DOC itself, and the disturbance in the original midband and high-frequency behaviors of the forward-path circuitry.

The proposed inside-opamp DOC are described in Fig. 5 by using the inherent signal-conversion characteristic [i.e., voltage (V) and current (I)] of a two-stage opamp $A_{OL}(s)$. Divided into three subcircuits, $A_1(s)$, $A_2(s)$ and $A_3(s)$, represent

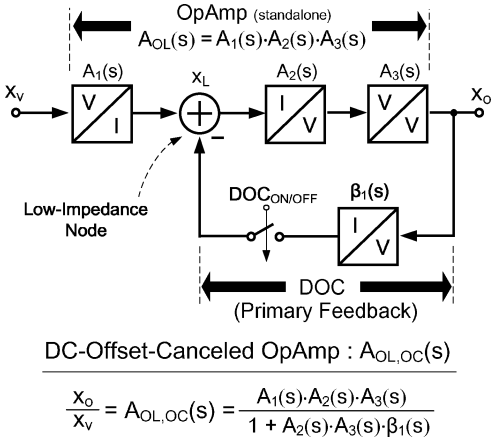


Fig. 5. Internal signal conversion of a two-stage opamp with DOC feedback.

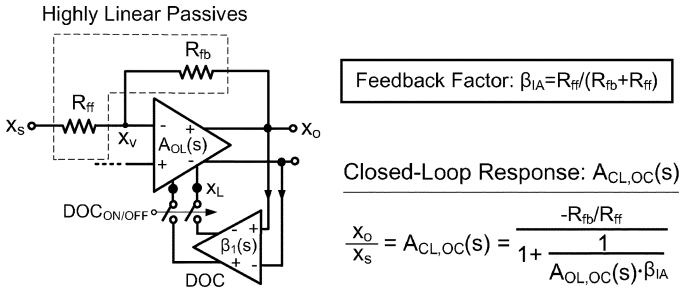


Fig. 6. Inverting amplifier using opamp with built-in DOC.

a transconductance, transimpedance and voltage amplifier, respectively. The former two subcircuits constitute the first *gain* stage and create an inherent low-impedance node x_L at their interface. It is known that a low-impedance node permits a linear sum of multiple current signals. Closing the primary feedback loop around $A_2(s)$ and $A_3(s)$, thus, creates a dc-offset-cancelled opamp $A_{\rm OL,OC}(s)$ while minimizing the loading effects between $A_1(s)$, $A_2(s)$ and $\beta_1(s)$. Realizing $\beta_1(s)$ as a transconductance integrator directly complies with the opamp internal signal conversion and creates a unilateral low-frequency feedback path from $x_{\rm O}$ to x_L.

B. Basic Principle 2 –Negative Feedback for Noise and Nonlinearity Reductions

In addition to the switchability concern, applying the DOC feedback at node x_L rather than the commonly employed virtual ground can lower the noise and nonlinearity induced by the DOC. It can be explained more generally in Fig. 6 by using an inverting amplifier. $\beta_1(s)$ resides on the forward path closed by the feedback resistor $R_{\rm fb}$ that creates another loop gain. As a result, the input-referred noise of $\beta_1(s)$ is divided by the preceding $A_1(s)$, which is a wideband transconductance amplifier. Likewise, the nonlinearity of $\beta_1(s)$ can be suppressed by the opamp-$R_{\rm fb}$-created loop gain, which can be made stable by concurrently applying the SCR technique.

C. Basic Principle 3—Negative Feedback for Area Savings

The idea of area savings is described by Fig. 7, which shows the constitution of an inverting amplifier in the frequency domain. The basic property of the negative feedback

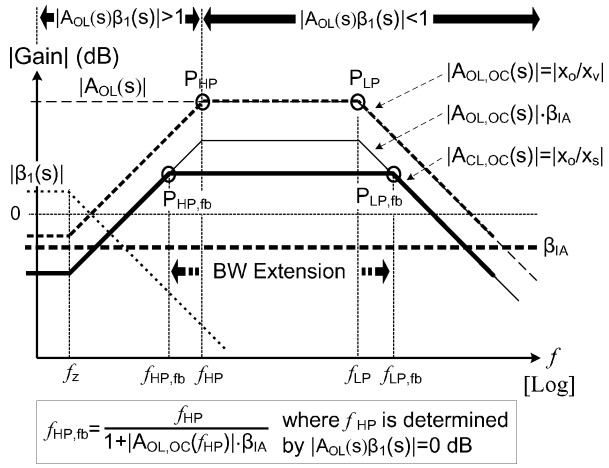


Fig. 7. Formation of inverting amplifier using opamp with built-in DOC illustrated in frequency domain.

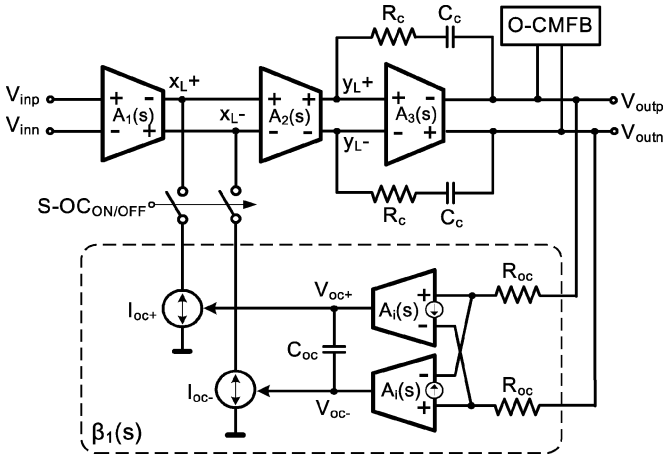


Fig. 8. Block schematic of the opamp with built-in DOC.

in BW-extension [15] is that any high-pass (low-pass) pole is shifted to a lower (higher) frequency value by an amount of the loop gain, [i.e., $f_{\rm LP}$ to $f_{\rm LP,fb}$ for low-pass and $f_{\rm HP}$ to $f_{\rm HP,fb}$ for high-pass]. This means that the dc-offset-cancelled opamp $A_{\rm OL,OC}(s)$, used in closed-loop, can lower its high-pass pole with no area overhead. It is different from the traditional case that only one global DOC is employed where the lower cutoff needs to be frequently adjusted once the forward path changes gain. The current case, instead, embeds each stage a dedicated DOC. The cutoff frequency, hence, depends simply on the feedback factor of the closed-loop circuit. The obtained rejection at dc is given by

$$\frac{|A_{\rm CL,OC}(f_{\rm HP,fb})|}{|A_{\rm CL,OC}(f_z)|} \approx \left|\frac{\beta_1(f_z)}{A_1(f_z)}\right| \frac{1}{\beta_{IA}}. \tag{13}$$

One may consider to make $\beta_1(s)$ feed back at the virtual ground because it will result in a higher rejection at dc, by a gain factor of $|A_1(f_z)|$, as given by

$$\frac{|A_{\rm CL,OC}(f_{\rm HP,fb})|}{|A_{\rm CL,OC}(f_z)|} \approx \frac{|\beta_1(f_z)|}{\beta_{IA}}. \tag{14}$$

In this way, however, a higher cutoff frequency will be resulted and the rejection at dc will become gain dependent.

D. Block-Level Design—Convergent Speed, Stability and Coverable Range

Fig. 8 shows the block schematic of the proposed opamp with a built-in DOC, where $A_1(s)$, $A_2(s)$, and $A_3(s)$ are the corresponding sub-amplifiers of the opamp as referred to Fig. 5. $\beta_1(s)$ refers to the DOC. Its front-end resistor R_{oc} interfaces the high swing output, $V_{{\rm out}p}$ and $V_{{\rm out}n}$, to two differential-input single-ended-output current amplifiers $A_i(s)$*'s*. The two $A_i(s)$*'s* drive differentially the capacitor C_{oc} and form a pseudo-differential *gm-C* integrator. This avoids systematic dc-offset while offering common-mode rejection internally. Their low-impedance inputs allow R_{oc}*'s* to be cross-coupled between the two $A_i(s)$*'s* for better matching. The output stage is an inverter-based charge pump $I_{oc+}(I_{oc-})$ that can source or sink current. Based on that, the speed in cancelling the dynamic dc-offset is doubled and the output swing is extended to *almost* rail-to-rail.

E. Transistor-Level Implementation

1) opamp: Fig. 9(a) shows the schematic of the differential opamp that was designed. A p-channel differential pair (M_{b1}, M_1 and M_2) implements $A_1(s)$ for its higher common-mode rejection ratio (CMRR). $A_1(s)$ sets the minimum $V_{\rm DD}(V_{\rm DD} \geq |V_{T,p}| + 2V_{\rm SDsat} + V_{\rm DSsat})$ of the entire opamp. A cross-coupled active load (M_{3A}, M_{3B}, M_{4A} and M_{4B}) [16] is employed to realize a wideband n-channel folded-cascode intermediate stage. $A_2(s)$ is a common-gate amplifier (M_5 and M_6) with a shunt-shunt feedback to further lowering its input resistance Rx_L+ as given by

$$Rx_{L+} = \frac{1}{(g_{m5}+g_{m5b})}\left(1+\frac{r_{o,b2}}{r_{o,1}//r_{o,3A}//r_{o,3B}//r_{o,5}}\right) \cdot\left(\frac{1}{1+(g_{m3A}-g_{m3B})\,r_{o,b2}}\right) \tag{15}$$

where g_{m5} (g_{m5b}) are the transconductance (body transconductance) of M_5. $r_{o,1}$, $r_{o,b2}$, $r_{o,3A}$, $r_{o,3B}$ and $r_{o,5}$ are the output resistances of M_1, M_{b2}, M_{3A}, M_{3B}, and M_5, respectively. g_{m3A} (g_{m3B}) are the transconductances of M_{3A} (M_{3B}). The loop gain $(g_{m3A}-g_{m3B})r_{o,b2}$ diminishes for differential signals when $g_{m3A}=g_{m3B}$, but it is effective [i.e., $(g_{m3A}+g_{m3B})r_{o,b2}$] in suppressing Rx_{L+} for common-mode signals.

The output resistance of $A_2(s)$ is lowered by another loop gain as given by

$$Ry_{L+} = \frac{r_{o,b2}}{1+\frac{(g_{m3A}-g_{m3B})(g_{m5}+g_{m5b})r_{o,1}r_{o,b2}}{(g_{m5}+g_{m5b})r_{o,1}+1}}. \tag{16}$$

For differential signals at y_{L+}, Ry_{L+} is dominated by $r_{o,b2}$ when $g_{m3A}=g_{m3B}$, which exhibits a high resistance to boost the gain. Differently for common-mode signals, Ry_{L+} is relatively low, i.e., $1/(g_{m3A}+g_{m3B})$, allowing the CMFB to be closed solely at the output stage (at M_7 and M_8). The phase margin is optimized, firstly by adding a feedforward capacitor C_{cp} to $A_2(s)$, and secondly by adding R_c and C_c (i.e., miller compensation) to $A_3(s)$. The component sizes of the opamp and DOC are listed in Table I, where the value of the main current sources and the nature of the passive components are specified as well.

2) DOC: To realize a large time constant, in the order of 0.1 ms, two circuit techniques are reinforced into the DOC.

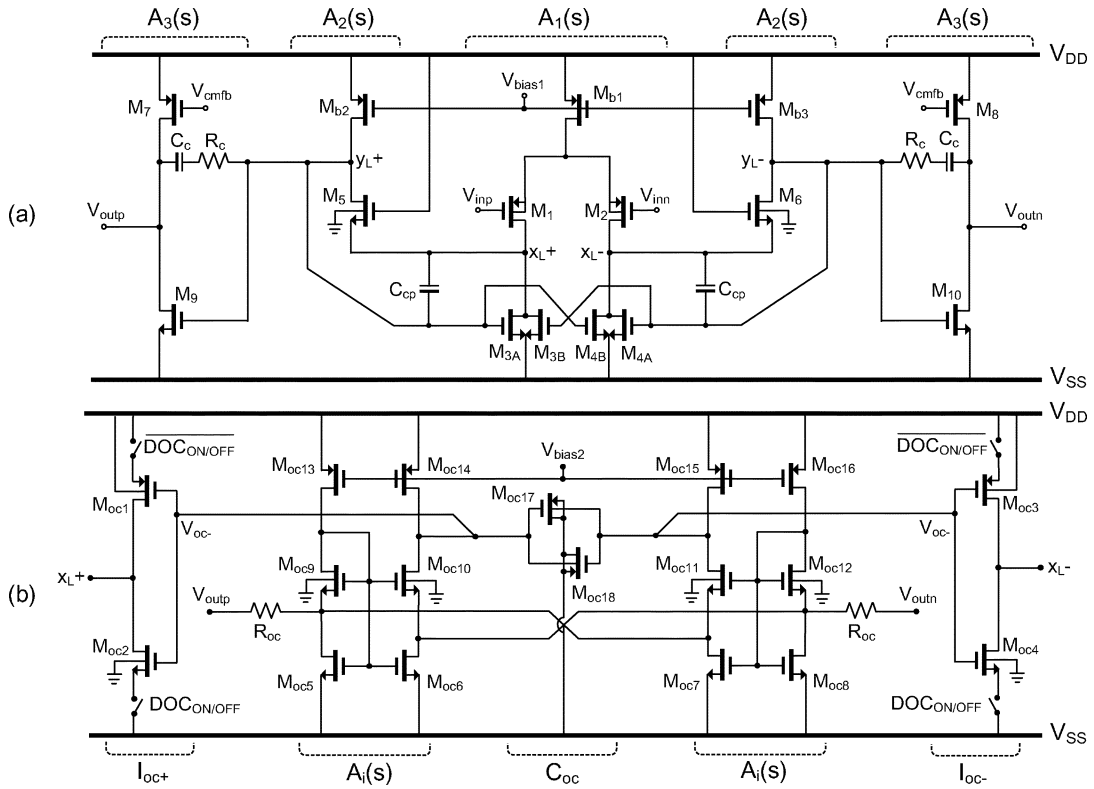
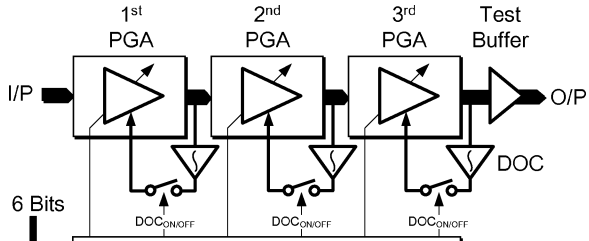


Fig. 9. Full-circuit schematics of the (a) opamp and its built-in (b) DOC. [Symbols correspond to Fig. 8].

TABLE I
COMPONENT SIZES FOR THE OPAMP AND DOC

Symbol	Size (μm)
$M_{b,1}$ *(0.43mA)*	2000/0.7
$M_{b,2\text{-}b,3}$ *(0.21mA)*	960/0.7
$M_{1\text{-}2,\ 7\text{-}8}$	1200/0.35
$M_{3A\text{-}4A}$, $M_{3B\text{-}4B}$	400/1.4
$M_{5\text{-}6}$	80/0.85
$M_{9\text{-}10}$	600/0.35
$M_{oc,1}$, $M_{oc,3}$	320/4
$M_{oc,2}$, $M_{oc,4}$	100/4
$M_{oc,5\text{-}8}$	320/2
$M_{oc,9\text{-}12}$	8/14
$M_{oc,13\text{-}16}$ *(10 nA)*	2/320
$M_{oc,17\text{-}18}$	320/4
$R_{oc,1\text{-}2}$ (poly)	40 kΩ
R_c (poly)	0.6 kΩ
C_c (poly-poly cap)	1.8 pF
C_{cp} (poly-poly cap)	3 pF
C_{oc} (MOS cap)	~4.1 pF
Switch ($DOC_{ON/OFF}$)	40/0.35



PLAN	1ST	2ND	3RD	TOTAL
MAX.	12dB	12dB	6dB	30dB
MIN.	-12dB	-12dB	2dB	-22dB
STEP	6dB	6dB	2dB	

Fig. 10. Implemented 3-stage PGA and gain plan.

The first comprises a self-biased subthreshold cascode current mirror. As shown in Fig. 9(b), M_{oc5} and M_{oc6} are biased in the saturation region to absorb the dc current ($\sim 10\ \mu$A) from V_{outp} and V_{outn}, respectively. Due to the body effect associated with M_{oc9} and M_{oc10}, and using long channel length devices for M_{oc13} and M_{oc14} to deliver ultra small biasing currents (~ 10 nA), M_{oc9} and M_{oc10} are operated in the subthreshold region. It is known that a MOS transistor in this region offers a very high intrinsic gain that is independent of device geometry [15], ultimately for realizing a large time-constant low-dc-offset integrator on-chip.

The second technique involves a sink-/source-exchangeable charge pump (M_{oc1} and M_{oc2}) which is adopted as the output stage. It not only relaxes the linearity requirement of $A_i(s)$, but also reduces the signal swing associated with the integration capacitor C_{oc}. Thus, for further area savings, C_{oc} is implemented with more nonlinear an antiparallel-compensated depletion-mode MOS capacitor (M_{oc17} and M_{oc18}) [17].

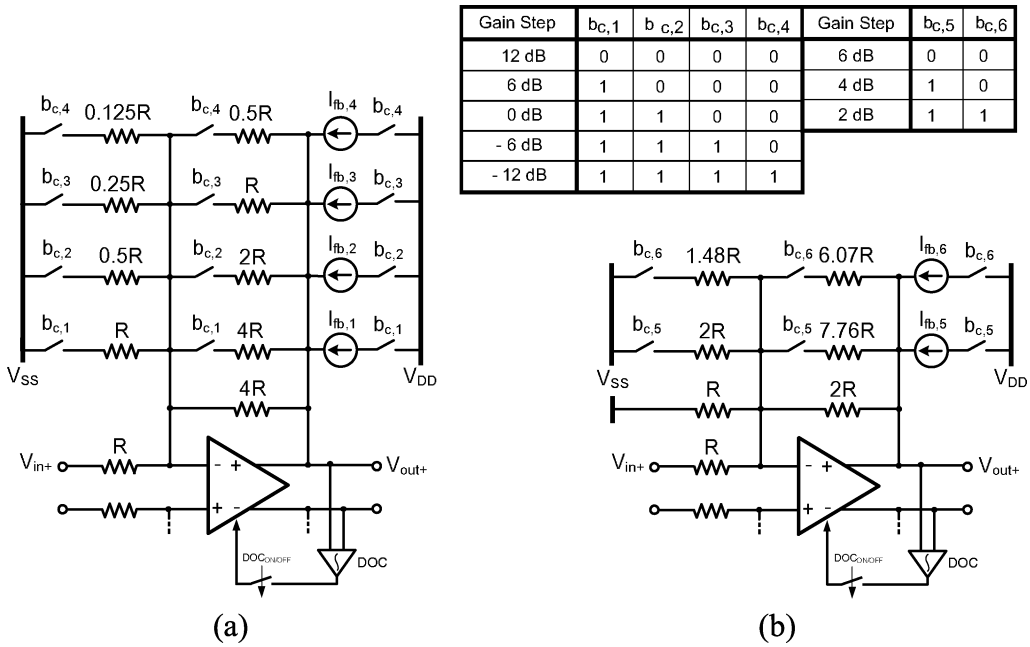


Fig. 11. Simplified schematics of the PGA's (a) first/second and (b) third stage.

Breaking the feedback loop of $\beta_1(s)$, the s-domain transfer function of the DOC standalone is given by

$$\frac{I_{oc+}(s) - I_{oc-}(s)}{V_{\text{out}p}(s) - V_{\text{out}n}(s)} = 2\frac{gm_{oc}}{R_{oc}} \frac{A_{i,dc} r_{o,Ai}}{(sr_{o,Ai}C_{oc} + 1)} \tag{17}$$

where $A_{i,dc}$ and $r_{o,Ai}$ are the current-to-current dc gain and output resistance of $A_i(s)$, respectively, while gm_{oc} is the transconductance of I_{oc+} (either M_{oc1} or M_{oc2}). The previously mentioned A_v is also given by (17) with $gm_{oc} = 1$. Controlling the C_{oc} can minimize the corner frequency without disturbing the gain while the other parameters have to be designed in parallel. R_{oc} dominates the DOC induced noise.

Conventionally, component mismatch inside the DOC *directly* limits the elimination of the dc-offset. Differently here, the intrinsic dc-offset of the DOC after being referred to the opamp's input is lowered by $A_1(s)$. The residual becomes part of the opamp's dc-offset that will be multiplied by $1 + R_{\text{fb}}/R_{\text{ff}}$ at the PGA's output. Since $A_1(s)$ (i.e., a differential pair) offers a dc gain close to 25 dB, the dc-offset induced by the DOC is of minor level when compared with that induced by the opamp.

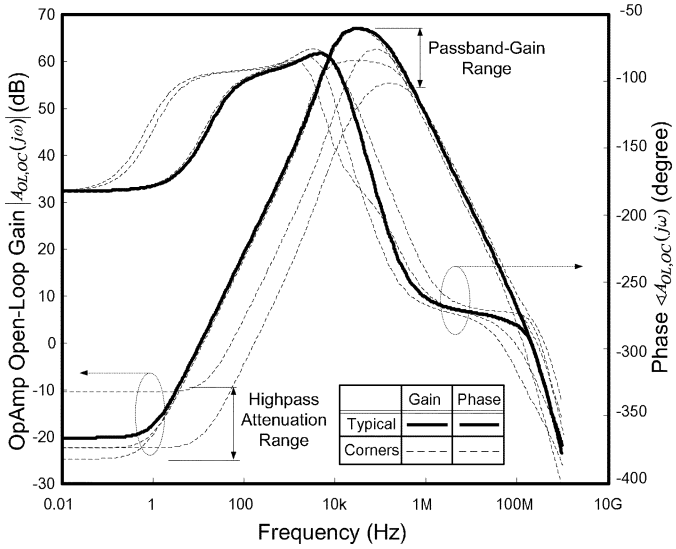


Fig. 12. Typical and corner AC performances of the opamp with the DOC.

V. Prototype Design and Simulation Results

A. PGA Gain Plan and Circuit Structure

To demonstrate the proposed two techniques, a 52-dB gain range 3-stage PGA was designed which incorporates a 20-dB gain channel-selection filter to meet the largest required gain, i.e., 50 dB. As shown in Fig. 10, unlike the conventional servo loop that closes the feedback with multiple forward stages, here each-stage of the opamp has a local DOC to ensure a balanced internal signal transfer and facilitates the stability concerns [6]. Coarse (6 dB/step) followed by fine (2 dB/step) gain controls were structured to shorten the global gain-control transients [18]. The simplified schematics of the PGA's first-(2nd-) and 3rd-stage are depicted in Fig. 11(a) and (b), respectively. The resistor ratios that are shown maintain the feedback factor constant at 0.2 and stabilize the quiescent-operating points of the opamp, I-CMFB and O-CMFB by generating $I_{\text{fb},1-6}$ and using the above-mentioned R-to-I conversion circuit. The round-off error in the 3rd-stage is due to the deliberate reduction of β_2 from its original minimum of 0.39, to 0.2, such that the opamps in all stages share the same specifications. Certain simulation results are given next to substantiate the performance claims.

B. Opamp With DOC—Frequency Response

The open-loop AC responses of the opamp with DOC simulated in the typical and the four process corners with a 1-pF capacitor, as testing load, are shown in Fig. 12, demonstrating that the presence of the DOC does not degrade the robustness of the opamp. In the typical case, the midband gain is 65 dB while

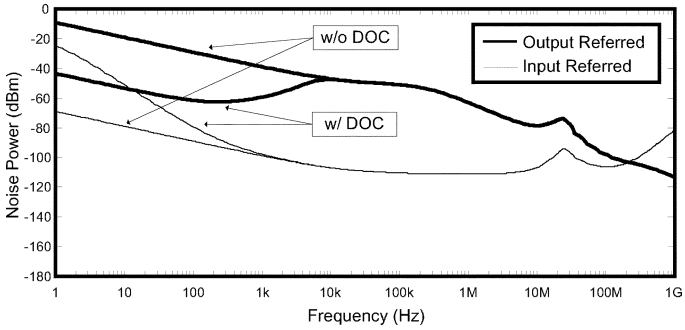


Fig. 13. Input-/output-referred noise of the opamp with/without the DOC.

the dc attenuation is -20 dB. The lower -3-dB frequency is 10 kHz while the unity-gain frequency is 372 MHz. The low-frequency region shows an unconditional stable response, whereas the high-frequency region shows a phase margin of roughly 50°.

C. Opamp With DOC—Noise Response

As mentioned before, the PGA is dc-offset-cancelled and should be preceded by a high-gain filter in the receiver. The design parameters are thus optimized for linearity and power. As shown in Fig. 13, the opamp's $1/f$ noise is suppressed by 33 dB (at 1 Hz) with the DOC enabled. Independently of the DOC status, the white noise was measured to be -45 dBm (at 100 kHz), demonstrating that the DOC can suppress the $1/f$ noise while the white noise is not increased. In this particular design, the SCR technique compared with the switched-resistor one shows a loss in signal-to-noise ratio of 3.7 dB. It constitutes an overhead of using the SCR technique because under LV constraints certain auxiliary circuits must be added.

D. Comparison Between Switched-Resistor and SCR PGAs in Terms of DC-Offset Rejection

Employing such an opamp in the switched-resistor PGA and SCR PGA originates the closed-loop gains depicted in Fig. 14(a) and (b), respectively. A high-level estimation of the closed-loop gain (i.e., assuming that the phase shift is small at low frequency) can be given by

$$A_{\mathrm{CL,OC}}(j\omega) = -\frac{R_{\mathrm{fb}}}{R_{\mathrm{ff}}}\frac{1}{\left(1+\frac{1}{A_{\mathrm{OL,OC}}(j\omega)\beta}\right)} \tag{18}$$

where β refers to β_{IA} for switched-resistor PGA; but refers to β_{PGA} for SCR PGA. The former offers an inconstant attenuation at dc (22 to 34 dB) due to a variation of β_{IA} (0.8 to 0.2). Differently, the latter offers a 34-dB constant attenuation at dc due to a constant β_{PGA} of 0.2. It implies that not just the BW is stabilized, but also the rejection at dc, giving a true dc-offset transient free gain control.

E. PGA—Composite Lower -3-dB Point

With a constant β_{PGA} of 0.2, the lower -3-dB point in each PGA stage $S_{-3\ \mathrm{dB,stage}}$ is fixed at 40 Hz for all gain levels {i.e., $10k/[1+\log^{-1}(62/20)\cdot 0.2]$}. When there are N identical high-pass PGA stages in the cascade, the composite lower -3-dB point $S_{-3\ \mathrm{dB,full}}$ is shifted to a higher frequency value as given by

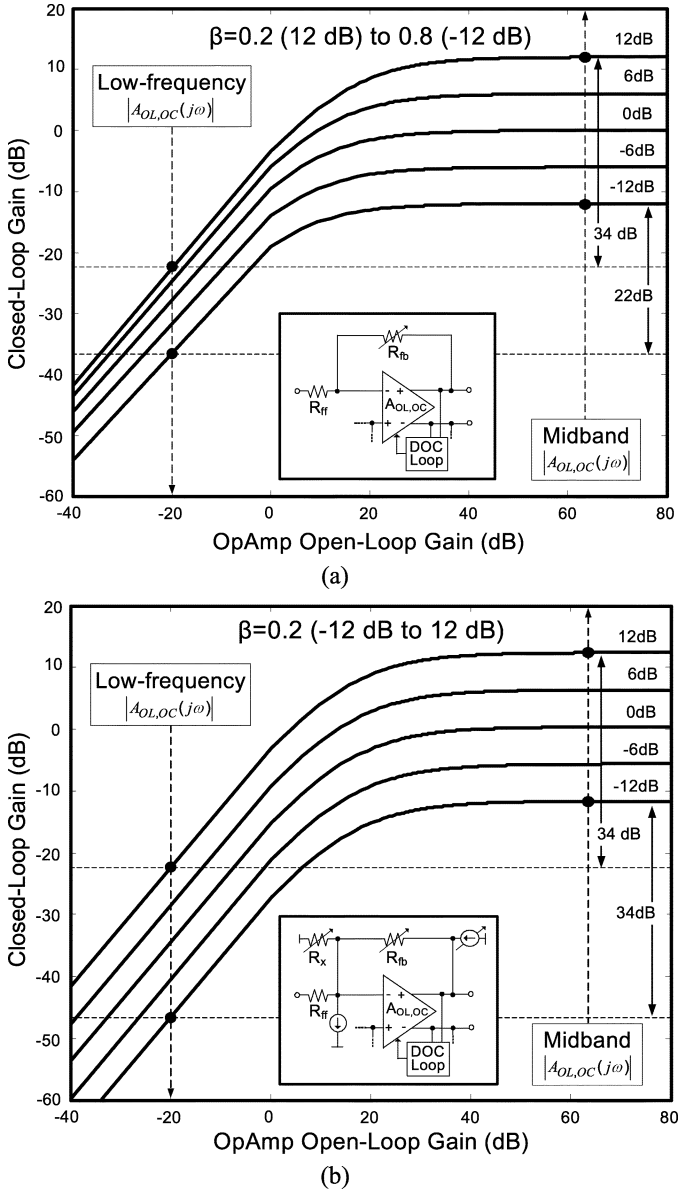


Fig. 14. PGA's closed-loop gain versus opamp's open-loop gain at low-frequency and midband. (a) Switched-resistor PGA. (b) SCR PGA.

$$S_{-3\ \mathrm{dB,full}} = \frac{f_{-3\ \mathrm{dB,stage}}}{\sqrt{2^{1/N}-1}}. \tag{19}$$

With $N = 3$, $S_{-3\ \mathrm{dB,full}}$ is still kept at a sufficiently low frequency, around 78 Hz. However, in practice, component mismatches will flatten the high-pass notch and shift the lower -3-dB point to a higher/lower frequency. Although the exact value of the lower -3-dB point is uncritical for the targeted applications, the composite value (i.e., the composite value is determined by counting all DOCs inside the receiver chain) must be less than 10 kHz to avoid considerably damaging the signal spectrum, stimulating the use of Monte Carlo simulations to encounter the PVT. The PGA's magnitude responses simulated over random mismatch and process variation show a

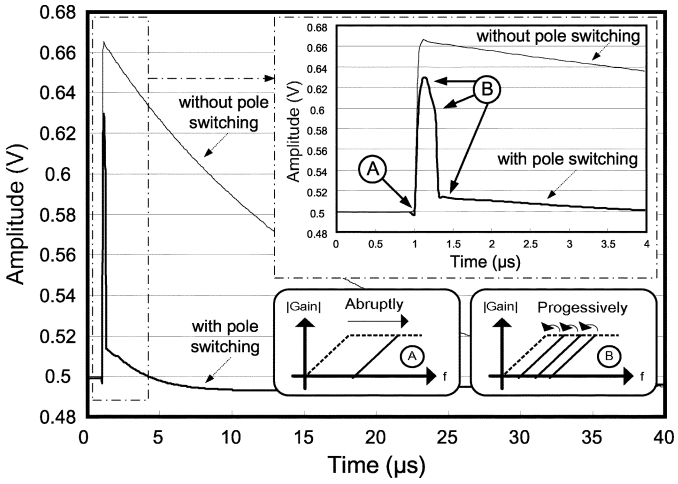


Fig. 15. PGA step response with and without a pole-frequency control in the DOC.

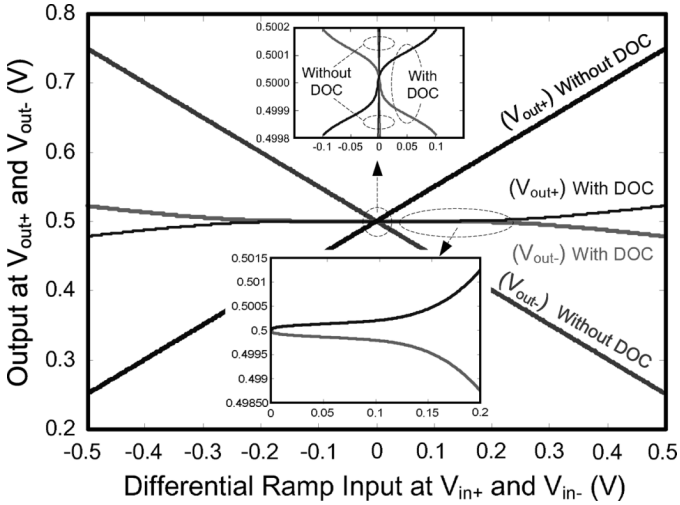


Fig. 16. Output dc-offset of a single-stage 0-dB-gain PGA versus a ramp input.

lower -3-dB point of maximally < 3 kHz while offering a dc rejection of minimally 65.2 dB.

F. PGA —Step Response

To provide a fast tracking for dc-offset transient, the 3-stage PGA is followed by a first-order passive-*RC* high-pass filter (HPF) in the receiver testbench. Its high-pass pole is switchable to a high/low frequency value for preamble/normal reception, such that the composite lower -3-dB point is $\sim$ 1MHz/ $\sim$ 10kHz, respectively. Simulated at the highest (i.e., 30 dB) gain level with a step input and 5% channel mismatch artificially assigned in all PGA stages, the settling time is extremely long if no switching is applied (Fig. 15), but is shorted to less than 0.5 μs (6.25% of the 8-μs short preamble in 802.11a and g) by abruptly switching off the 3 DOCs and shifting the pole of the HPF to high frequency at the beginning. Afterwards, the 3 DOCs are switched on progressively in 3 time slots that are synchronized with the pole switching of the HPF back to lower frequencies.

G. PGA—Ramp Response

The dead zone only happens when the input is extremely small. The output within the dead zone has a slope that matches the case when the DOC is disabled (upper subplot), showing also that the irremovable dc-offset ($V_{\text{in}+} - V_{\text{in}-}$) is less than 5 mV. A differential ramp input can determine the systematic dc-offset removability of the PGA. Fig. 16 plots the simulated output dc-offset of a single-stage 0-dB-gain PGAs versus a differential ramp input swapped between ± 0.5 V. The output follows the ramp input with the same slope when the DOC is disabled, but it is suppressed notably when it is enabled. From the lower subplot of Fig. 16, we can observe that the residual output dc-offset after suppression is 2.4-/3.8-/8.9-/19.6-mV differential, with an input dc-offset of 100-/200-/300-/400-mV differential applied.

H. PGA—Stage and Overall DC-Offsets

Monte-Carlo simulation is a tool that can simultaneously take systematic and random dc-offsets into account. The dc-offset followed a normal distribution shows a mean value of 0 and a

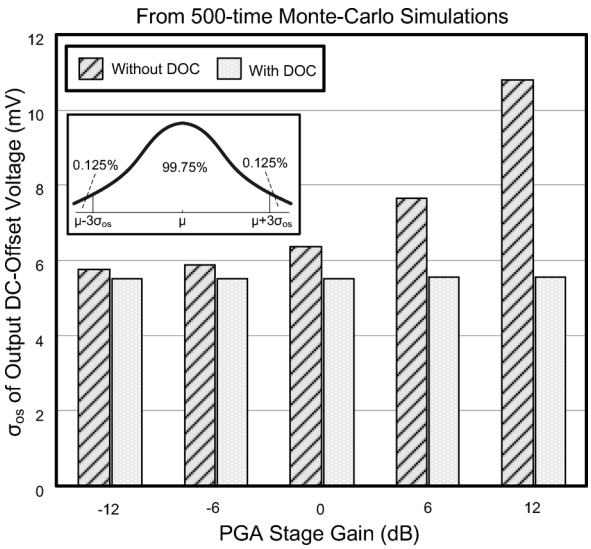


Fig. 17. σ_{os} of a single-stage PGA's output dc-offset.

TABLE II
SIMULATED TOTAL (3-STAGE) OUTPUT DC-OFFSET

Output Gain Level	Total-Output DC-Offset (mV)	
	with DOC	without DOC
	$V_{\text{os,total}}$	$V_{\text{os,total}}$
-22 dB	5.79	15.84
30 dB	5.9	115.6

standard deviation of σ_{os} related to the gain step. The simulated σ_{os}'s of a single-stage PGA at 12, 6, 0, -6, and -12-dB gain are shown in Fig. 17. With the DOC disabled, σ_{os} increases with the gain from 5.8 to 10.7 mV. Alternatively, with the DOC enabled, σ_{os} is less than 6 mV, implying 99.75% ($3\sigma_{\text{os}}$) one stage yields less than 18-mV dc-offset. Based on such results, we can estimate the total output dc-offset $V_{\text{os,total}}$ of the overall three-stage PGA, as listed in Table II.

With the DOC enabled, the largest $V_{\text{os,total}}$ ($3\sigma_{\text{os}}$) at 30-dB gain is suppressed from 346.8 to 17.7 mV, verifying the effectiveness of the DOC in lowering both stage and full-chain

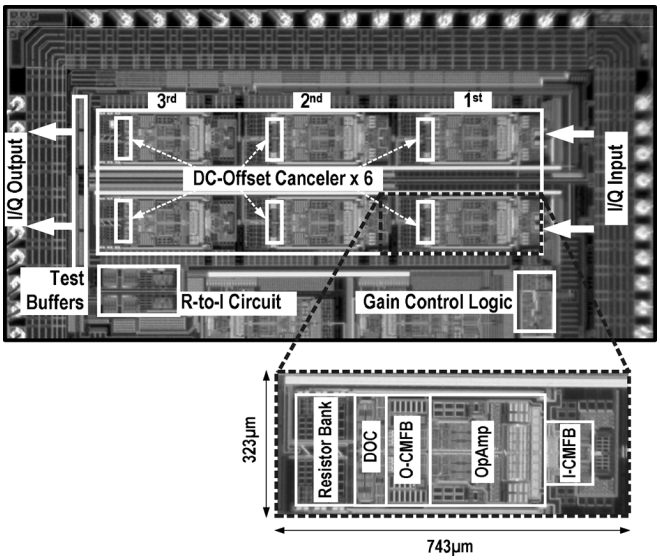


Fig. 18. Chip micrograph.

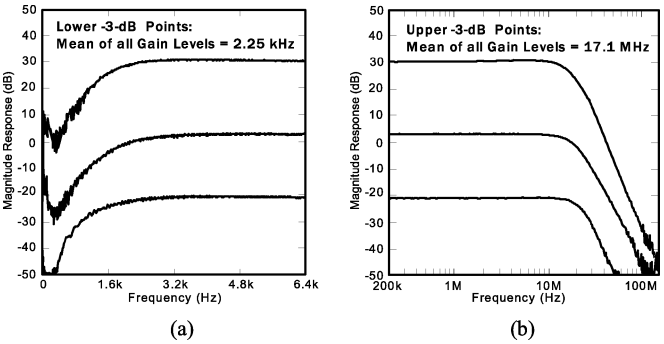


Fig. 19. Magnitude responses at 30-/4-/-22-dB gain levels in (a) low and (b) high-frequency regions.

dc-offset. It is also obvious that $V_{\mathrm{os},3}$ dominates $V_{\mathrm{os,total}}$ by 96.6% because the DOC is locally adopted in each stage. The fine-gain control, thus, should be located at the backmost to minimize the overshoot due to dynamic dc-offset.

VI. Experimental Results

Two parallel paths were implemented for the in-phase (I) and quadrature-phase (Q) channels of an IEEE 802.11a/b/g-WLAN receiver using a 0.35-μm CMOS process as shown in Fig. 18. All measurements described below have been taken under a 1-V V_{DD}.

The magnitude responses measured at 30/4/-22 dB gain levels are shown in Fig. 19(a) and (b) for low-and high-frequency cutoffs, respectively. The means of the lower and upper -3-dB cutoffs are 2.25 kHz ($\sigma = 11.2\%$, -19 dB) and 17.1 MHz ($\sigma = 8.3\%$, -21.6 dB), respectively. The BW variation is dominated by the gain steps ≤ -10 dB due to a decreased impedance level of the resistive load. The designed gains versus the measured values, gain error, output offset voltage V_{os} are plotted in Fig. 20. A linear gain control was achieved with less than 1-dB gain error but with a positive offset measured in all cases. The practically noncancelled V_{os}, increases with the gain but fluctuates randomly, which should be due to random component mismatches. The experimental

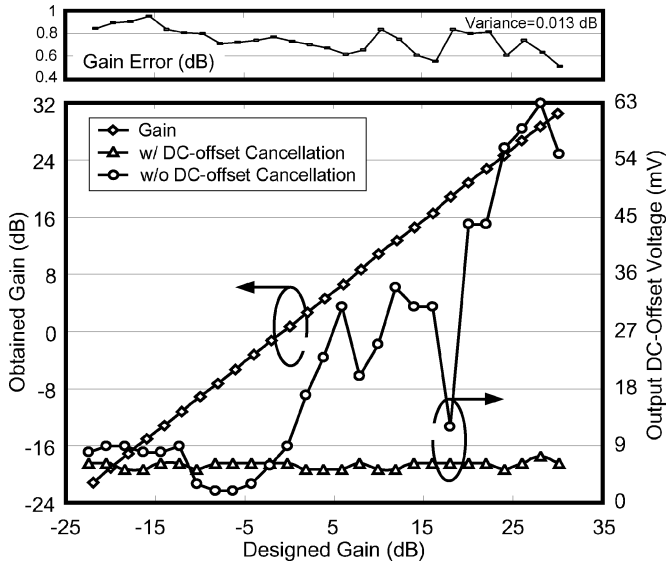


Fig. 20. Designed gain versus output gain, gain error, output dc-offset with and without the DOC enabled.

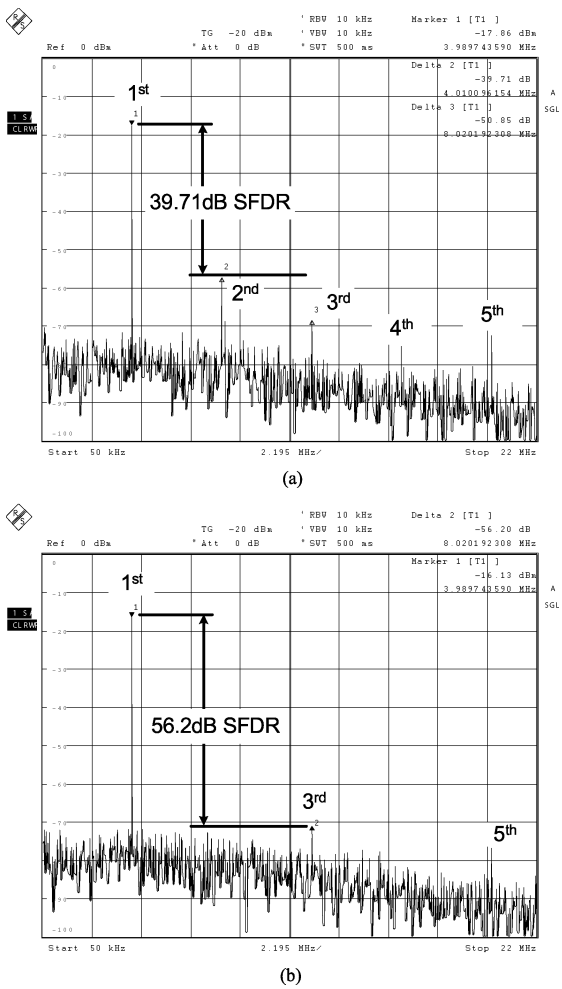


Fig. 21. SFDR with a 4-MHz single-tone input (a) without and (b) with the DOC enabled.

V_{os} is close to 5.7 mV for all gain levels, close to the result of one σ_{os} obtained from the simulations. For linearity, as shown in Fig. 21(a) and (b), the spurious-free dynamic ranges (SFDRs)

TABLE III
BRIEF COMPARISONS OF SEVERAL STATE-OF-THE-ART BASEBAND PGAS AND VGAS

	T. Yamaji *et al.* [20]	C. C. Hsu [21]	C. P. Wu *et al.* [22]	O. Jeon *et al.* [23]	S.-C. Tsou *et al.* [24]	This Work
Supply Voltage	2.5 V	3.3 V	3 V	1.6 to 2 V	1.8 V	1 V
Bandwidth	30 to 210 MHz	125 MHz	71 MHz	18 MHz	500 kHz ~ 30 MHz	17 MHz
Input-Referred (white) Noise	8 dB (double-sideband noise figure)	8.63 nV/$\sqrt{}$ Hz at 19 dB gain	N/A	77.5 nV/$\sqrt{}$ Hz at 0 dB Gain	11.2 nV/$\sqrt{}$ Hz at 20 dB gain	8.6 nV/$\sqrt{}$ Hz at 30 dB gain
IIP3	-28 to 7 dBm	12 to 35 dBm	-75.4 dBv	N/A	N/A	+8.4 dBm
Power Consumption	27.5 mW	21.1 mW	15 mW	10.4 mW	2.43 mW	6.8 - 7.9 mW
Gain Range	-35…+55 dB	0…+19 dB	+-8…80 dB	-8…+32 dB	-10…+20 dB	-22…+30 dB
Active Area	0.49 mm^2	0.18 mm^2	2.2 mm^2 (including pads)	0.56 mm^2	0.3 mm^2	0.72 mm^2
Technology	0.25 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.35 μm CMOS

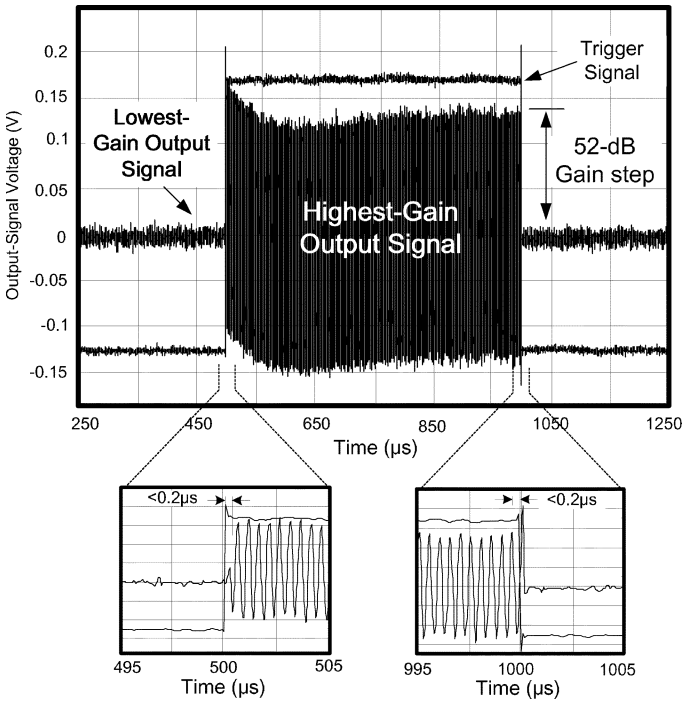


Fig. 22. Transient measurement with a 52-dB gain step applied.

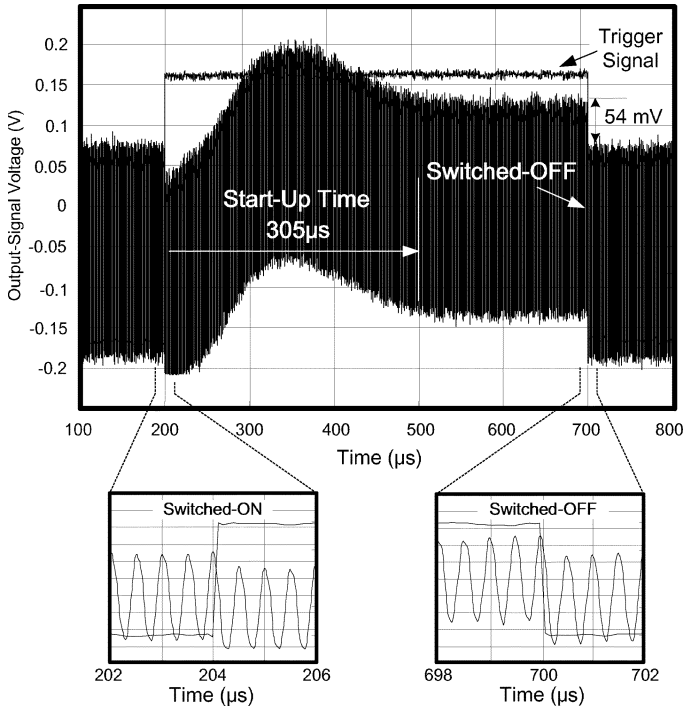


Fig. 23. Transient measurement with all DOCs switched on and off.

with the DOC disabled and enabled are 39.7 and 56.2 dB, respectively, showing that the even-harmonic rejection is highly improved by enabling the DOC. The worst transient measured with a 52-dB gain step applied is 0.2 μs (Fig. 22). Fig. 23 shows the dynamic behavior of the PGA when all DOCs are being started up together. No noticeable transient happens at the start and stop slots, and the dc-offset voltage is cancelled within 305 μs. The overshoot is within the output signal swing (i.e., no hard distortion due to clipping). Fig. 23 also shows that the circuit is free from dc-offset transients when all DOCs are switched off.

The power consumption ranges from 6.8 (highest gain) to 7.9 mW (lowest-gain), with a mean value of roughly 7.4 mW. Additional experimental results are summarized in [19].

VII. CONCLUSIONS AND BENCHMARKS

The continuous advance in lithography has resulted in thinner transistor's gate-oxide and lower supply voltage down to 1 V, or even below, rendering the classical implementation of many analog functions ineffectual. This paper has presented two circuit techniques to gain back the performance of PGA under LV constraints.

1) The SCR Stabilizes the PGA's quiescent operating point and feedback factor, resulting in a transient-free constant-BW gain adjustment;
2) The *inside-opamp DOC* reduces the area required for building a large time constant on chip while providing a high switchability to shorten the global dc-offset transients.

Comparing the demonstrated 1-V prototype with the state-of-the-art baseband PGAs and variable-gain amplifiers (VGAs) in Table III [20]–[24], this work, to our knowledge, is the lowest voltage reported design, while offering a medium gain range of 52 dB without resorting from specialized devices, or voltage boosting at any node.

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