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Improved Dielectric and Interface Properties of 4H-SiC MOS Structures Processed by Oxide Deposition and N_2O Annealing

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Abstract. Oxide deposition followed by high-temperature annealing in N_2O has been investigated to improve the quality of 4H-SiC MOS structures. Annealing of deposited oxides in N_2O at 1300°C significantly enhances the breakdown strength and decreases the interface state density to 3×10^{11} $cm^{-2}eV^{-1}$ at $E_C - 0.2$ eV. As a result, high channel mobility of 34 cm^2/Vs and 52 cm^2/Vs has been attained for inversion-type MOSFETs fabricated on 4H-SiC(0001)Si and (000-1)C faces, respectively. The channel mobility shows a maximum when the increase of oxide thickness during N_2O annealing is approximately 5 nm. A lateral RESURF MOSFET with gate oxides formed by the proposed process has blocked 1450 V and showed a low on-resistance of 75 mΩcm^2, which is one of the best performances among lateral SiC MOSFETs reported.

Introduction

SiC power MOSFETs have been recognized as an ideal power switch, showing high voltage, low on-resistance, and fast switching speed. In recent years, a variety of efforts have been made for improving the quality of MOS interface. Nitridation of SiC MOS interface is a widely accepted technique, by which the channel mobility is remarkably enhanced in MOSFETs fabricated on 4H-SiC(0001) [1-3] as well as on other crystal faces [4]. Although the origin of interface defects has not been fully understood, several analyses have revealed that the SiO_2/SiC interface is not abrupt and a high density of carbon (SiC_xO_y or SiO_2+C clusters) is detected near the interface [4-6]. Since the residual carbon near the MOS interface might be inherent to thermal oxidation of SiC, the authors have investigated the potential of deposited oxides for SiC MOSFET fabrication. Though a few studies on deposited oxides have been reported [7-9], more systematic investigation and device application are described in this paper.

Experiments

SiO_2 films were deposited on 4H-SiC(0001)Si and (000-1)C epilayers by plasma-enhanced CVD at 400°C by using TEOS and O_2 as source gases. The thickness of deposited oxides was varied in the range from 40 nm to 85 nm. In order to improve the oxide quality, the samples were annealed in Ar or N_2O (10% in N_2) at 1300°C for 60-360 min. During the N_2O annealing (nitridation), the oxide thickness increased by Δd, as shown in Fig.1. MOS structures formed by N_2O oxidation at 1300°C [8] were also prepared as a reference.

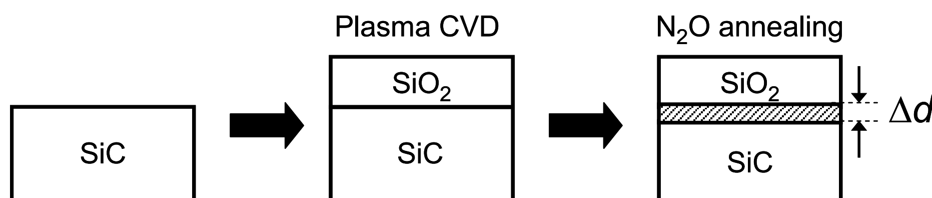

Fig.1. Schematic flow of "CVD + N_2O annealing" process. The increase of oxide thickness by N_2O annealing is denoted by Δd.

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To characterize the dielectric and interface properties, n-type MOS capacitors were fabricated. The diameter of Al electrodes was 300 μm. The donor concentration of n-type epilayers was 1-3x10^{16} cm^{-3}. The channel mobility was assessed by processing planar inversion-type MOSFETs on p-type epilayers doped to 1x10^{16} cm^{-3}. Lateral high-voltage MOSFETs with a two-zone RESURF (Reduced Surface Field) structure [10,11] were also fabricated.

Characterization of MOS capacitors

Figure 2 depicts the current density (J)–electric field (E) characteristics of n-type 4H-SiC(0001) MOS capacitors (d_{ox} = 60-72 nm) formed by (a) plasma CVD and Ar annealing, (b) plasma CVD and N_2O annealing, and (c) N_2O oxidation. The typical characteristics among 20 MOS capacitors for each process are shown. The annealing time was 180 min in this particular case. Although the oxide formed by the "CVD + Ar anneal" process is leaky, N_2O annealing resulted in significantly improved dielectric properties (resistivity: 10^{16} Ωcm, breakdown field > 10 MV/cm). From the ln(J/E^2)–1/E plot (not shown), the barrier height was estimated to be 2.84 eV, in good agreement with a value theoretically expected. It should be noted that the oxides formed by CVD and N_2O annealing exhibited almost the same (or slightly better) dielectric properties as those of N_2O-grown oxides. Tanimoto et al. reported that ONO stack films formed on 4H-SiC by the CVD and oxidation process showed significantly improved dielectric properties, compared to standard thermal oxides [12]. Thus, "deposited oxides" may possess much potential if proper annealing such as N_2O annealing at high temperature is performed.

Figure 3 represents the distribution of interface state density (D_{it}) for various MOS structures, which was determined from quasi-static and high-frequency (1 MHz) C-V curves of n-type 4H-SiC(0001) MOS capacitors (d_{ox} = 60-72 nm). The "CVD + Ar anneal" sample showed very high interface state density, indicating that the interface formed by deposition itself is rather defective. However, both the CVD + N_2O annealing and N_2O oxidation processes yielded relatively low D_{it} values. The D_{it} values of "CVD + N_2O anneal" sample are higher in the energetically deep region but lower near the conduction band edge (D_{it} = 3x10^{11} cm^{-2}eV^{-1} at E_C – 0.2 eV), compared to the N_2O-grown sample. Since electron trapping induced by a high density of interface states near the conduction band edge is the main cause for low channel mobility of 4H-SiC MOSFETs [13], the reduced D_{it} values near the band edge for "CVD + N_2O anneal" sample will be promising.

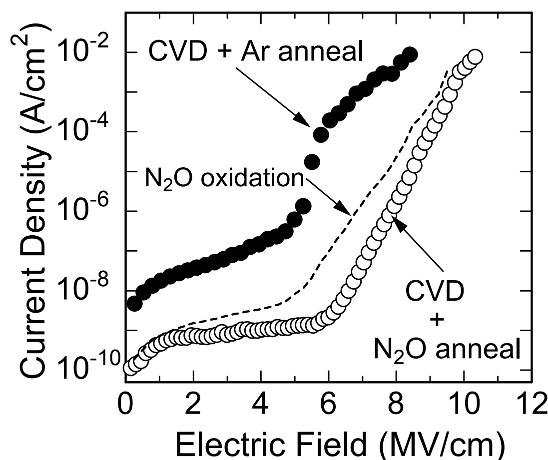

Fig.2. Typical current density – electric field characteristics of n-type 4H-SiC(0001) MOS capacitors formed by different processes.

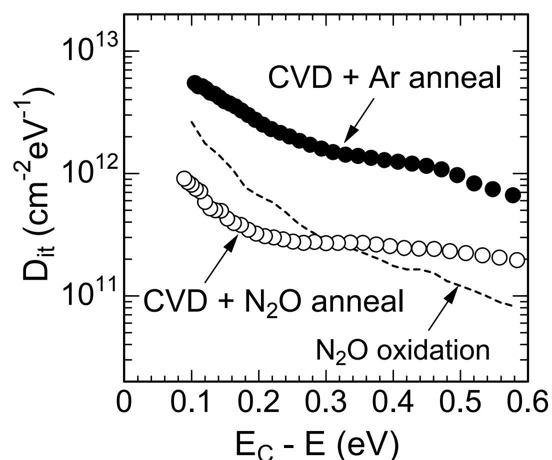

Fig.3. Distribution of interface state density for n-type 4H-SiC(0001) MOS capacitors formed by different processes (determined by a hi-lo method).

Characteristics of MOSFETs

Inversion-type test MOSFETs were processed on p-type 4H-SiC{0001} epilayers with an acceptor concentration of $1x10^{16}$ cm^{-3}. The channel length and width were 50 μm and 200 μm, respectively. The source/drain regions were formed by high-dose ($4x10^{15}$ cm^{-2}) P^+ ion implantation at 300°C followed by annealing at 1700°C for 20 min. Ni metals annealed in Ar at 1000°C were employed as ohmic contacts.

The MOSFET with a "CVD + Ar anneal" oxide showed a poor mobility of 4 cm^2/Vs, as predicted from its high D_{it}. When the time of post-deposition annealing in N_2O was changed, the channel mobility showed a maximum value for 90 min-annealing in the case of 50 nm-thick deposited oxide and 180 min for 85 nm-thick oxide, meaning that the optimum annealing time is dependent on the thickness of deposited oxide. This oxide-thickness dependence of the optimum annealing time may be more easily understood in Fig.4, where the channel mobility is plotted against the increase of oxide thickness during N_2O annealing (Δd shown in Fig.1). At the Δd value of about 5 nm, maximum channel mobilities of 30-34 cm^2/Vs were attained for two different thicknesses of deposited oxides. This result indicates about 50% improvement in mobility, compared to the standard N_2O oxidation in the authors' group. The interface of deposited oxide/SiC should be modified, but the interface quality approaches that of N_2O-grown interface when oxidation proceeds too much during the N_2O annealing. The effective interface charge density of an optimized MOS structure was estimated to be $5\text{-}7x10^{11}$ cm^{-2} (negative) from the difference between experimental and theoretical threshold voltages. MOSFETs fabricated on the 4H-SiC(000-1)C face showed even higher mobilities of 46-52 cm^2/Vs.

The proposed process (CVD + N_2O anneal) with the optimum condition (Δd = 5 nm) was applied to fabrication of lateral RESURF MOSFETs. The MOSFETs were fabricated on 10 μm-thick p-type 4H-SiC(0001) epilayers with an acceptor concentration of 7.0×10^{15} cm^{-3}. The N^+ implant doses of 0.6 μm-deep two-zone RESURF regions were $2.4x10^{12}$ cm^{-2} and $7.8x10^{12}$ cm^{-2}. The details of device structure are described elsewhere [11]. Post-implantation annealing was performed at 1700°C for 20 min. The thickness of deposited oxide was 85 nm, and the channel length and width were 2 μm and 200 μm, respectively. Figure 5 shows the output characteristics of the fabricated 4H-SiC(0001) RESURF MOSFET measured at room temperature. The fabricated RESURF MOSFET exhibited a high breakdown voltage of 1450 V and a low on-resistance of 75 mΩcm^2 at an oxide field of 3.0 MV/cm. The effective channel mobility of test MOSFETs processed on the same substrate was 31

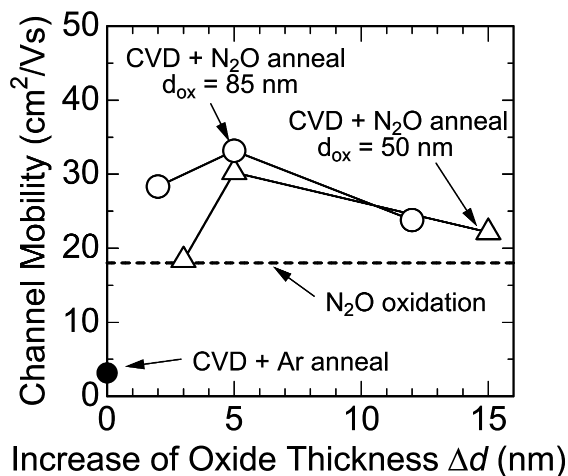

Fig.4. Effective channel mobility vs. increase of oxide thickness during N_2O annealing (4H-SiC(0001) face).

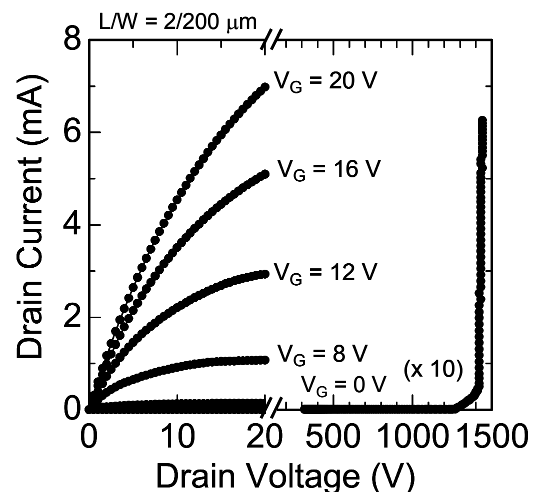

Fig.5. Drain characteristics of a 4H-SiC(0001) RESURF MOSFET with a deposited oxide followed by N_2O annealing at 1300°C.

cm^2/Vs. The threshold voltage was 3.6 V, and the leakage current at 1000 V under zero-gate bias was 14 nA. The gate leakage at a drain voltage of 1000 V was below 20 pA. These characteristics are comparable to those of the MOSFET with a N_2O-grown oxide and the same dose (breakdown voltage: 1280-1320 V, on-resistance: 67-84 mΩcm^2), and the present result is one of the best performances (V_B^2/R_{on} = 28 MW/cm^2) among any normally-off lateral MOSFETs. Advantages of the proposed process include the reduction of process time, especially on (0001)Si face, and nearly isotropic formation of oxides on trench sidewalls.

Summary

4H-SiC MOS structures formed by oxide deposition followed by high-temperature annealing in N_2O has been investigated. Although the deposited oxides annealed in Ar showed poor dielectric and interface properties, N_2O annealing at 1300°C significantly improved the breakdown characteristics and reduced the interface state density to $3x10^{11}$ $cm^{-2}eV^{-1}$ at $E_C - 0.2$ eV. The channel mobility was increased from about 20 cm^2/Vs for N_2O-grown oxides to 34 cm^2/Vs by the "CVD + N_2O annealing" process. The maximum channel mobility was obtained when the increase of oxide thickness during N_2O annealing was about 5 nm. A high mobility of 51 cm^2/Vs was realized by employing the 4H-SiC(000-1)C face. The lateral RESURF MOSFET with gate oxides formed by the proposed process blocked 1450 V and showed a low on-resistance of 75 mΩcm^2 at a gate oxide field of 3.0 MV/cm, which is one of the best performances among lateral SiC MOSFETs reported. Although the deposited oxides have not been an attractive choice in Si technology, the "CVD + N_2O annealing" is a promising process for SiC MOS devices.

Acknowledgements

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References

[1] G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, R. Chanana, R.A. Weller, S.T. Pantelides, L.C. Feldman, O.W. Holland, M.K. Das and J.W. Palmour: IEEE Electron Device Lett. Vol. 22 (2001), p. 176.

[2] S. Dimitrijev, H.F. Li, H.B. Harrison, D. Sweatman: IEEE Trans. Electron Dev. Lett. Vol. 18 (1997), p. 175.

[3] C.Y. Lu, J.A. Cooper, Jr., T. Tsuji, G. Chung, J.R. Williams, K. McDonald, and L.C. Feldman: IEEE Trans. Electron Devices, Vol. 50 (2003), p. 1582.

[4] T. Kimoto, Y. Kanzaki, M. Noborio, and H. Matsunami: Jpn. J. Appl. Phys. Vol. 44 (2005), p. 1213.

[5] K.C. Chang, N.T. Nuhfer, L.M. Porter, and Q. Wahab: Appl. Phys. Lett. Vol. 77 (2000), p. 2186.

[6] V.V. Afanas'ev, F. Ciobanu, G. Pensl, and A. Stesmans: *Silicon Carbide- Recent Major Advances*, W.J. Choyke, H. Matsunami, and G. Pensl, Eds. Springer, Berlin (2003), p. 343.

[7] G.Y. Chung, J.R. Williams, T. Isaacs-Smith, F. Ren, K. McDonald, and L.C. Feldman: Appl. Phys. Lett. Vol. 81 (2002), p. 4266.

[8] L.A. Lipkin, M.K. Das and J.W. Palmour: Mater. Sci. Forum Vols. 389-393 (2002), p. 985.

[9] H. Yano, T. Hatayama, Y. Uraoka, and T. Fuyuki: Mat. Sci. Forum Vols. 483-485 (2005), p. 685.

[10] W. Wang, S. Banerjee, T.P. Chow and R.J. Gutmann: IEEE Electron Device Lett. Vol. 25 (2004), p. 185.

[11] T. Kimoto, H. Kosugi, J. Suda, Y. Kanzaki, and H. Matsunami: IEEE Trans. Electron Devices Vol. 52 (2005), p. 112.

[12] S. Tanimoto, H. Tanaka, T. Hayashi, Y. Shimoida, M. Hoshi, and T. Mihara: Mat. Sci. Forum Vols. 483-485 (2005), p. 677.

[13] N.S. Saks: *Silicon Carbide- Recent Major Advances*, W.J. Choyke, H. Matsunami, and G. Pensl, Eds. Springer, Berlin (2003), p. 387.