Statistical Modeling and Simulation of Threshold Variation under Dopant Fluctuations and Line-Edge Roughness

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ABSTRACT

The threshold voltage (V_{th}) of a nanoscale transistor is severely affected by random dopant fluctuations and line-edge roughness. The analysis of these effects usually requires atomistic simulations that are too expensive in computation for statistical circuit design. In this work, we develop an efficient *SPICE simulation method* and *statistical transistor model* that accurately predict threshold variation as a function of dopant fluctuations and gate length change caused by sub-wavelength lithography and the gate etching process. By understanding the physical principles of atomistic simulations, we (a) identify the appropriate method to divide a non-uniform gate into slices in order to map those fluctuations into the device model; (b) extract the variation of V_{th} from the strong-inversion region instead of the leakage current, benefiting from the linearity of the saturation current with respect to V_{th}; and (c) propose *a compact model of V_{th} variation* that is scalable with gate size and the amount of dopant and gate length fluctuations. The proposed SPICE simulation method is fully validated against atomistic simulation results. Given the post-lithography gate geometry, this approach correctly models the variation of device output current in all operating regions. Based on the new results, we further project the amount of V_{th} variation at advanced technology nodes, helping shed light on the challenges of future robust circuit design.

Keywords: Threshold Variation, Random Dopant Fluctuations, Line-Edge Roughness, Non-Rectangular Gate, Atomistic Simulations, SPICE Simulation, Predictive Modeling.

1. INTRODUCTION

The aggressive scaling of CMOS technology has inevitably lead to a drastic increase in process variations, such as random dopant fluctuations (RDF) and line-edge roughness (LER) [1][2], Fig. 1 illustrates these variations in the structure of a scaled transistor. These variations interact with each other, profoundly impacting all aspects of circuit performance, especially in the design of SRAM cells which are extremely sensitive to V_{th} mismatch [3][4]. We traditionally rely on TCAD simulation and compact models to quantify these random variations in circuit analysis, but such methods become incorrect as the minimum feature size of a transistor is approaching the characteristic length of these atom-level effects. Instead, 3D Monte-Carlo atomistic simulations become necessary in order to achieve adequate accuracy. For example, [5] and [6] demonstrated the need for and accuracy of atomistic simulations in the prediction of transistor variations under RDF and LER. However atomistic simulation is not efficient for statistical circuit analysis, such as the optimization of SRAM cells, since it is too computationally expensive to incorporate in traditional circuit analysis and statistical optimization. To alleviate this problem, we need a methodology that enables the compact modeling and SPICE simulation of these random variations with sufficient efficiency, accuracy, and scalability in transistor topology. This modeling and simulation methodology should keep the physicality of atomistic simulation, correctly represent the statistical characteristics, and capture the interaction between RDF and LER in the prediction

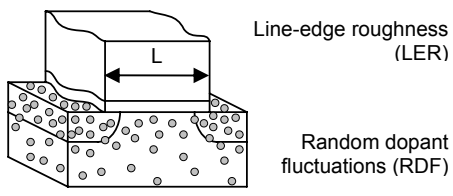


Figure 1. Primary variation sources in a nanoscale device.

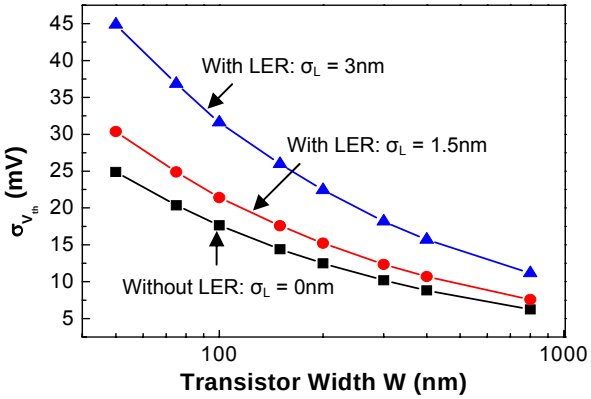


Figure 2. LER increases the variation of V_{th}, in addition to RDF. Results are predicted from our SPICE simulation method using 65nm PTM [11].

of threshold voltage changes.

In this work, we develop such a methodology based on the understanding of the underlying physics, particularly the principles of atomistic simulations and short-channel device physics. RDF is mainly a random effect; but LER is induced by both sub-wavelength lithography and the etching process. Lithography usually has a low spatial frequency and causes the so-called non-rectangular gate (NRG) effect [7][8]. Both RDF and LER change the output current of a transistor by modifying the threshold voltage [9][10]; they further interact *with each other*, resulting in a significant increase in leakage current [8], and leading to additional V_{th} variation. Using our newly developed simulation method, we illustrate in Fig. 2 that in addition to the well-known relationship between V_{th} variation and gate width W [9], LER further exacerbates the deviation of V_{th} (σ_{Vth}). Thus increase in the standard deviation of V_{th} is more pronounced when the transistor width is small, which is the typical condition in SRAM design. To handle these random effects and predict V_{th} variation from a given gate geometry, we propose to split a non-uniform device into slices, which have *an appropriate slice width* (d) that is larger than the correlation length of RDF in the leakage region, but small enough to track the spatial frequency of NRG. Each slice is then modeled as a sub-transistor with correct assignment of narrow-width and short-channel effect, as shown in Fig. 3 [8]. Such a representation maps a non-uniform transistor into an array of transistors which can easily be implemented in SPICE. It well captures the statistical characteristics of a transistor under RDF and NRG with sufficient simulation efficiency.

Since we choose the slice width to be larger than the atomistic correlation length of RDF, the concept of V_{th} in a compact device model, *which is a statistical average of channel doping*, is no longer suitable, particularly in the sub-threshold region [10]. We overcome this problem by extracting V_{th} from the strong-inversion region. Note that the pronounced velocity saturation effect causes the output current to be a linear function to V_{th} in the strong-inversion region [11]. Therefore, it provides a correct mathematical basis to partition the channel dopant under RDF, and then linearly superpose them together to monitor the overall change in V_{th}. Combining this approach with the Equivalent Gate Length (EGL) model that describes the nominal device behavior under non-rectangular gate effect [8], we are able to predict the amount of V_{th} variation under any given transistor characteristics (e.g., non-rectangular gate, narrow-width effect, etc.).

We systematically validate the proposed method with available atomistic simulation results under various conditions, including different amount of LER variations and various transistor sizes. This paper is organized as follows: Section 2 presents the theoretical background from atomistic simulation and device physics, identifying the appropriate slice width and transistor operating region for gate slicing and V_{th} extraction, respectively. As verified with atomistic simulations, the new SPICE simulation method is shown to accurately predict the variability of saturation current (I_{on}), leakage (I_{off}), and V_{th}. Based on this method, we further investigate the interaction of RDF, LER, and NRG on V_{th} variation in Section 3 and show that while the high spatial-frequency component of LER only affects the mean value of I_{off}, NRG has a significant impact on both the average and the distribution of the leakage and V_{th}. We propose a compact model to directly calculate σ_{Vth} from RDF and LER (Eq. (6)). Finally, we project the trend of V_{th} variation under RDF and LER toward future technology generations.

2. SIMULATION METHODOLOGY

In this section, we present the theoretical background and the flow of the proposed method. The practicality and limitations of gate slicing are well understood from the physical fundamentals. Based on appropriate slice width (d) to split a non-uniform gate, we exploit the linearity of saturation current on V_{th} change to assign V_{th} variation due to RDF and LER to each gate slice, and then extract the equivalent threshold variation from the summation of all these slices (Fig. 3). The approach incorporates other effects due to non-uniform gate through the integration of EGL and narrow-width effect models. We comprehensively verify the predicted change of I_{on}, I_{off}, and V_{th} under various RDF and LER conditions, as compared to 3D atomistic simulation results from [4][5].

2.1 The Fundamentals of Gate Slicing

To model a non-rectangular gate in the SPICE environment, a rudimental method is to partition the non-uniform edge into many slices, such that each slice can be approximated into a regular transistor with a uniform gate length. We can then apply the nominal device model

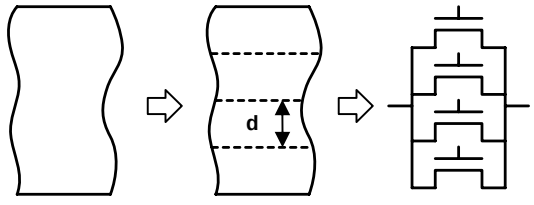


Figure 3. The flow to divide a non-uniform gate into slices. Each slice has a unique V_{thi} and L_i due to RDF and LER.

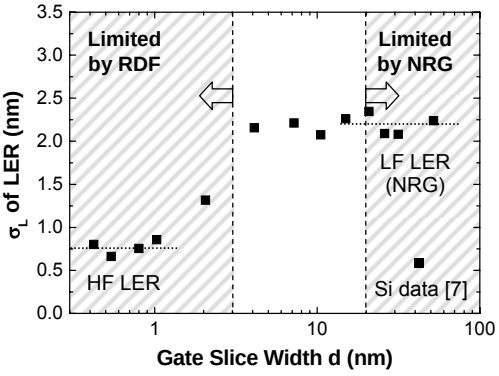


Figure 4. The appropriate slice width under both effects of RDF and LER [5][7].

to each SPICE for the prediction of I-V characteristics. The final performance of the transistor under NRG is calculated from the summation of currents from all the slices [8][12][13]. This procedure is illustrated in Fig. 3. As long as the current in each slice maintains the direction of source-to-drain, i.e., there is no significant distortion of the electrical field along the channel direction, this method can provide an accurate prediction on the change of I-V under NRG [8][13].

On the other hand, there are two fundamental limitations on the slice width (d) in this approach, especially when we consider the effect of random dopant fluctuations, which requires atomistic simulation to provide sufficient accuracy:

1. *Upper bound of d*: the spatial frequency of LER. The primary factors to cause LER include sub-wavelength lithography and the etching process. These different factors lead to different spatial frequency and amplitude of the distortion of gate length. Fig. 4 illustrates the silicon data of gate length change under LER [7]. The data clearly shows that two regions of LER have distinct spatial frequency: the high-frequency region (HF) that has a characteristic length smaller than 5nm and a low-frequency one (LF) has a characteristic length larger than 10nm [7]. While the HF component is usually caused by the property of the photo-resist and the etching condition, the LF component is mainly due to sub-wavelength lithography, i.e., NRG, which can be well predicted from layout by lithography tools [8]. The exact values of their characteristic lengths depend on the fabrication technology. When we split a non-uniform gate under LER, the width of each slice needs to be smaller than the characteristic length in order to track the change in gate lengths with adequate accuracy. For instance, to model a typical NRG gate, the slice width should be smaller than 20nm, as shown in the right side of Fig. 4 [7][8]. This phenomenon defines the upper bound of d during the slicing.

2. *Lower bound of d*: random dopant fluctuations. Due to the random position of dopants in the channel, V_{th} exhibits an increasing amount of variations with continuous scaling of transistor size [5]. For a relatively long channel device, this behavior is well recorded in the Pelgrom's model [9]. However, as the channel length is approaching the length scale of the fluctuation, such atom-level randomness can no longer be represented by V_{th} model in the weak-inversion region, which is usually modeled by averaging the potential in the channel. Such an approach hardly tracks the atomistic change [5]. In order to apply the slicing approach with compact V_{th}-based device model, the slice width must be larger than the correlation length of random channel potential near the threshold. Such length is typically around several nanometers, depending on the doping concentration [5]. The left side of Fig. 4 shows this lower bound of d during the slicing. If d is smaller than the correlation length, then the partitioning of a NRG gate into many slices is not a correct model for the statistical device behavior under RDF, particularly for the weak-inversion current [5].

Considering these two limits, Fig. 4 illustrates the appropriate region of d where the slicing approach is applicable. Only when d satisfies both limits, the partition of a single NRG transistor is meaningful in physics to prediction the current in all regions. Note that the lower region, which is limited by RDF, usually overlaps with that of the HF component of LER. Therefore, the slicing method may work well for RDF and NRG, but not RDF and HF LER. Since the distribution of gate length under LER approximately follows the Gaussian function [7][8], we use the correlation length of NRG (W_c) as the slice width [14], and follow the normal distribution to generate the length for each slice in the experiments [12][15].

2.2 Saturation Current (I_{on})-Based Method

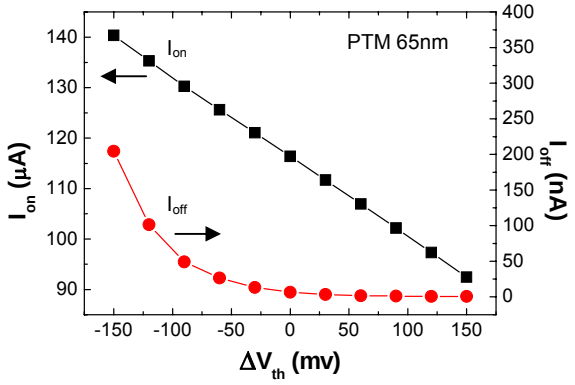


Figure 5. The linear and exponential dependence of I_{on} and I_{off} on V_{th} change, respectively.

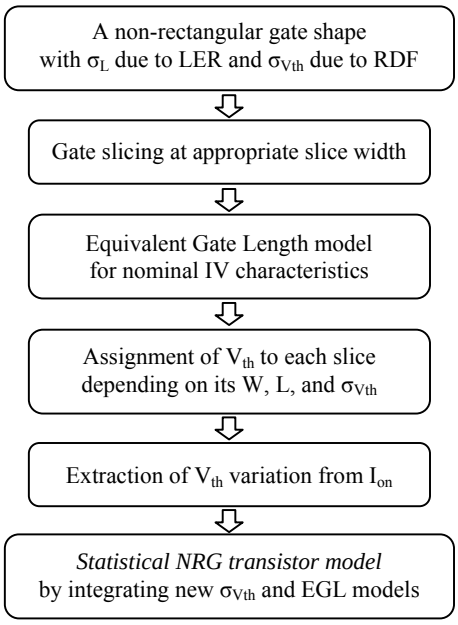


Figure 6. The flow to generate a single device model for statistical analysis of a NRG gate.

After appropriately slicing the gate with a non-rectangular shape, we can describe the characteristic of each slice using compact device model. The summation of all the slices provides the behavior of the original NRG gate. For the nominal condition, each slice has different

V_{th} from the deterministic effects of narrow-width and DIBL. They lead to the increase in the leakage current and the reduction in the effective gate length. The changes of I_{on} and I_{off} under these effects are well captured through the Equivalent Gate Length (EGL) model [8], i.e., a smaller L_{min} for I_{off} and a larger L_{max} for I_{on}. In this work, we follow the same modeling approach to formulate the nominal transistor model.

However, the situation becomes much more complicated when we incorporate statistical variation due to random dopant fluctuation into each slice. Since the slice width is longer than the correlation length of RDF in the weak-inversion, the concept of V_{th} is no longer applicable to the leakage current in order to extract V_{th} variation of the entire NRG transistor [5]. In fact, since I_{off} is an exponential function of V_{th} (Fig. 5), which is very non-linear, the mean and distribution of V_{th} can not be extracted from the statistical analysis of the summation of I_{off} from each slice:

$$\text{mean of } \exp\left(-\frac{V_{th}}{nkT/q}\right) \neq \exp\left(-\frac{\text{mean of } V_{th}}{nkT/q}\right) \qquad (1)$$

To overcome this barrier and still maintain the correctness in physics, we leverage the linearity of I_{on} to study the statistics of V_{th}. For a short-channel device, I_{on} has a linear dependence on V_{th}, due to strong velocity saturation [11]. This behavior is illustrated in Fig. 5 for PTM 65nm technology. This trend becomes even stronger for scaled CMOS devices [11]. As a result, the limitation that fails the statistical V_{th} extraction from I_{off} (Eq. (1)) is removed. The strong linearity of I_{on} provides a well-behaved basis to study V_{th} variation under RDF in all cases of NRG. Therefore, we propose to use an I_{on}-based method to extract V_{th} variation, embed it into the nominal device model, and then predict I_{off} change.

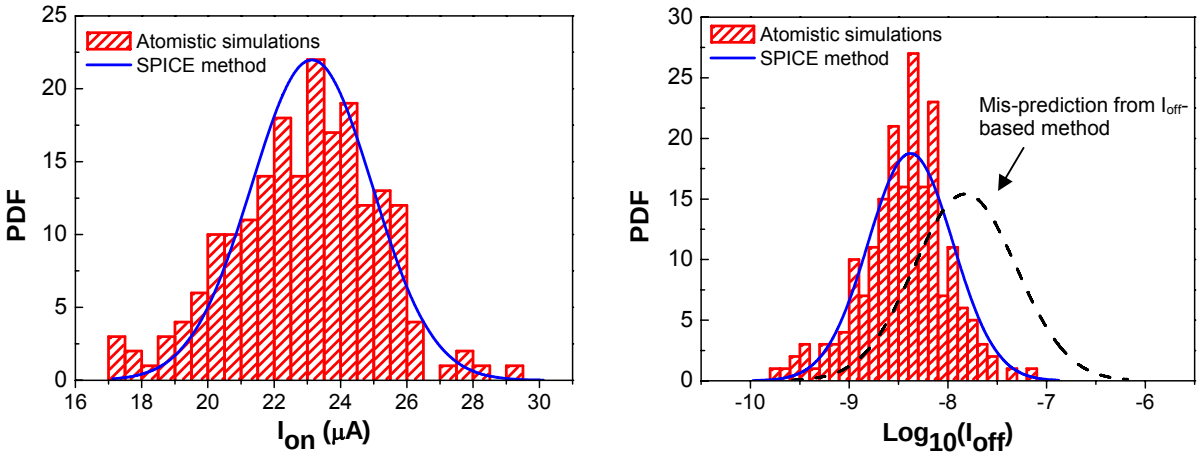
Fig. 6 summarizes this flow that supports the development of a single device model for statistical analysis under RDF and NRG. Given the shape of a NRG gate, we first divide it into slices with a suitable width, following the guidance in Fig. 4. Then, the model of EGL is produced for the nominal case under NRG [8]. To investigate the interaction of LER and RDF on V_{th} variation, we assign Vth to each slice as a statistical variable. While its mean value is determined by the width and length of the slice (i.e., narrow-width and DIBL effect [8]), its standard deviation is also dependent on the size of the slice [6][9][10]:

$$\sigma_{V_{th}} \propto \frac{1}{\sqrt{WL}} \qquad (2)$$

The exact value of σ_{Vth} due to RDF is technology dependent [2]. From the summation of Ion, we finally extract the variation of the threshold voltage of the entire transistor under NRG and RDF. Since the length of each slice is different under LER, such non-linear relation between σ_{Vth} and L (Eq. (2)) leads to an increase in V_{th} variation of the entire transistor, as demonstrated in Fig. 1. The outcome from this procedure is a single device model with EGL and a new σ_{Vth}, which supports efficient statistical performance analysis for any given NRG and RDF.

2.3 Validation with Atomistic Simulations

We implement this method into the SPICE environment and validate its prediction with available 3D Monte-Carlo atomistic simulation results. Fig. 7 compares the prediction of I_{on} and I_{off} variations under random dopant fluctuations [5]. It indicates that under normally distributed RDF, the variation of I_{on} follows the Gaussian distribution due to its linear dependence on V_{th}. Meanwhile, the variation of I_{off} follows the log-normal distribution because of the exponential dependence of I_{off} on V_{th}. Both mean and sigma of I_{on} and I_{off} are well predicted from the I_{on}-based extraction method. Fig. 7b further shows that if we directly sum the leakage current from every slice to estimate V_{th} variation, it results in a significant error, as implied in Eq. (1).



(a) Prediction of I_{on} variation

(b) Prediction of I_{off} variation

Figure 7. Validation of I_{on} and I_{off} variations under RDF [5].

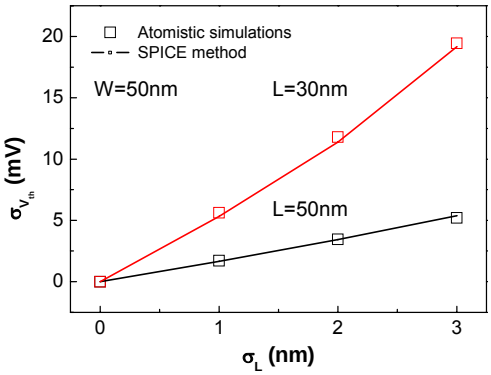


Figure 8. Validation of σ_{Vth} under NRG [5].

In addition to the verification of the I_{on}-based method under RDF, Fig. 8 evaluates the prediction of σ_{Vth} under different conditions of gate length variations due to LER, assuming a uniform channel doping concentration (i.e., no RDF) [5]. Two devices are studied, with both gate width at 50nm, and gate length at 30nm and 50nm, respectively. The correlation length of the NRG effect (W_c) is 20nm [5]. For the low-frequency component of LER (NRG), the increase of σ_L results in a larger amount of threshold variation, due to the interaction between σ_{Vth} and L, as shown in Eq. (2). This interaction is more pronounced when gate length is shorter, in which case the threshold voltage of each slice is more strongly coupled with L through DIBL effect [8].

As shown in Fig. 8, for a gate with the width of 50nm and the physical length of 30nm, which is typical for a SRAM transistor at the 65nm node, threshold variations can be more than 20mV, purely due to the NRG effect. Meanwhile, the nominal leakage current may increase by more than 15x due to NRG at the same condition [8]. Combining the information together, such effect will be a dominant factor to impact the leakage and circuit stability at the worst case corner. Therefore, it is crucial to incorporate accurate and efficient modeling capability into optimization, in order to mitigate impact of NRG with minimum overhead. Our proposed approach captures this complicated dependence very well, as compared to time-consuming atomistic simulations. It is also ready to be integrated with circuit design tools. While NRG has a pronounced effect on V_{th} variation, the high-frequency component of LER only has a marginal interaction with V_{th} variation [5][10]. Since its spatial frequency is quite high, its impact is averaged out across the slice [5]. Instead, it mainly affects the mean value of I_{off}, which has been well modeled in the EGL model [8].

Finally Fig. 9 verifies the prediction of threshold variation in the presence of both RDF and NRG. The variation of V_{th} is evaluated through the distribution of I_{off}, which is very sensitive to V_{th} change due to its exponential dependence. Three sets of experiments are carried out: NRG only with σ_L at 2nm, RDF with a rectangular gate (i.e., no NRG), and RDF with the NRG shape. Again, gate width is 50nm. Since V_{th} depends on L through the DIBL effect [8][11]:

$$V_{th} = V_{th0} - V_{ds}\exp\left(-\frac{L}{l'}\right) \tag{3}$$

where V_{th0} is a function of channel doping, the change of V_{th} due to L and RDF can be approximated as:

$$\Delta V_{th} = \Delta V_{th0} + V_{ds}\exp\left(-\frac{L}{l'}\right)\cdot\frac{\Delta L}{l'} \tag{4}$$

Therefore, the total variation of V_{th} follows the relationship below, as long as σ_L and RDF are independent and not excessive:

$$\sigma_{total}^{\ 2} = \sigma_{RDF}^{\ 2} + \sigma_{NRG}^{\ 2} \tag{5}$$

where σ_{RDF}, σ_{NRG}, σ_{total} are V_{th} variations due to RDF only, NRG only, and the total amount, respectively. The contributions of NRG and RDF are independent to the statistics of V_{th}. The relationship is well verified with atomistic simulations, as shown in Fig. 9.

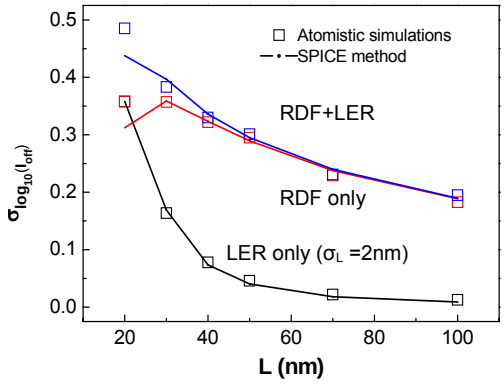


Figure 9. Validation of σ_{Vth} under both RDF and NRG [4][5].

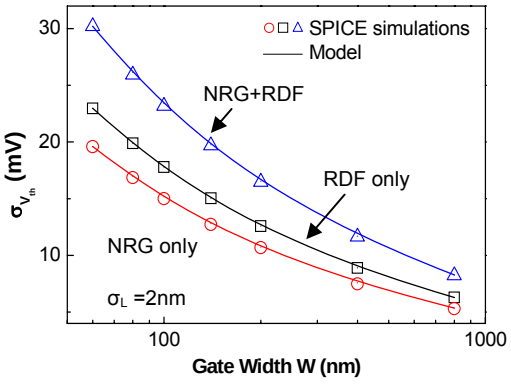


Figure 10. Validation of predictive modeling with SPICE results.

Fig. 9 indicates that when L is large, RDF is the dominant factor in threshold variation. As gate length decreases, the importance of NRG rapidly increases in the calculation of V_{th} variation. Again, the main reason is the strong DIBL effect, which is an exponential function of L, as shown in Eq. 3. Overall, our I_{on}-based simulation method provides excellent predictions of V_{th} variation under all situations, as compared to 3D Monte-Carlo atomistic simulations. It significantly enhances the simulation efficiency, with fully compatibility to circuit simulators.

3. PREDICTIVE MODELING

Based on the underlying physical mechanisms, we have successfully developed a SPICE simulation method from gate slicing to the extraction of V_{th} variation in the strong inversion region. In this section, we further propose a compact model that directly predicts V_{th} variation from RDF and NRG. This model updates traditional Pelgrom's model with the additional consideration of NRG effect. Using this model, we extrapolate the variation of V_{th} towards future technology nodes, helping shed light on robust circuit design with scaled CMOS technology.

3.1 Modeling of Threshold Variation

For traditional long-channel device, V_{th} mismatch is mainly induced by random effects, such as the dopant fluctuation. This consideration is the basis for the well known Pelgrom's model and other V_{th} variation models, in which σ_{Vth} is inversely proportional to the square root of the transistor size [2][6][9]. This fact is also shown in Fig. 9, in which the σ_{Vth} due to RDF is a straight-line in log scale with respect to L. However, as shown in Figs. 1 and 9, the impact of NRG on V_{th} variation becomes pronounced with further scaling of L, and can no longer be ignored in the calculation of threshold mismatch. These two effects superpose each other in the statistical property of V_{th}, as shown in Fig. 9 and Eq. (5).

As developed in [6][9][10], random dopant fluctuations induce the deviation of V_{th} as a linear function of $(WL)^{-0.5}$. For a larger transistor, the random distribution of dopants is averaged out in the modeling of V_{th}. Akin to this effect, the random distribution of gate length under NRG also leads to a linear function of $W^{-0.5}$, since the longer gate width is, the more the length distortion is average out. On the other hand, due to the DIBL effect, NRG induced V_{th} variation has an exponential dependence on L (Eq. (4)). Therefore, we can improve Eq. (5) with the following formula:

$$\sigma_{total}^{\ 2} = \frac{C_1}{WL} + \frac{C_2}{\exp(L/l')} \cdot \frac{W_c}{W} \cdot \sigma_L^{\ 2} \qquad (6)$$

where W_c is the correlation length of NRG, and C_1, C_2 and l' are technology dependent coefficients. The first term describes conventional Pelgrom's model. The second term is designated to the variation due to NRG. The exponential dependence on L is demonstrated in Fig. 9, with Fig. 10 further verifies Eq. (6) at different gate width. Our model accurately captures the superposition of these two statistical components, as well as the inverse square root dependence on W. As compared to the consideration of both NRF and RDF, traditional RDF only model significantly underestimates the total amount of V_{th} variation, as shown in Fig. 10. Note that due to the exponential dependence on L of the second term in Eq. (6), the impact of NRG diminishes at long gate length. Yet the second term rapidly affects threshold variation for a device with short gate length and width. For instance, at W=50nm, it has a comparable influence as that of RDF. Therefore, its role can not be neglected, particularly when we design the circuits with minimum size transistors in scaled technologies.

3.2 Projection to Future Technology Nodes

After extensive verification with atomistic simulations, the proposed simulation method and compact model offers a solid and convenient tool to explore threshold variation under NRG and RDF effects. As shown in Fig. 9 and 10, such approach has the right sensitivity to the transistor definition, as well as the amount of variations. In this section, we extrapolate these models for future technology generations, with the goal to generate early stage insights to future robust design under increased variations.

Continuous scaling exacerbates both RDF and NRG effects. With the scaling of transistor size, the total number of dopants in the channel significant reduces [1]. Consequently, it becomes more challenging to precisely control the position of dopants and as a consequence RDF will be more significant. For line-edge roughness, although the etching process may improve in the future, the situation

Table 1. Projection of threshold variation

NRG parameters		σ_{Vth} (mV)			
W_c (nm)	σ_L (nm)	65nm	45nm	32nm	22nm
20	0	19.9	23.8	28.1	45.8
	1	21.6	27.8	39.0	71.2
	2	26.3	39.2	69.4	
50	0	19.9	23.8	28.1	45.8
	1	23.8	33.3	51.7	98.6
	2	33.3	55.2	105.2	

of the low-frequency component, NRG, is not optimistic. Since it is difficult to reduce the wavelength in the photo-lithograph process, the distortion in gate length is expected to increase [12], even though lithography recipes and layout techniques, such as regular layout fabrics, may help improve the situation [12][16].

Using the new V_{th} variation model (Eq. (6)), we project the amount of threshold variation, under possible scenario of RDF and NRG. The nominal model file is adopted from PTM [11]. Table 1 summarizes the results for various NRG parameters of W_c and σ_L. Even under the same amount of NRG, the variation of the threshold variations keeps increasing due to the aggressive scaling of the feature size, as well as the increase of short-channel effects. As the trend goes, future design will suffer a dramatic amount of random V_{th} variation, leading to severe degradation in circuit matching property, memory stability, and the leakage control. While the improvement of process technology will continue, it but may be limited in the future, innovative circuit design and optimization techniques are critical to overcome these barriers.

4. Conclusion

Random variation in the threshold voltage is prominent in scaled CMOS technology and can severely affect circuit stability as well as performance distribution. In addition to the well known random dopant fluctuation effect, line-edge roughness, particularly non-rectangular gate, is emerging as a new contributor to V_{th} variation. Instead of 3D Monte-Carlo atomistic simulations, we propose an efficient simulation method in standard SPICE environment that accurately captures the impact of RDF and NRG on V_{th} variation. The development of the new method is based on the physical understanding of the atomistic simulations as well as the device physics. In our method, a non-uniform gate is first divided into appropriate slices; then threshold variation is assigned and extracted from the strong-inversion region, with the benefit from the linear dependence of I_{on} on V_{th}. The method significantly alleviates the computation cost, provides sufficient fidelity to atomistic simulations and scalability to process and design conditions. Based on this method, we further incorporate the impact of NRG into traditional Pelgrom's model, identifying the exponential dependence on gate length. With the continuous scaling towards the 22nm node, the effect of RDF and NRG on V_{th} variations becomes even more critical for future robust design exploration. Our method and compact model provides a physical and efficient tool for statistical circuit performance analysis and optimization.

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